General Description

The EA3056 is a 4-CH power management IC for applications powered by one Li-Ion battery or a DC 5V adapter. It integrates three synchronous buck regulators and one N-MOS LDO in a single chip. The internal compensation architecture simplifies the application circuit design. Besides, the independent enable control makes the designer have the greatest flexibility to optimize timing for power sequencing purposes. The EA3056 is available in a 24 pin QFN 4x4 package.

Features

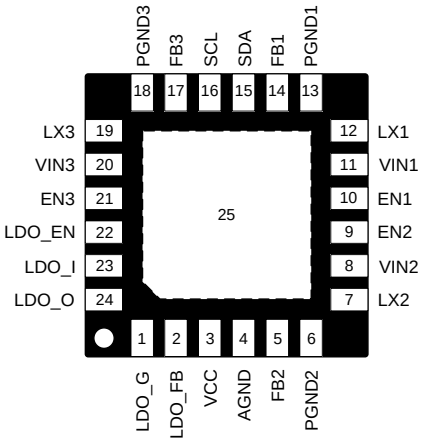
- 2.7V to 5.5V Input Voltage Range
- Three Buck Converters
  - I^2C Controlled VID Programmable Reference Voltage from 0.58V to 0.8V
  - -- 6 Bits VID in 5mV Steps
  - Output Voltage Can Also be Set by Resistor Divider
  - -- The Initial Reference Voltage is 0.6V
  - Continuous Load Current: 3A (CH1), 1.5A (CH2), 2A (CH3)
  - Peak Load Current: 3.5A (CH1), 2A (CH2), 2.5A (CH3)
  - Fixed 1.5MHz Switching Frequency
  - 180° Out of Phase Operation
  - 100% Duty Cycle Low Dropout Operation
  - Independent Enable Control
  - Internal Compensation
  - Cycle-by-Cycle Current Limit
  - <1uA Shutdown Current
  - Hiccup Short Circuit Protection
- One LDO Regulator
  - I^2C Controlled VID Programmable Reference Voltage from 0.58V to 0.8V
  - -- 6 Bits VID in 5mV Steps
  - Output Voltage Can Also be Set by Resistor Divider
  - -- The Initial Reference Voltage is 0.6V
  - 300mA Output Current (Peak 500mA Output Current)
  - Maximum 500mV Dropout Voltage
  - Independent Enable Control
- 4 channels total output power consumption must be less than 10W
- I^2C Compatible Interface with Standard Mode(100KHz) and Fast Mode(400KHz)
- Auto Recovery OTP Protection
- Available in 24-pin 4mm x 4mm QFN Package

Applications

- Smart Phone
- IP Camera
- OTT
- Digital Camera

Pin Configurations

(TOP VIEW)



QFN 4x4-24

Pin Description

Pin Name	Function Description	Pin No.
LDO_G	Ground pin of LDO.	1
LDO_FB	Feedback input of LDO. Connect to LDO_O with a resistor divider.	2
VCC	Input supply pin for internal control circuit.	3
AGND	Analog ground pin.	4
FB2	Feedback input of CH2. Connect to output voltage with a resistor divider.	5
PGND2	Power ground pin of CH2.	6
LX2	Internal MOSFET switching output of CH2. Connect LX2 pin with a low pass filter circuit to obtain a stable DC output voltage.	7
VIN2	Power input pin of CH2. Recommended to use a 4.7uF MLCC capacitor between VIN2 pin and PGND2 pin.	8
EN2	CH2 turns on/turns off control input. Don't leave this pin floating.	9
EN1	CH1 turns on/turns off control input. Don't leave this pin floating.	10
VIN1	Power input pin of CH1. Recommended to use two 10uF MLCC capacitors between VIN1 pin and PGND1 pin.	11
LX1	Internal MOSFET switching output of CH1. Connect LX1 pin with a low pass filter circuit to obtain a stable DC output voltage.	12
PGND1	Power ground pin of CH1.	13
FB1	Feedback input of CH1. Connect to output voltage with a resistor divider.	14
SDA	I^2C interface data pin.	15
SCL	I^2C interface clock pin.	16

Pin Name	Function Description	Pin No.
FB3	Feedback input of CH3. Connect to output voltage with a resistor divider.	17
PGND3	Power ground pin of CH3.	18
LX3	Internal MOSFET switching output of CH3. Connect LX3 pin with a low pass filter circuit to obtain a stable DC output voltage.	19
VIN3	Power input pin of CH3. Recommended to use a 10uF MLCC capacitor between VIN3 pin and PGND3 pin.	20
EN3	CH4 turns on/turns off control input. Don't leave this pin floating.	21
LDO_EN	LDO turns on/turns off control input. Don't leave this pin floating.	22
LDO_I	Power input pin of LDO. Recommended to use a 1uF MLCC capacitor between LDO_I pin and LDO_G pin.	23
LDO_O	The output pin of the LDO.	24
Exposed Pad	The Exposed Pad must be soldered to a large PCB copper plane and connected to GND for appropriate dissipation.	25

Function Block Diagram

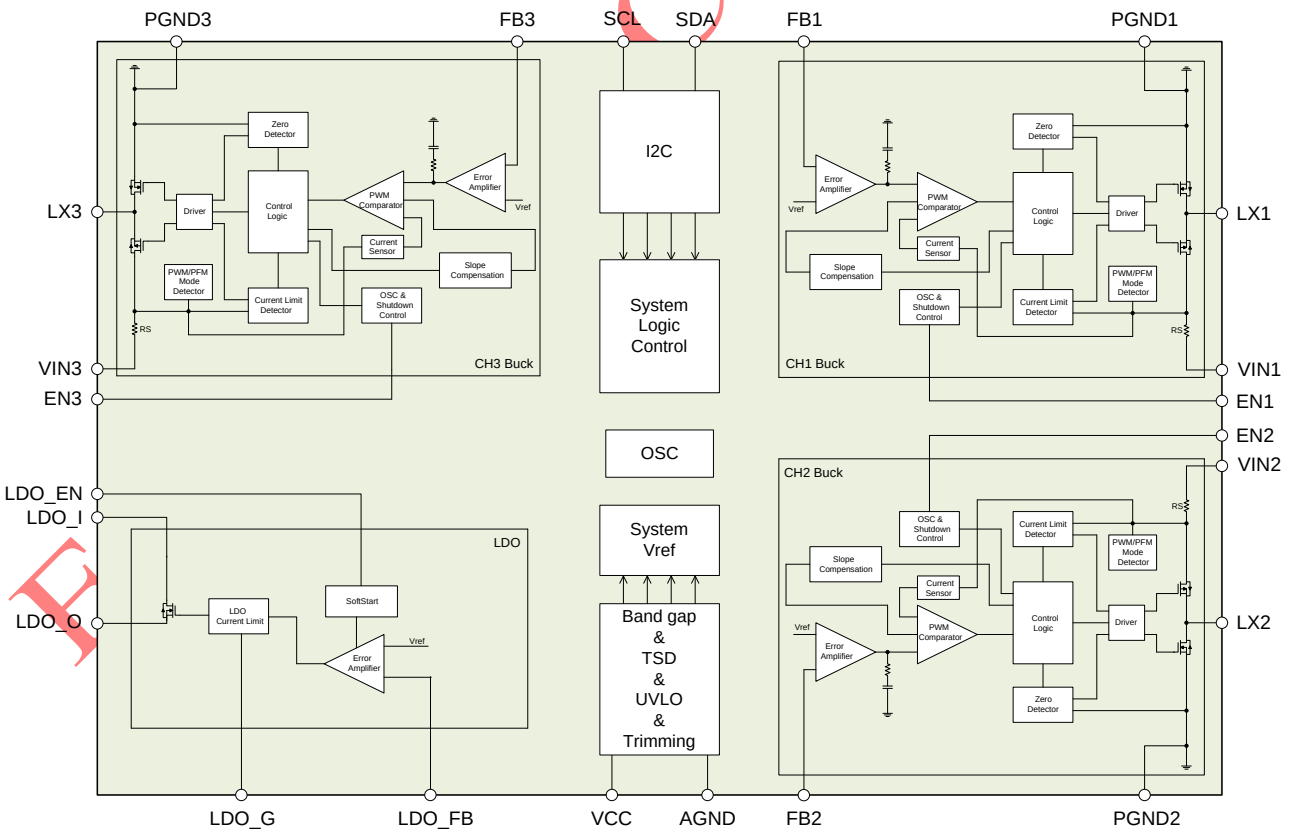


Figure 1. EA3056 internal function block diagram

Absolute Maximum Ratings

Parameter	Value
Input Voltage (V_{VIN1}, V_{VIN2}, V_{VIN3}, V_{LDO_I}, V_{VCC})	-0.3V to +6.5V
LX Pin Voltage (V_{LX1}, V_{LX2}, V_{LX3})	-0.3V to V_{VINX}+0.3V
All Other Pins Voltage	-0.3V to +6.5V
Ambient Temperature operating Range (T_A)	-40°C to +85°C
Maximum Junction Temperature (T_{Jmax})	+150°C
Lead Temperature (Soldering, 10 sec)	+260°C
Storage Temperature Range (T_S)	-65°C to +150°C

Note (1): Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability and lifetime.

Package Thermal Characteristics

Parameter	Value
QFN 4x4-24 Thermal Resistance (θ_{JC})	7.5°C/W
QFN 4x4-24 Thermal Resistance (θ_{JA})	50°C/W
QFN 4x4-24 Power Dissipation at T_A=25°C (P_{Dmax})	2.5W

Note (1): P_{Dmax} is calculated according to the formula: $P_{DMAX}=(T_{JMAX}-T_A)/\theta_{JA}$.

Recommended Operating Conditions

Parameter	Value
Input Voltage (V_{VIN1}, V_{VIN2}, V_{VIN3}, V_{LDO_I}, V_{VCC})	+2.7V to +5.5V
Junction Temperature Range (T_J)	-40°C to +125°C

Electrical Characteristics

V_{VINX}=5V, V_{VCC}=5V, T_A=25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply Voltage						
Input Voltage	V_{INX}		2.7		5.5	V
Control Circuit Input Voltage	V_{VCC}		2.7		5.5	V
Buck Converter 1						
Shutdown Supply Current	I_{SD1}	V_{EN1} = 0V		0.1	1	uA
Quiescent Current	I_{Q1}	Non-switching, No Load		100	150	uA
UVLO Threshold	V_{UVLO1}	V_{VIN1} Rising	1.7	2.0	2.2	V
UVLO Hysteresis	$V_{UV-HYST1}$			0.2		V
Input OVP Threshold	V_{OVP1}	V_{VIN1} Rising		6.4		V
Input OVP Hysteresis	$V_{OVP-HYST1}$			0.15		V
Output Load Current	I_{LOAD1}				3	A
Reference Voltage	V_{REF1}		0.588	0.6	0.612	V
Reference Voltage Range		VID control, 5mV steps	0.58		0.8	V
Switching Frequency	F_{SW1}	I_{LOAD1} = 300mA	1.2	1.5	1.8	MHz
PMOS Current Limit	I_{LIM1-P}		4.5	5.5		A
PMOS On-Resistance	$R_{DS(ON)1-P}$	I_{LOAD1} = 300mA		100		mΩ
NMOS On-Resistance	$R_{DS(ON)1-N}$	I_{LOAD1} = 300mA		70		mΩ
Enable Pin Input Low Voltage	V_{EN1-L}				0.4	V
Enable Pin Input High Voltage	V_{EN1-H}		2			V
Maximum Duty Cycle	D_{MAX1}		100			%
Minimum On Time	$T_{ON1(MIN)}$			50		ns
Buck Converter 2						
Shutdown Supply Current	I_{SD2}	V_{EN2} = 0V		0.1	1	uA
Quiescent Current	I_{Q2}	Non-switching, No Load		100	150	uA
UVLO Threshold	V_{UVLO2}	V_{VIN2} Rising	1.7	2.0	2.2	V
UVLO Hysteresis	$V_{UV-HYST2}$			0.2		V
Input OVP Threshold	V_{OVP2}	V_{VIN2} Rising		6.4		V

Electrical Characteristics

V_{VINX}=5V, V_{VCC}=5V, T_A=25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input OVP Hysteresis	$V_{OVP-HYST2}$			0.15		V
Output Load Current	I_{LOAD2}				1.5	A
Reference Voltage	V_{REF2}		0.588	0.6	0.612	V
Reference Voltage Range		VID control, 5mV steps	0.58		0.8	V
Switching Frequency	F_{SW2}	I_{LOAD1} = 300mA	1.2	1.5	1.8	MHz
PMOS Current Limit	I_{LIM1-P}		2.5	3		A
PMOS On-Resistance	$R_{DS(ON)2-P}$	I_{LOAD} = 300mA		130		mΩ
NMOS On-Resistance	$R_{DS(ON)2-N}$	I_{LOAD} = 300mA		100		mΩ
Enable Pin Input Low Voltage	V_{EN2-L}				0.4	V
Enable Pin Input High Voltage	V_{EN2-H}		2			V
Maximum Duty Cycle	D_{MAX2}		100			%
Minimum On Time	$T_{ON2(MIN)}$			50		ns
Buck Converter 3						
Shutdown Supply Current	I_{SD3}	V_{EN3} = 0V		0.1	1	uA
Quiescent Current	I_{Q3}	Non-switching, No Load		100	150	uA
UVLO Threshold	V_{UVLO3}	V_{VIN1} Rising	1.7	2.0	2.2	V
UVLO Hysteresis	$V_{UV-HYST3}$			0.2		V
Input OVP Threshold	V_{OVP3}	V_{VIN1} Rising		6.4		V
Input OVP Hysteresis	$V_{OVP-HYST3}$			0.15		V
Output Load Current	I_{LOAD3}				2	A
Reference Voltage	V_{REF3}		0.588	0.6	0.612	V
Reference Voltage Range		VID control, 5mV steps	0.58		0.8	V
Switching Frequency	F_{SW3}	I_{LOAD1} = 300mA	1.2	1.5	1.8	MHz
PMOS Current Limit	I_{LIM3-P}		3	4		A
PMOS On-Resistance	$R_{DS(ON)3-P}$	I_{LOAD1} = 300mA		100		mΩ
NMOS On-Resistance	$R_{DS(ON)3-N}$	I_{LOAD1} = 300mA		90		mΩ
Enable Pin Input Low Voltage	V_{EN3-L}				0.4	V

Electrical Characteristics

V_{VINX}=5V, V_{VCC}=5V, T_A=25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Pin Input High Voltage	V_{EN3-H}		2			V
Maximum Duty Cycle	D_{MAX3}		100			%
Minimum On Time	$T_{ON3(MIN)}$			50		ns
LDO Regulator						
Standby Current	I_{ST}	LDO_EN short to GND		0.1	1	uA
Quiescent Current	I_{Q_LDO}	I_{OUT} = 0A		100	150	uA
Current Limit	I_{LIM_LDO}		1			A
Feedback Voltage	V_{FB_LDO}		0.588	0.6	0.612	V
Reference Voltage Range		VID control, 5mV steps	0.58		0.8	V
Dropout Voltage	V_{DROP}	I_{OUT} = 300mA		50	65	mV
Power Supply Rejection Rate	PSRR	f = 10KHz, I_{OUT} = 10mA		65		dB
Enable Pin Input Low Voltage	V_{EN_LDO-L}				0.4	V
Enable Pin Input High Voltage	V_{EN_LDO-H}		1.5			V
Thermal Shutdown						
Thermal Shutdown Threshold	T_{OTP}			160		°C
Thermal Shutdown Hysteresis	T_{HYST}			30		°C
I^2C Interface						
Device Address					35H	
Input High Voltage	V_{IH}		1.5			V
Input Low Voltage	V_{IL}				0.4	V
SDA Output Low Voltage	V_{OL_SDA}	Open drain, Sink current = 3mA			0.4	V

Application Circuit Diagram

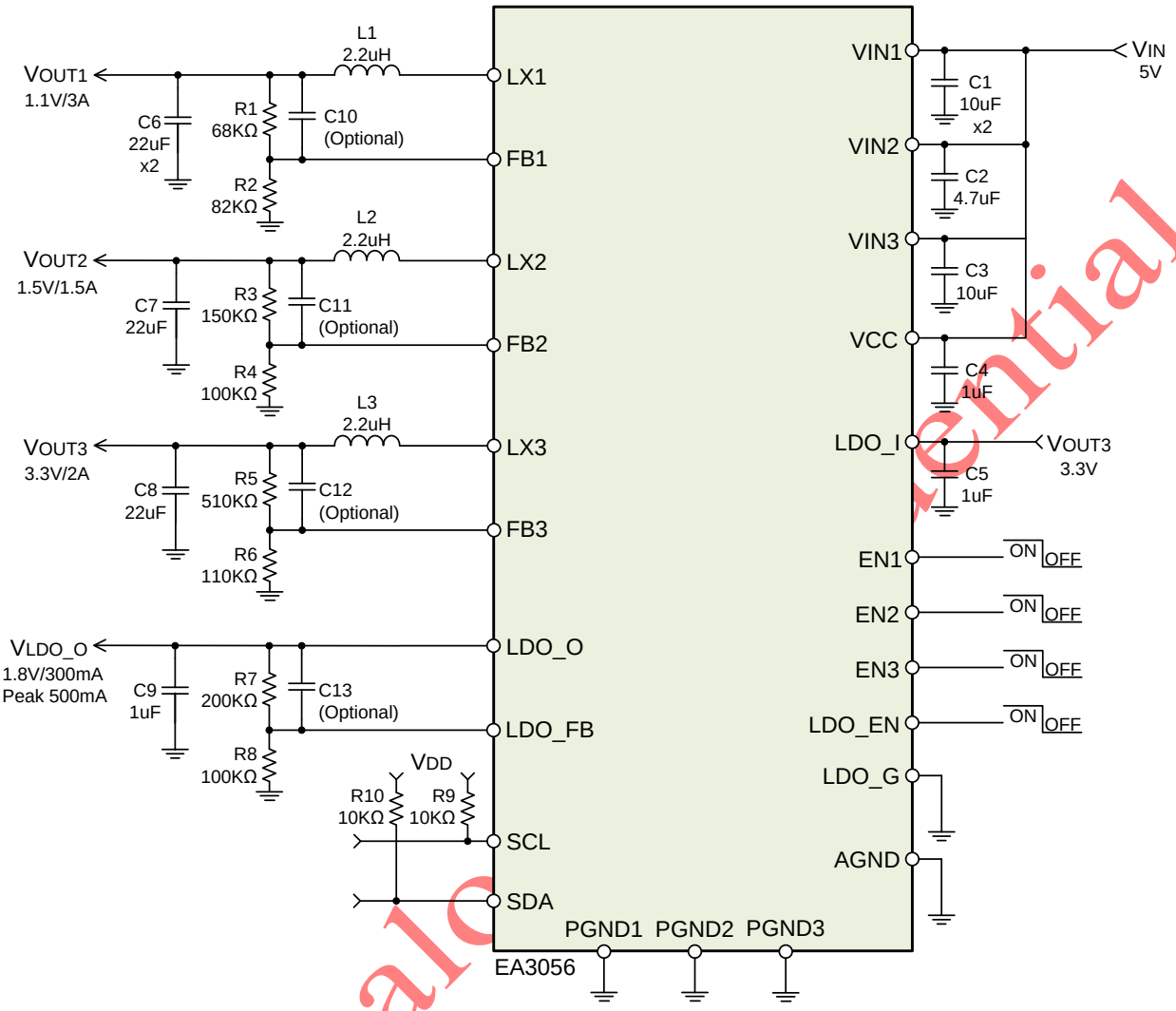


Figure 2. Typical application circuit diagram

Ordering Information

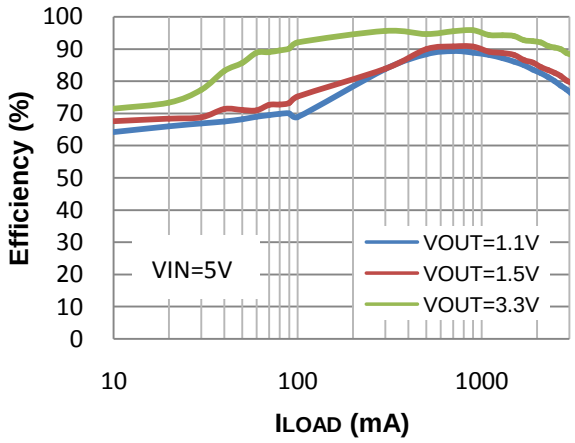
Part Number	Package Type	Packing Information
EA3056QDR	QFN 4mm x 4mm-24	Tape & Reel / 3000

Note (1):"QD": Package type code.
(2):"R": Tape & Reel.

Typical Operating Characteristics

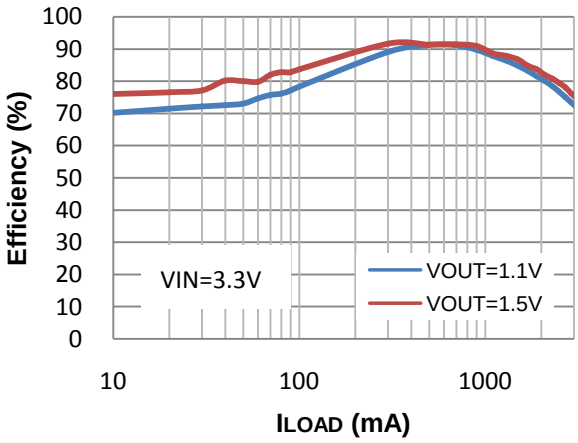
V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.1V, V_{OUT2}=1.5V, V_{OUT3}=3.3V, V_{LDO}=1.8V, L1=2.2uH, L2=2.2uH, L3=2.2uH, T_A=25°C, unless otherwise noted

Efficiency vs. Load Current



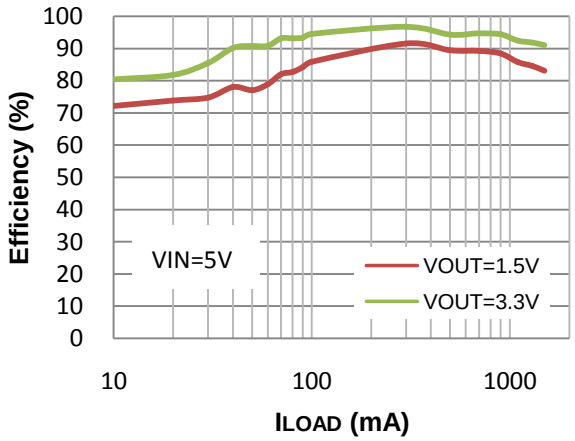
CH1 Buck Converter Efficiency Curve

Efficiency vs. Load Current



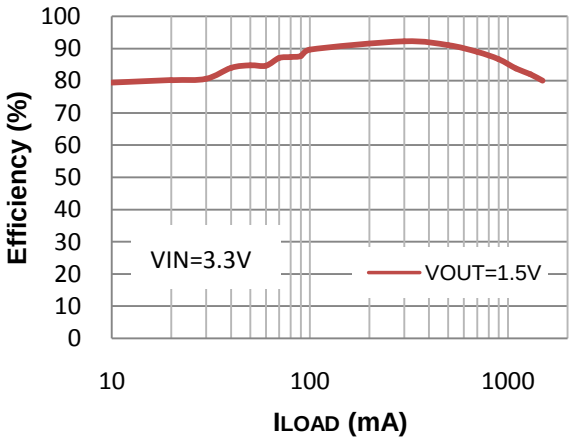
CH1 Buck Converter Efficiency Curve

Efficiency vs. Load Current



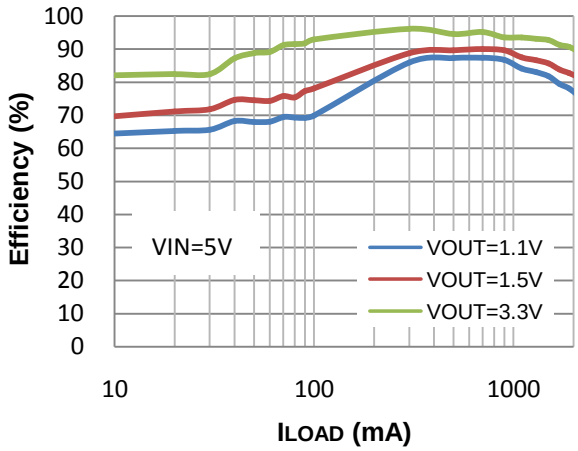
CH2 Buck Converter Efficiency Curve

Efficiency vs. Load Current



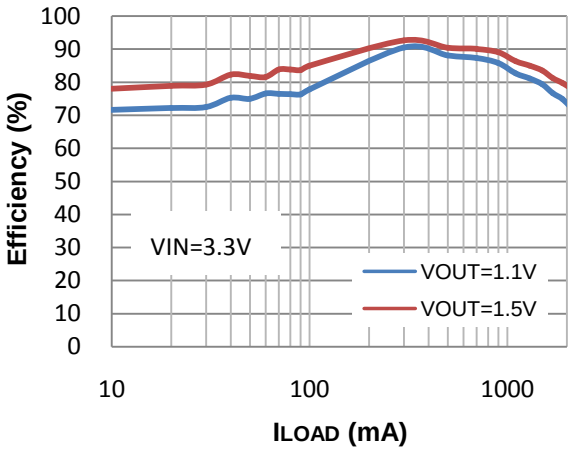
CH2 Buck Converter Efficiency Curve

Efficiency vs. Load Current



CH3 Buck Converter Efficiency Curve

Efficiency vs. Load Current

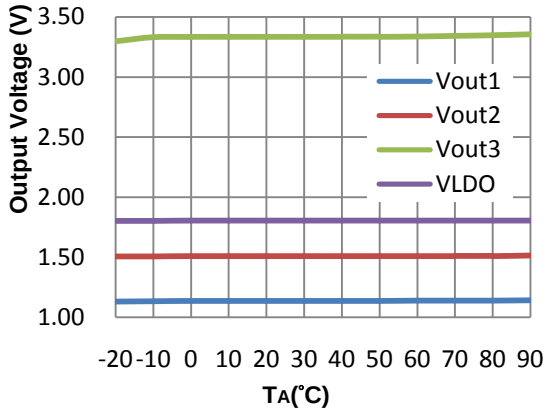


CH3 Buck Converter Efficiency Curve

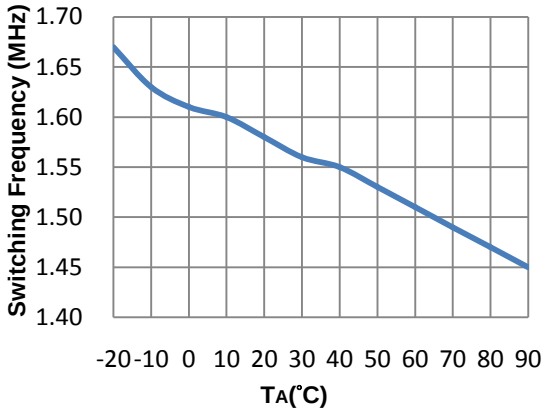
Typical Operating Characteristics

V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.1V, V_{OUT2}=1.5V, V_{OUT3}=3.3V, V_{LDO}=1.8V, L1=2.2uH, L2=2.2uH, L3=2.2uH, T_A=25°C, unless otherwise noted

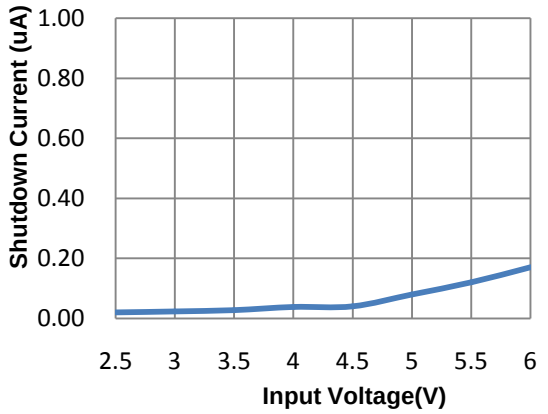
Output Voltage vs. TA



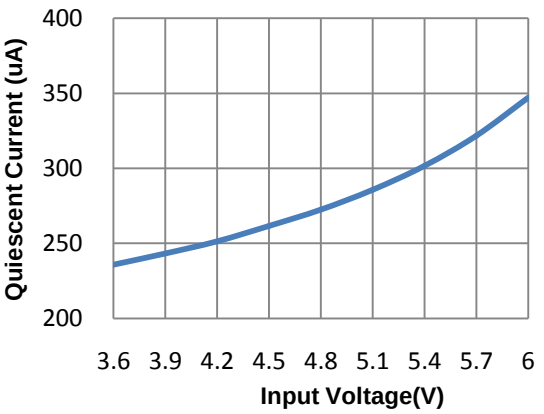
Switching Frequency vs. TA

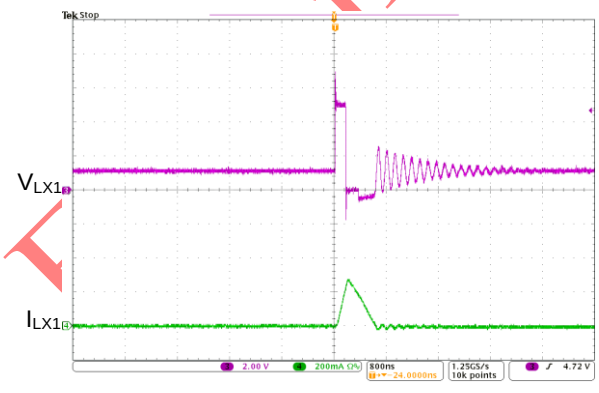


Shutdown Current vs. VIN

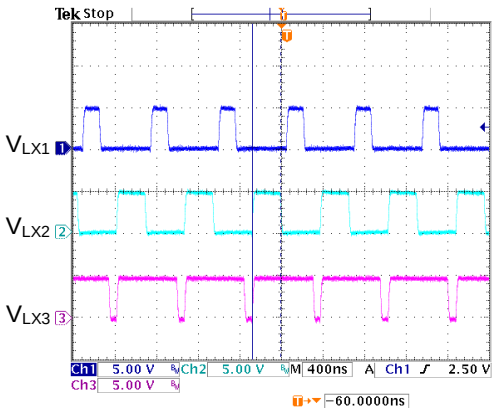


Quiescent Current vs. VIN





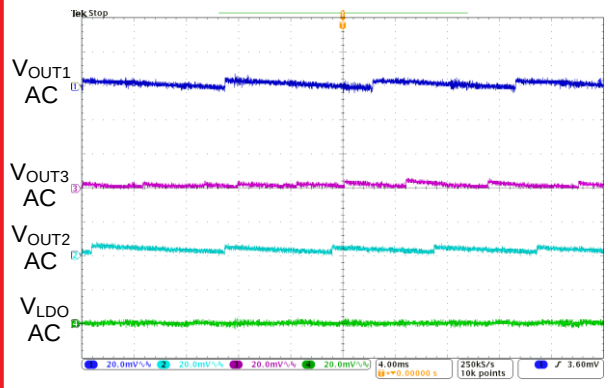
0A Loading LX1 Waveform



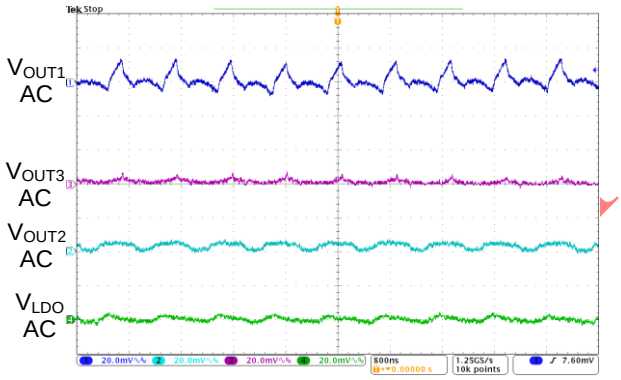
1A Loading LX Waveform

Typical Operating Characteristics

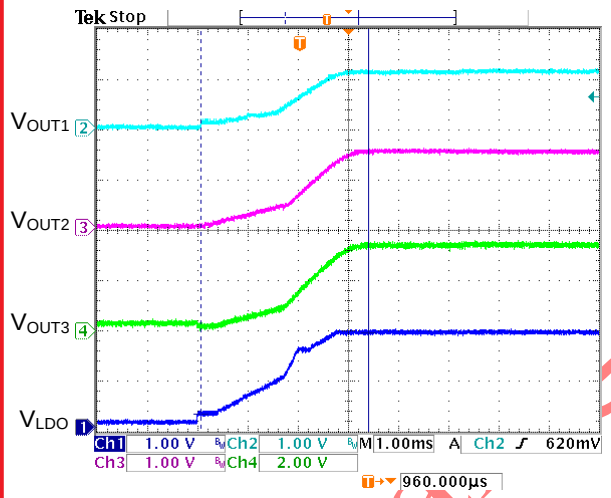
V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.1V, V_{OUT2}=1.5V, V_{OUT3}=3.3V, V_{LDO}=1.8V, L1=2.2uH, L2=2.2uH, L3=2.2uH, T_A=25°C, unless otherwise noted



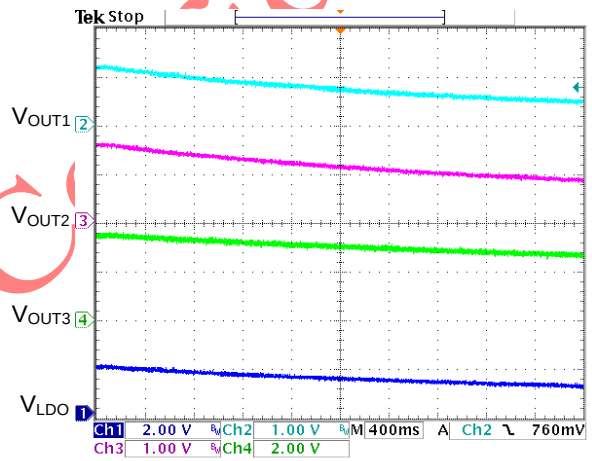
0A Loading Steady State Waveform



1A Loading Steady State Waveform



0A Loading I2C Control EN Turn On Waveform



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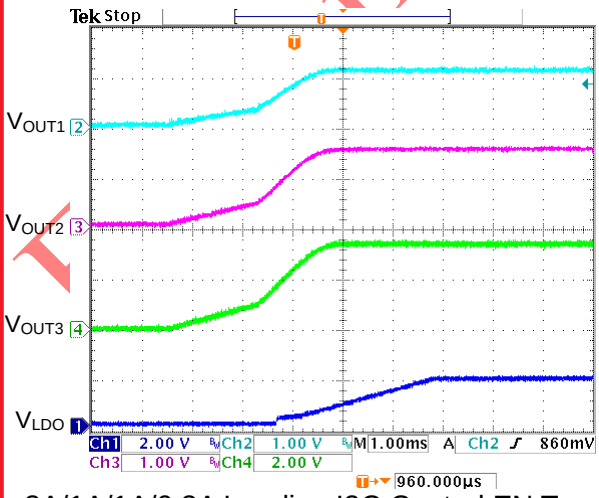
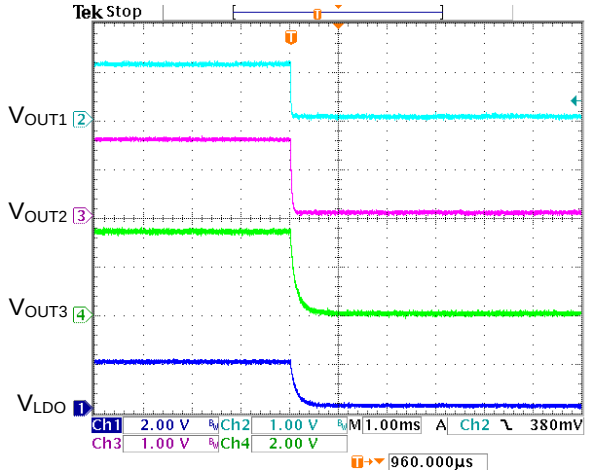


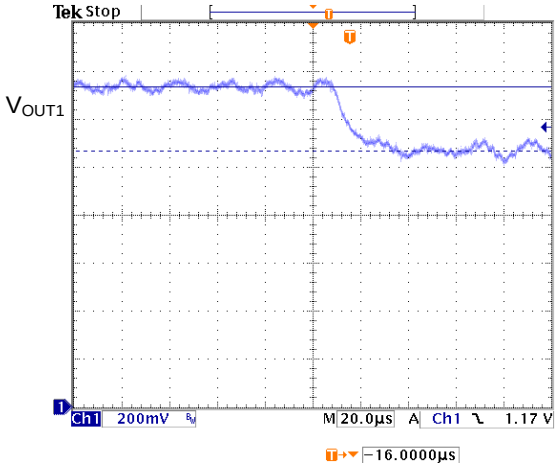
3A/1A/1A/0.3A Loading I2C Control EN Turn On Waveform



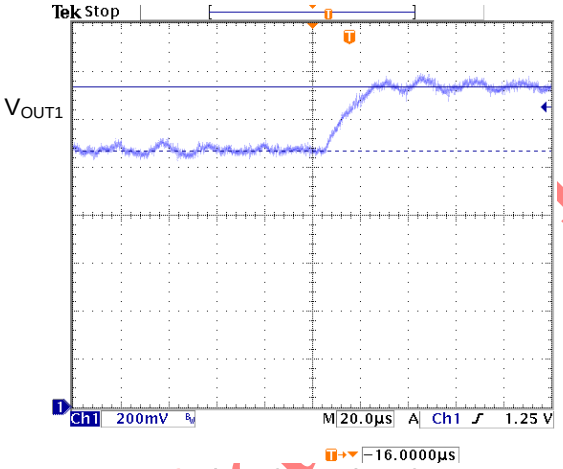
3A/1A/1A/0.3A Loading I2C Control EN Turn Off Waveform

Typical Operating Characteristics

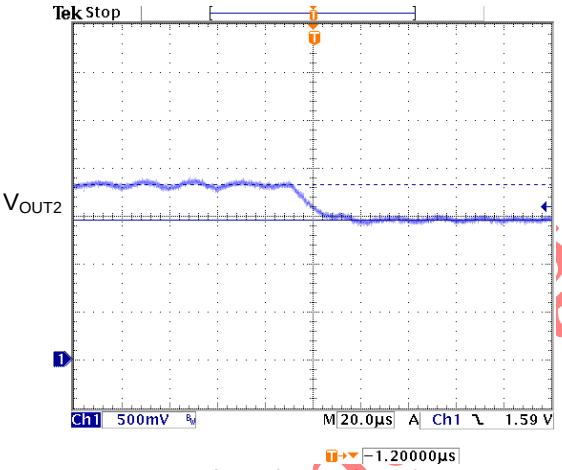
V_{IN}=5V, V_{VCC}=5V, V_{OUT1}=1.1V, V_{OUT2}=1.5V, V_{OUT3}=3.3V, V_{LDO}=1.8V, L1=2.2uH, L2=2.2uH, L3=2.2uH, T_A=25°C, unless otherwise noted



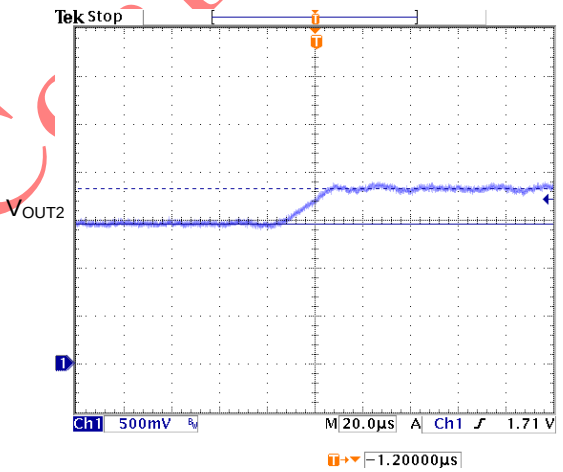
CH1 I2C Control Vref transient from 0.735V to 0.585V with 3A Loading



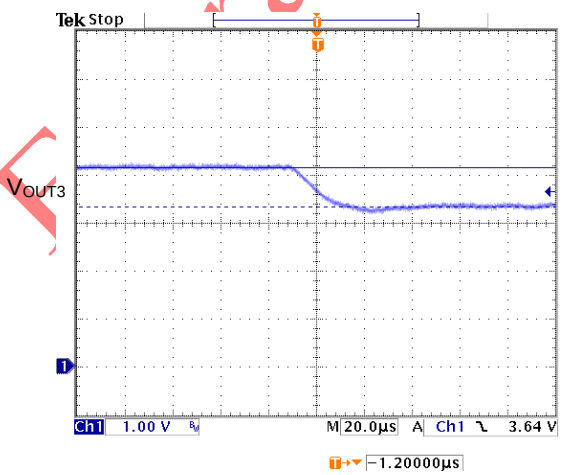
CH1 I2C Control Vref transient from 0.585V to 0.735V with 3A Loading



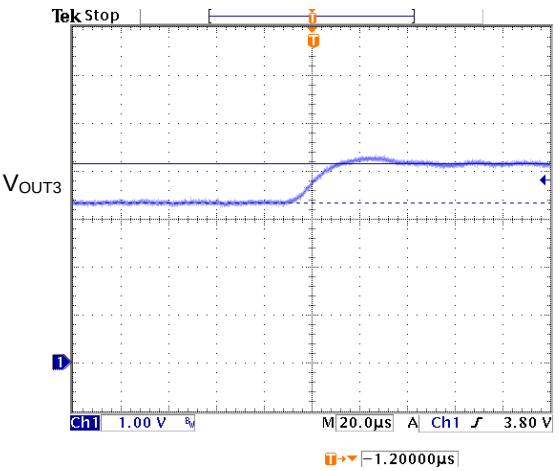
CH2 I2C Control Vref transient from 0.735V to 0.585V with 1.5A Loading



CH2 I2C Control Vref transient from 0.585V to 0.735V with 1.5A Loading



CH3 I2C Control Vref transient from 0.735V to 0.585V with 1A Loading



CH3 I2C Control Vref transient from 0.585V to 0.735V with 1A Loading

Functional Description

Output Voltage Setting

The EA3056 buck regulator each channel output voltage and LDO output voltage can be set by using external resistor dividers. The initial reference voltage is 0.6V. Once the voltage identification VID data is set via the I^{2}C interface, the reference voltage can be programmed from 0.58V to 0.8V in 5mV steps.

Short Circuit Protection

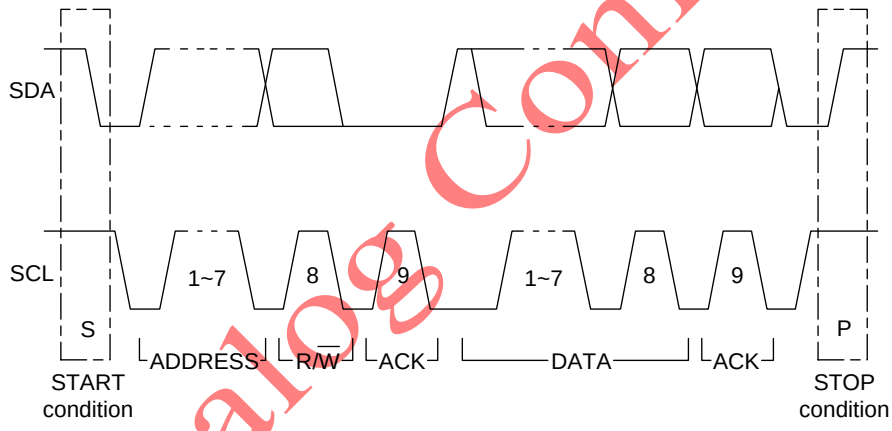
The EA3056 buck regulator enters short circuit operation mode once the FB voltage is below 60% of the reference voltage. The short operation architecture is hiccup mode.

Out of Phase Operation

The EA3056 buck regulators operate at 180° out of phase architecture and can reduce input ripple current.

I^{2}C Control Mode Description

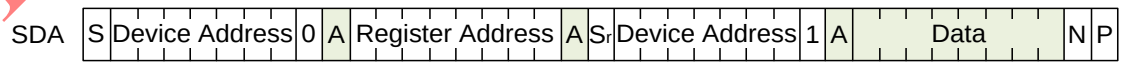
The EA3056 works as a slave device and supports standard and fast modes I^{2}C protocol. The I^{2}C pspecification is shown as below:



The EA3056 has a 7-bit address 35H (0110101) and the command format is shown as below:

I^{2}C Write Data Format:

I^{2}C Read Data Format:



S: START
A: ACK
Sr: Rep. START
☐: Master Chip

P: STOP
N: NACK

☐: Slave Device

Each channel of the buck regulator and the LDO can be I^{2}C controlled for enabling/disabling output voltage and setting the output voltage.

When the EA3056 is shutdown by hardware controlling (EN1, EN2, EN3, EN_LDO pin short to ground), the software enabling/disabling control is not functional.

Register Map:

Address	Name	R/W	Default	Description
00H	EN_Ctrl	R/W	XFH	CH1~CH3 and LDO disable control
01H	Vref1_Set	R/W	00H	Setting CH1 reference voltage
02H	Vref2_Set	R/W	00H	Setting CH2 reference voltage
03H	Vref3_Set	R/W	00H	Setting CH3 reference voltage
04H	Vldo_ref_Set	R/W	00H	Setting LDO reference voltage

EN Pins Disable Control Register:

Address	Name	Bit	R/W	Default	Description
00H	EN1_Ctrl	0	R/W	0	CH1 disable control (0: enable, 1: disable)
	EN2_Ctrl	1	R/W	0	CH2 disable control (0: enable, 1: disable)
	EN3_Ctrl	2	R/W	0	CH3 disable control (0: enable, 1: disable)
	LDOEN_Ctrl	3	R/W	0	LDO disable control (0: enable, 1: disable)
		4			Reserved
		5			Reserved
		6			Reserved
		7			Reserved

V_{ref1} Reference Voltage Setting Register:

Address	Name	Bit	R/W	Default	Description
01H	V_{ref1}_0	0	R/W	0	V_{ref1} voltage setting bit 0
	V_{ref1}_1	1	R/W	0	V_{ref1} voltage setting bit 1
	V_{ref1}_2	2	R/W	0	V_{ref1} voltage setting bit 2
	V_{ref1}_3	3	R/W	0	V_{ref1} voltage setting bit 3
	V_{ref1}_4	4	R/W	0	V_{ref1} voltage setting bit 4
	V_{ref1}_5	5	R/W	0	V_{ref1} voltage setting bit 5
	V_{ref1}_6	6	R/W	0	Set “1” to enable I^{2}C voltage control
	V_{ref1}_7	7			Reserved

V_{ref2} Reference Voltage Setting Register:

Address	Name	Bit	R/W	Default	Description
02H	V_{ref2}_0	0	R/W	0	V_{ref2} voltage setting bit 0
	V_{ref2}_1	1	R/W	0	V_{ref2} voltage setting bit 1
	V_{ref2}_2	2	R/W	0	V_{ref2} voltage setting bit 2
	V_{ref2}_3	3	R/W	0	V_{ref2} voltage setting bit 3
	V_{ref2}_4	4	R/W	0	V_{ref2} voltage setting bit 4
	V_{ref2}_5	5	R/W	0	V_{ref2} voltage setting bit 5
	V_{ref2}_6	6	R/W	0	Set “1” to enable I^2C voltage control
	V_{ref2}_7	7			Reserved

V_{ref3} Reference Voltage Setting Register:

Address	Name	Bit	R/W	Default	Description
03H	V_{ref3}_0	0	R/W	0	V_{ref3} voltage setting bit 0
	V_{ref3}_1	1	R/W	0	V_{ref3} voltage setting bit 1
	V_{ref3}_2	2	R/W	0	V_{ref3} voltage setting bit 2
	V_{ref3}_3	3	R/W	0	V_{ref3} voltage setting bit 3
	V_{ref3}_4	4	R/W	0	V_{ref3} voltage setting bit 4
	V_{ref3}_5	5	R/W	0	V_{ref3} voltage setting bit 5
	V_{ref3}_6	6	R/W	0	Set “1” to enable I^2C voltage control
	V_{ref3}_7	7			Reserved

V_{ldo_ref} LDO Reference Voltage Setting Register:

Address	Name	Bit	R/W	Default	Description
04H	V_{ldo_ref}_0	0	R/W	0	V_{ldo_ref} voltage setting bit 0
	V_{ldo_ref}_1	1	R/W	0	V_{ldo_ref} voltage setting bit 1
	V_{ldo_ref}_2	2	R/W	0	V_{ldo_ref} voltage setting bit 2
	V_{ldo_ref}_3	3	R/W	0	V_{ldo_ref} voltage setting bit 3
	V_{ldo_ref}_4	4	R/W	0	V_{ldo_ref} voltage setting bit 4
	V_{ldo_ref}_5	5	R/W	0	V_{ldo_ref} voltage setting bit 5
	V_{ldo_ref}_6	6	R/W	0	Set “1” to enable I^2C voltage control
	V_{ldo_ref}_7	7			Reserved

$V_{ref1}/V_{ref2}/V_{ref3}/V_{ldo\_ref}$ Reference Voltage Setting Table

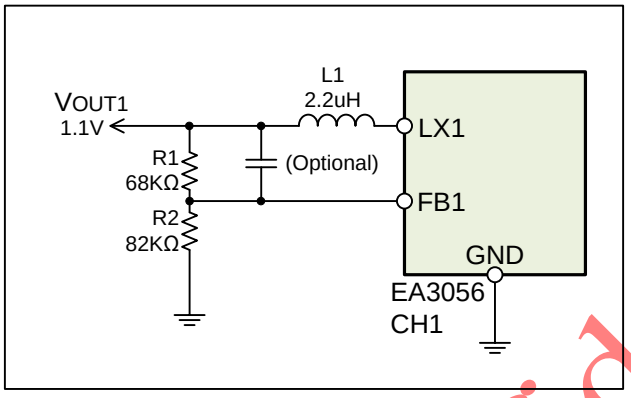
V_{REFX} [6:0]	V_{REFX} Voltage (V)	V_{REFX} [6:0]	V_{REFX} Voltage (V)
40H	0.580	60H	0.740
41H	0.585	61H	0.745
42H	0.590	62H	0.750
43H	0.595	63H	0.755
44H	0.600	64H	0.760
45H	0.605	65H	0.765
46H	0.610	66H	0.770
47H	0.615	67H	0.775
48H	0.620	68H	0.780
49H	0.625	69H	0.785
4AH	0.630	6AH	0.790
4BH	0.635	6BH	0.795
4CH	0.640	6CH	0.800
4DH	0.645		
4EH	0.65		
4FH	0.655		
50H	0.66		
51H	0.665		
52H	0.670		
53H	0.675		
54H	0.680		
55H	0.685		
56H	0.690		
57H	0.695		
58H	0.700		
59H	0.705		
5AH	0.710		
5BH	0.715		
5CH	0.720		
5DH	0.725		
5EH	0.730		
5FH	0.735		

Application Information

Output Voltage Setting

Each of the regulators default output voltage can be set via a resistor divider (ex. R1, R2). The output voltage is calculated by following equation:

$$V_{OUT1} = 0.6 \times \frac{R1}{R2} + 0.6\ V$$



The following table lists common output voltage and the corresponding R1, R2 resistance value for reference.

Output Voltage	R1 Resistance	R2 Resistance	Tolerance
3.3V	510KΩ	110KΩ	1%
1.8V	200KΩ	100KΩ	1%
1.5V	150KΩ	100KΩ	1%
1.1V	68KΩ	82KΩ	1%

Input / Output Capacitors Selection

The input capacitors are used to suppress the noise amplitude of the input voltage and provide a stable and clean DC input to the device. Because the ceramic capacitor has low ESR characteristic, so it is suitable for input capacitor use. It is recommended to use X5R or X7R MLCC capacitors in order to have better temperature performance and smaller capacitance tolerance. In order to suppress the output voltage ripple, the MLCC capacitor is also the best choice. The suggested part numbers of input / output capacitors are as follows:

Vendor	Part Number	Capacitance	Edc	Parameter	Size
TDK	C2012X5R1A106M	10uF	10V	X5R	0805
TDK	C3216X5R1A106M	10uF	10V	X5R	1206
TDK	C2012X5R1A226M	22uF	10V	X5R	0805
TDK	C3216X5R1A226M	22uF	10V	X5R	1206

Output Inductor Selection

The output inductor selection mainly depends on the amount of ripple current through the inductor ΔI_L. Large ΔI_L will cause larger output voltage ripple and loss, but the user can use a smaller inductor to save cost and space. On the contrary, the larger inductance can get smaller ΔI_L and

thus the smaller output voltage ripple and loss. But it will increase the space and the cost. The inductor value can be calculated as:

$$L = \frac{V_{PWR} - V_{OUT}}{\Delta I_L \times F_{SW}} \times \frac{V_{OUT}}{V_{PWR}}$$

For most applications, 1.0uH to 2.2uH inductors are suitable for EA3056.

Power Dissipation

The total output power dissipation of EA3056 should not to exceed the maximum 10W range. The total output power dissipation can be calculated as:

$$P_{D(total)} = V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2} + V_{OUT3} \times I_{OUT3} + V_{OUT4} \times I_{OUT4}$$

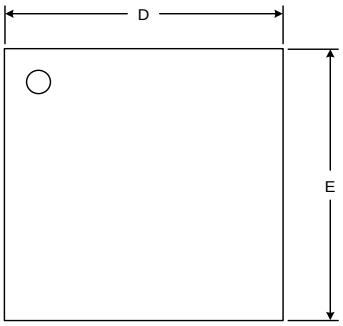
PCB Layout Recommendations

Layout is very critical for PMIC designs. For EA3056 PCB layout considerations, please refer to the following suggestions to get best performance.

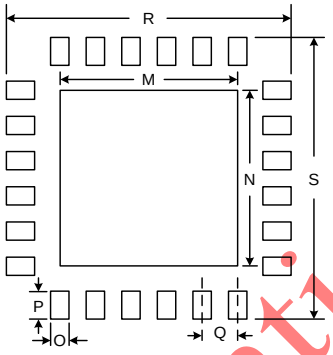
- It is suggested to use 4-layer PCB layout and place LX plane and output plane on the top layer, place VIN plane in the inner layer.
- The top layer SMD input and output capacitors ground plane should be connected to the internal ground layer and bottom ground plane individually by using vias.
- The AGND should be connected to inner ground layer directly by using via.
- High current path traces need to be widened.
- Place the input capacitors as close as possible to the VINx pin and VCC pin to reduce noise interference.
- Keep the feedback path (from V_{OUTX} to FBx) away from the noise node (ex. LXx). LXx is a high current noise node. Complete the layout by using short and wide traces.
- The top layer exposed pad ground plane should be connected to the internal ground layer and bottom ground plane by using a number of vias to improve thermal performance.

Package Information

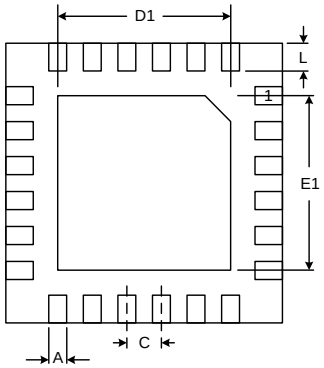
QFN 4mm x 4mm-24 Package



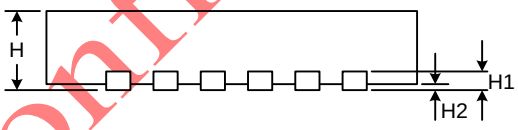
Top View



Recommended Layout Pattern



Bottom View



Side View

Unit: mm

Symbol	Dimension Min	Dimension Max	Symbol	Dimension Typ
A	0.18	0.30	M	2.60
C	0.45	0.55	N	2.60
D	3.95	4.05	O	0.30
E	3.95	4.05	P	0.80
D1	2.30	2.70	Q	0.50
E1	2.30	2.70	R	4.70
L	0.35	0.45	S	4.70
H	0.80	1.00		
H1	0.17	0.25		
H2	0.00	0.05		

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