

High Performance PDM Stereo Audio ADC

FEATURES

- High performance advanced delta-sigma audio ADC
- 90 dB dynamic range at 26 dB PGA
- -85 dB THD+N
- Low noise PGA
- 8 to 96 kHz sampling frequency
- Low power

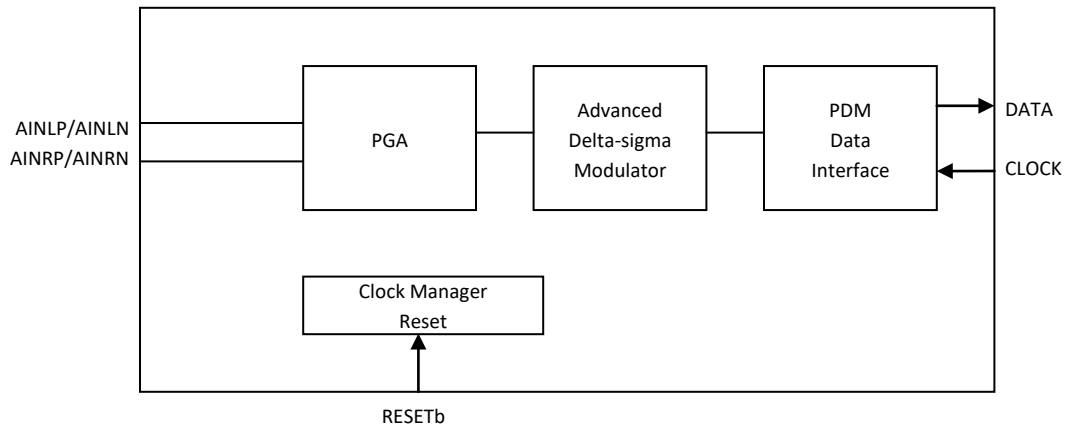
APPLICATIONS

- Mic Array
- Soundbar
- Audio Interface
- Digital TV
- A/V Receiver
- DVR
- NVR

ORDERING INFORMATION

ES7201 -40°C ~ +85°C
QFN-12

BLOCK DIAGRAM



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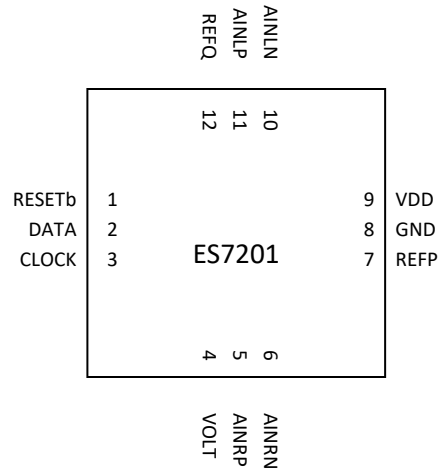
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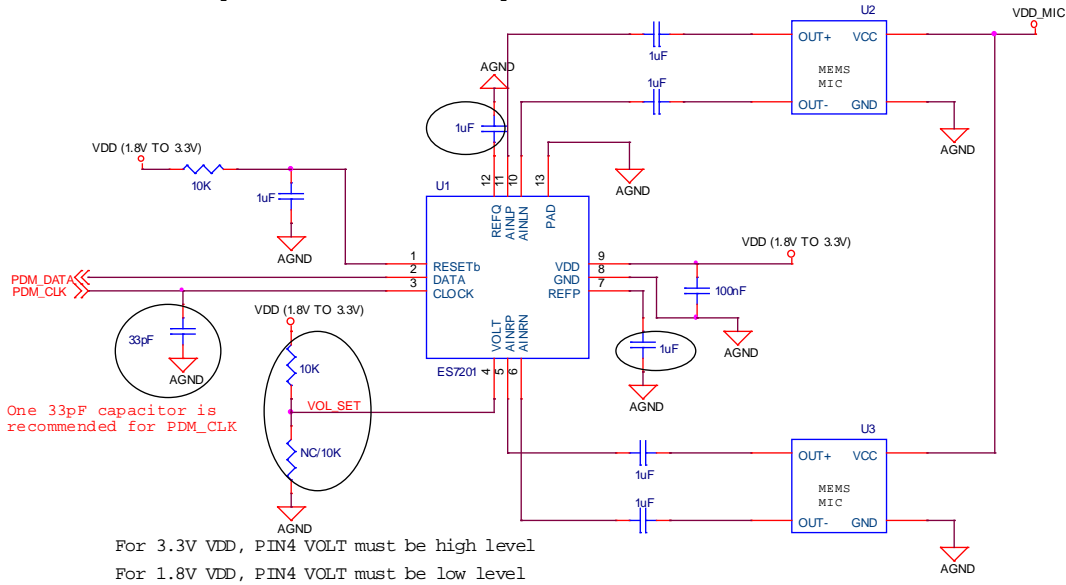
1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
DATA, CLOCK	2, 3	O, I	PDM clock and data
RESETb	1	I	Active low reset
VOLT	4	I	High: VDD = 3.3V Low: VDD = 1.8V
AINLP, AINLN	11,10	I	Analog left inputs
AINRP, AINRN	5, 6	I	Analog right inputs
VDD, GND	9, 8	I	Power supply
REFP	7	O	Filtering capacitor connection
REFQ	12	O	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT

The filter capacitors on REFP and REFQ pins must be located as close to ES7201 package as possible. 4.7uF or 10uF capacitor is for better audio performance.



3. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	GND-0.3V	VDD+0.3V
Digital Input Voltage Range	GND-0.3V	VDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDD	1.7	1.8/3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDD=3.3V, GND=0V, ambient temperature=25°C, CLOCK=6.144 MHz.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Dynamic Range (A-weight, 26 dB PGA)	87	90	93	dB
THD+N (26 dB PGA)	-88	-85	-82	dB
Channel Separation (1KHz)	97	100	103	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Analog Input				
Full Scale Input Level		±0.0708*VDD/3.3		Vrms
Input Impedance		9.6 (23 dB PGA)		KΩ

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDD=3.3V (16 kHz)		22		mW
VDD=1.8V (16 kHz)		4.6		
Power Down Mode		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*VDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		VDD		V
Output Low-level Voltage		0		V

PDM DATA SWITCHING SPECIFICATIONS

PARAMETER		Symbol	MIN	MAX	UNIT
CLOCK frequency			0.512	6.144	MHz
CLOCK duty cycle	≤ 3.072 MHz		40	60	%
DATA valid	VDDD=3.3V	T_{VALID}	11	27	ns
	VDDD=1.8V		19	61	
DATA hold	VDDD=3.3V	T_{HOLD}	10	26	ns
	VDDD=1.8V		18	56	

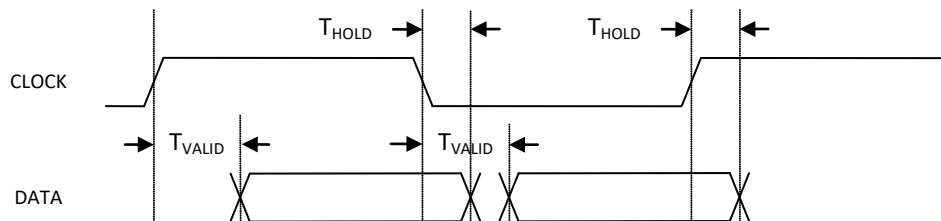
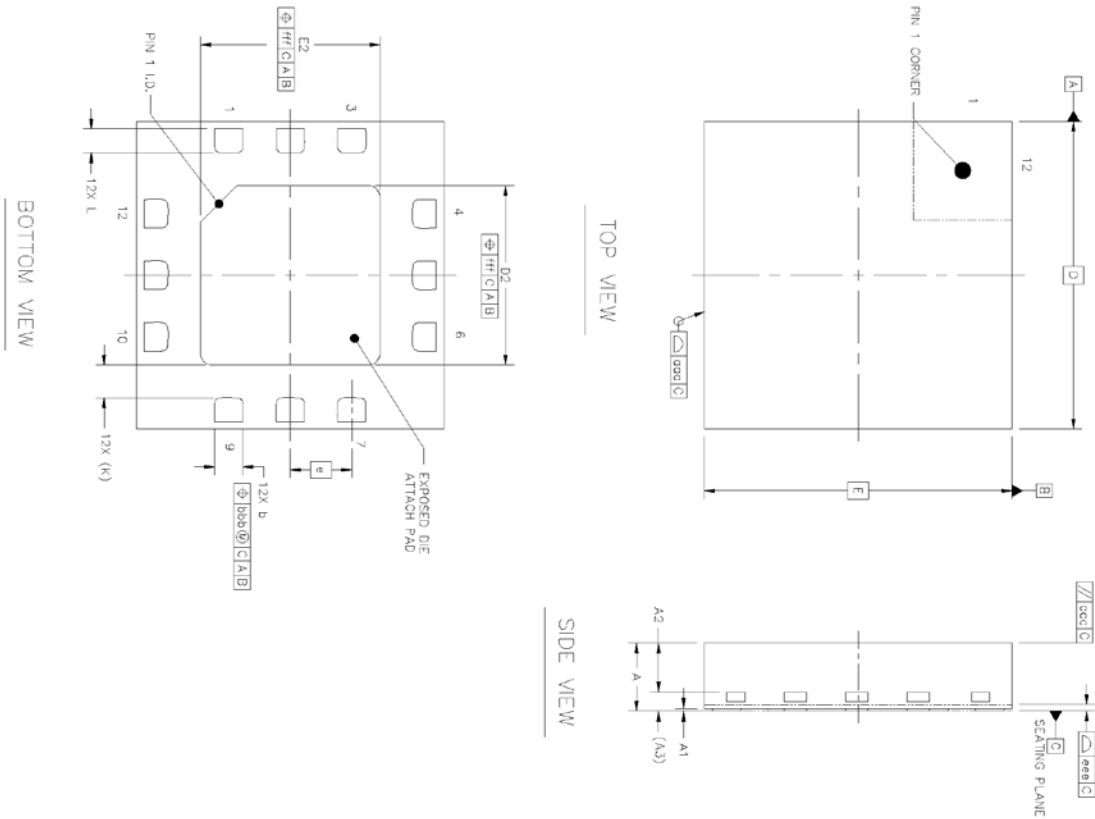


Figure 1 PDM Data Timing

4. PACKAGE (UNIT: MM)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.4	---
L/F THICKNESS	A3	0.15Z REF		
LEAD WIDTH	b	0.18	0.23	0.28
BODY SIZE	X	2.5 BSC		
	Y	2.5 BSC		
LEAD PITCH	X	0.5 BSC		
	Y	0.5 BSC		
EP SIZE	X	1.36	1.46	1.56
	Y	1.36	1.46	1.56
LEAD LENGTH	L	0.1425	0.1925	0.2425
	K	0.265 REF		
LEAD TIP TO EXPOSED PAD EDGE	ccc	0.1		
PACKAGE EDGE TOLERANCE	ddd	0.1		
MOLD FLATNESS	eee	0.05		
COP PLANARITY	fff	0.1		
LEAD OFFSET	bbb	0.1		
EXPOSED PAD OFFSET	fff	0.1		

NOTES
 1:REFER TO JEDEC MO-220;
 2:COP PLANARITY APPLIES TO LEADS, CORNER LE

5. CORPORATE INFORMATION

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