ES7243L

High Performance Stereo Audio ADC

FEATURES

- High performance multi-bit delta-sigma audio ADC
- 101 dB signal to noise ratio
- -90 dB THD+N
- Low noise PGA
- 24-bit, 8 to 96 kHz sampling frequency
- I^2S/PCM master or slave serial data port
- Support TDM up to 16 channels
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- Support digital mic
- Low power

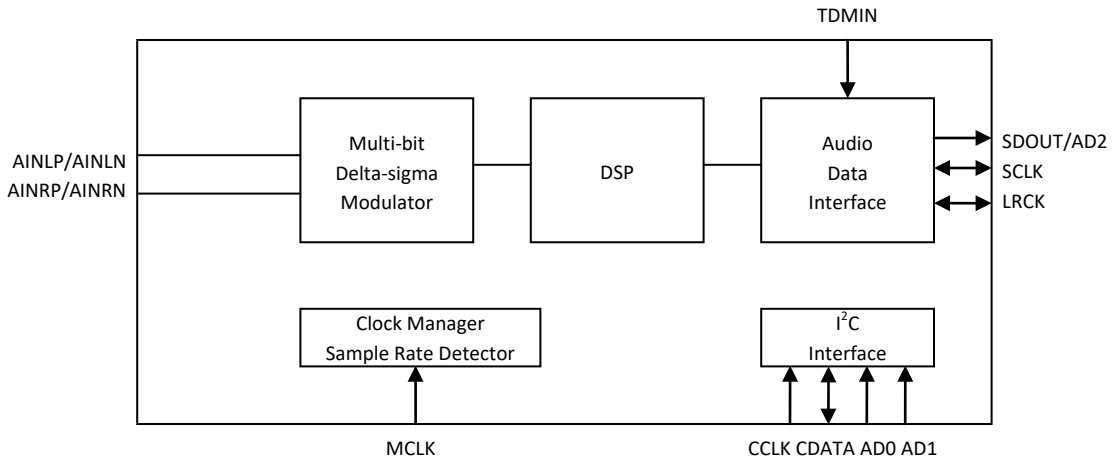
APPLICATIONS

- Mic Array
- Soundbar
- Audio Interface
- Digital TV
- A/V Receiver
- DVR
- NVR

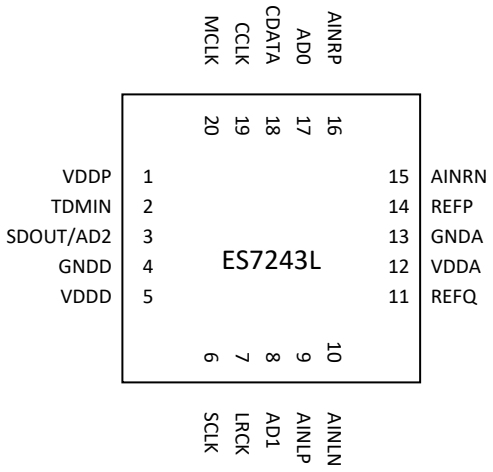
ORDERING INFORMATION

ES7243L -40°C ~ +85°C
QFN-20

BLOCK DIAGRAM

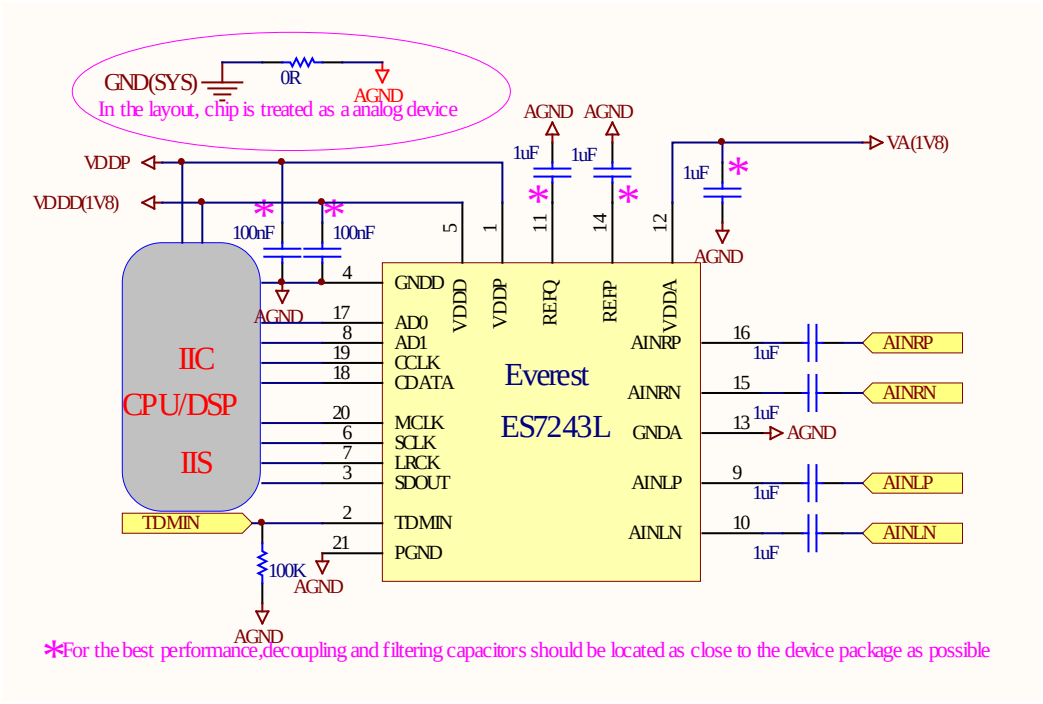


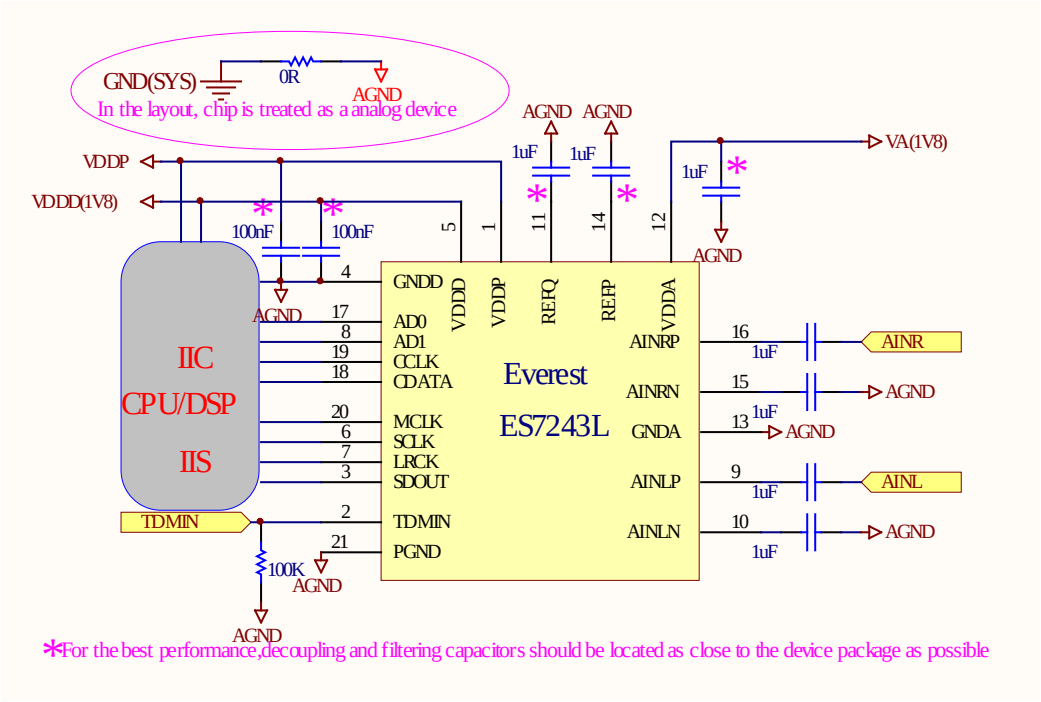
1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA	19, 18	I, I/O	I^2C clock and data
AD0, AD1	17,8	I	I^2C addresses
MCLK	20	I	Master clock
SCLK	6	I/O	Serial data bit clock
LRCK	7	I/O	Serial data left and right channel frame clock
TDMIN	2	I	TDM data in
SDOUT/AD2	3	O	Serial data output/ I^2C address AD2
AINLP, AINLN AINRP, AINRN	9, 10 16, 15	I	Analog left and right inputs MIC1P can be used as digital mic data input
VDDP	1	I	Power supply for the digital input and output
VDDD/GNDD	5, 4	I	Digital power supply
VDDA/GNDA	12, 13	I	Analog power supply
REFP	14	O	Filtering capacitor connection
REFQ	11	O	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT





3. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (25 MHz, 26 MHz, etc).

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

4. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0010 x, where x equals AD2 AD1 AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0010 AD2 AD1 AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

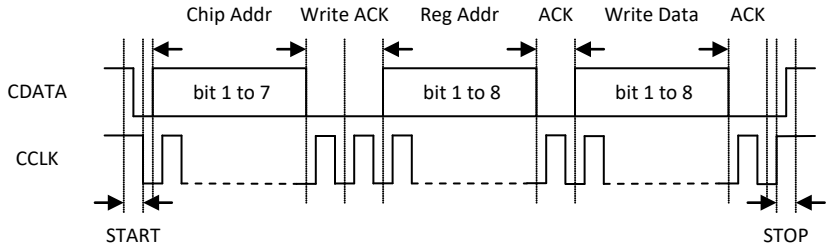


Figure 1a I^{2}C Write Timing

Table 2 Read Data from Register in I^{2}C Interface Mode

	Chip Address	R/W		Register Address		
Start	0010 AD2 AD1 AD0	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0010 AD2 AD1 AD0	1	ACK	Data	NACK	Stop

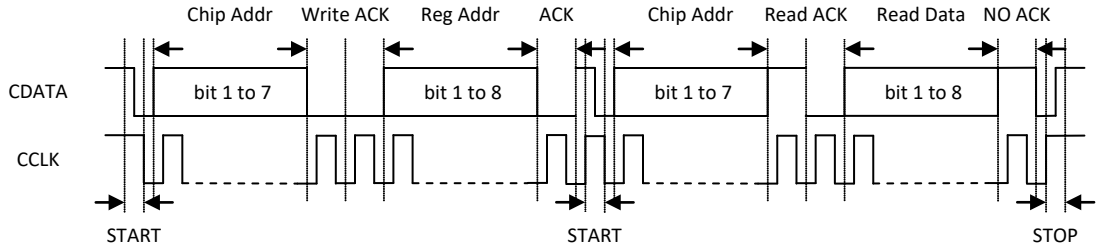


Figure 1b I^{2}C Read Timing

5. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the output from the ADC through LRCK, SCLK and SDOUT pins. These formats are I^2S, left justified, DSP/PCM mode and TDM. ADC data is out at SDOUT on the falling edge of SCLK. The relationships of SDOUT, SCLK and LRCK with these formats are shown through Figure 2a to Figure 2f. ES7243L can be cascaded up to 16-ch through single I^2S or TDM, please refer to the user guide for detail description.

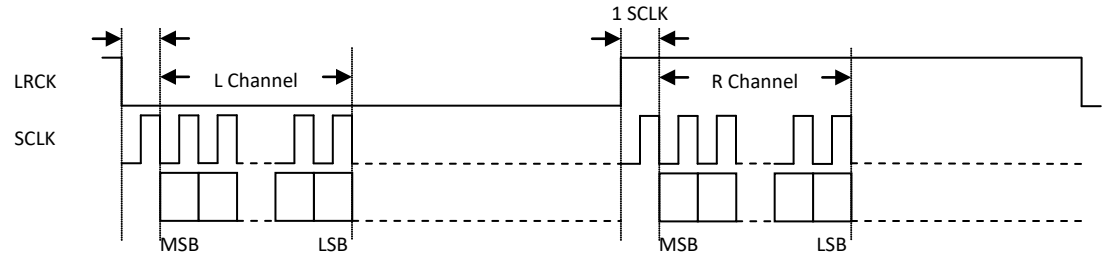


Figure 2a I^2S Serial Audio Data Format

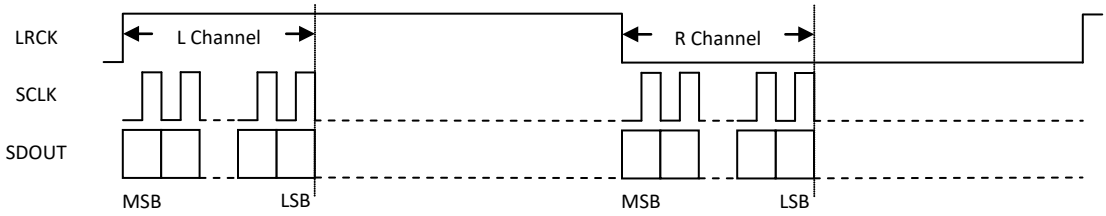


Figure 2b Left Justified Serial Audio Data Format

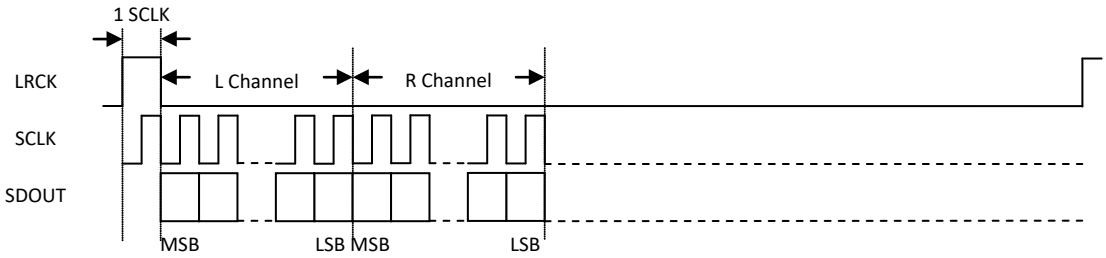


Figure 2c DSP/PCM Mode A Serial Audio Data Format

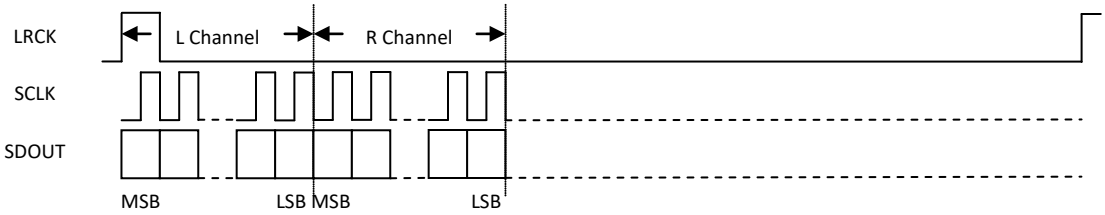


Figure 2d DSP/PCM Mode B Serial Audio Data Format

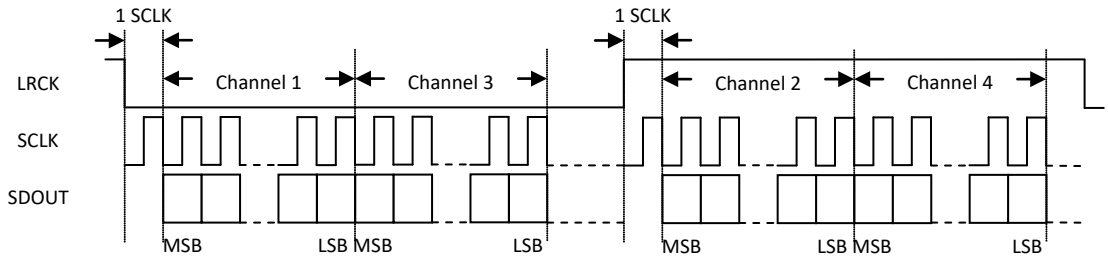


Figure 2e TDM I^{2}S Serial Audio Data Format

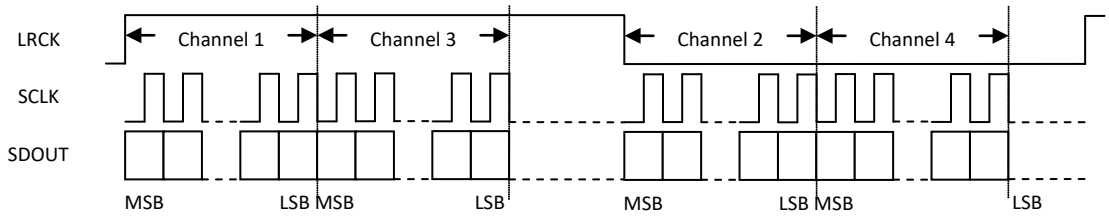


Figure 2f TDM DSP/PCM Mode A Serial Audio Data Format

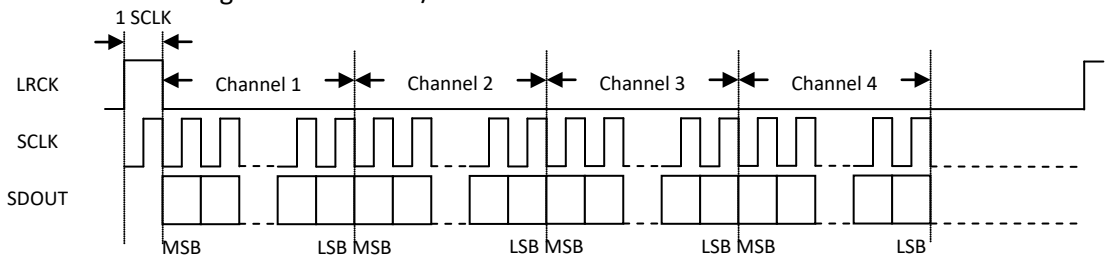


Figure 2g TDM DSP/PCM Mode A Serial Audio Data Format

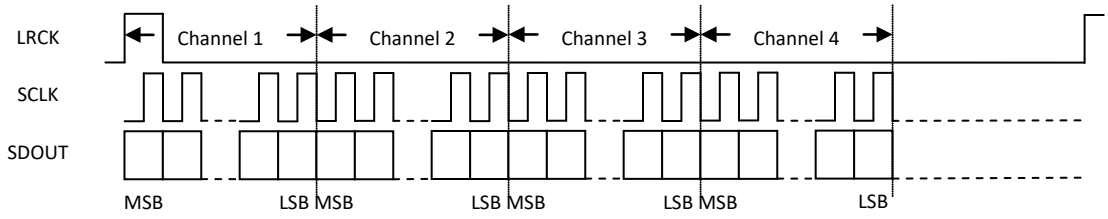


Figure 2h TDM DSP/PCM Mode B Serial Audio Data Format

6. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+1.98V
Digital Supply Voltage Level	-0.3V	+1.98V
Analog Input Voltage Range	GNDA-0.3V	VDDA+0.3V
Digital Input Voltage Range	GNDD-0.3V	VDDP+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDDA	1.62	1.8	1.98	V
VDDD	1.62	1.8	1.98	V
VDDP	1.62	1.8	1.98	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDDA=1.8V, VDDD=1.8V, GNDA=0V, GNDD=0V, ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	96	101	104	dB
THD+N	-95	-90	-85	dB
Channel Separation (1KHz)	95	100	105	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level (±: differential P/N)		±VDDA/3.3		±Vrms
Input Impedance		8 (0 dB PGA) 6 (33 dB PGA)		KΩ

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDDD=1.8V, VDDP=1.8V, VDDA=1.8V (48 kHz) VDDD=1.8V, VDDP=1.8V, VDDA=1.8V (16 kHz)				mW
Power Down Mode (Note 1)		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*VDDP			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		VDDP		V
Output Low-level Voltage		0		V

Note 1: recommend all power supply on, entering low power through control register setting, then stopping input clock.

I^2C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

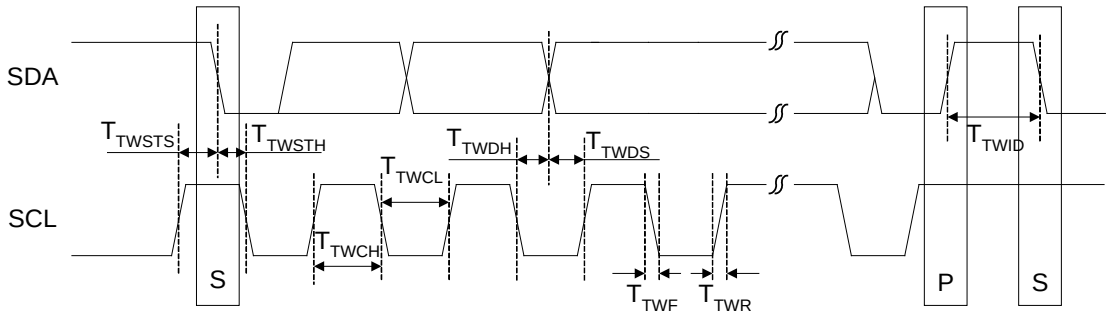


Figure 3 I^2C Timing

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency (Note 3)			50	KHz
LRCK duty cycle (Note 4)		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to SDOUT valid VDDD=3.3V VDDD=1.8V	T_{SDO}		16 39	ns
LRCK edge to SDOUT valid (Note 5) VDDD=3.3V VDDD=1.8V	T_{LDO}		11 25	ns
TDMIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to TDMIN hold time	T_{SDIH}	10		ns

Note 2: up to N*50 KHz when cascaded up to 8-ch through single I^2S or TDM.

Note 3: one SCLK period of high time in DSP/PCM modes.

Note 4: only apply to MSB of Left Justified or DSP/PCM mode B.

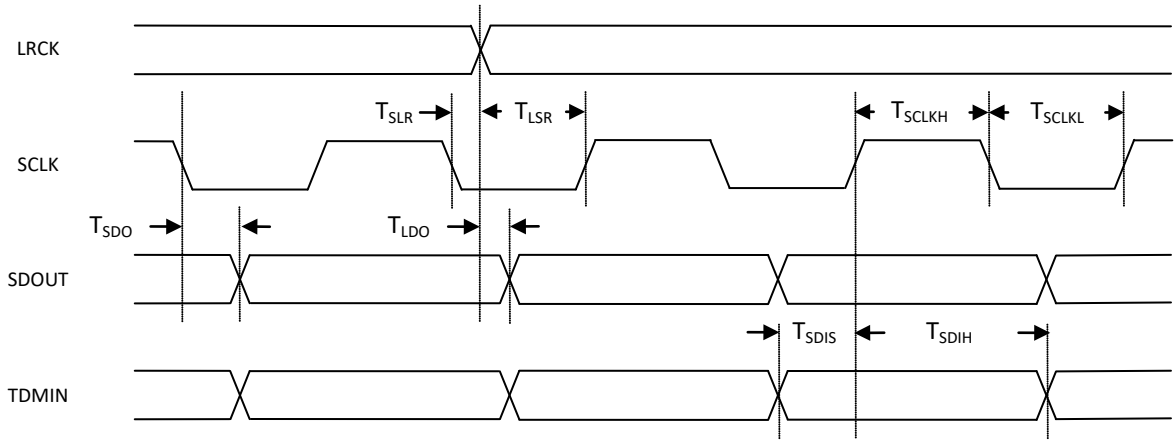


Figure 4 Serial Audio Port Timing

7. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 –RESET, DEFAULT 00011110

Bit Name	Bit	Description
CSM_ON	7	Chip FSM ON/OFF control 0 - csm power down(default) 1 - csm power up
MSC	6	Master/Slave select for SDP 0 - slave mode(default) 1 - master mode
SEQ_DIS	5	Power up sequence enable control 0 - power up sequence enable(default) 1 - power up sequence disable
RST_DIG	4	Digital circuits reset 0 - Not reset(default) 1 - Reset
RST_CMG	3	Clock manager circuit reset 0 - Not reset (default) 1 - Reset
RST_MST	2	Master circuit reset 0 - Not reset (default) 1 - Reset
RST_ADC_DIG	1	Adc digital circuit reset 0 - Not reset (default) 1 - Reset

REGISTER 0X01 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
MCLK_ON	5	MCLK ON/OFF control 0 - MCLK off (default) 1 - MCLK on
BCLK_ON	4	BCLK ON/OFF control 0 - BCLK off (default) 1 - BCLK on
CLKADC_ON	3	Clock clk_adcON/OFF control 0: clk_adc off(default) 1: clk_adc on
ANACLKADC_ON	1	Clock anaclk_adc ON/OFF control 0 - anaclk_adc off(default) 1 - anaclk_adc on

REGISTER 0X02 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
MCLK_SEL	7	Internal mclk select 0 - from MCLK PAD(default) 1 - from BCLK PAD
MSTBCLK_SEL	6	Master BCLK derive clocks 0 - from bclk_out[divided by DIV_BCLK](default) 1 - from anaclk_adc
MSTCLK_SEL	5:4	At master mode, source clock select

		0 - internal mclk(default) 1 - dig_mclk 2 -DSP_clk 3 - CF_clk
BCLK_FITBIT	2	BCLK out control when master mode 0 - continual bclk(default) 1 - master bclk stop after data transfer out
MCLK_INV	1	Internal mclk invert 0 - normal(default) 1 - invert
BCLK_INV	0	BCLK invert 0 - normal(default) 1 - BCLK invert

REGISTER 0X03 – CLOCK MANAGER, DEFAULT 0010 0000

Bit Name	Bit	Description
ADC_OSR	5:0	ADC Over Sample Rate control 0~14 - not used 15 - 60*fs 16 - 64*fs ... 31 - 124*fs 32 - 128*fs (default) ... 63 - 252*fs

REGISTER 0X04 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_PRE	7:4	Pre-divided mclk Divide = DIV_PRE + 1
MULT_PRE	1:0	Pre-multiplication 0 - 1x(default) 1 - 2x 2 - 4x 3 - 8x

REGISTER 0X05 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_CLKCF	7:4	CF clock divider Divide = DIV_CLKCF + 1
DIV_CLKDSP	3:0	DSP clock divider Divide = DIV_CLKDSP + 1

REGISTER 0X06 – CLOCK MANAGER, DEFAULT 00000011

Bit Name	Bit	Description
DIV_BCLK	6:0	BCLK divider at master mode Divide = DIV_BCLK + 1

REGISTER 0X07 – CLOCK MANAGER, DEFAULT 0000 0001

Bit Name	Bit	Description

TRI_BCLK	6	BCLK Tri-state control 0 - normal(default) 1 - Tri-state
TRI_LRCK	5	LRCK Tri-state 0 - normal(default) 1 - Tri-state
TRI_SDOUT	4	SDOUT Tri-state 0 - normal(default) 1 - Tri-state
DIV_LRCK[11:8]	3:0	Master LRCK divider bit 11 to bit 8 0~4095 - divide by 1~4096 511 - divide by 512(default)

REGISTER 0X08 – CLOCK MANAGER, DEFAULT 11111111

Bit Name	Bit	Description
DIV_LRCK[7:0]	7:0	Master LRCK divider bit 7 to bit 0 0~4095 - divide by 1~4096 511 - divide by 512(default)

REGISTER 0X09 – CLOCK MANAGER, DEFAULT 1100 0001

Bit Name	Bit	Description
VMIDSEL_S1	7:6	VMIDSEL at S1 state 00 – NA 01 – VMIDSEL=1 10 – VMIDSEL=2 11 – VMIDSEL=3(default)
S1_TIME	5:0	Timer for S1 ForLRCK=48KHz: 0 - 21us 1 - 104us(default) 2 - 5ms … 63 - 167ms(max)

REGISTER 0X0A – SDP, DEFAULT 1000 0001

Bit Name	Bit	Description
VMIDSEL_S3	7:6	VMIDSEL at S3 state 00 – NA 01 – VMIDSEL=1 10 – VMIDSEL=2(default) 11 – VMIDSEL=3
S3_TIME	5:0	Timer for S3 ForLRCK=48KHz: 0 - 21us 1 - 104us(default) 2 - 5ms … 63 - 167ms(max)

REGISTER 0X0B – SDP, DEFAULT 1100 0000

Bit Name	Bit	Description
SDP_OUT_MUTE	7:6	SDP out mute control 0 - unmute 1 - mute R channel 2 - mute L channel 3 - mute L/R channels(default)
SDP_LRP	5	I2S/Left Justify case: 0 - L/R normal polarity(default) Left/Right=High/Low (LJ) Left/Right=Low/High (I2S) 1 - L/R invert polarity Left/Right=Low/High (LJ) Left/Right=High/Low (I2S) DSP mode case: 0 - Mode A, MSB is available on 2nd SCLK rising edge after LRCK rising edge(default) 1 - Mode B, MSB is available on 1st SCLK rising edge after LRCK rising edge
SDP_WL	4:2	SDP word length 0 – 24-bit(default) 1 – 20-bit 2 – 18-bit 3 – 16-bit 4 – 32-bit others - 24-bit
SDP_FMT	1:0	SDP format 0 - I2S(default) 1 - LJ 2 - reserved 3 - DSP

REGISTER 0X0C – SDP, DEFAULT 0000 0000

Bit Name	Bit	Description
TDM_FLAG	5:4	NFS flag at slot0/LSB 0 - no flag(default) 1 - first chip, generate flag '1' at slot0/LSB 2 - sync chip, get tdm flag '1' and sync, and send flag '1' at current slot 3 - all LSB is flag '0'
TDM_MODE	3:0	TDM mode selection 0 - ADC no TDM(default) 1 - 2FS 2 - 3FS 3 - 4FS 4 - 5FS 5 - 6FS 6 - 7Fs 7 - 8FS 8 - ADC + TDM shift (1FS) 9 - TDM loop other - not used

REGISTER 0X0D – ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC_DATASEL	7:6	ADC data mux 0 - output L - R (default) 1 - output L - L 2 - output R - R 3 - output R - L
ADC_INV	5:4	ADC polarity inverted 0 - normal(default) 1 - ADCR invert 2 - ADCL invert 3 - ADCL/R invert
ADC_RAMCLR	3	ADC ram clear when lrck/adc_mclk active
ADC_SCALE	2:0	ADC gain scale up (normally used with ADC_OSR) 0 - 0dB (recommended whenADC_OSR=0x1C~0x20) (default) 1 - 6dB (recommended when ADC_OSR=0x18~0x1B) 2 - 12dB (recommended when ADC_OSR=0x14~0x17) 3 - 18dB (recommended when ADC_OSR=0x11~0x13) 4 - 24dB (recommended when ADC_OSR=0x10) 5 - 30dB 6 - 36dB 7 - 42dB

REGISTER 0X0E – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC_VOLUME	7:0	ADC volume control 0x00 - '-95.5dB' (default) 0x01 - '-90.5dB' … 0.5dB/step 0xBE - '-0.5dB' 0xBF - '0dB' 0xC0 - '+0.5dB' … 0xFF - '+32dB'

REGISTER 0X0F – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC_HPF	7	ADC offset freeze 0 - freeze offset(default) 1 - dynamic HPF
ADC_RAMPRATE	3:0	ADC VC ramp rate 0 - disable (default) ForLRCK=48KHz: 1 -0.25dB/80us 2 - 0.25dB /160us 3 - 0.25dB /320us 4 - 0.25dB /640us 5 - 0.25dB /1.28ms 6 - 0.25dB /2.56ms 7 - 0.25dB /5.12ms 8 - 0.25dB /10.24ms

		9 - 0.25dB /20.48ms 10 - 0.25dB /40.96ms 11 - 0.25dB /81.92ms 12 - 0.25dB /163.84ms 13 - 0.25dB /327.68ms 14 - 0.25dB /655.36ms 15 - 0.25dB /1.3s

REGISTER 0X10 – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description

REGISTER 0X11 – ADC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description

REGISTER 0X12 – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description

REGISTER 0X13 – ADC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description

REGISTER 0X14 – ADC CONTROL, DEFAULT 0000 1100

Bit Name	Bit	Description
ADC_HPFS1	4:0	ADCHPF stage1 coeff 0x0C (default)

REGISTER 0X15 – ADC CONTROL, DEFAULT 0000 1100

Bit Name	Bit	Description
ADC_HPFS2	4:0	ADCHPF stage2 coeff 0x0C (default)

REGISTER 0X16 – ANALOG, DEFAULT 1111 1111

Bit Name	Bit	Description
PDN_ANA	7	0 – enable analog circuits 1 – power down analog circuits(default)
PDN_ADCVREFGEN	6	0 – enable analog ADC bias circuits 1 – power down analog ADC bias circuits(default)
MODTOP1_RST	5	0 – disable(default) 1 – reset modulator1
MODTOP2_RST	4	0 – disable(default) 1 – reset modulator2
PDN_MOD1	3	0 – enable analog ADC modulator1 1 – power down analog ADC modulator1(default)
PDN_MOD2	2	0 – enable analog ADC modulator2 1 – power down analog ADC modulator2(default)
PDN_PGA1	1	0 – enable analog PGA1 1 – power down analog PGA 1(default)
PDN_PGA2	0	0 – enable analog PGA2 1 – power down analog PGA2(default)

REGISTER 0X17 – ANALOG, DEFAULT 0000 0010

Bit Name	Bit	Description
VMIDSEL_S0	3:2	VMIDSEL at Power Down (S0) state 00 - 0(default) 01 - 1 10 - 2 11 - 3
VMIDSEL_S2	1:0	0 –power down 1 –speed charge1 2 – normal vmid operation(default) 3 –speed charge3

REGISTER 0X18 – ANALOG, DEFAULT 00100100

Bit Name	Bit	Description
ADCBIAS_SW	5:4	0 –bias setting level0, (default) 1 –bias setting level1 2 –bias setting level2 3 –bias setting level3(highest bias)
ADCFL_SW	3:0	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X19 – ANALOG, DEFAULT 1010 1010

Bit Name	Bit	Description
PGA1BIAS_SW	7:4	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10(default) 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13

		1110 - bias setting level14 1111 - bias setting level15(highest)
PGA2BIAS_SW	3:0	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10(default) 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X1A – ANALOG, DEFAULT 1000 1000

Bit Name	Bit	Description
ADCI1BIAS_SW	7:4	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
ADCI23BIAS_SW	3:0	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8(default) 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14

		1111 - bias setting level15(highest)

REGISTER 0X1B – ANALOG, DEFAULT 0100 0100

Bit Name	Bit	Description
ADCSMBIAS_SW	7:4	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
ADCCMBIAS_SW	3:0	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X1C – ANALOG, DEFAULT 0100 0100

Bit Name	Bit	Description
ADCVRPBIAS_SW	7:4	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11

		1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)
ADCCPPBIAS_SW	3:0	0000 – not allowed 0001 - bias setting level1(lowest) 0010 - bias setting level2 0011 - bias setting level3 0100 - bias setting level4 0101 - bias setting level5 0110 - bias setting level6 0111 - bias setting level7 1000 - bias setting level8 1001 - bias setting level9 1010 - bias setting level10 1011 - bias setting level11 1100 - bias setting level12 1101 - bias setting level13 1110 - bias setting level14 1111 - bias setting level15(highest)

REGISTER 0X1D – ANALOG, DEFAULT 0000 0000

Bit Name	Bit	Description
LP_VRP	7	0 – default 1 – low power
LP_VRPOUT	6	0 – default 1 – low power
LP_ADCMOD1	5	0 – default 1 – low power
LP_ADCMOD2	4	0 – default 1 – low power
LP_ADCMODF1	3	0 – default 1 – low power
LP_ADCMODF2	2	0 – default 1 – low power
LP_ADCMODI1	1	0 – default 1 – low power
LP_ADCMODI2	0	0 – default 1 – low power

REGISTER 0X1E – ANALOG, DEFAULT 0000 0101

Bit Name	Bit	Description
LP_PGA1	5	0 – default 1 – low power
LP_PGA2	4	0 – default 1 – low power
LP_PGA11	3	0 – default 1 – low power
LP_PGA12	2	0 – default 1 – low power
LP_PGA21	1	0 – default

		1 – low power
LP_PGA22	0	0 – default 1 – low power

REGISTER 0X1F – ANALOG, DEFAULT 00000000

Bit Name	Bit	Description
ADC_DMIC_ON	5	0 – default 1 – enable Dmic
REFSEL	4	0 – default 1 – internal use
VMIDLVL	1:0	0 –'vdda/2' (default) 1 – vmid level1 2 – vmid level2 3 – vmid level3

REGISTER 0X20 – ANALOG, DEFAULT 0000 0000

Bit Name	Bit	Description
SELMIC1	4	0 – default 1 – select MIC1 as PGA1 input
PGA1GAIN_SETTING	3:0	PGA1 gain 0 – 0dB(default) 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB 11 – 33dB 12 – 34.5dB 13 – 36dB 14 – 37.5dB

REGISTER 0X21 – ANALOG, DEFAULT 0000 0000

Bit Name	Bit	Description
SELMIC2	4	0 – default 1 – select MIC2 as PGA2 input
PGA2GAIN_SETTING	3:0	PGA2 gain 0 – 0dB(default) 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB

		9 – 27dB 10 – 30dB 11 – 33dB 12 – 34.5dB 13 – 36dB 14 – 37.5dB

REGISTER 0XF6 – TEST MODE, DEFAULT 0000 0000

Bit Name	Bit	Description
ANACLK_SEL	3	Analog clock selection 0 - from adc_cfclk/4(default) 1 - from pre_dll (MULT_PRE=2 or 3)
CFCLK_SEL	2	Comb filter clock selection 0 - from dig_mclk(default) 1 - from main_clk
DSPCLK_SEL	1	ADC DSP clock selection 0 - from dig_mclk(default) 1 - from main_clk
REGULAR_OSR	0	Regularly over sample PGA data 0 - auto control over sample rate(default) 1 - regularly over sample rate

REGISTER 0XF7 – TEST MODE, DEFAULT 1111 0000

Bit Name	Bit	Description
PULLUPSE_BCLK	7	BCLK pullup control 0 - BCLK no pullup 1 - BCLK pullup(default)
PULLUPSE_LRCK	6	LRCK pullup control 0 - LRCK no pullup 1 - LRCK pullup(default)
PULLDNSE_TDMIN	5	TDMIN pulldown control 0 - TDMIN no pulldown 1 - TDMIN pulldown(default)
PULLDNSE_SDOUT	4	SDOUT pulldown control 0 - SDOUT no pulldown 1 - SDOUT pulldown(default)

REGISTER 0XF8 – TEST MODE, DEFAULT 0000 0000

Bit Name	Bit	Description
SDOUT_FAST	7	Internal use
PATHSEL	6	Internal use
DELYSEL	5:4	Internal use
ADC_DLY_SEL	3	Internal use

REGISTER 0XF9 – TEST MODE, DEFAULT 0000 0000

Bit Name	Bit	Description
DLL_PWD	0	Internal use

REGISTER 0XFA – I2C CONFIGURE, DEFAULT 0000 0000

Bit Name	Bit	Description

I2C_RETIME	1	I2C signals retime 0 - normal(default) 1 - retime mode
INI_REG	0	Initial registers 0 - normal(default) 1 - reset registers to default

REGISTER 0XFC – FLAG, DEFAULT 0000 0000

Bit Name	Bit	Description
FLAG_CSM_CHIP	5:4	CSM flag, read only 0 - S0 1 - S1 2 - S2 3 - S3

REGISTER 0XFD – CHIP ID1, DEFAULT 0111 0010

Bit Name	Bit	Description
CHIP_ID1	7:0	0X72, read only

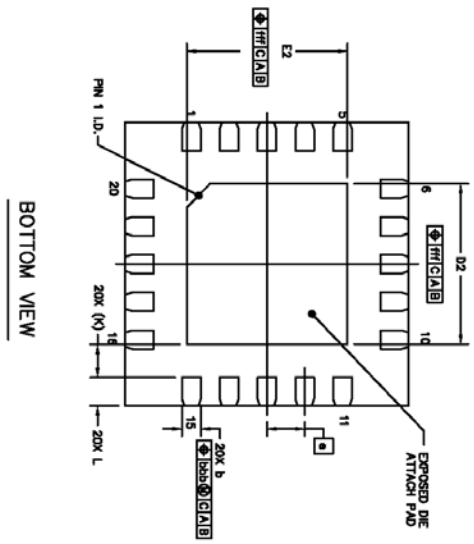
REGISTER 0XFE – CHIP ID2, DEFAULT 0100 0011

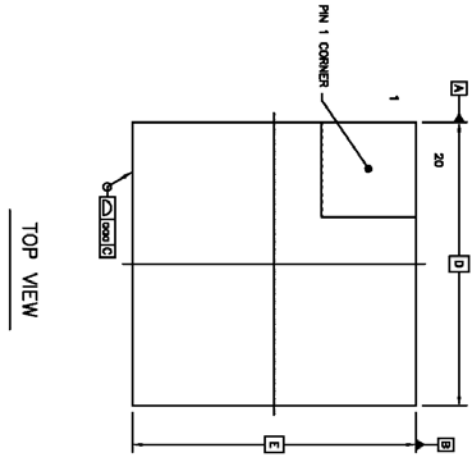
Bit Name	Bit	Description
CHIP_ID2	7:0	0X43, read only

REGISTER 0XFF – CHIP VERSION, DEFAULT 0001 0000

Bit Name	Bit	Description
CHIP_ID3	7:4	0X1, read only
CHIP_VER	3:0	0X0, read only

8. PACKAGE (UNIT: MM)





	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	----	0.4	----
L/F THICKNESS	A3		0.152 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		3 BSC	
BODY SIZE Y	E		3 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	D2	1.6	1.7	1.8
EP SIZE Y	E2	1.6	1.7	1.8
LEAD LENGTH	L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE	K		0.35 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.1	
EXPOSED PAD OFFSET	fff		0.1	

9. CORPORATE INFORMATION

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