



ES8336

Low Power Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I²S/PCM master or slave serial data port
- Two pairs of analog input with differential input option
- 256/384Fs and USB 12/24 MHz system clocks
- I²C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 92 dB signal to noise ratio, -85 dB THD+N
- Low noise pre-amplifier
- Auto level control (ALC) and noise gate
- Mic bias
- Support digital mic

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 93 dB signal to noise ratio, -85 dB THD+N
- Ground centered headphone driver
- Headphone and external mic detection
- Pop and click noise suppression

Low Power

- 1.8V to 3.3V operation
- 7 mW playback; 16 mW playback and record

APPLICATIONS

- MID/Tablet
- Wireless audio
- Portable audio

ORDERING INFORMATION

ES8336 -40°C ~ +85°C
QFN-32

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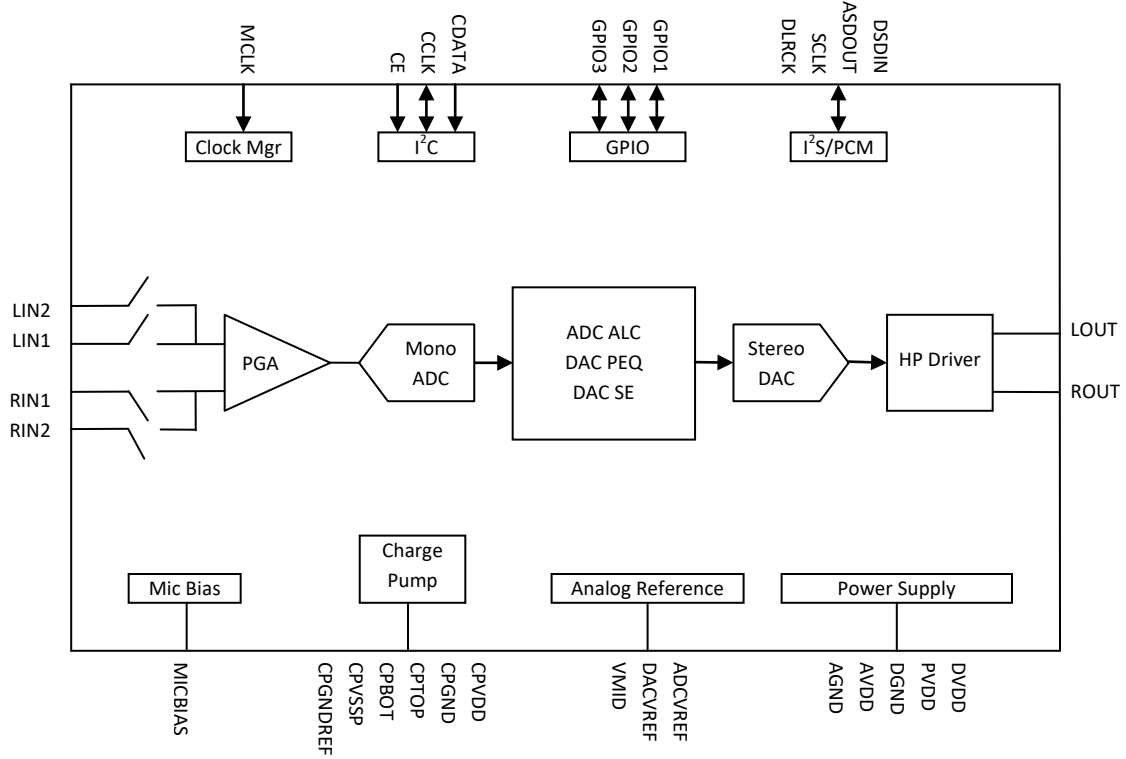
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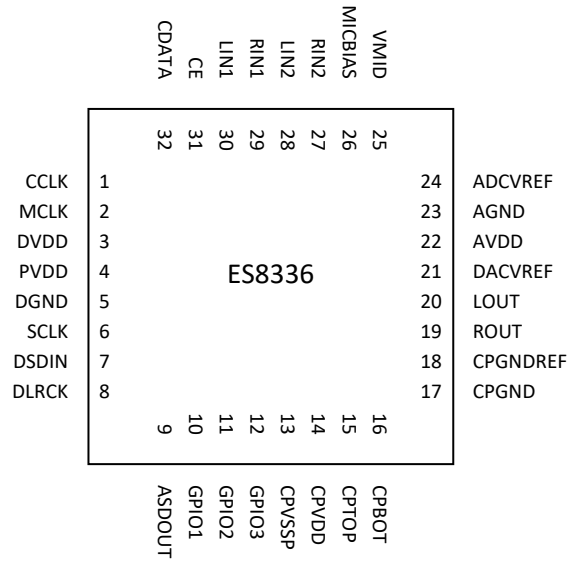
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1. BLOCK DIAGRAM

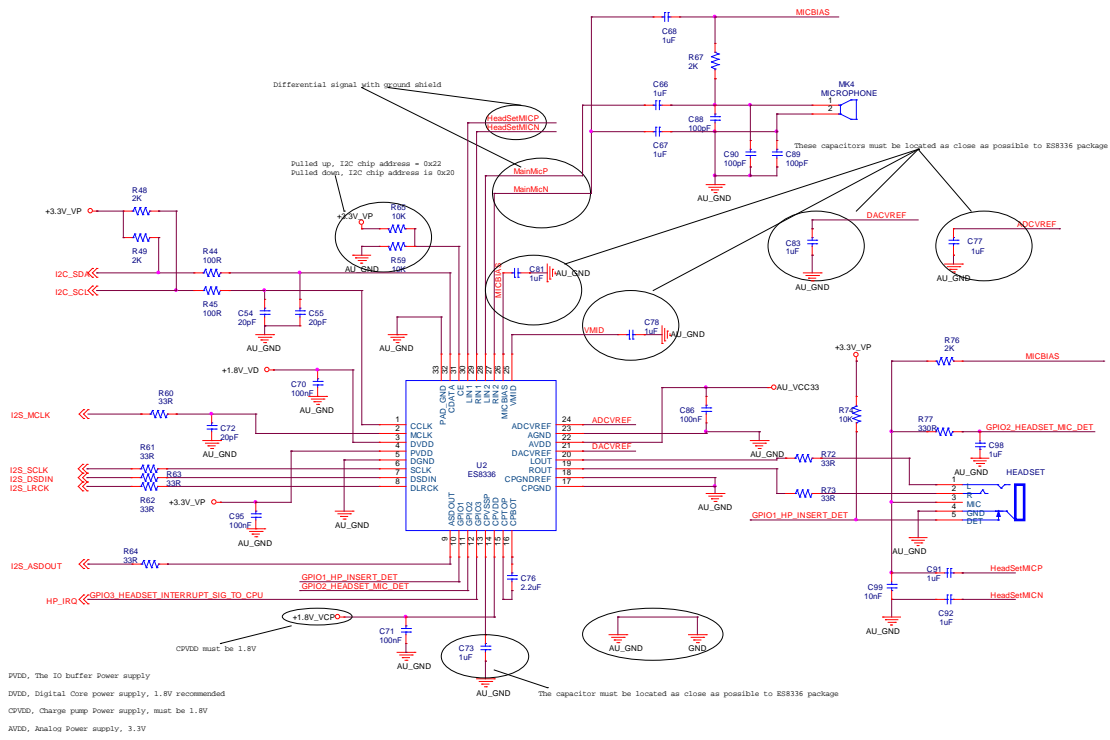


2. PIN OUT AND DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	CCLK	I	I ² C clock input
2	MCLK	I	Master clock
3	DVDD	Supply	Digital core supply
4	PVDD	Supply	Digital IO supply
5	DGND	Supply	Digital ground
6	SCLK	I/O	Audio data bit clock
7	DSDIN	I	DAC audio data
8	DLRCK	I/O	DAC audio data left and right clock
9	ASDOUT	O	ADC audio data
10	GPIO1	I/O	General purpose IO
11	GPIO2	I/O	General purpose IO
12	GPIO3	I/O	General purpose IO
13	CPVSSP		Charge pump filtering
14	CPVDD		Charge pump power supply
15	CPTOP		Charge pump capacitor top
16	CPBOT		Charge pump capacitor bottom
17	CPGND		Charge pump ground
18	CPGNDREF		Charge pump filtering
19	ROUT	O	Right analog output
20	LOUT	O	Left analog output
21	DACVREF	O	Decoupling capacitor
22	AVDD	Supply	Analog supply
23	AGND	Supply	Analog ground
24	ADCVREF	O	Decoupling capacitor
25	VMID	O	Decoupling capacitor
26	MICBIAS	O	Mic bias
27	RIN2	I	Right analog input
28	LIN2	I	Left analog input
29	RIN1	I	Right analog input
30	LIN1	I	Left analog input
31	CE	I	I ² C device address selection
32	CDATA	I/O	I ² C data input or output

3. TYPICAL APPLICATION CIRCUIT



4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports two types of clocking: standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and non standard audio clocks like 19.2 MHz.

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I²C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I²C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 400 kbps.

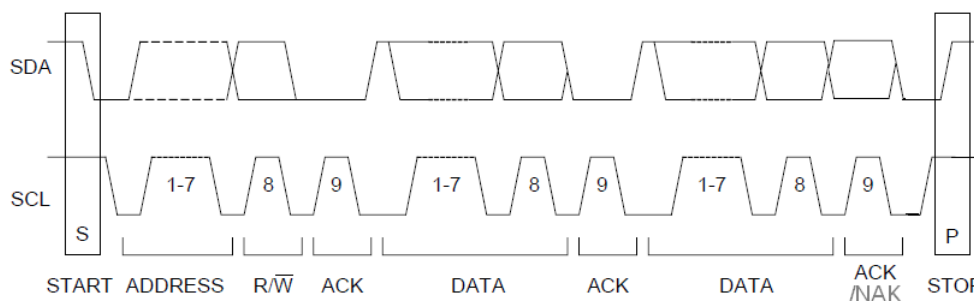


Figure 1 Data Transfer for I²C Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals ADO. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I²C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I²C Interface Mode

Chip Address	R/W		Register Address		Data to be written
001000	AD0	0	ACK	RAM	ACK
					DATA

Table 2 Read Data from Register in I²C Interface Mode

Chip Address	R/W		Register Address
001000	AD0	0	ACK
			RAM
Chip Address	R/W		Data to be read
001000	AD0	1	ACK
			Data

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, BCLK (SCLK) and DACDAT/ADCDAT pins. These formats are I²S, left justified, DSP/PCM and TDM mode. DAC input DACDAT is sampled by the device on the rising edge of SCLK. ADC data is out at ADCDAT on the falling edge of SCLK. The relationship of SDATA (DACDAT/ADCDAT), SCLK and LRCK with these formats are shown through Figure 2 to Figure 6.

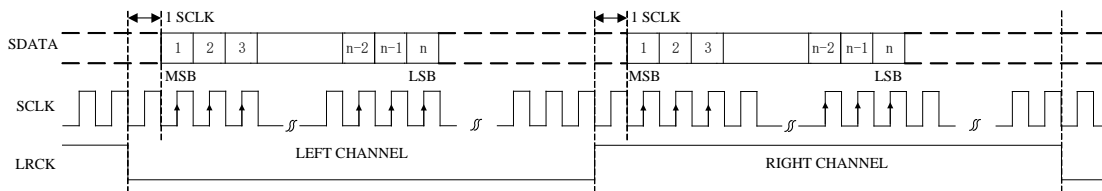


Figure 2 I²S Serial Audio Data Format Up To 24-bit

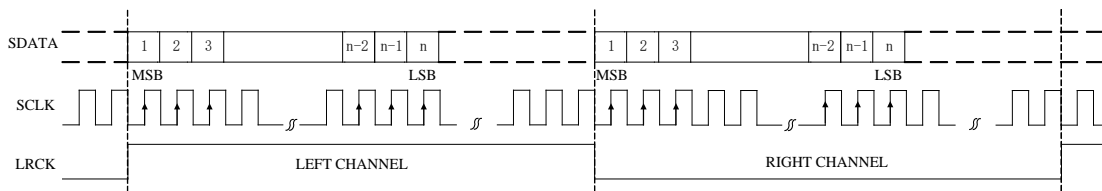


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

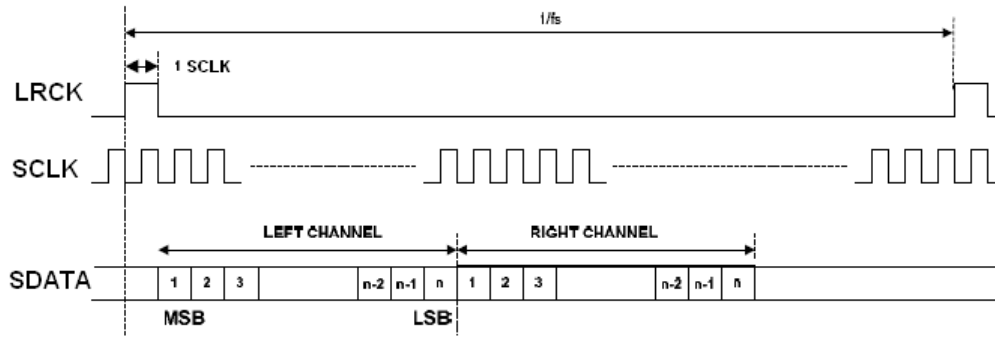


Figure 5 DSP/PCM Mode A

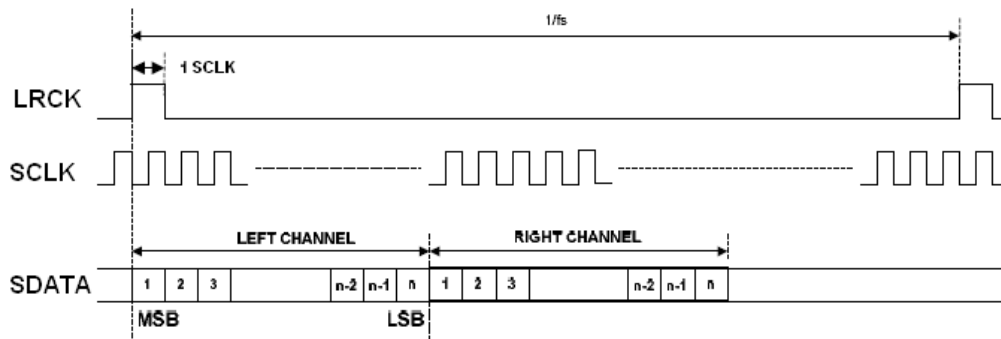


Figure 6 DSP/PCM Mode B

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
AVDD	2.0	3.3	3.6	V
CPVDD	1.6	1.8	2.0	V
DVDD	1.6	1.8/3.3	3.6	V
PVDD	1.6	1.8/3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weight)	85	92	95	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Double Speed				
Passband	0		0.2268	Fs
Stopband	0.4535			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	50			dB
Analog Input				
Full Scale Input Level		±AVDD/3.3		±Vrms
Input Impedance		20		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weight)	83	93	95	dB
THD+N	-85	-83	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.05		dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	40			dB
Filter Frequency Response – Double Speed				
Passband	0		0.2268	Fs
Stopband	0.4535			Fs
Passband Ripple			±0.005	dB

Stopband Attenuation	40			dB
De-emphasis Error at 1 KHz (Single Speed Mode Only)				
Fs = 32KHz			0.002	dB
Fs = 44.1KHz			0.013	
Fs = 48KHz			0.0009	
Analog Output				
Full Scale Output Level		AVDD/3.3		Vrms

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=1.8V: Play back		7		mW
Play back and record		16		
DVDD=3.3V, PVDD=3.3V, AVDD=3.3V: Play back		31		
Play back and record		59		
Power Down Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=1.8V		TBD		mW
DVDD=3.3V, PVDD=3.3V, AVDD=3.3V		TBD		

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	-10	10	ns
SCLK falling to SDOOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

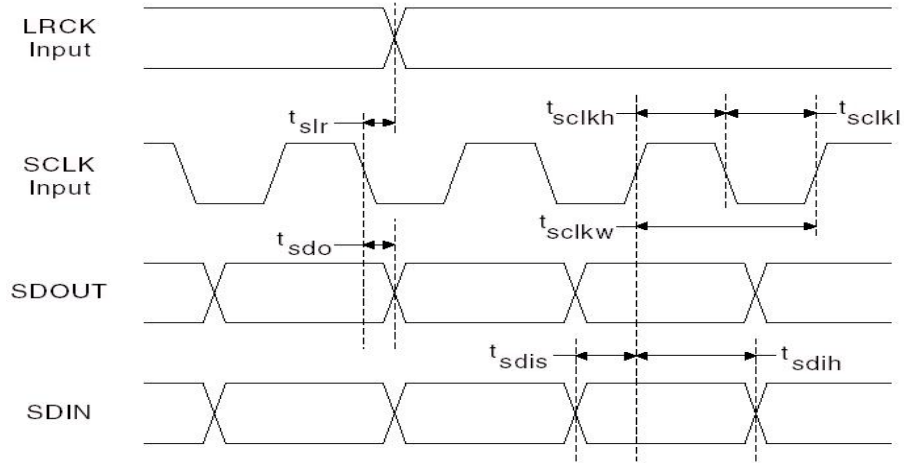


Figure 8 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F _{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T _{TWID}	4.7/1.3		us
Start Condition Hold Time	T _{TWSTH}	4.0/0.6		us
Clock Low time	T _{TWCL}	4.7/1.3		us
Clock High Time	T _{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T _{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T _{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T _{TWDS}	0.25/0.1		us
Rise Time of CCLK	T _{TWR}		1.0/0.3	us
Fall Time CCLK	T _{TWF}		1.0/0.3	us

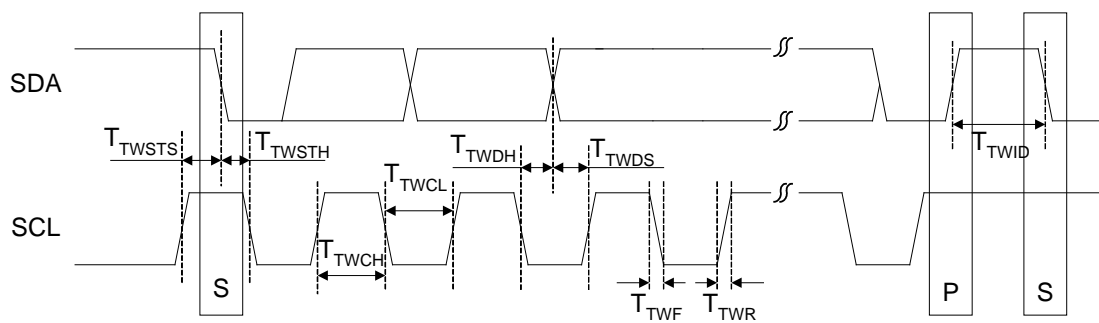


Figure 10 I²C Timing

8. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 – RESET, DEFAULT 0X03

Bit Name	Bit	Description
csm_on	7	Chip current state machine control 0 – csm power down(default) 1 – csm power on
seq_en	6	Power up sequence control 0 – power up sequence disable (default) 1 – power up sequence enable
rst_dig	5	Digital reset 0 – normal(default) 1 – reset digital except control port block
rst_regs	4	registers reset 0 – normal(default) 1 – reset all registers to default value except “rst_regs”
rst_clkmgr	3	clock manager block reset 0 – normal(default) 1 – reset clock manager block
rst_master	2	master block reset 0 – normal(default) 1 – reset master block
rst_adc_dig	1	ADC digital block reset 0 – normal 1 – reset ADC digital block (default)
rst_dac_dig	0	DAC digital block reset 0 – normal 1 – reset DAC digital block (default)

REGISTER 0X01 – CLOCK MANAGER, DEFAULT 0X03

Bit Name	Bit	Description
mclk_div2	7	MCLK divide by 2 control 0 – normal (default) 1 – MCLK divide by 2
mclk_on	6	MCLK in control 0 – MCLK off(default) 1 – MCLK on
bclk_on	5	SDP bit clock control 0 – BCLK off(default) 1 – BCLK on
clk_cp_on	4	Charge pump clock control 0 – CLK_CP off(default) 1 – CLK_CP on
clk_adc_on	3	ADC digital clock control 0 – adc_mclk off(default) 1 – adc_mclk on
clk_dac_on	2	DAC digital clock control 0 – dac_mclk off(default) 1 – dac_mclk on
anaclk_adc_on	1	ADC analog clock control

		0 – anaclk_adc off 1 – anaclk_adc on(default)
anaclk_dac_on	0	DAC analog clock control 0 – anaclk_dac off 1 – anaclk_dac on(default)

REGISTER 0X02 – CLOCK MANAGER, DEFAULT 0X00

Bit Name	Bit	Description
clk_adc_double	5	clk_adc divide by 2 control 0 – normal(default) 1 – clk_adc divide by 2
clk_dac_double	4	clk_dac divide by 2 control 0 – normal(default) 1 – clk_dac divide by 2
tm_sel	3	timer select 0 – use adclrck_out(default) 1 – use daclrck_out
adclrck_sel	2	adclrck select 0 – use DACLRC (default) 1 – use ADCLRC
clk_adc_sel	1	adc_mclk select 0 – use clk_adc(default) 1 – use clk_dac
syncMode	0	sync mode 0 – normal(default) 1 – sync mode

REGISTER 0X03 – CLOCK MANAGER, DEFAULT 0X20

Bit Name	Bit	Description
adc_osr[5:0]	5	ADC delta sigma over sample rate $adc_osr = f(adc_mclk) / fs / 8$ f(adc_mclk) refer to clk_adc_div and clk_adc_double

REGISTER 0X04 – CLOCK MANAGER, DEFAULT 0X11

Bit Name	Bit	Description
clk_adc_div[3:0]	7	adc_mclk clock divider
adclrck_div[11:8]	3	Internal adclrck divider bit 11 to bit 8

REGISTER 0X05 – CLOCK MANAGER, DEFAULT 0X00

Bit Name	Bit	Description
adclrck_div[7:0]	7	Internal adclrck divider bit 7 to bit 0

REGISTER 0X06 – CLOCK MANAGER, DEFAULT 0X11

Bit Name	Bit	Description
clk_dac_div[3:0]	7	dac_mclk clock divider
daclrck_div[11:8]	3	Internal daclrck divider bit 11 to bit 8

REGISTER 0X07 – CLOCK MANAGER, DEFAULT 0X00

Bit Name	Bit	Description

daclrck_div[7:0]	7	Internal daclrck divider bit 7 to bit 0
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REGISTER 0X08 – CLOCK MANAGER, DEFAULT 0X00

Bit Name	Bit	Description
div_cp	5:0	charge pump clock divider 0 – divide by 32 (default) 1 to 60 – divide by 1 to 60 61 – divide by 64 62 – divide by 96 63 – divide by 127

REGISTER 0X09 – SERIAL DATA PORT, DEFAULT 0X01

Bit Name	Bit	Description
MSC	7	0 – slave serial port mode 1 – master serial port mode (default)
TRI	6	0 – normal (default) 1 – Hi-Z output
BCLK_INV	5	0 – normal (default) 1 – BCLK inverted
BCLKDIV	4:0	0 – no BCLK (default) 1 to 18 – MCLK/BCLKDIV 19 – MCLK/20 20 – MCLK/22 21 – MCLK/24 22 – MCLK/25 23 – MCLK/30 24 – MCLK/32 25 – MCLK/33 26 – MCLK/34 27 – MCLK/36 28 – MCLK/44 29 – MCLK/48 30 – MCLK/66 31 – MCLK/72

REGISTER 0X0A – SERIAL DATA PORT, DEFAULT 0X00

Bit Name	Bit	Description
adc_sdp_mute	6	ADC SDP mute control 0 – ADC SDP unmute(default) 1 – ADC SDP mute
ADCLRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after ALRCK rising edge 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edge
ADCWL	4:2	000 – 24-bit serial audio data word length(default) 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length

ADCFORMAT	1:0	00 – I2S serial audio data format(default) 01 – left justify serial audio data format 10 – right justify serial audio data format 11 – DSP/PCM mode serial audio data format
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REGISTER 0X0B – SERIAL DATA PORT, DEFAULT 0X00

Bit Name	Bit	Description
dac_sdp_mute	6	DAC SDP mute control 0 – DAC SDP unmute(default) 1 – DAC SDP mute
DACLRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after DLRCK rising edge 1 – MSB is available on 1st BCLK rising edge after DLRCK rising edge
DACWL	4:2	000 – 24-bit serial audio data word length(default) 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
DACFORMAT	1:0	00 – I2S serial audio data format(default) 01 – left justify serial audio data format 10 – right justify serial audio data format 11 – DSP/PCM mode serial audio data format

REGISTER 0X0C – SYSTEM, DEFAULT 0XF8

Bit Name	Bit	Description
vmid_seq1	7:6	vmidSel at Pseq1 $MCLK * adcSampleRate * 512$ from 0.042ms min to 170ms max
vmid_seq2	5:4	vmidSel at Pseq2 $MCLK * dacSampleRate * 512$ from 0.042ms min to 170ms max
vmidSel_reg	3:2	vmidSel sequence result
vmidSel	1:0	vmidSel user configure sequence: vmidSel(00,default) -> vmid_seq1(11) -> vmid_seq2(10) -> vmidSel_reg(10) -> write vmidSel

REGISTER 0X0D – SYSTEM, DEFAULT 0X3F

Bit Name	Bit	Description
pdnMic	5	Power down internal micBias circuits
pdn_ana	4	Power down overall analog circuits
ibiasgen_pdn	3	Power down bias circuits
pdn_adcBiasgen	2	Power down ADC bias circuits
pdn_adcVrefgen	1	Power down ADC reference circuits
pdn_dacVrefgen	0	Power down ADC reference circuits

REGISTER 0X0E – SYSTEM, DEFAULT 0X00

Bit Name	Bit	Description
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LPCPNLDO	5	Low power mode negative supply
LPVcmMod	4	Low power mode ADC modulator reference
LPADCVrp	3	Low power mode ADC reference
LPadcVrp	2	Low power mode ADC reference
flashLP	1	Low power mode ADC flash
int1LP	0	Low power mode ADC modulator

REGISTER 0X0F – SYSTEM, DEFAULT 0X00

Bit Name	Bit	Description
LPPGA	4	Low power PGA
LPDaCL	3	Low power LDAC
LPDaCR	2	Low power RDAC
LPHP	1	Low power HP output driver
LPHPMix	0	Low power HP mixer

REGISTER 0X10 – SYSTEM, DEFAULT 0X01

Bit Name	Bit	Description
dac_ibias_sw	4	DAC bias selection
vmidLow	3:2	Vmid selection 00 – vdda/2 01 – vdda/2-50mv 10 – vdda/2-100mv 11 – vdda/2-150mv
vx2off	1	disable vx2
vx1Sel	0	Vx1 selection

REGISTER 0X11 – SYSTEM, DEFAULT 0XFC

Bit Name	Bit	Description
vsel	7:0	11111100 – normal (default)

REGISTER 0X12 – SYSTEM, DEFAULT 0X28

Bit Name	Bit	Description
hp_ref2	5	HP output driver ref 0 light load 1 heavy load; this bit work together with hp_ref1
hp_ref1	4	HP output driver ref 0 light load 1 heavy load; this bit work together with hp_ref2
HPmix_ref2	3	HPmixer ref2
HPmix_ref1	2	HPmixer ref1
mref2	1	ADC ref control 0 default
mref1	0	ADC ref control 0 default

REGISTER 0X14 – HEADPHONE MIXER, DEFAULT 0X00

Bit Name	Bit	Description
LD2LHPMIX	7	LDAC signal to LHPmixer

RD2RHPMIX	3	RDAC signal to RHPmixer

REGISTER 0X15 – HEADPHONE MIXER, DEFAULT 0X33

Bit Name	Bit	Description
LHPMIX_HI	7	LHPmixer gain high
LHPMIX_LO	6	LHPmixer gain low
LHPMIX_MUTE	5	LHPmixer mute
pdnLHPMix	4	Power down LHPmixer
RHPMIX_HI	3	RHPmixer gain high
RHPMIX_LO	2	RHPmixer gain low
RHPMIX_MUTE	1	RHPmixer mute
pdnRHPMix	0	Power down RHPmixer

REGISTER 0X16 – HEADPHONE MIXER, DEFAULT 0X00

Bit Name	Bit	Description
LHPMIXVol[3:0]	7:4	0000 – -12dB 0001 – -10.5dB 0010 – -9dB 0011 – -7.5dB 0100 – -6dB 1000 – -4.5dB 1001 – -3dB 1010 – -1.5dB 1011 – 0dB
RHPMIXVol[3:0]	3:0	0000 – -12dB 0001 – -10.5dB 0010 – -9dB 0011 – -7.5dB 0100 – -6dB 1000 – -4.5dB 1001 – -3dB 1010 – -1.5dB 1011 – 0dB

REGISTER 0X17 – HEADPHONE, DEFAULT 0X00

Bit Name	Bit	Description
HPL_zcen	7	Enable LHP output driver zero cross
EnHPL	6	Enable LHP output driver
HPL_outen	5	Enable LHP output
HPLcal	4	Enable LHP output driver calibration
HPR_zcen	3	Enable RHP output driver zero cross
EnHPR	2	Enable RHP output driver
HPR_outen	1	Enable RHP output
HPRcal	0	Enable RHP output driver calibration

REGISTER 0X18 – HEADPHON , DEFAULT 0X88

Bit Name	Bit	Description
pdn_Lical	7	Reserved

HPL_iCal_sw	6	Reserved
HPLVol[1:0]	5:4	00 – 0dB 01 – -12dB 10 – -24dB 11 – -48dB
pdn_Rical	3	Reserved
HPR_iCal_sw	2	Reserved
HPRVol[1:0]	1:0	00 – 0dB 01 – -12dB 10 – -24dB 11 – -48dB

REGISTER 0X19 – HEADPHONE, DEFAULT 0X06

Bit Name	Bit	Description
pdn_CPHP	2	Power down HP output driver
EnRefr_HP	1	Enable HP reference
VROI_HP	0	Reserved

REGISTER 0X1A – HEADPHONE, DEFAULT 0X22

Bit Name	Bit	Description
pdn_cp	5	Power down charge pump circuits
cp_HIPWR	4	CP power level 0 – normal 1 - high power
cpn_swcomp_en	3	Reserved
cp_swldly_auto	2	Reserved, automatic CP power up sequence
cp_swldly_reg	1	Reserved, user register controlled CP power up sequence
cp_clkdly_en	0	Default 0

REGISTER 0X1B – HEADPHONE, DEFAULT 0X03

Bit Name	Bit	Description
vhp_ldolvl[1:0]	7:6	HP output driver supply voltage select 00 – 1.5v 01 – 1.4v 10 – 1.3v 11 – 1.2v
cpn_ldolvl[1:0]	5:4	HP output driver supply voltage select 00 – -1.15v 01 – -1.25v 10 – -1.35v 11 – -1.45v
cpn_swlv[1:0]	3:2	Reserved, CP power automatic switching level 00 – -1.5v 01 – -1.4v 10 – -1.3v 11 – -1.2v
pdn_CPNLDO	1	Power down CP negative supply regulator
pdn_cpvncomp	0	Reserved, power down level switching

REGISTER 0X1C – CALIBRATION, DEFAULT 0X0F

Bit Name	Bit	Description
HPL_iCal_on	3	ical: analog calibration, mV level 0 – iCal off 1 – iCal on(default), auto clear to "0" after iCal
HPL_mCal_on	2	mCal: digital calibration, uV level 0 – mCal off 1 – mCal on(default), auto clear after mCal
HPR_iCal_on	1	ical: analog calibration, mV level 0 – iCal off 1 – iCal on(default), auto clear to "0" after iCal
HPR_mCal_on	0	mCal: digital calibration, uV level 0 – mCal off 1 – mCal on(default), auto clear after mCal

REGISTER 0X1D – CALIBRATION, DEFAULT 0X00

Bit Name	Bit	Description
mcal_fast	7	mcal fast mode 0 – normal mode 1 – fast mode
ical_raw	6	ical raw 0 – use mcal to find a better ical data 1 – ical raw
mCal_step	5:4	mCal resolution 00 – vpp/8192 01 – vpp/4096 10 – vpp/2048 11 – vpp/1024
cal_stl	3:2	Calibration settling time, per calculate 00 – 4 (default) 01 – 8 10 – 16 11 – 32
HPL_iCal_8	1	HPL_iCal MSB
HPR_iCal_8	0	HPR_iCal MSB

REGISTER 0X1E – CALIBRATION, DEFAULT 0X80

Bit Name	Bit	Description
HPL_iCal[7:0]	7:0	Reserved

REGISTER 0X1F – CALIBRATION, DEFAULT 0X80

Bit Name	Bit	Description
HPF_iCal[7:0]	7:0	Reserved

REGISTER 0X20 – CALIBRATION, DEFAULT 0X00

Bit Name	Bit	Description
HPL_mCal[7:0]	7:0	Reserved

REGISTER 0X21 – CALIBRATION, DEFAULT 0X00

Bit Name	Bit	Description
HPR_mCal[7:0]	7:0	

REGISTER 0X22 – ADC, DEFAULT 0XC0

Bit Name	Bit	Description
PdnAInL	7	Power down PGA
PdnModL	6	Power down ADC modulator
LInSel[1:0]	5:4	PGA input select 00 – Lin1-Rin1 (MIC DF) 01 – Lin2-Rin2 (Board DF) 10 – Lin1 DF2SE (MIC) 11 – Lin2 DF2SE (Board)

REGISTER 0X23 – ADC, DEFAULT 0X00

Bit Name	Bit	Description
LPGAGain[3:0]	7:4	Left PGA gain 0000 – -3.5dB (default) 0001 – 0dB 0010 – 2.5dB 0011 – 4.5dB 0100 – 7dB 0101 – 10dB 0110 – 13dB 0111 – 16dB 1000 – 18dB 1001 – 21dB 1010 – 24dB others – 0dB

REGISTER 0X24 – ADC, DEFAULT 0X01

Bit Name	Bit	Description
DCM	1	DC measure 0 – disable 1 – enable
DF2SE_15dB	0	DF2SE intensive: 0 – 0dB 1 – 15dB

REGISTER 0X25 – ADC, DEFAULT 0X08

Bit Name	Bit	Description
adcFsMode	4	adc fs mode 0 – single speed 1 – double speed
adc_HPF_L	3	0 – disable ADC left channel high pass filter 1 – enable ADC left channel high pass filter (default)
dmic_src[1:0]	1:0	digital mic control 0x – dmic disable 10 – DMIC high 11 – DMIC low

REGISTER 0X26 – ADC, DEFAULT 0X10

Bit Name	Bit	Description
adcMute	5	ADC mute 0 – normal 1 – mute ADC volume to -96dB
adcSoftRamp	4	adc soft ramp 0 – disable 1 – adc soft ramp enable
adcInVL	1	0 – normal (default) 1 – left channel polarity inverted

REGISTER 0X27 – ADC, DEFAULT 0XC0

Bit Name	Bit	Description
adcVolumeL	7:0	00000000 – 0dB 00000001 – -0.5dB 00000010 – -1dB ... 11000000 – -96dB(default)

REGISTER 0X29 – ADC, DEFAULT 0X1C

Bit Name	Bit	Description
ALCSEL	7:6	00 – alc off other – alc on
ALCMODE	5	Determines the ALC mode of operation: 0 – ALC mode (Normal Operation) 1 – Limiter mode.
MAXGAIN[4:0]	4:0	ALC MAXGAIN[1:0] for PGA max gain 00000 – -6.5dB 00001 – -5 dB 00010 – -3.5dB 00011 – -2dB 00100 – -0.5dB 00101 – +1dB 00100 – +2.5dB 00111 – +4dB 01000 – +5.5dB 01001 – +7dB 01010 – +8.5dB 01011 – +10dB 01100 – +11.5dB 01101 – +13dB 01110 – +14.5dB 01111 – +16dB 10000 – +17.5dB 10001 – +19dB 10010 – +20.5dB 10011 – +22dB 10100 – +23.5dB 10101 – +25dB 10110 – +26.5dB 10111 – +28dB

		11000 – +29.5dB 11001 – +31dB 11010 – +32.5dB 11011 – +34dB others – +35.5dB
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REGISTER 0X2A – ADC, DEFAULT 0X00

Bit Name	Bit	Description
MINGAIN[4:0]	4:0	ALC MINGAIN[1:0] for PGA min gain 00000 – -12dB 00001 – -10.5 dB 00010 – -9dB 00011 – -7.5dB 00100 – -6dB 00101 – -4.5dB 00100 – -3dB 00111 – -1.5dB 01000 – 0dB 01001 – +1.5dB 01010 – +3dB 01011 – +4.5dB 01100 – +6dB 01101 – +7.5dB 01110 – +9dB 01111 – +10.5dB 10000 – +12dB 10001 – +13.5dB 10010 – +15dB 10011 – +16.5dB 10100 – +18dB 10101 – +19.5dB 10110 – +21dB 10111 – +22.5dB 11000 – +24dB 11001 – +25.5dB 11010 – +27dB 11011 – +28.5dB others – +30dB

REGISTER 0X2B – ADC, DEFAULT 0XB0

Bit Name	Bit	Description
ALCLVL	7:4	ALC target 0000 – -16.5 dB 0001 – -15 dB 0010 – -13.5 dB 0111 – -6 dB 1000 – -4.5 dB 1001 – -3 dB 1010-1111 – -1.5 dB
ALCHLD	3:0	ALC hold time before gain is increased

		0000 – 0ms 0001 – 2.67ms 0010 – 5.33ms (time doubles with every step) 1001 – 0.68s 1010 or higher – 1.36s
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REGISTER 0X2C – ADC, DEFAULT 0X32

Bit Name	Bit	Description
ALCDCY	7:4	ALC decay (gain ramp up) time at ALC mode/limiter mode: 0000 – 410 us/90.8 us 0001 – 820 us/182us 0010 – 1.64 ms/363us (time doubles with every step) 1001 – 210 ms/46.5 ms 1010 or higher – 420 ms/93 ms
ALCATK	3:0	ALC attack (gain ramp down) time at ALC mode/limiter mode: 0000 – 104 us/22.7 us 0001 – 208 us/45.4 us 0010 – 416 us/90.8 us (time doubles with every step) 1001 – 53.2 ms/11.6 ms 1010 or higher – 106 ms/23.2 ms

REGISTER 0X2D – ADC, DEFAULT 0X03

Bit Name	Bit	Description
WIN_SIZE	4:0	Windows size for peak detector, set the window size to N*16 samples 00110 – 96 samples (default) 00111 – 102 samples ... 11111 – 496 samples

REGISTER 0X2E – ADC, DEFAULT 0X00

Bit Name	Bit	Description
ALC_NGG	6	noise gate type 0 – original gain(default) 1 – mute
ALC_NGAT	5	noise gate enable 0 – disable(default) 1 – enable
ALC_NGTH	4:0	Noise gate threshold 00000 – -76.5 dBFS 00001 – -75 dBFS 11110 – -31.5 dBFS 11111 – -30 dBFS

REGISTER 0X2F – DAC, DEFAULT 0X11

Bit Name	Bit	Description
PdnDacl	4	Pdn Left DAC

		0 – normal 1 – power down
PdnDacR	0	Power down right DAC 0 – normal 1 – power down

REGISTER 0X30 – DAC, DEFAULT 0X10

Bit Name	Bit	Description
dacDATSEL	7:6	for dacDATSEL 00 – Lin->Lout, Rin->Rout 01 – Lin->Lout, Lin->Rout 10 – Rin->Lout, Rin->Rout 11 – Rin->Lout, Lin->Rout
dacMute	5	dac mute 0 – normal 1 – mute dac volume to -96dB
dacSoftRamp	4	dac soft ramp 0 – normal 1 – dac soft ramp enable
dacRampRate	3:2	00 – 0.5 dB per 4 LRCKs (default) 01 – 0.5 dB per 32 LRCKs 10 – 0.5 dB per 64 LRCKs 11 – 0.5 dB per 128 LRCKs
dacInVL	1	0 – normal DAC left channel analog output no phase inversion (default) 1 – normal DAC left channel analog output 180 degree phase inversion
dacInVR	0	0 – normal DAC right channel analog output no phase inversion (default) 1 – normal DAC right channel analog output 180 degree phase inversion

REGISTER 0X31 – DAC, DEFAULT 0X00

Bit Name	Bit	Description
dacFsMode	7	fs mode 0 – single speed 1 – double speed
dacNotchMode	6	0 – normal 1 – DAC at DS, FS*2, to cancel DAC harmonic noise
dacAutoMute	5	auto mute control 0 – auto mute dis (default) 1 – auto mute en
automute_type	4	0 – mute L when L=0, mute R when R=0 1 – mute L/R when L and R=0
dacLeR	2	0 – normal (default) 1 – both channel gain control is set by DAC left gain control register

REGISTER 0X32 – DAC, DEFAULT 0X00

Bit Name	Bit	Description
Vpp_scale	7:6	00 – Vpp set at 3.5V (0.7 modulation index) (default) 01 – Vpp set at 4.0V 10 – Vpp set at 3.0V 11 – Vpp set at 2.5V
dacZeroL	5	0 – normal (default)

		1 – set Left Channel DAC output all zero
dacZeroR	4	0 – normal (default) 1 – set Right Channel DAC output all zero
dacMono	3	0 – stereo (default) 1 – mono (L+R)/2 into DACL and DACR
Se_strength	2:0	SE strength 000 – 0 (default) 111 – 7

REGISTER 0X33 – DAC, DEFAULT 0XCO

Bit Name	Bit	Description
dacVolumeL	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB. 00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB ... 11000000 – -96 dB (default)

REGISTER 0X34 – DAC, DEFAULT 0XCO

Bit Name	Bit	Description
dacVolumeR	7:0	Digital volume control attenuates the signal in 0.5 dB incremental from 0 to –96 dB. 00000000 – 0 dB 00000001 – -0.5 dB 00000010 – -1 dB ... 11000000 – -96 dB (default)

REGISTER 0X4D – GPIO, DEFAULT 0X00

Bit Name	Bit	Description
gpio3_sel	3:2	00 – Interrupt out 01 – clk_cp out 10 – adc_mclk out 11 – dac_mclk out
gpio2_sel	1	0 – GMShorted in 1 – DMIC_SCL out
gpio1_sel	0	0 – HPInserted in 1 – ADCLRCK inout

REGISTER 0X4E – GPIO, DEFAULT 0X00

Bit Name	Bit	Description
button_debounce[1:0]	7:6	Headset Button debounce: 00 – 256fs - 5.3ms 01 – 512fs - 10.6ms 10 – 1024fs - 21ms 11 – 2048fs - 42ms
insert_debounce[1:0]	5:4	Headset Detection debounce 00 – 512fs - 10.6ms 01 – 1024fs - 21ms 10 – 4096fs - 84ms

		11 – 16384fs - 341ms
int_en	1	interrupt control 0 – disable (default) 1 – enable
int_pol	0	interrupt polarity 0 – high active 1 – low active

REGISTER 0X4F – FLAG, DEFAULT 0X00

Bit Name	Bit	Description
csm_chip	5:4	chip csm 00 – PwDown 01 – Pseq1 11 – Pseq2 10 – Normal
Master_err	3	Reserved
FlagHPInserted	2	HP inserted read only flag 0 – HP not inserted 1 – HP inserted
FlagGMShorted	1	GM shorted read only flag 0 – GM not shorted 1 – GM shorted

10. CORPORATE INFORMATION

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