FORESEE®

2Gbit SPI NAND Flash

F35UQA002G

Datasheet

LM-00005

Rev 1.2

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Revision History

Rev.	Date	Changes	Editor
1.0	2021/01/15	1. Initial release.	Alex
1.1	2021/11/08	1. Fix typo issue in Table 4 and Table 14. 2. Revise descriptions in 4, 12.5, 12.7, 12.8, 14.1.	Alex
1.2	2021/12/01	1. Add chapter 15.	Alex

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1 General Description

The F35UQA002G is a 2G-bit (256Mx8bit) Serial NAND Flash Memory, operates on a single 1.8V VCC. The device supports the standard Serial Peripheral Interface (SPI), Dual/Quad SPI: Serial Clock, Chip Select, Serial Data SIO0 (DI), SIO1 (DO), SIO2 (WP#) and SIO3 (HOLD#). SPI clock frequencies of up to 83 MHz are supported.

The F35UQA002G supports JEDEC standard manufacturer and device ID, Unique ID, one parameter page and 62 OTP pages. An internal 1-bit ECC logic is available in the chip, which is enabled by default. The internal ECC can be disabled or enabled by command.

2 Features

Voltage Supply
- VCC: 1.7V ~ 1.95V

Organization
- Memory Cell Array: (256M + 8M) Byte
- Page Size: (2k + 64) Byte
- Block Size: 64 pages, (128k + 4k) Byte

Serial Interface
- Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
- Dual SPI: CLK, CS#, SIO0-SIO1, WP#, HOLD#
- Quad SPI: CLK, CS#, SIO0-SIO3

High Performance
- 83 MHz Standard/Dual/Quad SPI clocks
- Page Program Time: 350μs (Typ.)
- Block Erase Time: 2ms (Typ.)

Low Power
- Standby: 10μA (Typ.)
- Page Read: 10mA (Typ.)
- Program/Erase: 15mA (Typ.)

Advanced Features
- On chip 1-Bit ECC for memory array
- Software and Hardware write protect
- Unique ID
- One 2kB parameter page
- Sixty-two 2kB OTP Pages
- Promised golden block0

High Reliability
- Endurance: typical 100k cycles (1)
- Data Retention: 10 years (1)

Package
- 8-WSON (8x6mm)

Note:
(1) Endurance and Data Retention specification is based on 1bit / 528Byte ECC

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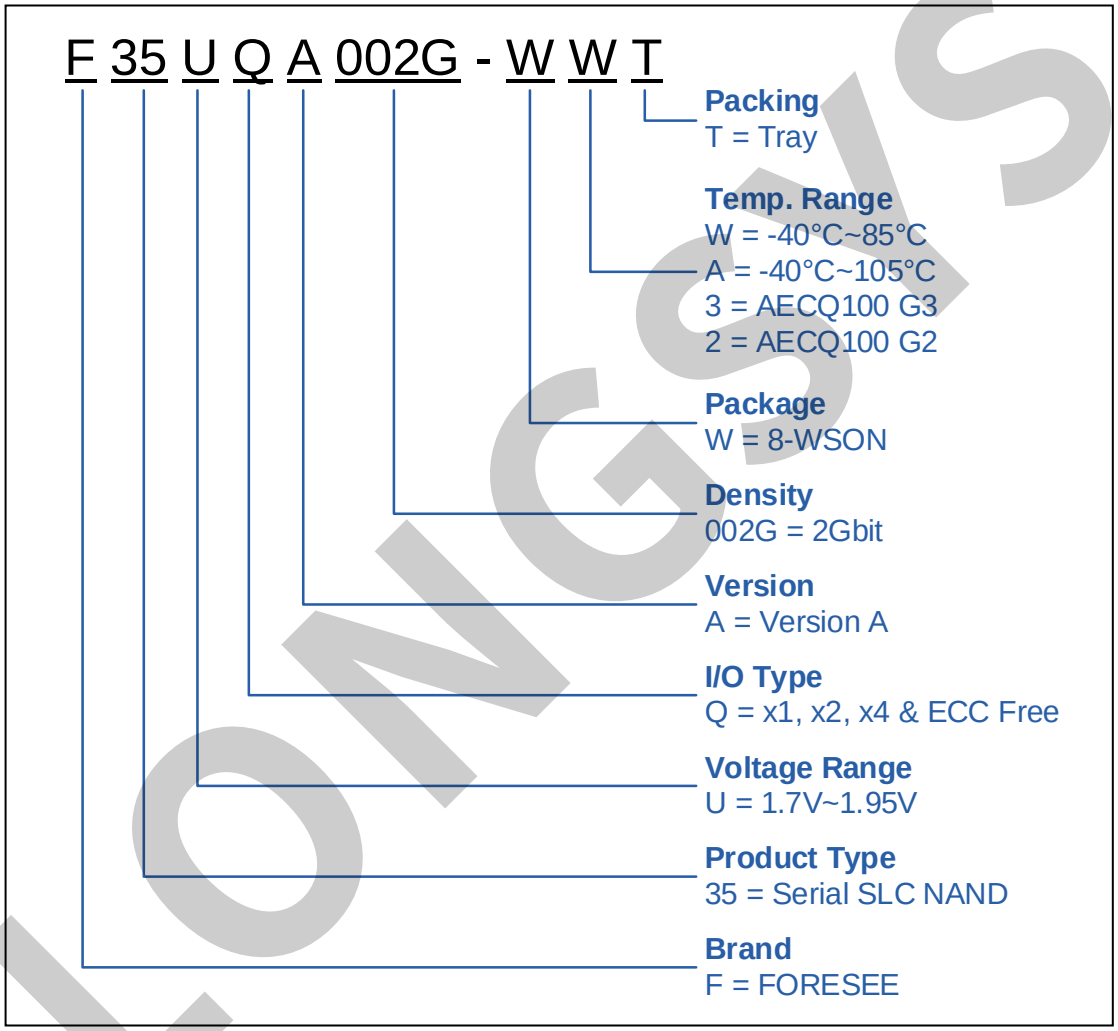
3 Product List

Table 1 Product List

Part Number	Density	I/O Type	Voltage Range	Package	Temp. Range	Packing
F35UQA002G-WWT	2Gb	x1, x2, x4	1.7V~1.95V	8-WSON (8x6mm)	-40°C ~ 85°C	Tray
F35UQA002G-WAT	2Gb	x1, x2, x4	1.7V~1.95V	8-WSON (8x6mm)	-40°C ~ 105°C	Tray

Figure 1 Marketing Part Numbering Chart



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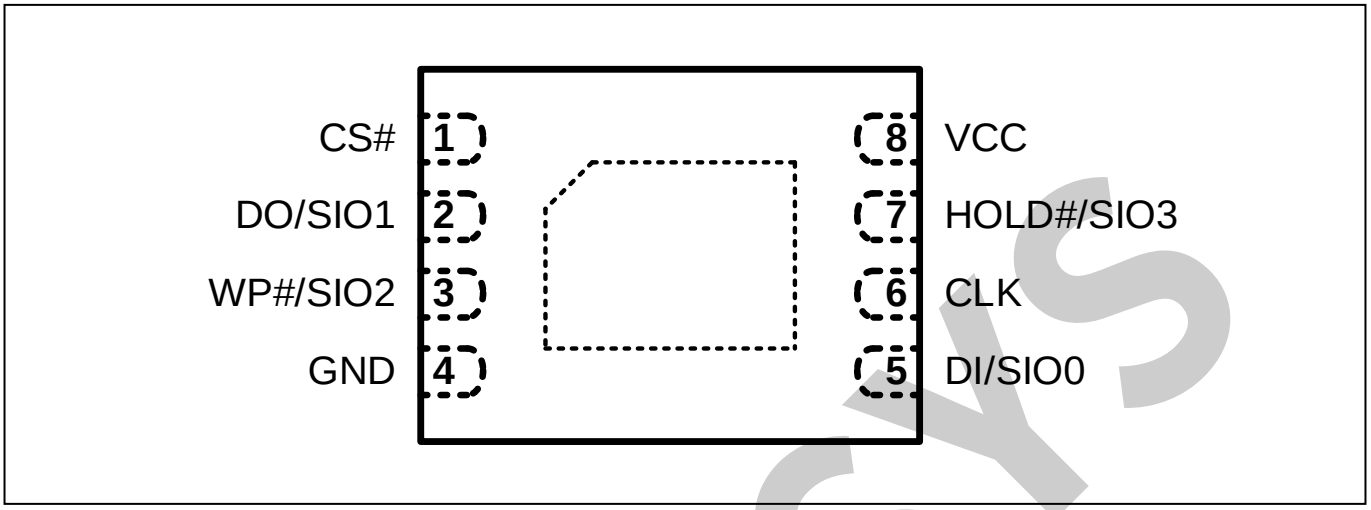
4 Package Types and Pin Configurations

Figure 2 Pin Configuration 8-WSON (8x6mm)



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5 Pin Descriptions

Table 2 Pin Description

Pin Name	Pin Functions
CS#	**Chip Select** The SPI Chip Select pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO or SIO0-3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.
DI, DO and SIO0-SIO3	**Serial Data Input, Output and IOs** The device supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK. Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.
WP#	**Write Protect** The WP# pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect bits (BP[3:0], TB) and Status Register Protect bits (BPRWD, SP), a portion as small as 128k-Byte (one block) or up to the entire memory array can be hardware protected.
HOLD#	**Hold** During Standard and Dual SPI operations, the HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD# is brought high, device operation can resume. The HOLD function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low. When a Quad SPI Read/Program Data Load command is issued, HOLD# pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finishes.
CLK	**Serial Clock** The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.
GND	**Ground**
VCC	**VCC** Power Supply
NC	**No Connection**

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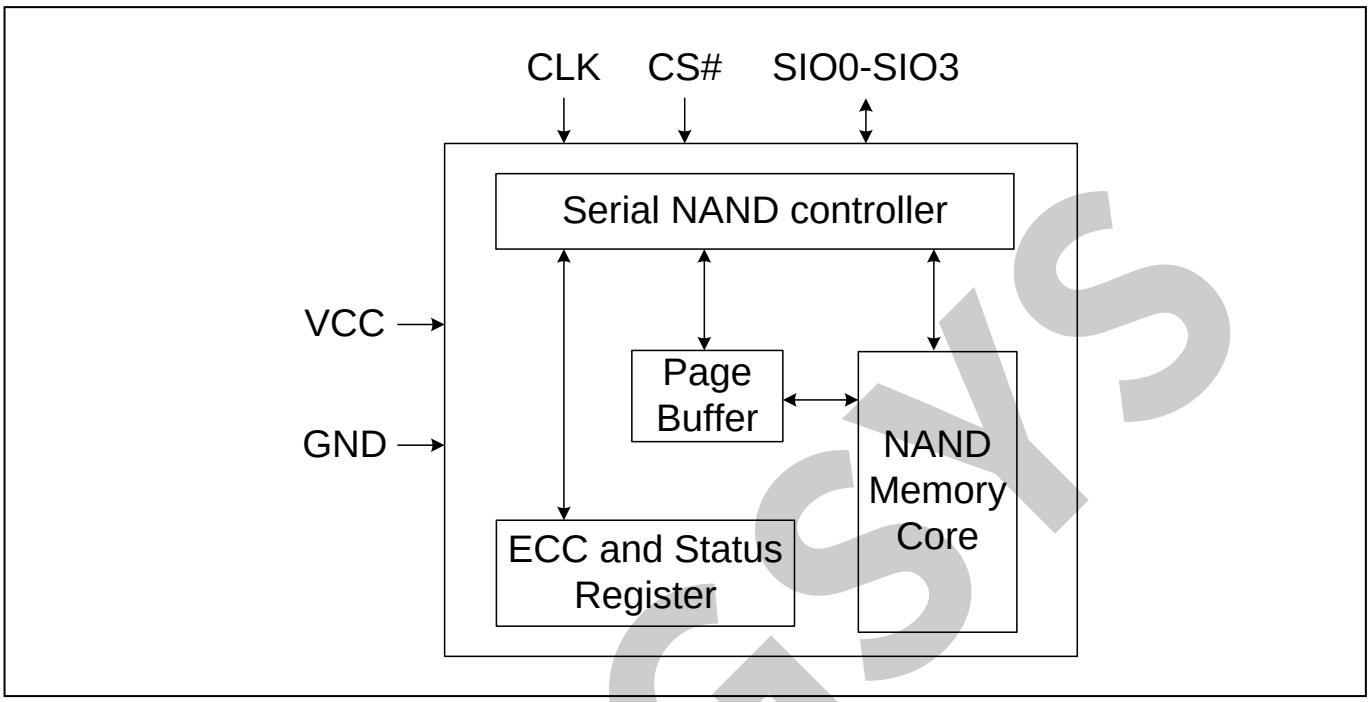
6 Block Diagram

Figure 3 Block Diagram



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7 Array Organization and Mapping

Figure 4 Array Organization

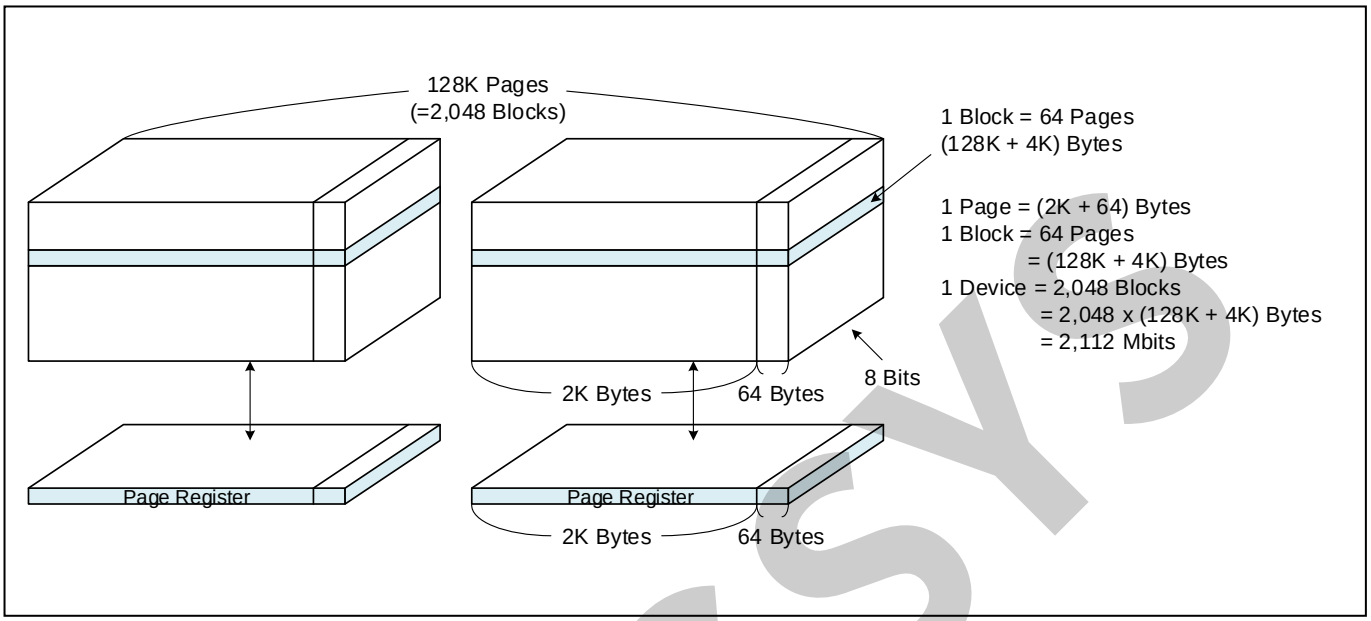
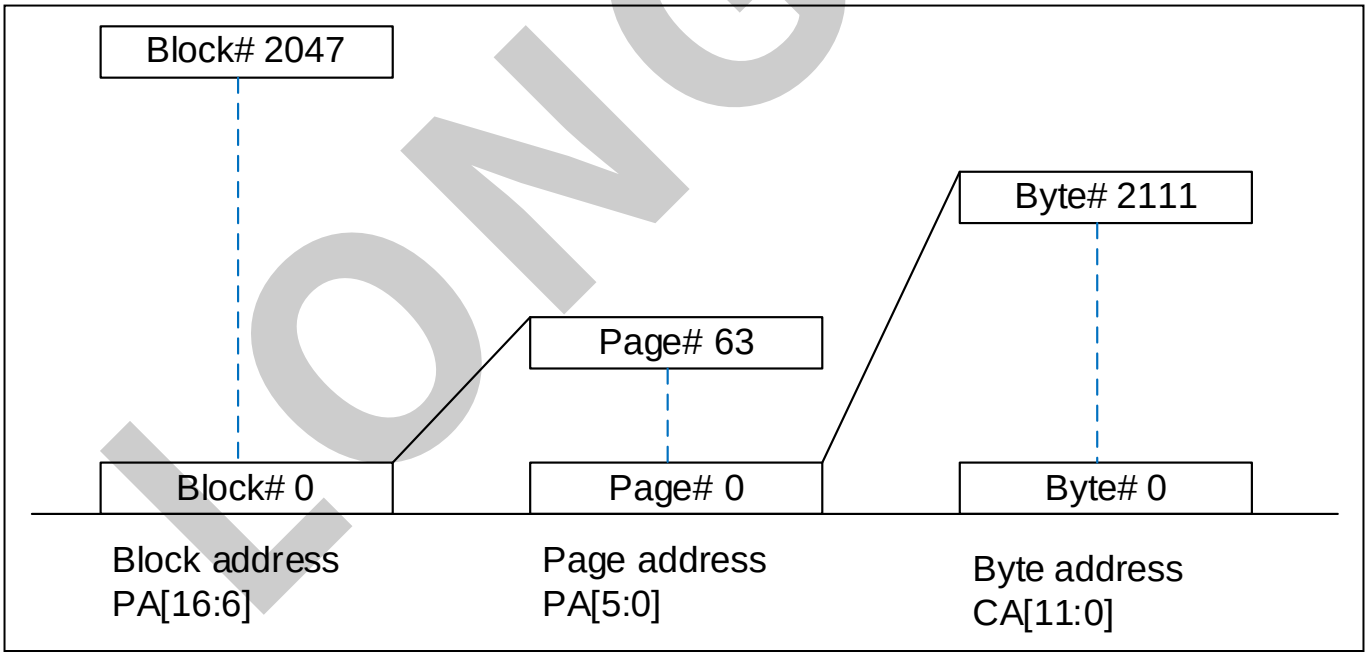


Figure 5 Address Mapping



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8 Device Operation

8.1 General

1. Before a command is issued, status register should be checked via get features operations to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SIO pin of this device should be High-Z.
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.

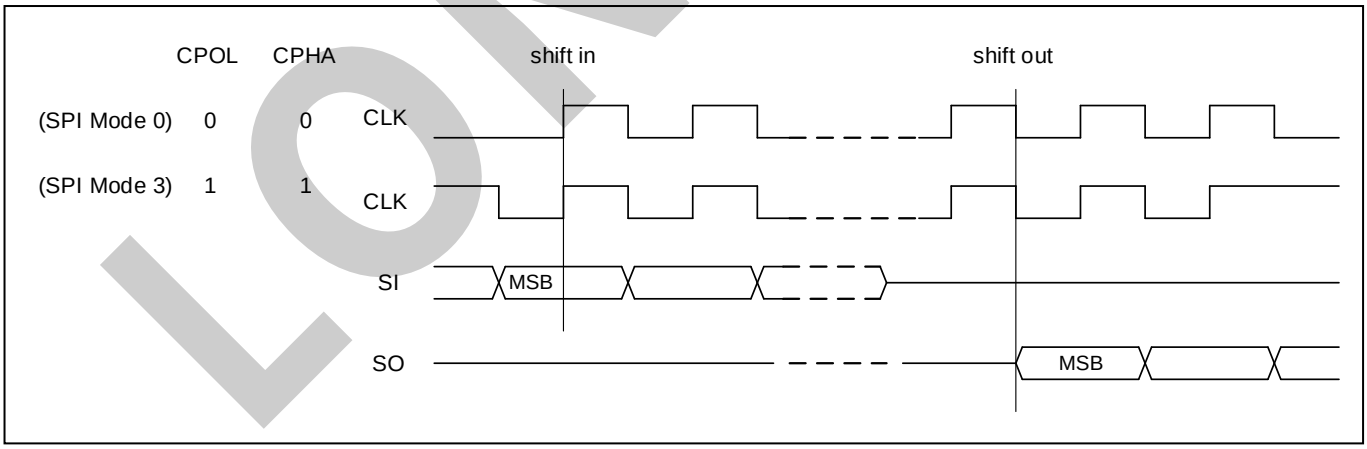
8.2 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of CLK and data shifts out on the falling edge of CLK for both modes. All timing diagrams shown in this data sheet are mode 0. The difference of Mode 0 and Mode 3 is shown as **Figure 6**.

Figure 6 SPI Mode Supported



Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI.

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When using the Dual SPI command the DI and DO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

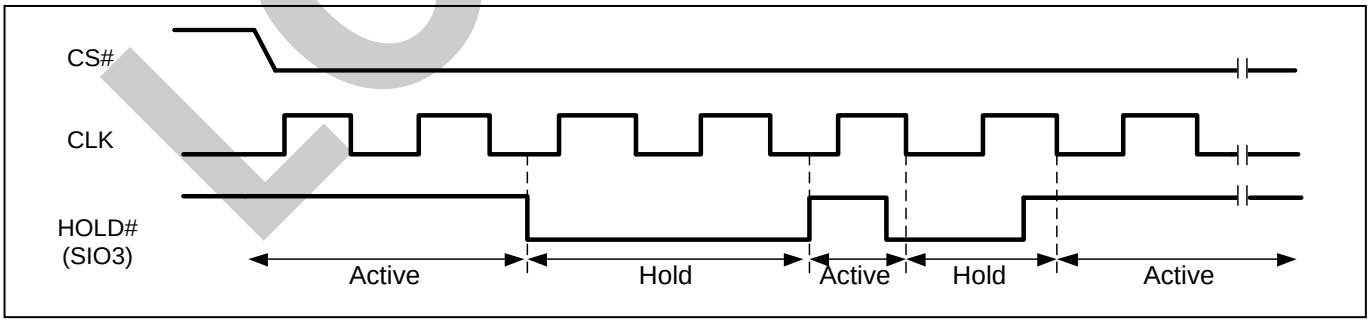
SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the DI and DO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

8.3 Hold Function

For Standard SPI and Dual SPI operations, the HOLD# signal allows the device operation to be paused while it is actively selected (when CS# is low). The Hold function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the Hold function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The Hold function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When a Quad SPI command is issued, HOLD# pin will act as a dedicated IO pin (SIO3).

To initiate a HOLD condition, the device must be selected with CS# low. A HOLD condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD condition will activate after the next falling edge of CLK. The HOLD condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD condition will terminate after the next falling edge of CLK. During a HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD operation to avoid resetting the internal logic state of the device. See **Figure 7** for more details.

Figure 7 Hold Condition



8.4 Write Protection

The device provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold

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- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute or Block Erase instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (BPRWD, SP) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the WP# pin, changes to the Status Register can be enabled or disabled under hardware control. See **Protection Register (SR-1)** for further information.

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9 Status Registers

Three Status Registers are: Protection Register (SR-1), Configuration Register (SR-2) and Status Register (SR-3). Each register is accessed by Get Feature (0Fh) and Set Feature (1Fh) commands combined with 1-Byte Register Address respectively.

Four Sector ECC Status Registers can be accessed by Get Feature (0Fh) command combined with 1-Byte Register Address respectively.

Table 3 Status Registers

Register	Address	Data Bits							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Protection	A0h	BPRWD	BP3	BP2	BP1	BP0	TB	R	SP
Configuration	B0h	OTP-L	OTP-E	R	ECC-E	R	DRV1	DRV0	QE
Status	C0h	R	R	ECCS1	ECCS0	P-FAIL	E-FAIL	WEL	OIP
Sector0 ECC Status	80h	R	R	0	0	S0ES3	S0ES2	S0ES1	S0ES0
Sector1 ECC Status	84h	R	R	0	1	S1ES3	S1ES2	S1ES1	S1ES0
Sector2 ECC Status	88h	R	R	1	0	S2ES3	S2ES2	S2ES1	S2ES0
Sector3 ECC Status	8Ch	R	R	1	1	S3ES3	S3ES2	S3ES1	S3ES0

Note:

(1) R: Reserved Bit and has no function. They may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a Set Feature command, the Reserved Bits can be written as “0”, but there will not be any effects.

The Reset command (FFh) will not clear the previous feature setting, the feature setting data bits remain until the power is being cycled or modified by the settings in the table below. After a Reset command is issued, the OIP bit will go high. This bit can be polled to determine when the Reset operation is complete, as it will return to the default value (0) after the reset operation is finished. Issuing the Reset command has no effect on the Block Protection and Configuration registers.

Table 4 Default Values of the Status Registers after power up and Device Reset

Register	Address	Bits	Shipment Default	Power Up	After Reset Command
Protection	A0h	BP3-0,TB	1 1 1 1 1	1 1 1 1 1	No Change
		BPRWD	0	0	No Change
		SP	0	0	No Change
Configuration	B0h	OTP-L	0	Locked:1, else 0	No Change
		OTP-E	0	0	No Change
		ECC-E	1	1	No Change
		QE	0	0	No Change
		DRV1-0	0 0	0 0	No Change

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Register	Address	Bits	Shipment Default	Power Up	After Reset Command
Status	C0h	ECCS1-0	0 0	Status of Page0 of Block0	0 0
		P-FAIL	0	0	0
		E-FAIL	0	0	0
		WEL	0	0	0
		OIP	0	0	0
Sector0 ECC Status	80h	S0ES3-0	0 0 0 0	Status of Page0 of Block0	0 0 0 0
Sector1 ECC Status	84h	S1ES3-0	0 0 0 0	Status of Page0 of Block0	0 0 0 0
Sector2 ECC Status	88h	S2ES3-0	0 0 0 0	Status of Page0 of Block0	0 0 0 0
Sector3 ECC Status	8Ch	S3ES3-0	0 0 0 0	Status of Page0 of Block0	0 0 0 0

9.1 Protection Register (SR-1)

9.1.1 Block Protect Bits (BP3-0, TB)

The Block Protect bits (BP3-0, TB) are volatile read/write bits that provide Write Protection control and status. Block Protect bits can be set using the Set Feature Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (See **Table 6**). The default values for the Block Protection bits are 1 after power up to protect the entire array.

9.1.2 Status Register Protect Bits (BPRWD, SP)

The Status Register Protect bits (BPRWD, SP) are volatile read/write bits which control the method of write protection: software protection, hardware protection, power supply lock-down.

Table 5 Status Register Protection

BPRWD	SP	QE	WP#	Descriptions
X	0	1	X	SR-1 can be changed No WP# functionality, WP# pin will always function as SIO2
X	1	X	X	SR-1 cannot be changed during the current power cycle
0	0	0	X	SR-1 can be changed
1	0	0	0	SR-1 can NOT be changed
1	0	0	1	SR-1 can be changed

Note:

(1) When SP =1, a power-down, power-up cycle will change (BPRWD, SP) to (0, 0) state.

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9.1.3 Status Register Memory Protection

Table 6 Block Protection Bits

TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[16:0]	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	2047	1FFC0h – 1FFFFh	128KB	Upper 1/2048
0	0	0	1	0	2046 & 2047	1FF80h – 1FFFFh	256KB	Upper 1/1024
0	0	0	1	1	2044 thru 2047	1FF00h – 1FFFFh	512KB	Upper 1/512
0	0	1	0	0	2040 thru 2047	1FE00h – 1FFFFh	1MB	Upper 1/256
0	0	1	0	1	2032 thru 2047	1FC00h – 1FFFFh	2MB	Upper 1/128
0	0	1	1	0	2016 thru 2047	1F800h – 1FFFFh	4MB	Upper 1/64
0	0	1	1	1	1984 thru 2047	1F000h – 1FFFFh	8MB	Upper 1/32
0	1	0	0	0	1920 thru 2047	1E000h – 1FFFFh	16MB	Upper 1/16
0	1	0	0	1	1792 thru 2047	1C000h – 1FFFFh	32MB	Upper 1/8
0	1	0	1	0	1536 thru 2047	18000h – 1FFFFh	64MB	Upper 1/4
0	1	0	1	1	1024 thru 2047	10000h – 1FFFFh	128MB	Upper 1/2
1	0	0	0	1	0	00000h – 0003Fh	128KB	Lower 1/2048
1	0	0	1	0	0 & 1	00000h – 0007Fh	256KB	Lower 1/1024
1	0	0	1	1	0 thru 3	00000h – 000FFh	512KB	Lower 1/512
1	0	1	0	0	0 thru 7	00000h – 001FFh	1MB	Lower 1/256
1	0	1	0	1	0 thru 15	00000h – 003FFh	2MB	Lower 1/128
1	0	1	1	0	0 thru 31	00000h – 007FFh	4MB	Lower 1/64
1	0	1	1	1	0 thru 63	00000h – 00FFFh	8MB	Lower 1/32
1	1	0	0	0	0 thru 127	00000h – 01FFFh	16MB	Lower 1/16
1	1	0	0	1	0 thru 255	00000h – 03FFFh	32MB	Lower 1/8
1	1	0	1	0	0 thru 511	00000h – 07FFFh	64MB	Lower 1/4
1	1	0	1	1	0 thru 1023	00000h – 0FFFFh	128MB	Lower 1/2
X	1	1	X	X	0 thru 2047	00000h – 1FFFFh	256MB	ALL

Note:

(1) X = don't care

(2) If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

9.2 Configuration Register (SR-2)

9.2.1 One Time Program Lock Bit (OTP-L)

OTP-L is non-volatile.

The device provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 62 pages of 2,112-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and the

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OTP area cannot be erased.

Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

9.2.2 Enter OTP Access Mode Bit (OTP-E)

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

9.2.3 ECC Enable Bit (ECC-E)

The device has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 64-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be changed by the Device Reset command.

9.2.4 Output Driver Strength (DRV1-0)

Table 7 Output Driver Strength

DRV1	DRV0	Output Driver Strength
0	0	100% (default)
0	1	75%
1	0	50%
1	1	25%

9.2.5 Quad Enable Bit (QE)

The Quad Enable (QE) bit is a volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, HOLD# are enabled. While QE is "1", it performs Quad I/O mode and WP#, HOLD# are disabled. In another word, if the system goes into four I/O mode (QE=1), the WP# and HOLD# function will be disabled. Upon power cycle, the QE bit will go into the factory default setting "0".

9.3 Status Register (SR-3)

9.3.1 ECC Status Bit (ECCS1-0)

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECCS1, ECCS0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a RESET command.

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The ECCS1-0 value reflects the ECC status of the content of the page 0 of block 0 after a power-on reset.

Table 8 ECC Bits Status

ECCS1	ECCS0	Description
0	0	No bit errors were detected during the previous read operation
0	1	1-bit error was detected in one or more sector and was corrected
1	X	More than 1-bit error was detected in one or more sector and cannot be corrected

9.3.2 Program/Erase Failure (P-FAIL, E-FAIL)

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. P-FAIL bit will also be set when the Program command is issued to a protected block or locked OTP area, and E-FAIL bit will also be set when the Erase command is issued to a protected block. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device Reset command.

9.3.3 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit. The WEL bit is set to 1 after executing a Write Enable Instruction. The WEL bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read, and Program Execute for OTP pages.

9.3.4 Operation in Progress (OIP)

OIP is a read only bit that is set to a 1 state when the device is powering up or executing a Page Read, Program Execute, Block Erase and OTP Locking. During this time the device will ignore further instructions except for the Get Feature or Soft Reset instructions. When the program, erase or page read instruction has completed, the OIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

9.4 Sector ECC Status Register (Sector ECC Status0-3)

A sector is composed by a 512 Byte main areas and a 16 Byte spare area, so a page has four sectors. The Sector ECC Status Register indicates the number of errors in each sector as identified from an ECC check during a read operation.

Table 9 2Kbyte Page Assignment

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare
512B	512B	512B	512B	16B	16B	16B	16B

Table 10 Definition of 528Btye Sector

Sector	Column Address (Byte)	
	Main Field	Spare Field

1st Sector	0 ~ 511	2,048 ~ 2,063
2nd Sector	512 ~ 1,023	2,064 ~ 2,079
3rd Sector	1,024 ~ 1,535	2,080 ~ 2,095
4th Sector	1,536 ~ 2,047	2,096 ~ 2,111

Table 11 ECC Status Register0-3

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Sector Information		Sector ECC Status			

9.4.1 Sector Information

Table 12 Sector Information

Bit 5 ~ Bit 4	Sector Information
00	1st Sector (Main and Spare area)
01	2nd Sector (Main and Spare area)
10	3rd Sector (Main and Spare area)
11	4th Sector (Main and Spare area)

9.4.2 Sector ECC Status

Table 13 Sector ECC Status

Bit 3 ~ Bit 0	Sector ECC Status
0000	No bit error was detected during the previous read operation
0001	1 bit error was detected in the sector and was corrected
001x	More than 1 bit errors were detected in the sector and cannot be corrected
Others	Reserved

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10 Commands

10.1 Command Set

Table 14 Command Set

Commands	Byte1	Byte2	Byte3	Byte4	Byte5	ByteN
Soft RESET	**FFh**					
Read JEDEC ID	**9Fh**	Dummy	MID	DID	DID	
Get Feature	**0Fh**	SR Addr	S7-0	S7-0	S7-0	S7-0
Set Feature	**1Fh**	SR Addr	S7-0			
Write Enable	**06h**					
Write Disable	**04h**					
Block Erase	**D8h**	**PA23-16**	**PA15-8**	**PA7-0**		
Program Data Load	**02h**	**CA15-8**	**CA7-0**	D7-D0	Next Byte	…
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	D7-D0	Next Byte	…
Quad Program Data Load	**32h**	**CA15-8**	**CA7-0**	D7-D0 / 4	Next Byte	…
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	D7-D0 / 4	Next Byte	…
Program Execute	**10h**	**PA23-16**	**PA15-8**	**PA7-0**		
Page Read (to cache)	**13h**	**PA23-16**	**PA15-8**	**PA7-0**		
Read From Cache	**03h or 0Bh**	**CA15-8**	**CA7-0**	Dummy	D7-D0	Next Byte
Read From Cache x 2	**3Bh**	**CA15-8**	**CA7-0**	Dummy	D7-D0 / 2	Next Byte
Read From Cache x 4	**6Bh**	**CA15-8**	**CA7-0**	Dummy	D7-D0 / 4	Next Byte

Note:

(1) Output designates data output from the device.

(2) Column Address (CA) only requires CA [11:0], CA [15:12] are considered as dummy bits.

(3) Page Address (PA) only requires PA [16:0], PA [23:17] are considered as dummy bits. PA [16:6] is the address for 128kB blocks (total 2,048 blocks), PA [5:0] is the address for 2kB pages (total 64 pages for each block).

(4) Dual SPI Data Output (D7-0 / 2) format:
SIO0 = D6, D4, D2, D0…
SIO1 = D7, D5, D3, D1…

(5) Quad SPI Data Input / Output (D7-0 / 4) format:
SIO0 = D4, D0 …
SIO1 = D5, D1 …
SIO2 = D6, D2 …
SIO3 = D7, D3 …

(6) All Quad Program/Read commands are disabled when QE bit is set to 0 in the Configuration Register

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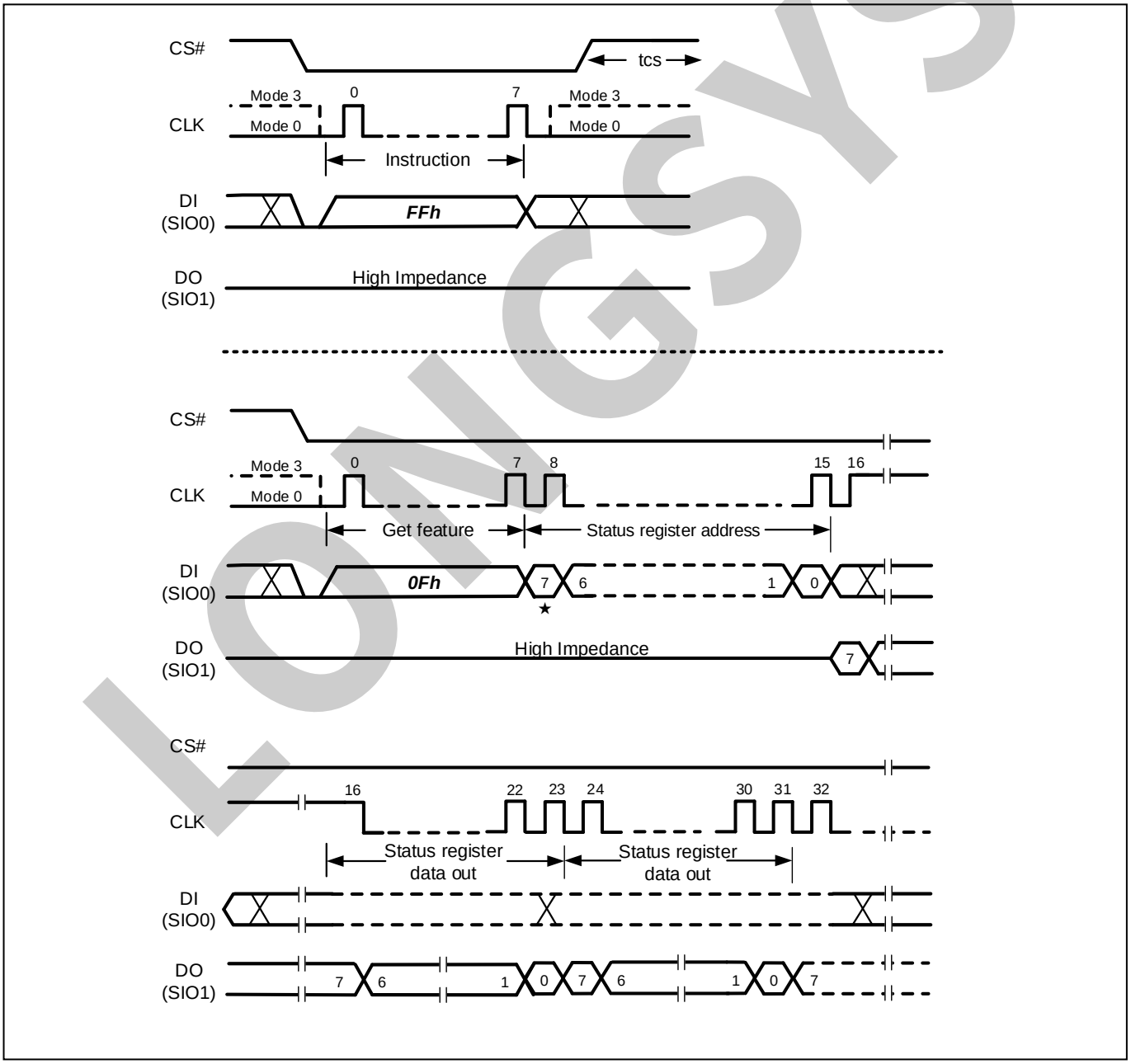
10.2 Soft Reset (FFh)

Once the Reset command is accepted by the device, the device will take approximately tRST to reset, depending on the current operation the device is performing, tRST can be 5us~200us. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command is accepted by the device. It is recommended to check the OIP bit in Status Register before issuing the Reset command.

Figure 8 Soft Reset Sequence



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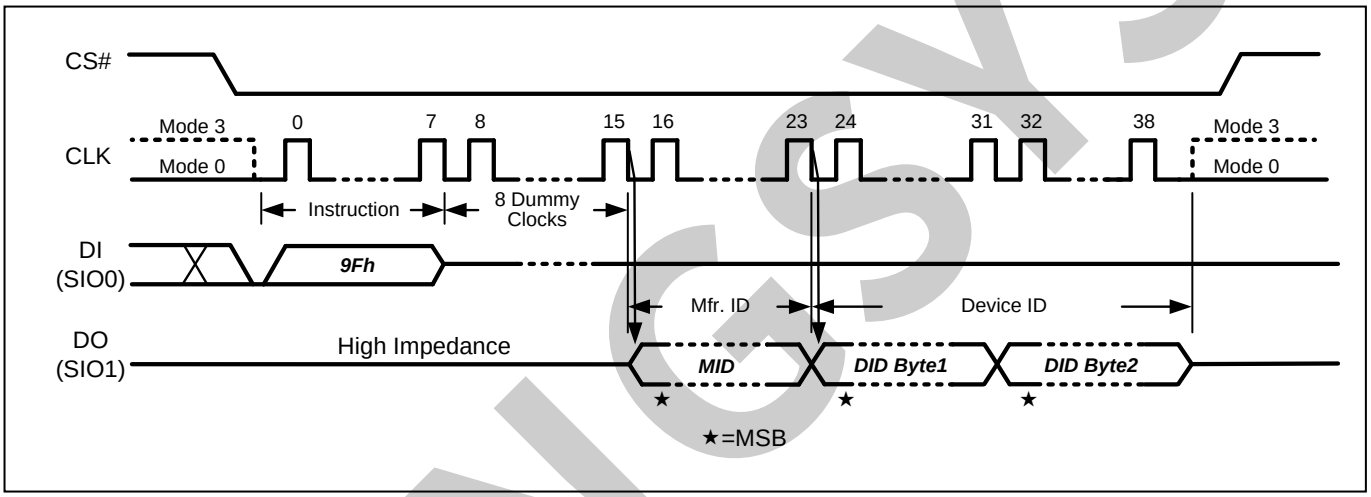
10.3 Read JEDEC ID (9Fh)

The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

Table 15 JEDEC ID

ID		Value
Manufacture ID		CDh
Device ID	Byte 1	62h
	Byte 2	62h

Figure 9 Read JEDEC ID



10.4 Feature Operations

10.4.1 Get Feature (0Fh) and Set Feature (1Fh)

The Get Feature (0Fh) and Set Feature (1Fh) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific feature bits. The status register is mostly read, except WEL, which is a writable bit with the Write Enable (06h) and Write Disable (04h) command. When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified, once the device is set, it remains set, even if a RESET (FFH) command is issued. Refer to **Status Registers** for detail information.

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Figure 10 Get Feature

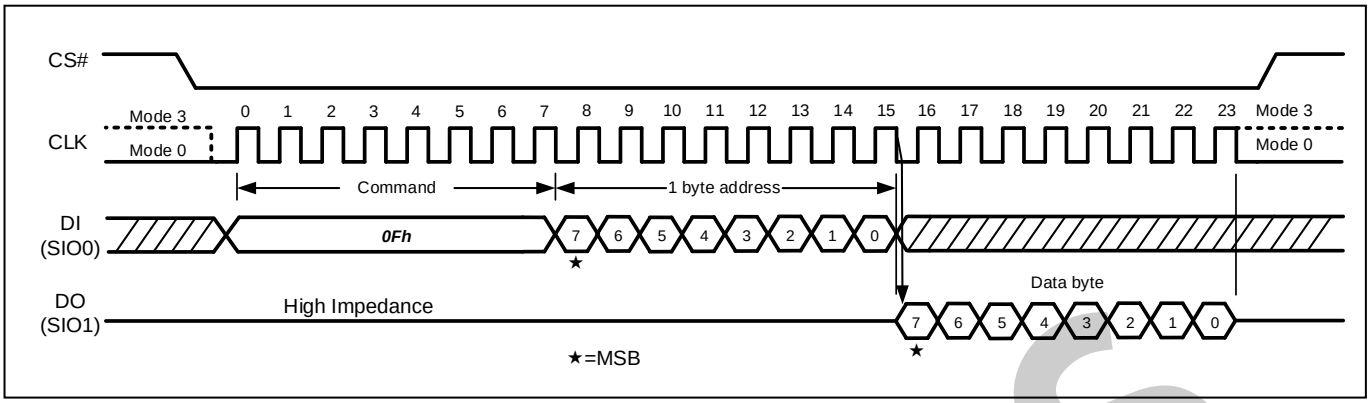
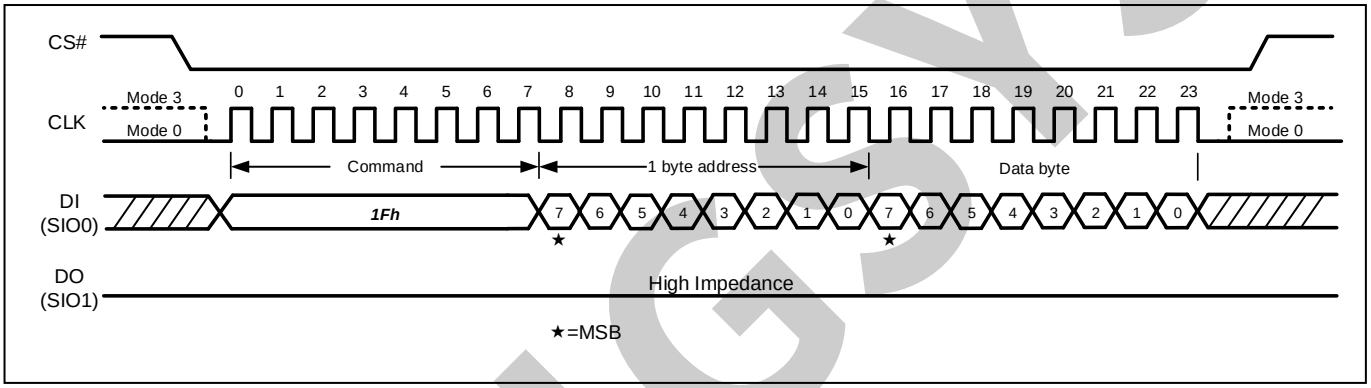


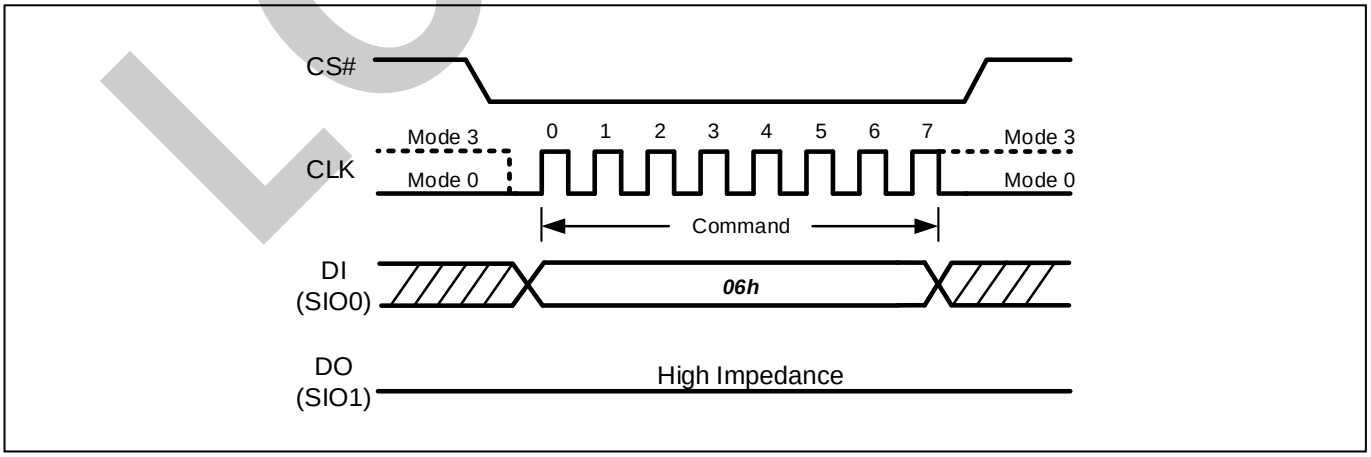
Figure 11 Set Feature



10.4.2 Write Enable (WREN, 06h)

The Write Enable (WREN, 06h) command is for setting Write Enable Latch (WEL) bit. The WEL bit must be set prior to every Page Program, Block Erase and OTP.

Figure 12 Write Enable Sequence



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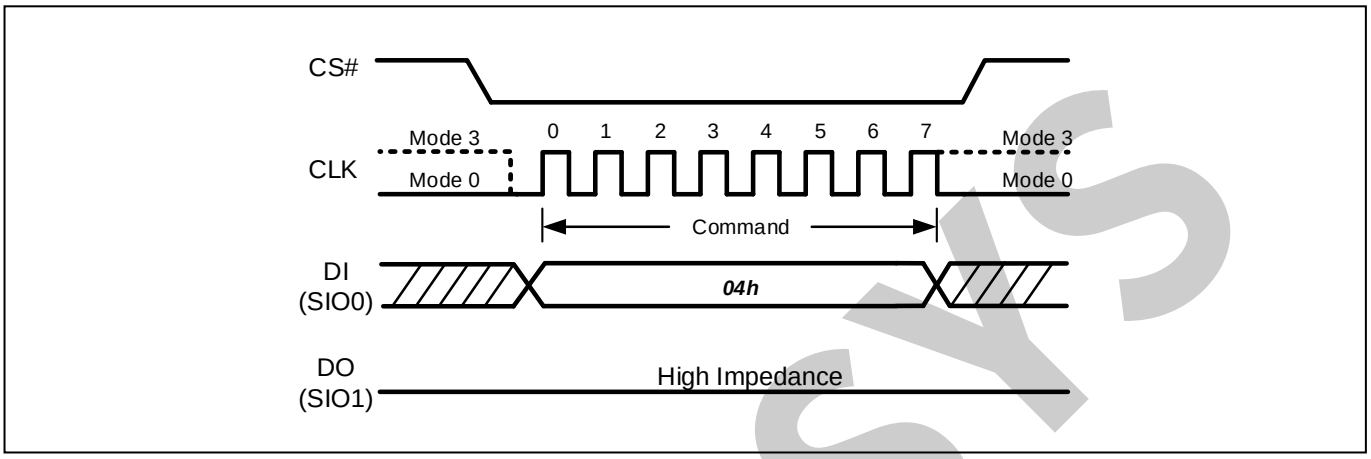
10.4.3 Write Disable (WRDI, 04h)

The Write Disable (WRDI, 04h) instruction is to reset Write Enable Latch (WEL) bit. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Program, Block Erase, and Reset commands.

Figure 13 Write Disable Sequence



10.5 Read Operations

The device supports Power-on Read function, after power up, the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the 1st page of 1st block data from the cache buffer.

10.5.1 Page Read (13h)

The page read operation transfers data from array to cache by issuing the Page Read (13h) command followed by the 24-bit address (including the dummy/block/page address).

The device will have a period of time (t_{RD} or t_{RD_ECC}) being busy after the CS# goes high. The Get Feature command may be used to poll the operation status.

After read operation is completed, the Read from Cache (03h or 0Bh), Read from cache (x2) (3Bh), Read from cache (x4) (6Bh) may be issued to fetch the data.

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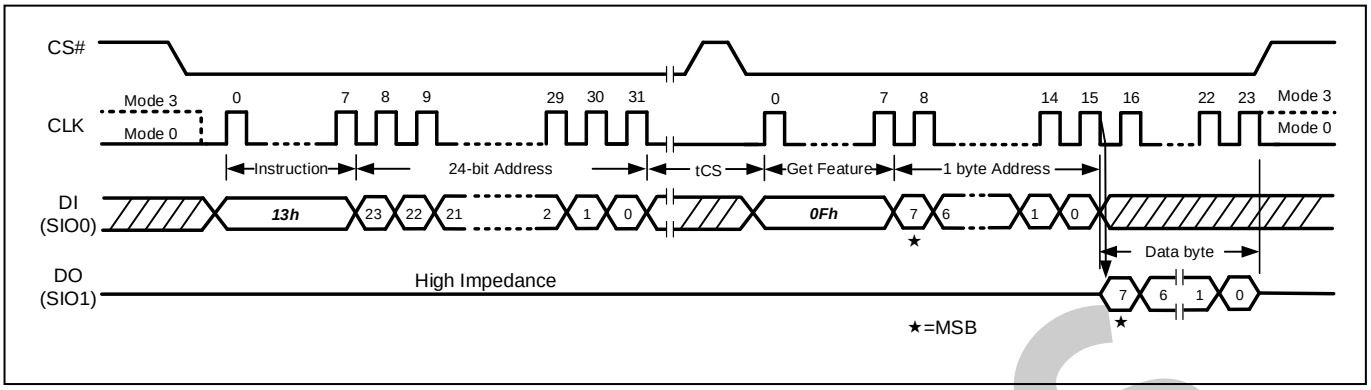
Figure 14 Page Read Sequence



10.5.2 Read From Cache (03h or 0Bh)

The Read From Cache command allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page command.

Figure 15 Read From Cache (03h) Sequence

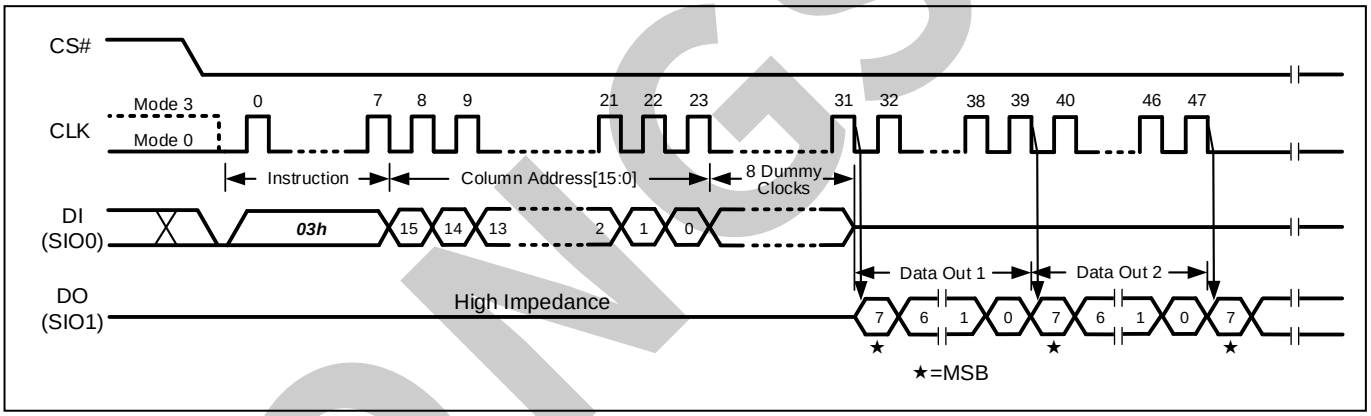
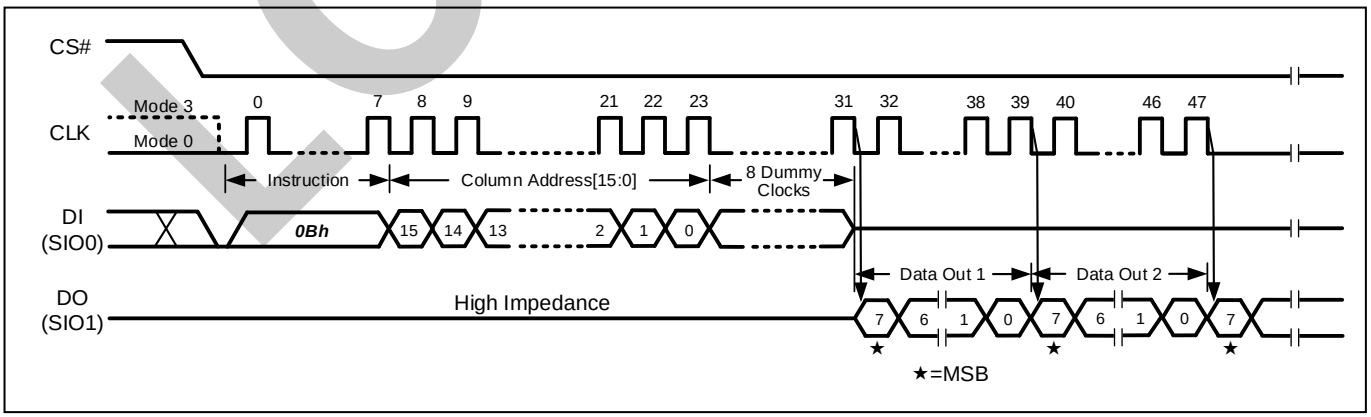


Figure 16 Read From Cache (0Bh) Sequence



10.5.3 Read From Cache x 2 (3Bh)

The Read From Cache x 2 (3Bh) command is similar to the Read From Cache (03h or 0Bh) command

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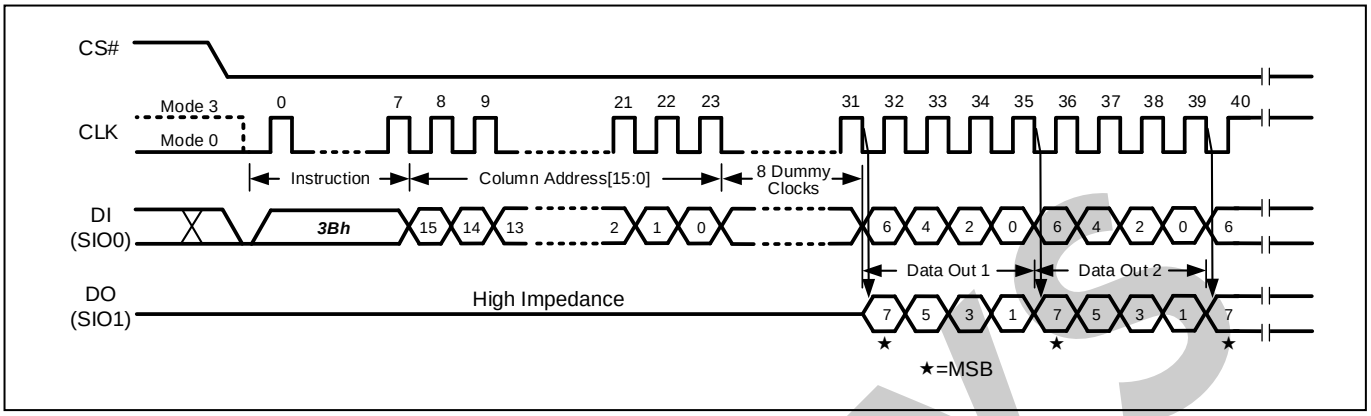
except that data is output on two pins: SIO0 and SIO1. This allows data to be transferred at twice the rate of standard SPI devices.

Figure 17 Read From Cache x2 (3Bh) Sequence

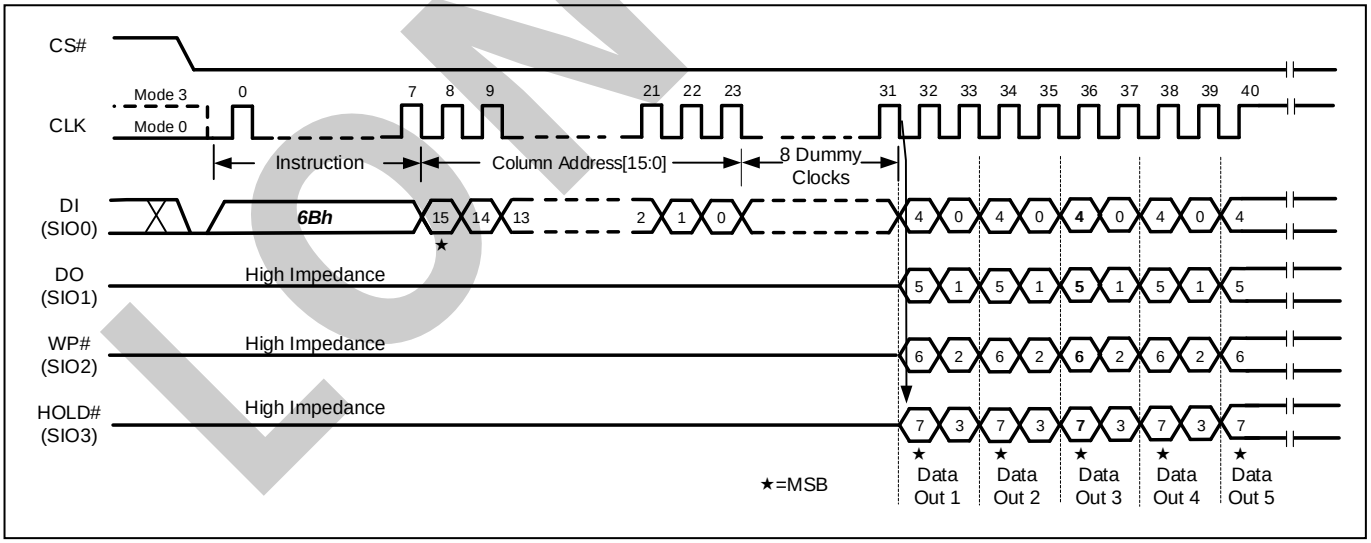


10.5.4 Read From Cache x 4 (6Bh)

The Read From Cache x 4 (6Bh) command is similar to the Read From Cache x 2 (3Bh) command except that data is output on four pins: SIO0, SIO1, SIO2 and SIO3. This allows data to be transferred at four times the rate of standard SPI devices.

When QE bit in the Status Register is set to a 0, this command is disabled.

Figure 18 Read From Cache x4 (6Bh) Sequence



10.6 Program Operations

10.6.1 Page Program

The Page Program operation sequence programs 1 byte to 2112 bytes of data within a page. The page program sequence is as follows:

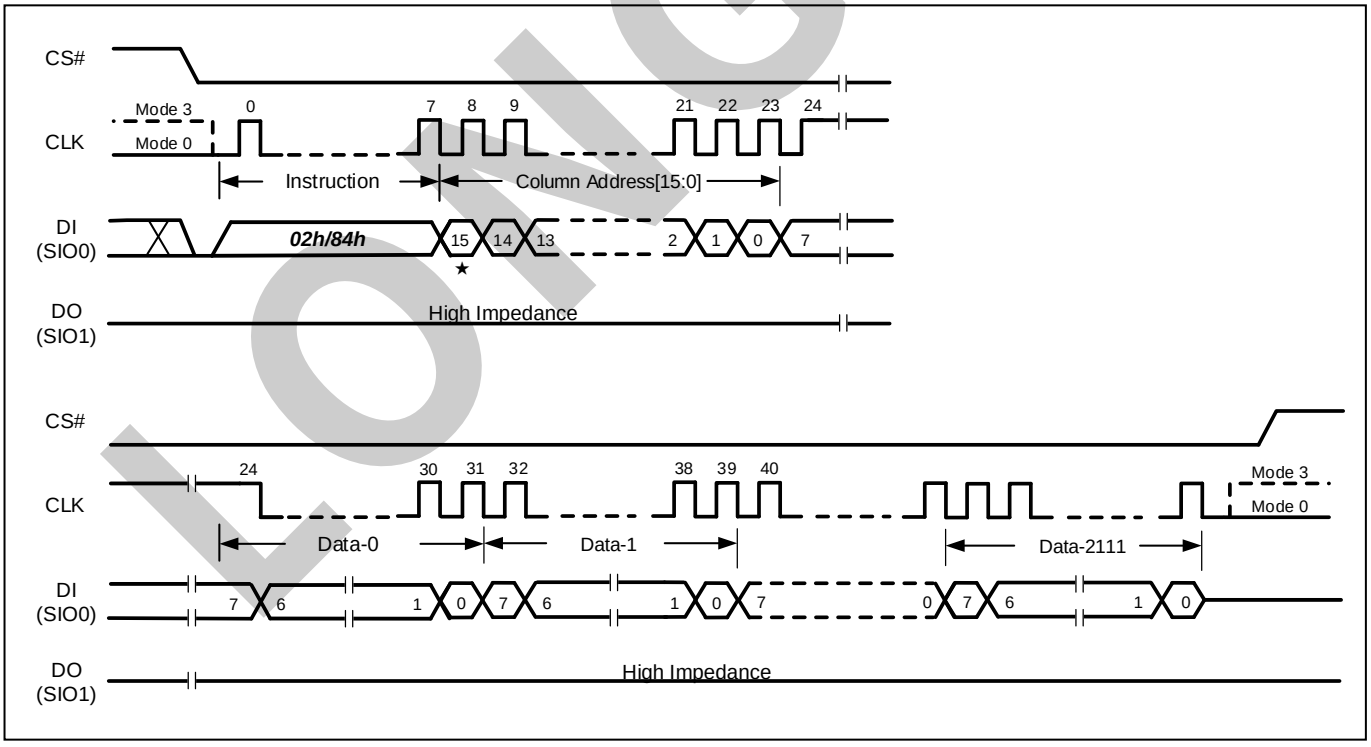
1. Issue Program Data Load (02h) / Program Data Load x4 (32h)
2. Issue Write Enable command (06h)
3. Issue Program Execute command (10h)
4. Issue Get Feature command (0Fh) to read the status

10.6.2 Program Data Load (02h) / Random Program Data Load (84h)

The Program Data Load or Random Program Data Load command is used to load the program data into the data buffer. The command is initiated by driving the CS# pin low then shifting the command code “02h” or “84h” followed by a 16-bit column address (only CA[11:0] is effective) and at least one byte of data into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device.

The Program Load Data command has to be issued prior to Random Program Load Data command for random page program. The difference is that Program Load Data command will reset the unused the data bytes in the Data Buffer to FFh value, while Random Program Load Data command will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

Figure 19 (Random) Program Data Load Sequence



10.6.3 Program Data Load x 4 (32h) / Random Program Data Load x 4 (34h)

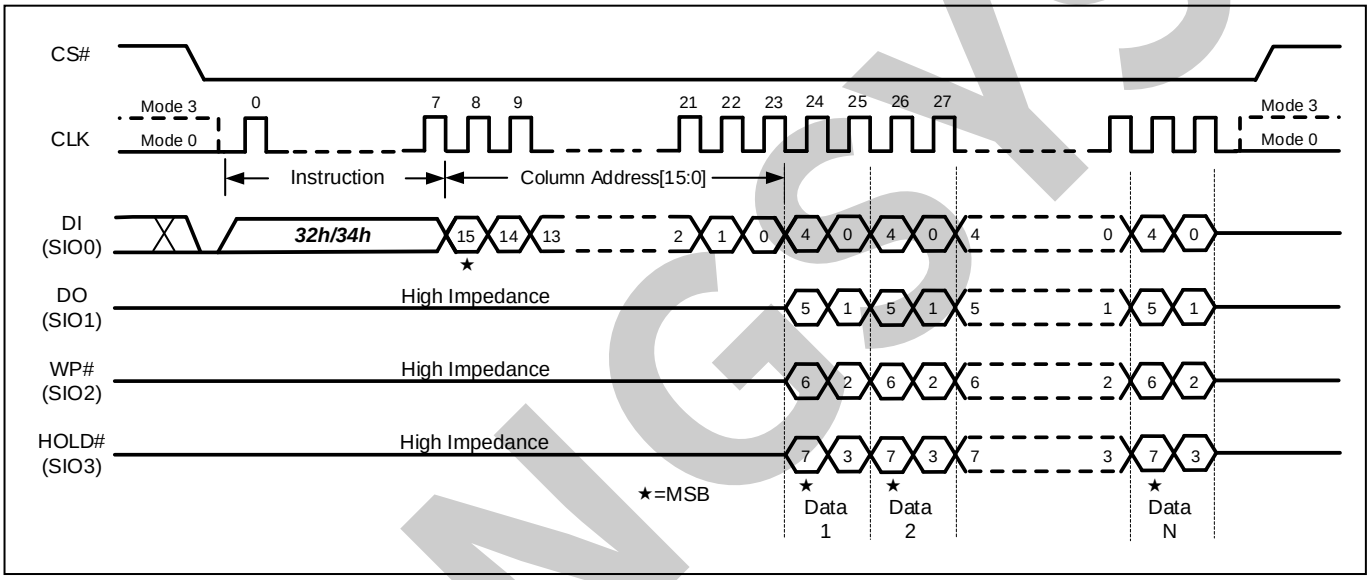
The Program Data Load x 4 and Random Program Data Load x 4 commands are similar to the Program Load Data and Random Program Load Data, the only difference is that “x4” commands will input the data

bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer.

The Program Data Load x 4 command has to be issued prior to Random Program Data Load x 4 command for random page program. The difference is that Program Data Load x 4 command will reset the unused data bytes in the Data Buffer to FFh value, while Random Program Data Load x 4 instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

When QE bit in the Status Register is set to 0, all Quad SPI instructions are disabled.

Figure 20 (Random) Program Data Load x4 Sequence



10.6.4 Program Execute (10h)

The Program Execute command will program the Data Buffer content into the physical memory page that is specified in the command. Prior to performing the Program Execute operation, a Write Enable (06h) command must be issued to set the WEL bit.

The Program Execute command is initiated by driving the CS# pin low then shifting the instruction code “10h” followed by 7-bit dummy clocks and the 17-bit Page Address into the DI pin.

After CS# is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for time duration of t_{PROG} or t_{PROG_ECC}. While the Program Execute cycle is in progress, the Get Feature command (0Fh) may be used for checking the status of the OIP bit. The OIP bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute command will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits. Only 4 partial page program times are allowed on every single page.

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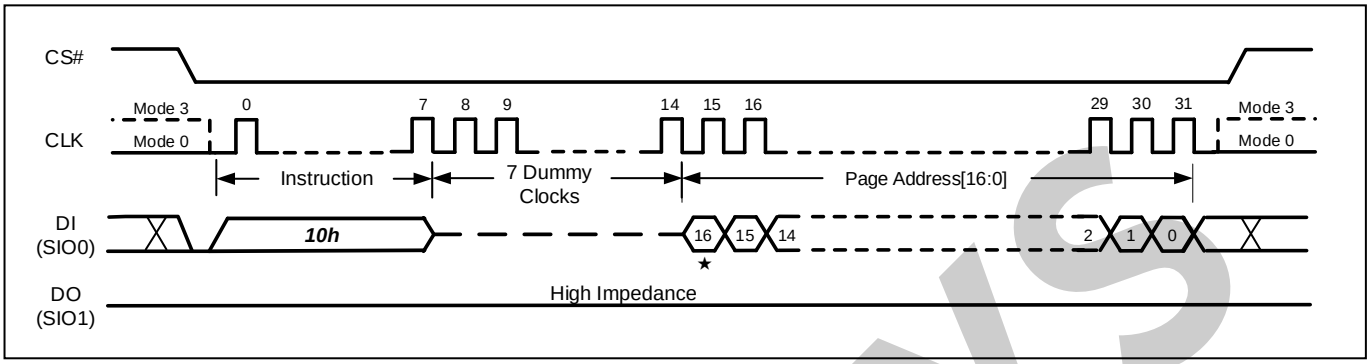
The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.

Figure 21 Program Execute Sequence



10.6.5 Internal Data Move

The Internal Data Move command sequence programs or replaces data in a page with existing data. The sequence is as follows:

1. Issue Page Read command (13h)
2. Program Load Random Data (Optional)
3. Issue Write Enable command (06h)
4. Issue Program Execute command (10h)
5. Issue Get Feature command (0Fh) to read the status

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a Page Read (13h) command. One or more Program Load Random Data (84h/34h) command can be issued, if user wants to update bytes of data in the page. After the data is loaded, the Write Enable command (06h) and the Program Execute (10h) command can be issued to start the program operation.

10.7 Block Erase Operations

The Block Erase instruction sets all memory within a specified block to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “D8h” followed by 7-bit dummy clocks and the 17-bit page address.

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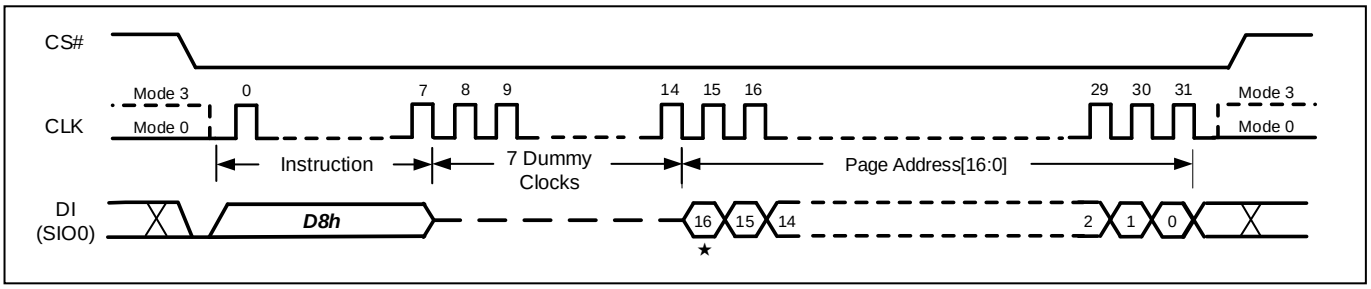
Figure 22 Block Erase Sequence



10.8 UID / Parameter / OTP Pages

In addition to the main memory array, the device has one Unique ID Page, one Parameter Page, and sixty-two OTP Pages.

Table 16 UID / Parameter / OTP Pages

Page Address PA[15:0]	Page Name	Descriptions	Data Length
00_00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
00_01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
00_02h	OTP Page [0]	Program Only, OTP lockable	2,112-Byte
…	OTP Pages [1:60]	Program Only, OTP lockable	2,112-Byte
00_3Fh	OTP Page [61]	Program Only, OTP lockable	2,112-Byte

Unique ID Page: To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies (each copy has 32 bytes) of the UID and the corresponding complement are stored. On each 32-byte, the first 16-byte and following 16-byte are complementary. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid.

Parameter Page: Contains at least three identical copies of the 256-Byte Parameter Data.

To access these additional data pages, the OTP-E bit in Configuration Register (SR-2) must be set to “1” first. Then, Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it’s not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

10.8.1 Read UID / Parameter / OTP Pages

The Read UID / Parameter / OTP pages sequence is as follows:

1. Issue Set Feature command (1Fh) to set OTP-E=1.
2. Issue Page Read command (13h) with address shown in the table above.
3. Issue Get Feature command (0Fh) to read the status.
4. Issue Read from cache command (03h/0Bh/3Bh/6Bh) to read data.

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Note:

(1) For OTP pages, Internal ECC can be enabled for the OTP page read operations to ensure the data integrity.

(2) When reading UID / Parameter page, Internal ECC is disabled by the chip.

10.8.2 Program OTP Pages and OTP Lock Operation

OTP pages provide the additional space (2K-Byte x 62) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed (change data from “1” to “0”) until being locked by OTP-L bit in the Configuration Register (SR-2).

The Program OTP Pages sequence is as follows:

1. Issue Set Feature command (1Fh) to set OTP-E=1
2. Issue WREN command (06h) to set WEL bit
3. Issue Program Data Load and Program Execute command
4. Issue Get Feature command (0Fh) to read the status.

When ECC is enabled, ECC calculation will be performed during Program Execute.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible.

The OTP Lock sequence is as follows:

1. Issue Set Feature command (1Fh) to set OTP-E=1 and OTP-L=1
2. Issue WREN command (06h) to set WEL bit
3. Issue Program Execute command (10h), page address is “don’t care”
4. Issue Get Feature command (0Fh) to read the status.
5. Issue Set Feature command (1Fh) to set OTP-E=0, return to the main memory array operation.

10.8.3 Parameter Page Data Definition

Table 17 Parameter Definition

Byte Number	Descriptions	Values
0~3	Parameter Page Signature, "ONFI" ASCII characters	4Fh 4Eh 46h 49h
4~5	Revision Number	00h 00h
6~31	Reserved (0)	all 00h
32~43	Device manufacturer, 12 ASCII characters	46h 4Fh 52h 45h 53h 45h 45h 20h 20h 20h 20h 20h
44-63	Device Model, 20 ASCII characters	46h 33h 35h 55h 51h 41h 30h 30h 32h 47h 20h 20h 20h 20h 20h 20h 20h 20h 20h 20h

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Byte Number	Descriptions	Values
64	JEDEC MID	CDh
65-66	Date Code	00h 00h
67-79	Reserved (0)	all 00h
80-83	Number of Data Bytes per Page	00h 08h 00h 00h
84-85	Number of Spare Bytes per Page	40h 00h
86-89	Number of Data Bytes per Partial Page	00h 02h 00h 00h
90-91	Number of Spare Bytes per Partial Page	10h 00h
92-95	Number of Pages per Block	40h 00h 00h 00h
96-99	Number of Block per Logic Unit	00h 08h 00h 00h
100	Number of Logic Units	01h
101	Reserved (0)	00h
102	Number of Bits per Cell	01h
103-104	Bad Blocks Maximum per Logic Unit	28h 00h
105-106	Block Endurance	01h 05h
107	Guaranteed Valid Blocks at Beginning of Target	01h
108-109	Block Endurance for Guaranteed Valid Blocks	01h 03h
110	Number of Programs per Page	04h
111	Partial Programming Attributes b5-b7 reserved (0) b4 1 = partial page layout is partial page data followed by partial page spare b1-b3 reserved (0) b0 1 = partial page programming has constraints	00h
112	Number of ECC Bits Correctability	00h
113-127	Reserved (0)	all 00h
128	I/O Pin Capacitance, Maximum	08h
129-132	Reserved (0)	all 00h
133-134	t_{PROG} Maximum Page Program Time (us)	BCh 02h
135-136	t_{ERS} Maximum Block Erase Time (us)	10h 27h
137-138	t_{RD} Maximum Page read Time (us)	3Ch 00h
139-163	Reserved (0)	all 00h
164-165	Vendor Specific Revision Number	00h 00h
166-253	Vendor Specific	all 00h
254-255	Integrity CRC	C7h 69h
256-511	Value of Bytes 0-255	
512-767	Value of Bytes 0-255	
768+	Additional Redundant Parameter Pages	

Note:

(1) The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details. The CRC shall be calculated using the following 16-bit generator polynomial: G(X) = X16 + X15 +X2 + 1

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11 Software Algorithm

11.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same electrical characteristics. An initial invalid block(s) does not affect the performance of valid block(s). The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

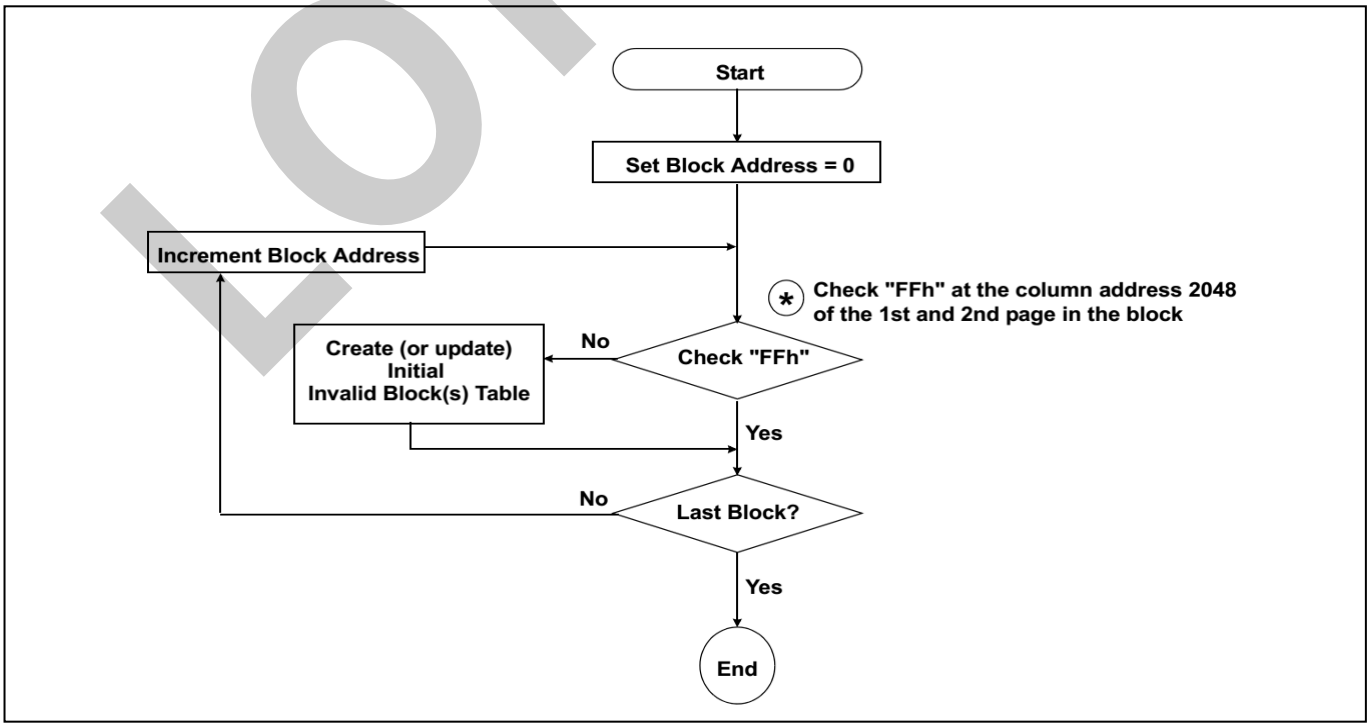
Table 18 Valid Block Number

Parameter	Symbol	Min	Max	Unit
Valid block number	N_{VB}	2008	2048	Blocks

11.2 Identifying Initial Invalid Block(s)

All device locations are erased (FFh) except locations where the initial invalid block(s) information is written prior to shipping. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the suggested flow (**Figure 23**). Any intentional erasure of the original initial invalid block information is prohibited.

Figure 23 Flow to Create Initial Invalid Block Table



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11.3 Error in Operation

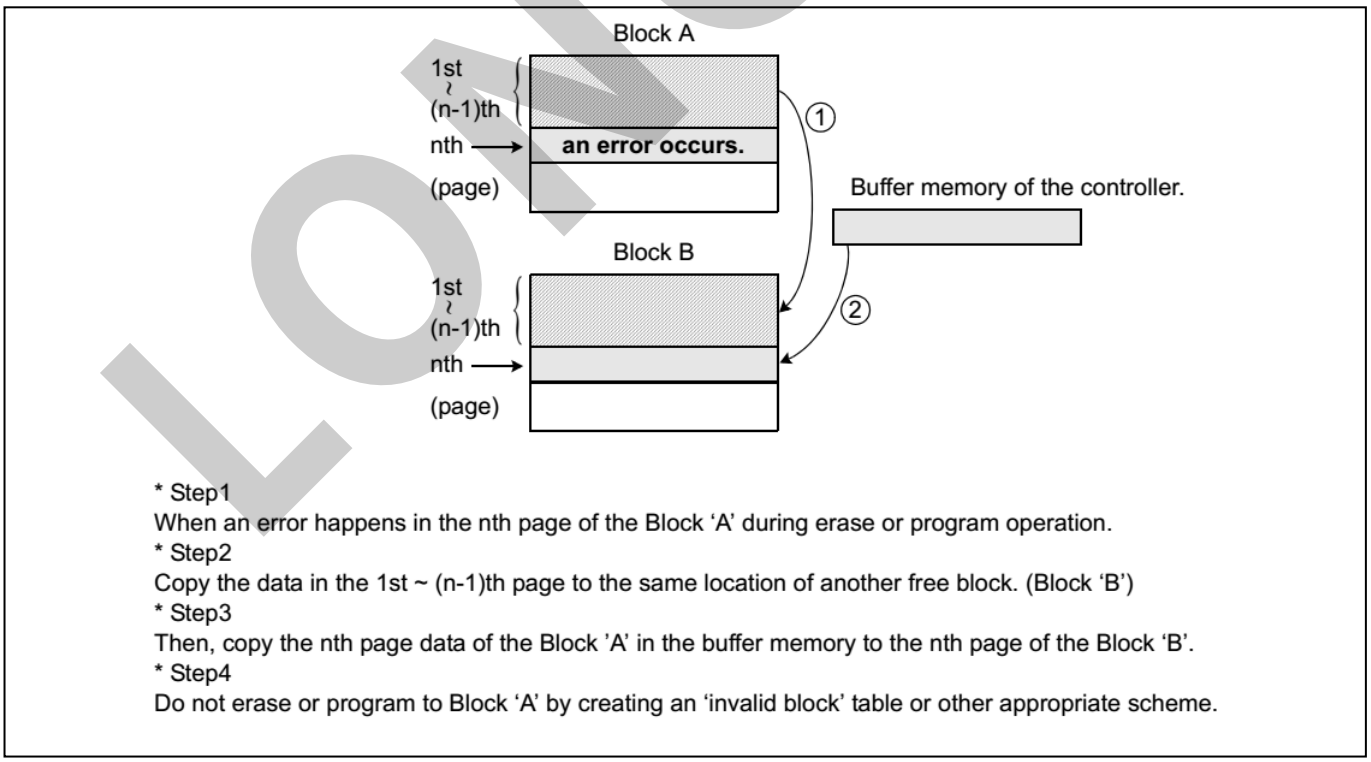
Within its life time, additional invalid blocks may develop with NAND Flash memory. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Note: When copy operation is executed without re-loading program data, the MSB of destination block address (PA[16]) must be the same as that of source block address.

Table 19 Failure Modes

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction

Figure 24 Bad Block Replacement



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11.4 Internal ECC

The internal ECC logic may detect 2-bit error and correct 1-bit error in an ECC segment. An ECC segment is composed by a main area (512 Byte) and a spare area (16 Byte). The default state of the internal ECC is enabled. To enable/disable the internal ECC, it is operated by the Set Feature operation to enable internal ECC or disable the internal ECC, and then check the internal ECC state by Get Feature operation.

The internal ECC is enabled by using Set Feature command (1Fh) to set ECC-E. To disable the internal ECC can be done by using the Set Feature command (1Fh) to clear ECC-E.

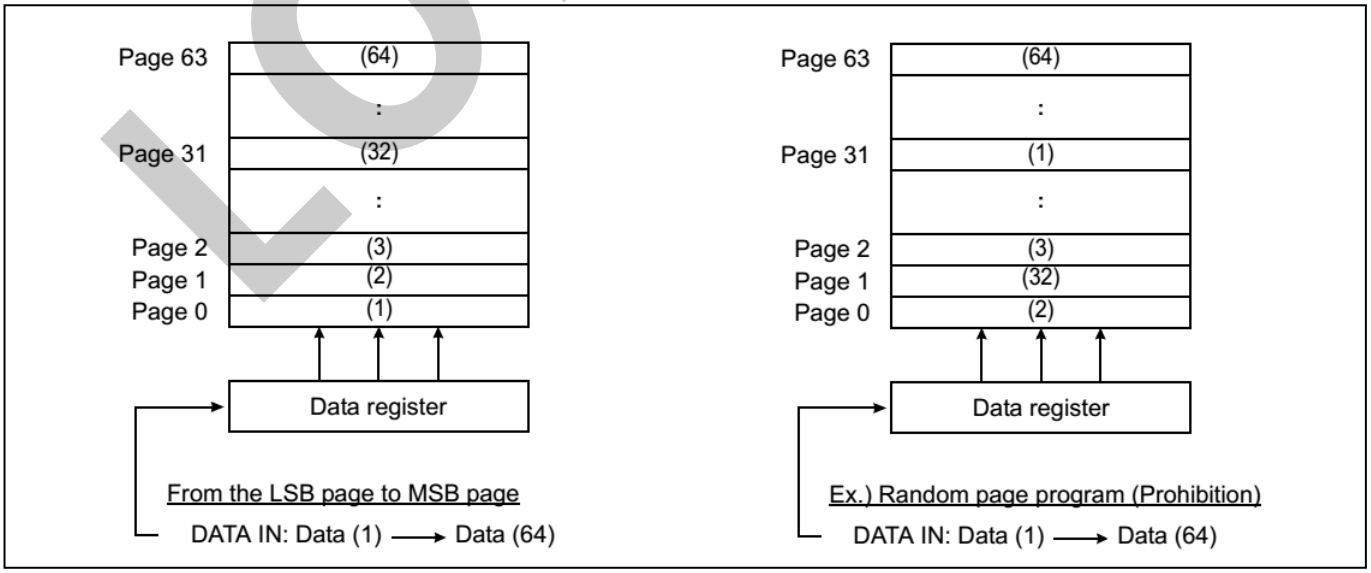
When the internal ECC is enabled, after the data transfer time (t_{RD_ECC}) is completed, a Status Read operation is required to check any uncorrectable read error happened. Please refer to **Status Register (SR-3)**.

The number of partial-page program is not 4 in an ECC segment, the user need to program the main area (512B) and spare area (16B) at one program time, so the ECC parity code can be calculated properly and stored in the additional hidden spare area.

11.5 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to the MSB (most significant bit) pages of the block. The LSB page is defined as the start page among the pages to be programmed, does not need to be page 0 in the block. Random page address programming is prohibited.

Figure 25 Addressing for Program Operation



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12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Table 20 Absolute Maximum Rating

Parameters	Symbol	Range	Unit
Supply Voltage	V_{CC}	–0.6 to +2.5	V
Voltage Applied to Any Pin	V_{IO}	–0.6 to V_{CC}+0.4	V
Temperature under Bias	T_{BIAS}	–40 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Short circuit output current, I/Os	I_{OS}	5	mA

Note:

(1) Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.

(2) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

12.2 Operating Ranges

Table 21 Operating Ranges

Parameters	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{CC}		1.7	1.95	V
Ambient Temperature	T_A	Industrial	-40	+85	°C
		Industrial plus	-40	+105	°C

12.3 Power-up and Power-down Timing Requirements

Table 22 Power-up Timing

Parameters	Symbol	Min	Max	Unit
V_{CC}(min) to read Status Register is allowed	t_{VSL}	200		µs
Time delay before device fully accessible	t_{PUW}	1		ms

Note:

(1) These parameters are characterized only.

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Figure 26 Power-up Timing

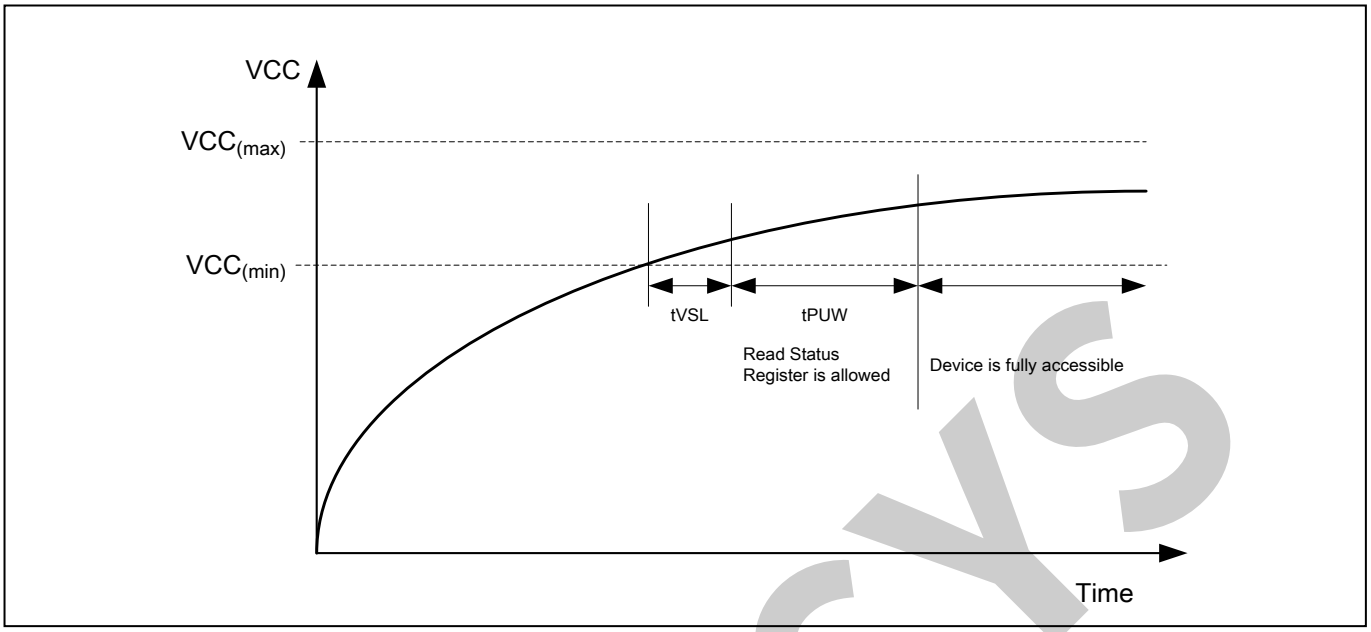
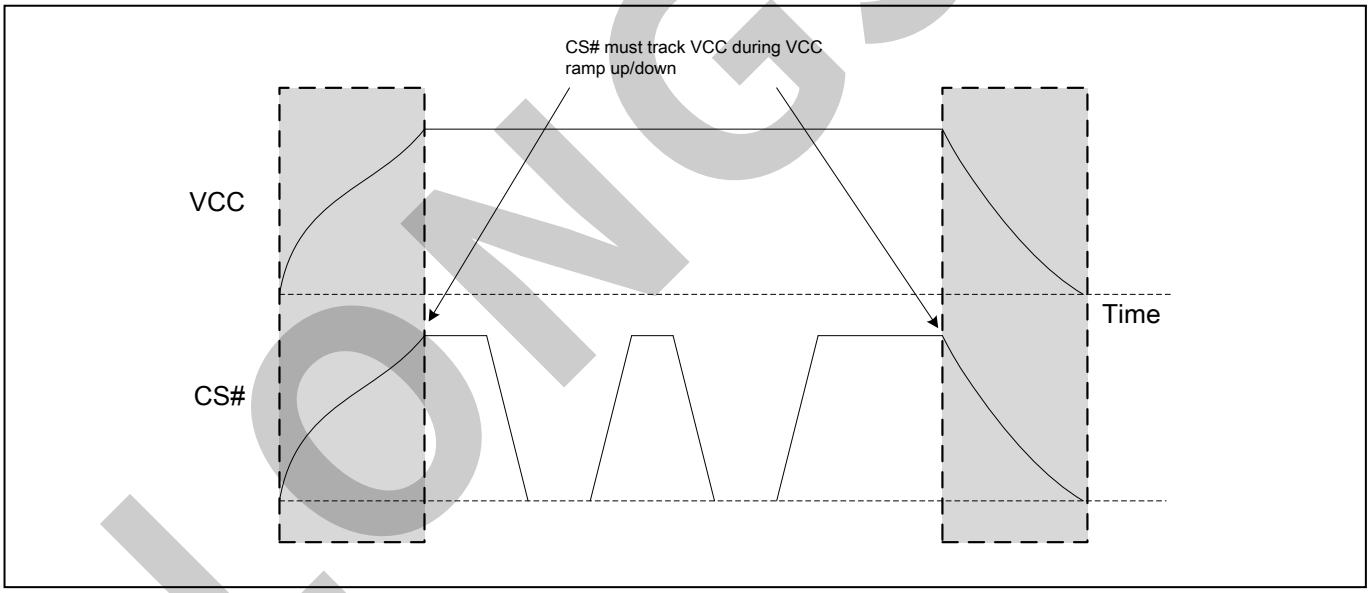


Figure 27 Power-up and Power-down Requirements



12.4 Pin Capacitance

Table 23 Pin Capacitance

Parameters	Symbol	Min	Max	Unit
Input / Output Capacitance	C_{IO}		8	pF
Input Capacitance	C_{IN}		8	pF

Note:

(1) Test conditions: TA=25°C, F=1MHz, V_{IN}=0V, V_{CC}=1.8V

(2) These parameters are characterized only.

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12.5 DC Electrical Characteristics

Table 24 DC Electrical Characteristics

Parameters	Symbol	Conditions	SPEC(1)			Unit
			Min	Typ	Max	
Standby Current	I_{CC1}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		10	50	μA
Page Read Current	I_{CC2}			10	25	mA
Program Current	I_{CC3}			15	25	mA
Erase Current	I_{CC4}			15	25	mA
Input Leakage Current	I_{LI}	V_{IN} = GND or V_{CC}			±2	μA
Output Leakage Current	I_{LO}	V_{OUT} = GND or V_{CC}			±2	μA
Input Low Voltage	V_{IL}		-0.3		$0.2V_{CC}$	V
Input High Voltage	V_{IH}		$0.8V_{CC}$		V_{CC}+0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 100μA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = -100μA	V_{CC}-0.2			V

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 1.7V to 1.95V, unless otherwise noted.

12.6 AC Measurement Conditions

Table 25 AC Measurement Conditions

Parameters	Symbol	Min	Max	Unit
Load Capacitance	C_L		30	pF
Input Rise Time	t_R		1.5	ns
Input Fall Time	t_F		1.5	ns
Input Pulse Voltages	V_{IN}	0 to V_{CC}		V
Input Timing Reference Voltages	IN	$0.5V_{CC}$		V
Output Timing Reference Voltages	OUT	$0.5V_{CC}$		V

12.7 AC Electrical Characteristics

Table 26 AC Electrical Characteristics

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
Clock frequency	F_R			83	MHz
Clock High, Low Time for all commands	t_{CLH}, t_{CLL}(2)	4.5			ns
Clock Rise Time	t_{CLCH}(3)	0.1			V/ns
Clock Fall Time	t_{CHCL}(3)	0.1			V/ns
Data In Setup Time	t_{DVCH}	3			ns

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Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
Data In Hold Time	t_{CHDX}	3			ns
Clock Low to Output Valid	t_{CLQV}			11.5	ns
Output Hold Time	t_{CLQX}	2			ns
Output Disable Time	t_{SHQZ}(3)			35	ns
CS# active Setup Time	t_{SLCH}	6			ns
CS# active Hold Time	t_{CHSH}	5			ns
CS# non-active Setup Time	t_{SHCH}	5			ns
CS# non-active Hold Time	t_{CHSL}	5			ns
CS# deselect Time	t_{SHSL}	35			ns
HOLD# active Setup Time	t_{HLCH}	5			ns
HOLD# active Hold Time	t_{CHHH}	5			ns
HOLD# non-active Setup Time	t_{HHCH}	5			ns
HOLD# non-active Hold Time	t_{CHHL}	5			ns
HOLD# to Output Low-Z	t_{HHQX}(3)			60	ns
HOLD# to Output High-Z	t_{HLQZ}(3)			60	ns
WP# Setup Time before CS# Low	t_{WHSL}	20			ns
WP# Hold Time after CS# Low	t_{SHWL}	100			ns
Device reset time (Read/Program/Erase)	t_{RST}(3)			5/20/200	µs

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 1.7V to 1.95V, unless otherwise noted.

(2) $t_{CLH} + t_{CLL} <= 1/F_R$

(3) These parameters are characterized only.

12.8 Read / Program / Erase Characteristics

Table 27 Read / Program / Erase Characteristics

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
Data Transfer from Cell to Data Register	t_{RD}			25	µs
Data Transfer from Cell to Data Register with internal ECC enabled	t_{RD_ECC}		60	70	µs
Program Time	t_{PROG}(2)		350	700	µs
Program Time with internal ECC enabled	t_{PROG_ECC}(2)		380	750	µs
Block Erase Time	t_{ERS}		2	10	ms
Number of Partial Program Cycles	NOP			4	cycles

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 1.7V to 1.95V, unless otherwise noted.

(2) Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 1.8V and 25°C.

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13 Timing Diagram

Figure 28 Serial Input Timing

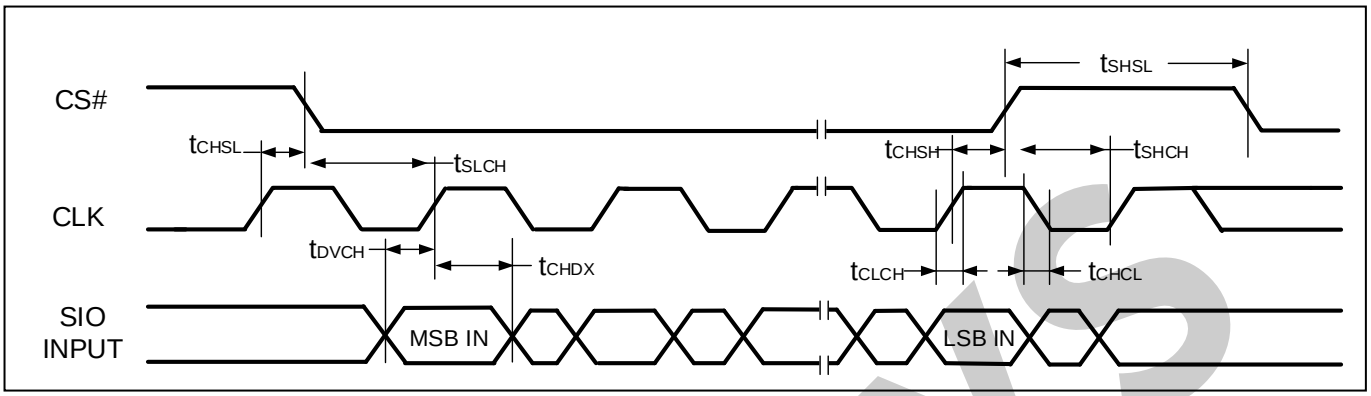

Figure 29 Serial Output Timing

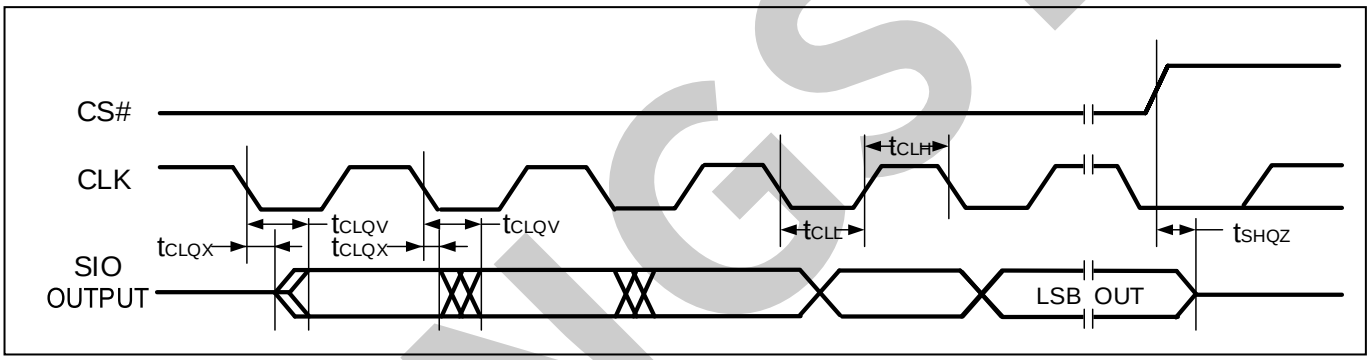

Figure 30 HOLD# Timing

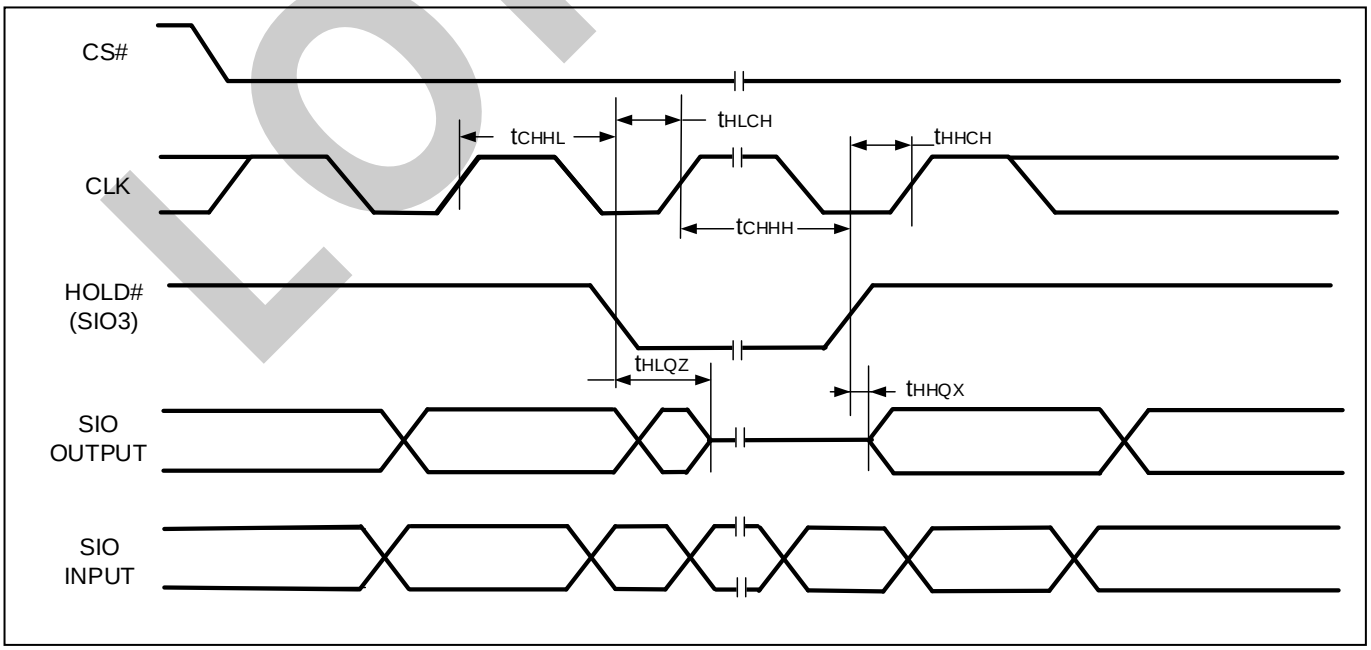

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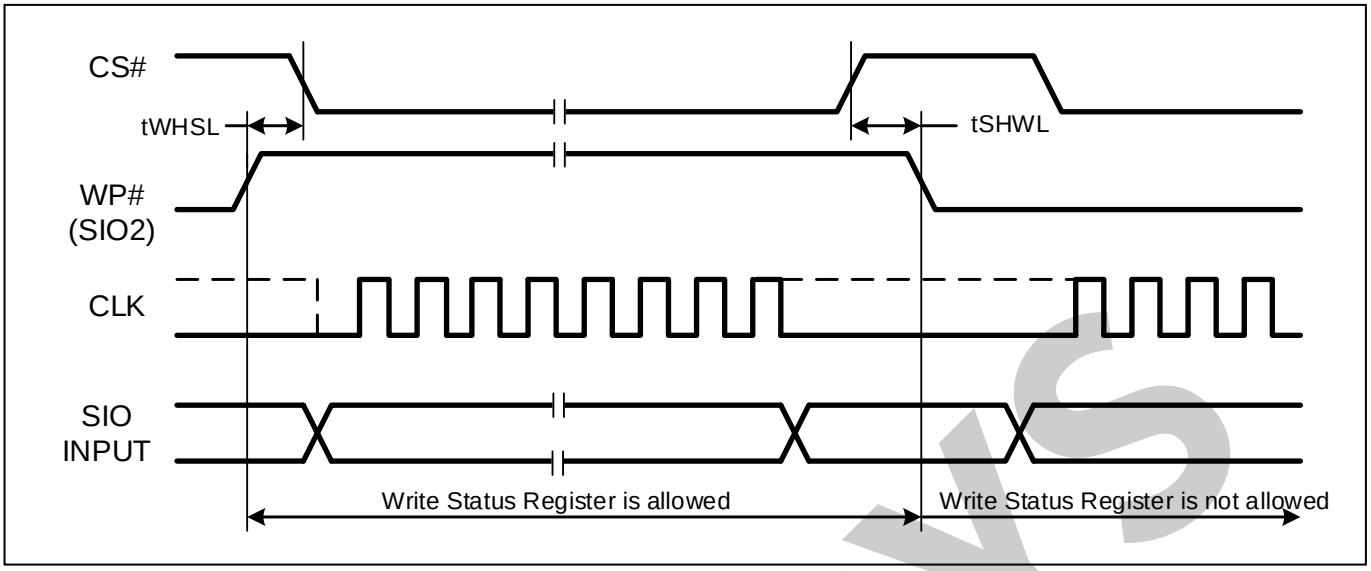
Figure 31 WP# Timing



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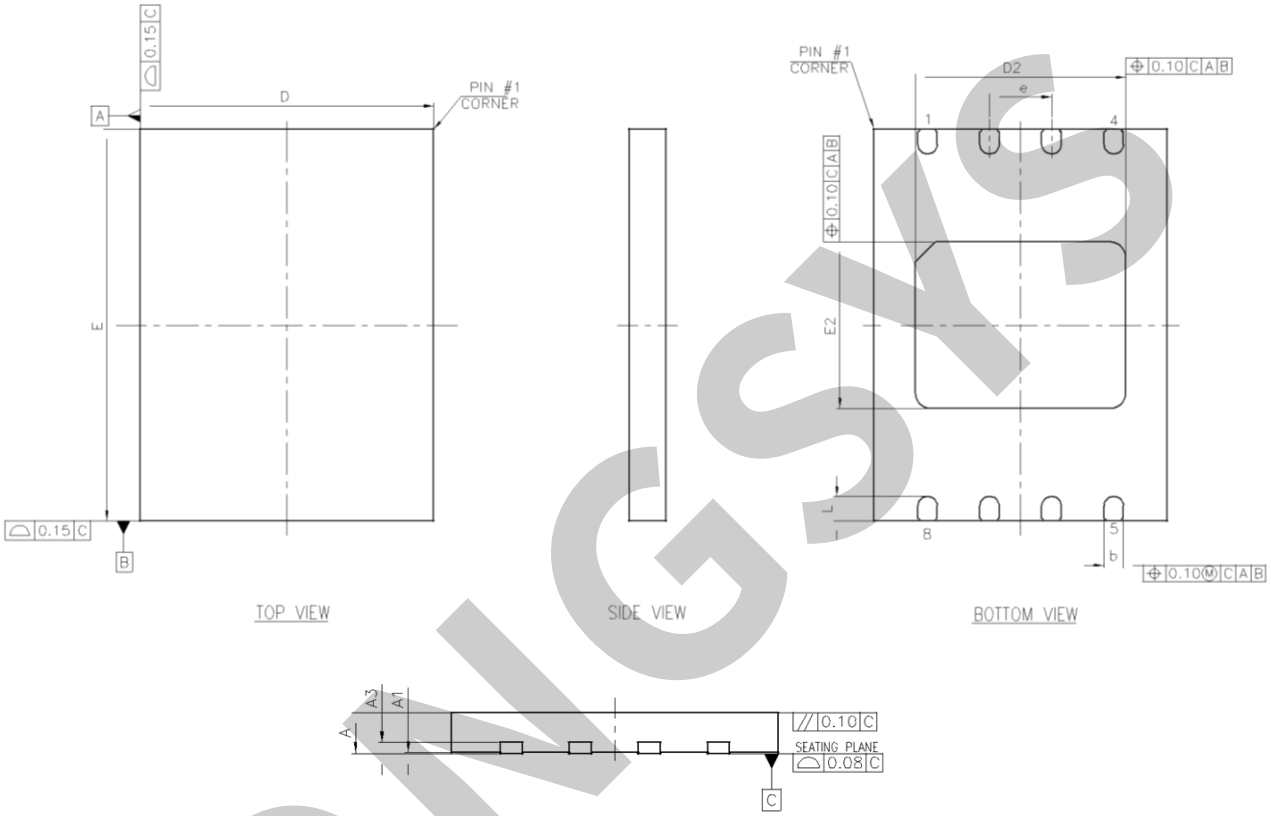
14 Packaging Information

14.1 8-WSON (8x6mm)

Figure 32 8-WSON (8x6mm) Package Information



SYMBOL	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
D	5.90	6.00	6.10
E	7.90	8.00	8.10
b	0.35	0.40	0.45
D2	4.20	4.30	4.40
E2	3.30	3.40	3.50
e		1.27 BSC	
L	0.45	0.50	0.55

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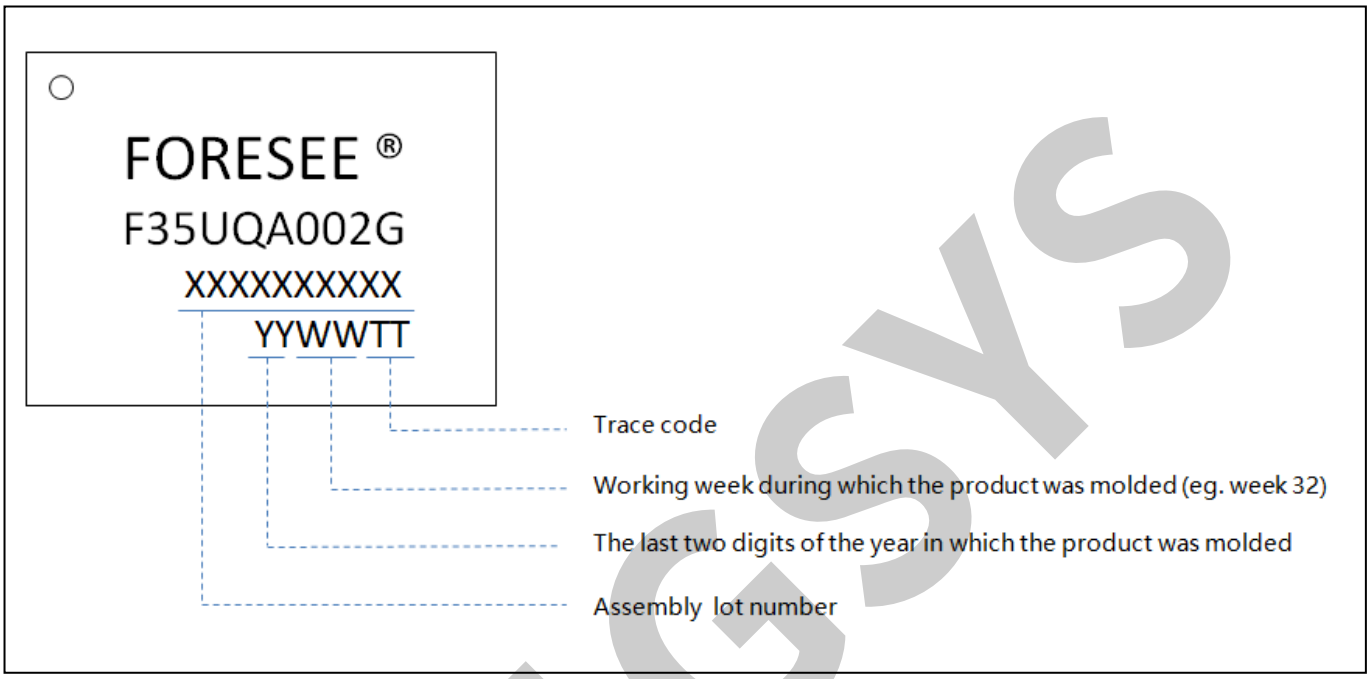
15 Part Marking Scheme

15.1 8-WSON (8x6mm)



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