# FORESEE DDR4 SDRAM SODIMM

Lead-Free & Halogen-Free
(RoHS Compliant)



## Datasheet

**Version: 1.1**

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# Revision History

| Revision NO. | History | Draft Date | Remark |
|---|---|---|---|
| 1.0 | First SPEC. Release | Jun. 2021 | - |
| 1.1 | Modify part of the description | Jul. 2021 | - |

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# 1. Description

FORESEE Unbuffered DDR4 SDRAM DIMMs (Unbuffered Double Data Rate Syn-chronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered DIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

# 2. Features

- VDD = 1.2V ± 60mv
- VPP = 2.5V (2.375V~2.75V)
- 8-bit pre-fetch
- On Die Termination using ODT pin
- Data Bus inversion (DBI) for data bus
- CRC (Cyclic Redundancy Check) for Read/Write data security
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- CapabilityPPR and sPPR is supported
- All of Lead-Free products are compliant for RoHS
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

# 3. Ordering Information

| Part Number | Density | Speed | Component Composition | # of ranks |
|---|---|---|---|---|
| FD4AS3200C4GZH | 4GB | DDR4-3200 | 512Mx16*4 | 1 |
| FD4AS3200C8GZH | 8GB | DDR4-3200 | 1Gx8*8 | 1 |

# 4. Key Parameters

| Grade | Speed (Mbps) | tCK (ns) | CAS Latency (tCK) | tRCD (ns) | tRP (ns) | tRAS (ns) | tRC (ns) | CL-tRCD-tRP |
|---|---|---|---|---|---|---|---|---|
| 1600K | 1600 | 1.25 | 11 | 13.75 | 13.75 | 35 | 48.75 | 11-11-11 |
| 1866M | 1866 | 1.071 | 13 | 13.92 | 13.92 | 34 | 47.92 | 13-13-13 |
| 2133P | 2133 | 0.937 | 15 | 14.04 | 14.04 | 33 | 47.06 | 15-15-15 |
| 2400T | 2400 | 0.833 | 17 | 14.16 | 14.16 | 32 | 46.16 | 17-17-17 |
| 2666V | 2666 | 0.75 | 19 | 14.25 | 14.25 | 32 | 46.25 | 19-19-19 |
| 2933Y | 2933 | 0.682 | 21 | 14.32 | 14.32 | 32 | 46.32 | 21-21-21 |
| 3200AA | 3200 | 0.625 | 22 | 13.75 | 13.75 | 32 | 45.75 | 22-22-22 |

# 5. Address Table

| Organization | Number of bank groups | Bank group address | Bank count per group | Bank Address in bank group | Row address | Column address |
|---|---|---|---|---|---|---|
| 512Mx16 | 2 | BG0 | 4 | BA[1:0] | A[15:0] | A[9:0] |
| 2Gx8 | 4 | BG[1:0] | 4 | BA[1:0] | A[15:0] | A[9:0] |

X XX X X XXXX X XX X X

**Module Manufacturer**
F=FORESEE

**DRAM Technology**
D3=DDR3
D4=DDR4
D5=DDR5

**Voltage**
A=1.2V
B=1.35V
C=1.5V
D=1.1V

**Product Family**
U=UDIMM
S=SODIMM
E=ECC DIMM
R=RDIMM

**Speed**
1600=1600Mbps
1866=1866Mbps
2133=2133Mbps
2400=2400Mbps
2666=2666Mbps
2933=2933Mbps
3200=3200Mbps
⋮

**Operating Temperatures**
C=0~85℃
I=-25~85℃
W=-40~85℃

**Density**
4G=4GB
8G=8GB
QG=16GB
WG=32GB

**DRAM Manufacturer**
C=CXMT
M=Micron
S=Samsung
T/Z=Longsys

**Die Revision**

# 6. Pin Descriptions

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| A0-A17 | SDRAM address bus | CK0_c, CK1_c | SDRAM clocks<br>(negative line of differential pair) |
| BA0,BA1 | SDRAM bank select | SCL | I2C serial bus clock for SPD-TSE |
| BG0, BG1 | SDRAM bank group select | SDA | I2C serial bus data line for SPD-TSE |
| RAS_n | SDRAM row address strobe | SA0–SA2 | I2C slave address select for SPD-TSE |
| CAS_n | SDRAM column address strobe | PARITY | SDRAM parity input |
| WE_n | SDRAM write enable | VDD | SDRAM I/O and core power supply |
| CS0_n, CS1_n | DIMM Rank Select Lines | 12 V | Optional power Supply on socket but not used on UDIMM |
| CKE0, CKE1 | SDRAM clock enable lines | VREFCA | |
| ODT0, ODT1 | SDRAM on-die termination control lines | VSS | Power supply return (ground) |
| ACT_n | SDRAM activate | VDDSPD | Serial SPD-TSE positive power supply |
| DQ0–DQ63 | DIMM memory data bus | ALERT_n | SDRAM ALERT_n |
| CB0–CB7 | DIMM ECC check bits | VPP | SDRAM Supply |
| TDQS0_t-TDQS8_t<br>TDQS0_c-TDQS8_c | Dummy loads for mixed populations of x4 based and x8 based RDIMMs.<br>Not used on UDIMMs | RESET_n | Set DRAMs to a Known State |
| DQS0_t–DQS8_t | SDRAM data strobes<br>(positive line of differential pair) | EVENT_n | SPD signals a thermal event has occurred |
| DQS0_c–DQS8_c | SDRAM data strobes<br>(negative line of differential pair) | VTT | SDRAM I/O termination supply |
| DM0_n–DM8_n,<br>DBI0_n-DBI8_n | SDRAM data masks/data bus inversion<br>(x8-based x64 DIMMs) | RFU | Reserved for future use |
| CK0_t, CK1_t | SDRAM clocks<br>(positive line of differential pair) | | |

**Note:**

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

# 7. Input/Output Functional Descriptions

| Symbol | Type | Function |
|---|---|---|
| CK_t, CK_c | Input | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c. |
| CKE(CKE1) | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE are disabled during Self-Refresh. |
| CS_n,(CS1_n) | Input | Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. |
| C0, C1, C2 | Input | Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. |
| ODT, (ODT1) | Input | On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM.When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM. |
| ACT_n | Input | Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14. |
| RAS_n/A16.<br>CAS_n/A15.<br>WE_n/A14 | Input | Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addressing like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table. |
| DM_n/DBI_n/TDQS_t,<br>(DMU_n/DBIU_n),<br>(DML_n/DBIL_n) | Input/Output | Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8. |
| BG0 - BG1 | Input | Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0. |

| Symbol | Type | Function |
|---|---|---|
| BA0 - BA1 | Input | Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| A0 - A17 | Input | Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configurations. |
| A10 / AP | Input | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. |
| A12 / BC_n | Input | Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details. |
| RESET_n | Input | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD. |
| DQ | Input/Output | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used. |
| DQS_t,DQS_c, DQSU_t,DQSU_c, DQSL_t, DQSL_c | Input/Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t , DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended. |
| TDQS_t, TDQS_c | Output | Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1. |
| PAR | Input | Command and Address Parity Input: DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0 and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low. |

| Symbol | Type | Function |
|---|---|---|
| ALERT_n | Input/Output | Alert : It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin works as input.Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board. |
| TEN | Input | Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. |
| NC | | No Connect: No internal electrical connection is present. |
| VDDQ | Supply | DQ Power Supply: 1.2 V +/- 0.06 V |
| VSSQ | Supply | DQ Ground |
| VDD | Supply | Power Supply: 1.2 V ± 0.06 V |
| VSS | Supply | Ground |
| VPP | Supply | DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max) |
| VREFCA | Supply | Reference voltage for CA |
| ZQ | Supply | Reference Pin for ZQ calibration. |

**Note:**

1. Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

# 8. Pin Assignments

| Pin | Front Side | Pin | Back Side | Pin | Front Side | Pin | Back Side |
|---|---|---|---|---|---|---|---|
| 1 | VSS | 2 | VSS | 131 | A3 | 132 | A2 |
| 3 | DQ5 | 4 | DQ4 | 133 | A1 | 134 | EVENT_n |
| 5 | VSS | 6 | VSS | 135 | VDD | 136 | VDD |
| 7 | DQ1 | 8 | DQ0 | 137 | CK0_t | 138 | CK1_t |
| 9 | VSS | 10 | VSS | 139 | CK0_c | 140 | CK1_C |
| 11 | DQS0_C | 12 | DM0_n, DBI0_n | 141 | VDD | 142 | VDD |
| 13 | DQS0_t | 14 | VSS | 143 | PARITY | 144 | A0 |
| 15 | VSS | 16 | DQ6 | KEY | | | |
| 17 | DQ7 | 18 | VSS | | | | |
| 19 | VSS | 20 | DQ2 | 145 | BA1 | 146 | A10/AP |
| 21 | DQ3 | 22 | VSS | 147 | VDD | 148 | VDD |
| 23 | VSS | 24 | DQ12 | 149 | CS0_n | 150 | BA0 |
| 25 | DQ13 | 26 | VSS | 151 | A14/WE_n | 152 | A16/RAS_n |
| 27 | VSS | 28 | DQ8 | 153 | VDD | 154 | VDD |
| 29 | DQ9 | 30 | VSS | 155 | ODT0 | 156 | A15/CAS_n |
| 31 | VSS | 32 | DQS1_C | 157 | CS1_n | 158 | A13 |
| 33 | DM1_n, DBI1_n | 34 | DQS1_t | 159 | VDD | 160 | VDD |
| 35 | VSS | 36 | VSS | 161 | ODT1 | 162 | C0, CS2_n, NC |
| 37 | DQ15 | 38 | DQ14 | 163 | VDD | 164 | VREFCA |
| 39 | VSS | 40 | VSS | 165 | C1, CS3_n, NC | 166 | SA2 |
| 41 | DQ10 | 42 | DQ11 | 167 | VSS | 168 | VSS |
| 43 | VSS | 44 | VSS | 169 | DQ37 | 170 | DQ36 |
| 45 | DQ21 | 46 | DQ20 | 171 | VSS | 172 | VSS |
| 47 | VSS | 48 | VSS | 173 | DQ33 | 174 | DQ32 |
| 49 | DQ17 | 50 | DQ16 | 175 | VSS | 176 | VSS |
| 51 | VSS | 52 | VSS | 177 | DQS4_C | 178 | DM4_n, DBI4_n |
| 53 | DQS2_c | 54 | DM2_n, DBI2_n | 179 | DQS4_t | 180 | VSS |
| 55 | DQS2_t | 56 | VSS | 181 | VSS | 182 | DQ39 |
| 57 | VSS | 58 | DQ22 | 183 | DQ38 | 184 | VSS |
| 59 | DQ23 | 60 | VSS | 185 | VSS | 186 | DQ35 |
| 61 | VSS | 62 | DQ18 | 187 | DQ34 | 188 | VSS |
| 63 | DQ19 | 64 | VSS | 189 | VSS | 190 | DQ45 |
| 65 | VSS | 66 | DQ28 | 191 | DQ44 | 192 | VSS |
| 67 | DQ29 | 68 | VSS | 193 | VSS | 194 | DQ41 |
| 69 | VSS | 70 | DQ24 | 195 | DQ40 | 196 | VSS |
| 71 | DQ25 | 72 | VSS | 197 | VSS | 198 | DQS5_c |
| 73 | VSS | 74 | DQS3_c | 199 | DM5_n, DBI5_n | 200 | DQS5_t |

| Pin | Front Side | Pin | Back Side | Pin | Front Side | Pin | Back Side |
|---|---|---|---|---|---|---|---|
| 75 | DM3_n, DBI3_n | 76 | DQS3_t | 201 | VSS | 202 | VSS |
| 77 | VSS | 78 | VSS | 203 | DQ46 | 204 | DQ47 |
| 79 | DQ30 | 80 | DQ31 | 205 | VSS | 206 | VSS |
| 81 | VSS | 82 | VSS | 207 | DQ42 | 208 | DQ43 |
| 83 | DQ26 | 84 | DQ27 | 209 | VSS | 210 | VSS |
| 85 | VSS | 86 | VSS | 211 | DQ52 | 212 | DQ53 |
| 87 | CB5, NC | 88 | CB4, NC | 213 | VSS | 214 | VSS |
| 89 | VSS | 90 | VSS | 215 | DQ49 | 216 | DQ48 |
| 91 | CB1, NC | 92 | CB0, NC | 217 | VSS | 218 | VSS |
| 93 | VSS | 94 | VSS | 219 | DQS6_C | 220 | DM6_n, DBI6_n |
| 95 | DQS8_c | 96 | DBI8_n | 221 | DQS6_t | 222 | VSS |
| 97 | DQS8_t | 98 | VSS | 223 | VSS | 224 | DQ54 |
| 99 | VSS | 100 | CB6, NC | 225 | DQ55 | 226 | VSS |
| 101 | CB2, NC | 102 | VSS | 227 | VSS | 228 | DQ50 |
| 103 | VSS | 104 | CB7, NC | 229 | DQ51 | 230 | VSS |
| 105 | CB3, NC | 106 | VSS | 231 | VSS | 232 | DQ60 |
| 107 | VSS | 108 | RESET_n | 233 | DQ61 | 234 | VSS |
| 109 | CKE0 | 110 | CKE1 | 235 | VSS | 236 | DQ57 |
| 111 | VDD | 112 | VDD | 237 | DQ56 | 238 | VSS |
| 113 | BG1 | 114 | ACT_n | 239 | VSS | 240 | DQS7_c |
| 115 | BG0 | 116 | ALERT_n | 241 | DM7_n, DBI7_n | 242 | DQS7_t |
| 117 | VDD | 118 | VDD | 243 | VSS | 244 | VSS |
| 119 | A12 | 120 | A11 | 245 | DQ62 | 246 | DQ63 |
| 121 | A9 | 122 | A7 | 247 | VSS | 248 | VSS |
| 123 | VDD | 124 | VDD | 249 | DQ58 | 250 | DQ59 |
| 125 | A8 | 126 | A5 | 251 | VSS | 252 | VSS |
| 127 | A6 | 128 | A4 | 253 | SCL | 254 | SDA |
| 129 | VDD | 130 | VDD | 255 | VDDSPD | 256 | SA0 |
| | | | | 257 | VPP | 258 | VTT |
| | | | | 259 | VPP | 260 | SA1 |

# 9. DQ Map

**Description:** DDRIV SDRAM, Single-Rank, x8-FBGA 78-Ball-based, x64 Unbuffered, 260-pin SODIMM

| Module Pin Number | Module DQ | Damping RES. | IC No. | IC DQ | Module Pin Number | Module DQ | Damping RES. | IC No. | IC DQ |
|---|---|---|---|---|---|---|---|---|---|
| 8 | 0 | R98 | U1 | 5 | 28 | 8 | R93 | U9 | 6 |
| 7 | 1 | R6 | | 7 | 29 | 9 | R12 | | 4 |
| 20 | 2 | R95 | | 6 | 41 | 10 | R15 | | 5 |
| 21 | 3 | R10 | | 4 | 42 | 11 | R89 | | 7 |
| 4 | 4 | R199 | | 3 | 24 | 12 | R94 | | 0 |
| 3 | 5 | R5 | | 1 | 25 | 13 | R11 | | 2 |
| 16 | 6 | R96 | | 2 | 38 | 14 | R90 | | 3 |
| 17 | 7 | R9 | | 0 | 37 | 15 | R14 | | 1 |
| 50 | 16 | R87 | U2 | 5 | 70 | 24 | R82 | U8 | 6 |
| 49 | 17 | R17 | | 7 | 71 | 25 | R23 | | 4 |
| 62 | 18 | R84 | | 6 | 83 | 26 | R26 | | 5 |
| 63 | 19 | R21 | | 4 | 84 | 27 | R78 | | 7 |
| 46 | 20 | R88 | | 3 | 66 | 28 | R83 | | 0 |
| 45 | 21 | R16 | | 1 | 67 | 29 | R22 | | 2 |
| 58 | 22 | R85 | | 2 | 79 | 30 | R25 | | 1 |
| 59 | 23 | R20 | | 0 | 80 | 31 | R79 | | 3 |
| 174 | 32 | R75 | U4 | 5 | 195 | 40 | R34 | U7 | 0 |
| 173 | 33 | R28 | | 7 | 194 | 41 | R70 | | 2 |
| 187 | 34 | R32 | | 4 | 207 | 42 | R37 | | 3 |
| 186 | 35 | R72 | | 6 | 208 | 43 | R66 | | 1 |
| 170 | 36 | R76 | | 3 | 191 | 44 | R33 | | 6 |
| 169 | 37 | R27 | | 1 | 190 | 45 | R71 | | 4 |
| 183 | 38 | R31 | | 0 | 203 | 46 | R36 | | 5 |
| 182 | 39 | R73 | | 2 | 204 | 47 | R67 | | 7 |
| 216 | 48 | R64 | U5 | 5 | 237 | 56 | R45 | U6 | 6 |
| 215 | 49 | R39 | | 7 | 236 | 57 | R59 | | 4 |
| 228 | 50 | R61 | | 6 | 249 | 58 | R48 | | 5 |
| 229 | 51 | R43 | | 4 | 250 | 59 | R55 | | 7 |
| 211 | 52 | R38 | | 1 | 232 | 60 | R60 | | 0 |
| 212 | 53 | R65 | | 3 | 233 | 61 | R44 | | 2 |
| 224 | 54 | R62 | | 2 | 245 | 62 | R47 | | 1 |
| 225 | 55 | R42 | | 0 | 246 | 63 | R56 | | 3 |

**First check the SPD data and EEPROM. Then check the following components for other problem.**

| | Clock loading | Boot failure |
|---|---|---|
| 1-RANK | R77,RN2 | SPD data U3 |

**Description:** DDRIV SDRAM, Single-Rank, x16-FBGA 96-Ball-based, x64 Unbuffered, 260-pin SODIMM

| Module Pin Number | Module DQ | Damping RES. | IC No. | IC DQ | Module Pin Number | Module DQ | Damping RES. | IC No. | IC DQ |
|---|---|---|---|---|---|---|---|---|---|
| 8 | 0 | 4AR9(3-6) | U1 | DQL3 | 50 | 16 | 4AR11(3-6) | U2 | DQL3 |
| 7 | 1 | 4AR1(2-7) | | DQL1 | 49 | 17 | 4AR3(2-7) | | DQL1 |
| 20 | 2 | 2AR10(1-4) | | DQL2 | 62 | 18 | 2AR12(1-4) | | DQL2 |
| 21 | 3 | 2AR1(2-3) | | DQL0 | 63 | 19 | 2AR3(2-3) | | DQL0 |
| 4 | 4 | 4AR9(4-5) | | DQL7 | 46 | 20 | 4AR11(4-5) | | DQL7 |
| 3 | 5 | 4AR1(1-8) | | DQL5 | 45 | 21 | 4AR3(1-8) | | DQL5 |
| 16 | 6 | 2AR10(2-3) | | DQL6 | 58 | 22 | 2AR12(2-3) | | DQL6 |
| 17 | 7 | 2AR1(1-4) | | DQL4 | 59 | 23 | 2AR3(1-4) | | DQL4 |
| 28 | 8 | 2AR11(1-4) | | DQU1 | 70 | 24 | 2AR13(1-4) | | DQU1 |
| 29 | 9 | 2AR2(2-3) | | DQU3 | 71 | 25 | 2AR4(2-3) | | DQU3 |
| 41 | 10 | 4AR2(4-5) | | DQU0 | 83 | 26 | 4AR4(4-5) | | DQU0 |
| 42 | 11 | 4AR10(1-8) | | DQU2 | 84 | 27 | 4AR12(1-8) | | DQU2 |
| 24 | 12 | 2AR11(2-3) | | DQU7 | 66 | 28 | 2AR13(2-3) | | DQU7 |
| 25 | 13 | 2AR2(1-4) | | DQU5 | 67 | 29 | 2AR4(1-4) | | DQU5 |
| 38 | 14 | 4AR10(2-7) | | DQU4 | 79 | 30 | 4AR4(3-6) | | DQU4 |
| 37 | 15 | 4AR2(3-6) | | DQU6 | 80 | 31 | 4AR12(2-7) | | DQU6 |
| 174 | 32 | 4AR13(3-6) | U3 | DQL3 | 216 | 48 | 4AR15(3-6) | U4 | DQL3 |
| 173 | 33 | 4AR5(2-7) | | DQL1 | 215 | 49 | 4AR7(2-7) | | DQL1 |
| 187 | 34 | 2AR6(2-3) | | DQL2 | 228 | 50 | 2AR16(1-4) | | DQL2 |
| 186 | 35 | 2AR14(1-4) | | DQL0 | 229 | 51 | 2AR8(2-3) | | DQL0 |
| 170 | 36 | 4AR13(4-5) | | DQL7 | 211 | 52 | 4AR7(1-8) | | DQL7 |
| 169 | 37 | 4AR5(1-8) | | DQL5 | 212 | 53 | 4AR15(4-5) | | DQL5 |
| 183 | 38 | 2AR6(1-4) | | DQL6 | 224 | 54 | 2AR16(2-3) | | DQL6 |
| 182 | 39 | 2AR14(2-3) | | DQL4 | 225 | 55 | 2AR8(1-4) | | DQL4 |
| 195 | 40 | 2AR7(2-3) | | DQU1 | 237 | 56 | 4AR8(2-7) | | DQU1 |
| 194 | 41 | 2AR15(1-4) | | DQU3 | 236 | 57 | 4AR16(3-6) | | DQU3 |
| 207 | 42 | 4AR6(4-5) | | DQU0 | 249 | 58 | 2AR17(2-3) | | DQU0 |
| 208 | 43 | 4AR14(1-8) | | DQU2 | 250 | 59 | 2AR9(1-4) | | DQU2 |
| 191 | 44 | 2AR7(1-4) | | DQU7 | 232 | 60 | 4AR16(4-5) | | DQU7 |
| 190 | 45 | 2AR15(2-3) | | DQU5 | 233 | 61 | 4AR8(1-8) | | DQU5 |
| 203 | 46 | 4AR6(3-6) | | DQU4 | 245 | 62 | 2AR9(1-4) | | DQU4 |
| 204 | 47 | 4AR14(2-7) | | DQU6 | 246 | 63 | 2AR17(2-3) | | DQU6 |

**First check the SPD data and EEPROM. Then check the following components for other problem.**

| | Clock loading | Boot failure |
|---|---|---|
| 1-RANK | R1,R3,R4 | SPD data TS1 |

# 10. Speed Bins

**DDR4-1600 Speed Bins and Operations**

| DDR4-1600 Speed Bin | | | | | | Unit |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 11-11-11 | | |
| Parameter | | | Symbol | Min | Max | |
| Internal READ command to first data | | | tAA | 13.75[15]<br>(13.50)[5, 13] | 18.00 | ns |
| Internal READ command to first data with read DBI enabled | | | tAA DBI | tAA(MIN) + 2*n*CK | tAA(MIN) + 2*n*CK | ns |
| ACTIVATE to internal READ or WRITE delay time | | | tRCD | 13.75<br>(13.50)[5, 13] | – | ns |
| PRECHARGE command period | | | tRP | 13.75<br>(13.50)[5, 13] | – | ns |
| ACTIVATE-to-PRECHARGE command period | | | tRAS | 35 | 9 x tREFI | ns |
| ACTIVATE-to-ACTIVATE or REFRESH command period | | | tRC | tRAS + tRP | – | ns |
| | Normal | Read DBI | | | | |
| CWL=9 | CL=9 | CL=11 | tCK(AVG) | 1.5<br>(Optional)[5, 13] | 1.6 | ns |
| | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| CWL=9, 11 | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| | CL=11 | CL=13 | tCK(AVG) | 1.25 | <1.5 | ns |
| | CL=12 | CL=14 | tCK(AVG) | 1.25 | <1.5 | ns |
| Supported CL Settings | | | | (9), 11, 12 | | nCK |
| Supported CL Settings with DBI | | | | (11), 13, 14 | | nCK |
| Supported CLW Settings | | | | 9, 11 | | nCK |

## DDR4-1866 Speed Bins and Operations

| DDR4-1866 Speed Bin | | | | | | Unit |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 13-13-13 | | |
| Parameter | | | Symbol | Min | Max | |
| Internal READ command to first data | | | tAA | 13.92[15]<br>(13.50)[5, 13] | 18.00 | ns |
| Internal READ command to first data with read DBI enabled | | | tAA DBI | tAA(MIN) + 2*n*CK | tAA(MIN) + 2*n*CK | ns |
| ACTIVATE to internal READ or WRITE delay time | | | tRCD | 13.92<br>(13.50)[5, 13] | – | ns |
| PRECHARGE command period | | | tRP | 13.92<br>(13.50)[5, 13] | – | ns |
| ACTIVATE-to-PRECHARGE command period | | | tRAS | 34 | 9 x tREFI | ns |
| ACTIVATE-to-ACTIVATE or REFRESH command period | | | tRC | tRAS + tRP | – | ns |
| | Normal | Read DBI | | | | |
| CWL=9 | CL=9 | CL=11 | tCK(AVG) | 1.5<br>(Optional)[5, 13] | 1.6 | ns |
| | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| CWL=9, 11 | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| | CL=11 | CL=13 | tCK(AVG) | 1.25 | <1.5 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=12 | CL=14 | tCK(AVG) | 1.25 | <1.5 | ns |
| CWL=10, 12 | CL=12 | CL=14 | tCK(AVG) | Reserved | | ns |
| | CL=13 | CL=15 | tCK(AVG) | 1.071 | <1.25 | ns |
| | CL=14 | CL=16 | tCK(AVG) | 1.071 | <1.25 | ns |
| Supported CL Settings | | | | 9, 11, 12, 13, 14 | | nCK |
| Supported CL Settings with DBI | | | | 11, 13, 14, 15, 16 | | nCK |
| Supported CLW Settings | | | | 9, 10, 11, 12 | | nCK |

## DDR4-2133 Speed Bins and Operations

| DDR4-2133 Speed Bin | | | | | | Unit |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 15-15-15 | | |
| Parameter | | | Symbol | Min | Max | |
| Internal READ command to first data | | | tAA | 14.06[15]<br>(13.50)[5, 13] | 18.00 | ns |
| Internal READ command to first data with read DBI enabled | | | tAA DBI | tAA(MIN) + 2*n*CK | tAA(MIN) + 2*n*CK | ns |
| ACTIVATE to internal READ or WRITE delay time | | | tRCD | 14.06<br>(13.50)[5, 13] | – | ns |
| PRECHARGE command period | | | tRP | 14.06<br>(13.50)[5, 13] | – | ns |
| ACTIVATE-to-PRECHARGE command period | | | tRAS | 33 | 9 x tREFI | ns |
| ACTIVATE-to-ACTIVATE or REFRESH command period | | | tRC | tRAS + tRP | – | ns |
| | Normal | Read DBI | | | | |
| CWL=9 | CL=9 | CL=11 | tCK(AVG) | 1.5<br>(Optional)[5, 13] | 1.6 | ns |
| | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| CWL=9, 11 | CL=11 | CL=13 | tCK(AVG) | 1.25 | <1.5 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=12 | CL=14 | tCK(AVG) | 1.25 | <1.5 | ns |
| CWL=10, 12 | CL=13 | CL=15 | tCK(AVG) | 1.071 | <1.25 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=14 | CL=16 | tCK(AVG) | 1.071 | <1.25 | ns |
| CWL=11, 14 | CL=14 | CL=17 | tCK(AVG) | Reserved | | ns |
| | CL=15 | CL=18 | tCK(AVG) | 0.937 | <1.071 | ns |
| | CL=16 | CL=19 | tCK(AVG) | 0.937 | <1.071 | ns |
| Supported CL Settings | | | | (9), (11), 12, (13), 14,15, 16 | | nCK |
| Supported CL Settings with DBI | | | | (11), (13), 14, (15), 16, 18, 19 | | nCK |
| Supported CLW Settings | | | | 9, 11, 11, 12, 14 | | nCK |

## DDR4-2400 Speed Bins and Operations

| DDR4-2400 Speed Bin | | | | | | Unit |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 17-17-17 | | |
| Parameter | | | Symbol | Min | Max | |
| Internal READ command to first data | | | tAA | 14.16 (13.75)[5, 13] | 18.00 | ns |
| Internal READ command to first data with read DBI enabled | | | tAA DBI | tAA(MIN) + 3*n*CK | tAA(MIN) + 3*n*CK | ns |
| ACTIVATE to internal READ or WRITE delay time | | | tRCD | 14.16 (13.75)[5, 13] | – | ns |
| PRECHARGE command period | | | tRP | 14.16 (13.75)[5, 13] | – | ns |
| ACTIVATE-to-PRECHARGE command period | | | tRAS | 32 | 9 x tREFI | ns |
| ACTIVATE-to-ACTIVATE or REFRESH command period | | | tRC | tRAS + tRP | – | ns |
| | Normal | Read DBI | | | | |
| CWL=9 | CL=9 | CL=11 (Optional)[5] | tCK(AVG) | Reserved | | ns |
| | CL=10 | CL=12 | tCK(AVG) | 1.5 | 1.6 | ns |
| CWL=9, 11 | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| | CL=11 | CL=13 | tCK(AVG) | 1.25 | <1.5 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=12 | CL=14 | tCK(AVG) | 1.25 | <1.5 | ns |
| CWL=10, 12 | CL=12 | CL=14 | tCK(AVG) | Reserved | | ns |
| | CL=13 | CL=15 | tCK(AVG) | 1.071 | <1.25 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=14 | CL=16 | tCK(AVG) | 1.071 | <1.25 | ns |
| CWL=11, 14 | CL=14 | CL=17 | tCK(AVG) | Reserved | | ns |
| | CL=15 | CL=18 | tCK(AVG) | 0.937 | <1.071 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=16 | CL=19 | tCK(AVG) | 0.937 | <1.071 | ns |
| CWL=12, 16 | CL=15 | CL=18 | tCK(AVG) | Reserved | | ns |
| | CL=16 | CL=19 | tCK(AVG) | Reserved | | ns |
| | CL=17 | CL=20 | tCK(AVG) | 0.833 | <0.937 | ns |
| | CL=18 | CL=21 | tCK(AVG) | 0.833 | <0.937 | ns |
| Supported CL Settings | | | | 10, 11, 12, 13, 14, 15, 16, 17, 18 | | nCK |
| Supported CL Settings with DBI | | | | 12, 13, 14, 15, 16, 18, 19, 20, 21 | | nCK |
| Supported CLW Settings | | | | 9, 10, 11, 12, 14, 16 | | nCK |

## DDR4-2666 Speed Bins and Operations

| DDR4-2666 Speed Bin | | | | | | Unit |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 19-19-19 | | |
| Parameter | | | Symbol | Min | Max | |
| Internal READ command to first data | | | tAA | 14.25 (13.75)[5, 13] | 18.00 | ns |
| Internal READ command to first data with read DBI enabled | | | tAA DBI | tAA(MIN) + 3*n*CK | tAA(MIN) + 3*n*CK | ns |
| ACTIVATE to internal READ or WRITE delay time | | | tRCD | 14.25 (13.75)[5, 13] | – | ns |
| PRECHARGE command period | | | tRP | 14.25 (13.75)[5, 13] | – | ns |
| ACTIVATE-to-PRECHARGE command period | | | tRAS | 32 | 9 x tREFI | ns |
| ACTIVATE-to-ACTIVATE or REFRESH command period | | | tRC | tRAS + tRP | – | ns |
| | Normal | Read DBI | | | | |
| CWL=9 | CL=9 | CL=11 | tCK(AVG) | Reserved | | ns |
| | CL=10 | CL=12 | tCK(AVG) | 1.5 | 1.6 | ns |
| CWL=9, 11 | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| | CL=11 | CL=13 | tCK(AVG) | 1.25 | <1.5 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=12 | CL=14 | tCK(AVG) | 1.25 | <1.5 | ns |
| CWL=10, 12 | CL=12 | CL=14 | tCK(AVG) | Reserved | | ns |
| | CL=13 | CL=15 | tCK(AVG) | 1.071 | <1.25 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=14 | CL=16 | tCK(AVG) | 1.071 | <1.25 | ns |
| CWL=11, 14 | CL=14 | CL=17 | tCK(AVG) | Reserved | | ns |
| | CL=15 | CL=18 | tCK(AVG) | 0.937 | <1.071 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=16 | CL=19 | tCK(AVG) | 0.937 | <1.071 | ns |
| CWL=12, 16 | CL=15 | CL=18 | tCK(AVG) | Reserved | | ns |
| | CL=16 | CL=19 | tCK(AVG) | Reserved | | ns |
| | CL=17 | CL=20 | tCK(AVG) | 0.833 | <0.937 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=18 | CL=21 | tCK(AVG) | 0.833 | <0.937 | ns |
| CWL=14, 18 | CL=17 | CL=20 | tCK(AVG) | Reserved | | ns |
| | CL=18 | CL=21 | tCK(AVG) | Reserved | | ns |
| | CL=19 | CL=22 | tCK(AVG) | 0.75 | <0.833 | ns |
| | CL=20 | CL=23 | tCK(AVG) | 0.75 | <0.833 | ns |

| DDR4-2666 Speed Bin | | | | Unit |
|---|---|---|---|---|
| CL-nRCD-nRP | | 19-19-19 | | |
| Parameter | Symbol | Min | Max | |
| Supported CL Settings | | 10, 11, 12, 13, 14, 15, 16, 17, 18 | | nCK |
| Supported CL Settings with DBI | | 12, 13, 14, 15, 16, 18, 19, 20, 21 | | nCK |
| Supported CLW Settings | | 9, 10, 11, 12, 14, 16 | | nCK |

## DDR4-2933 Speed Bins and Operations

| DDR4-2933 Speed Bin | | | | | | Unit |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 21-21-21 | | |
| Parameter | | | Symbol | Min | Max | |
| Internal READ command to first data | | | tAA | 14.32 (13.75)[5, 13] | 18.00 | ns |
| Internal READ command to first data with read DBI enabled | | | tAA DBI | tAA(MIN) + 4*n*CK | tAA(MIN) + 4*n*CK | ns |
| ACTIVATE to internal READ or WRITE delay time | | | tRCD | 14.32 (13.75)[5, 13] | – | ns |
| PRECHARGE command period | | | tRP | 14.32 (13.75)[5, 13] | – | ns |
| ACTIVATE-to-PRECHARGE command period | | | tRAS | 32 | 9 x tREFI | ns |
| ACTIVATE-to-ACTIVATE or REFRESH command period | | | tRC | tRAS + tRP | – | ns |
| | Normal | Read DBI | | | | |
| CWL=9 | CL=9 | CL=11 | tCK(AVG) | Reserved | | ns |
| | CL=10 | CL=12 | tCK(AVG) | 1.5 | 1.6 | ns |
| CWL=9, 11 | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| | CL=11 | CL=13 | tCK(AVG) | 1.25 | <1.5 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=12 | CL=14 | tCK(AVG) | 1.25 | <1.5 | ns |
| CWL=10, 12 | CL=12 | CL=14 | tCK(AVG) | Reserved | | ns |
| | CL=13 | CL=15 | tCK(AVG) | 1.071 | <1.25 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=14 | CL=16 | tCK(AVG) | 1.071 | <1.25 | ns |
| CWL=11, 14 | CL=14 | CL=17 | tCK(AVG) | Reserved | | ns |
| | CL=15 | CL=18 | tCK(AVG) | 0.937 | <1.071 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=16 | CL=19 | tCK(AVG) | 0.937 | <1.071 | ns |
| CWL=12, 16 | CL=15 | CL=18 | tCK(AVG) | Reserved | | ns |
| | CL=16 | CL=19 | tCK(AVG) | Reserved | | ns |
| | CL=17 | CL=20 | tCK(AVG) | 0.833 | <0.937 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=18 | CL=21 | tCK(AVG) | 0.833 | <0.937 | ns |
| CWL=14, 18 | CL=17 | CL=20 | tCK(AVG) | Reserved | | ns |
| | CL=18 | CL=21 | tCK(AVG) | Reserved | | ns |
| | CL=19 | CL=22 | tCK(AVG) | 0.75 | <0.833 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=20 | CL=23 | tCK(AVG) | 0.75 | <0.833 | ns |

| DDR4-2933 Speed Bin | | | | | | Unit |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 21-21-21 | | |
| Parameter | | | Symbol | Min | Max | |
| CWL=16, 20 | CL=19 | CL=23 | tCK(AVG) | Reserved | | ns |
| | CL=20 | CL=24 | tCK(AVG) | Reserved | | ns |
| | CL=21 | CL=25 | tCK(AVG) | 0.682 | <0.75 | ns |
| | CL=22 | CL=26 | tCK(AVG) | 0.682 | <0.75 | ns |
| Supported CL Settings | | | | 10, (11), 12, (13), 14, (15), 16, (17), 18, (19), 20, 21, 22 | | nCK |
| Supported CL Settings with DBI | | | | 12, (13), 14, (15), 16, (18), 19, (20), 21, (22), 23, 25, 26 | | nCK |
| Supported CLW Settings | | | | 9, 10, 11, 12, 14, 15, 16, 18, 20 | | nCK |

## DDR4-3200 Speed Bins and Operations

| DDR4-3200 Speed Bin | | | | | | Unit |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 22-22-22 | | |
| Parameter | | | Symbol | Min | Max | |
| Internal READ command to first data | | | tAA | 13.75 | 18.00 | ns |
| Internal READ command to first data with read DBI enabled | | | tAA DBI | tAA(MIN) + 4*n*CK | tAA(MIN) + 4*n*CK | ns |
| ACTIVATE to internal READ or WRITE delay time | | | tRCD | 13.75 | 18.00 | ns |
| PRECHARGE command period | | | tRP | 13.75 | 18.00 | ns |
| ACTIVATE-to-PRECHARGE command period | | | tRAS | 32 | 9 x tREFI | ns |
| ACTIVATE-to-ACTIVATE or REFRESH command period | | | tRC | tRAS + tRP | - | ns |
| | Normal | Read DBI | | | | |
| CWL=9 | CL=9 | CL=11 | tCK(AVG) | Reserved | | ns |
| | CL=10 | CL=12 | tCK(AVG) | 1.5 | 1.6 | ns |
| CWL=9, 11 | CL=10 | CL=12 | tCK(AVG) | Reserved | | ns |
| | CL=11 | CL=13 | tCK(AVG) | 1.25 | <1.5 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=12 | CL=14 | tCK(AVG) | 1.25 | <1.5 | ns |
| CWL=10, 12 | CL=12 | CL=14 | tCK(AVG) | Reserved | | ns |
| | CL=13 | CL=15 | tCK(AVG) | 1.071 | <1.25 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=14 | CL=16 | tCK(AVG) | 1.071 | <1.25 | ns |
| CWL=11, 14 | CL=14 | CL=17 | tCK(AVG) | Reserved | | ns |
| | CL=15 | CL=18 | tCK(AVG) | 0.937 | <1.071 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=16 | CL=19 | tCK(AVG) | 0.937 | <1.071 | ns |
| CWL=12, 16 | CL=15 | CL=18 | tCK(AVG) | Reserved | | ns |
| | CL=16 | CL=19 | tCK(AVG) | Reserved | | ns |
| | CL=17 | CL=20 | tCK(AVG) | 0.833 | <0.937 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=18 | CL=21 | tCK(AVG) | 0.833 | <0.937 | ns |
| CWL=14, 18 | CL=17 | CL=20 | tCK(AVG) | Reserved | | ns |
| | CL=18 | CL=21 | tCK(AVG) | Reserved | | ns |
| | CL=19 | CL=22 | tCK(AVG) | 0.75 | <0.833 | ns |
| | | | | (Optional)[5, 13] | | ns |
| | CL=20 | CL=23 | tCK(AVG) | 0.75 | <0.833 | ns |
| CWL=16, 20 | CL=20 | CL=24 | tCK(AVG) | Reserved | | ns |
| | CL=22 | CL=26 | tCK(AVG) | 0.625 | <0.75 | ns |
| | CL=24 | CL=28 | tCK(AVG) | 0.625 | <0.75 | ns |

| DDR4-3200 Speed Bin | | | | Unit |
|---|---|---|---|---|
| CL-nRCD-nRP | | 22-22-22 | | |
| Parameter | Symbol | Min | Max | |
| Supported CL Settings | | 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24 | | nCK |
| Supported CL Settings with DBI | | 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 26, 28 | | nCK |
| Supported CLW Settings | | 9, 10, 11, 12, 14, 16, 18, 20 | | nCK |

**Note:**

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled:Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071ns or 0.937ns or 0.833ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR4-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
12. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
13. Parameters apply from tCK(avg) min to tCK(avg) max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
14. CL number in parentheses, it means that these numbers are optional.
15. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
16. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

# 11. DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $T_{OPER}$ | Normal Operating Temperature Range | 0 to 85 | ℃ |

**Note:**

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85℃ under all operating conditions.

# 12. Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| VDD | Voltage on VDD pin relative to Vss | -0.3 ~ 1.5 | V |
| VDDQ | Voltage on VDDQ pin relative to Vss | -0.3 ~ 1.5 | V |
| VPP | Voltage on VPP pin relative to Vss | -0.3 ~ 3.0 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on any relative to VSS | -0.3 ~ 1.5 | V |
| $V_{STG}$ | Storage Temperature | -55 to +100 | ℃ |

**Note:**

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

# 13. AC & DC Operating Conditions

| Symbol | Parameter | Rating | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| VDD | Supply Voltage | 1.14 | 1.2 | VDD | V |
| VDDQ | Supply Voltage for Output | 1.14 | 1.2 | VDDQ | V |
| VPP | Peak-to-Peak Voltage | 2.375 | 2.5 | 2.75 | V |

**Note:**

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

# 14. Functional Diagram

**Figure 1: FD4AS3200C4GZH**

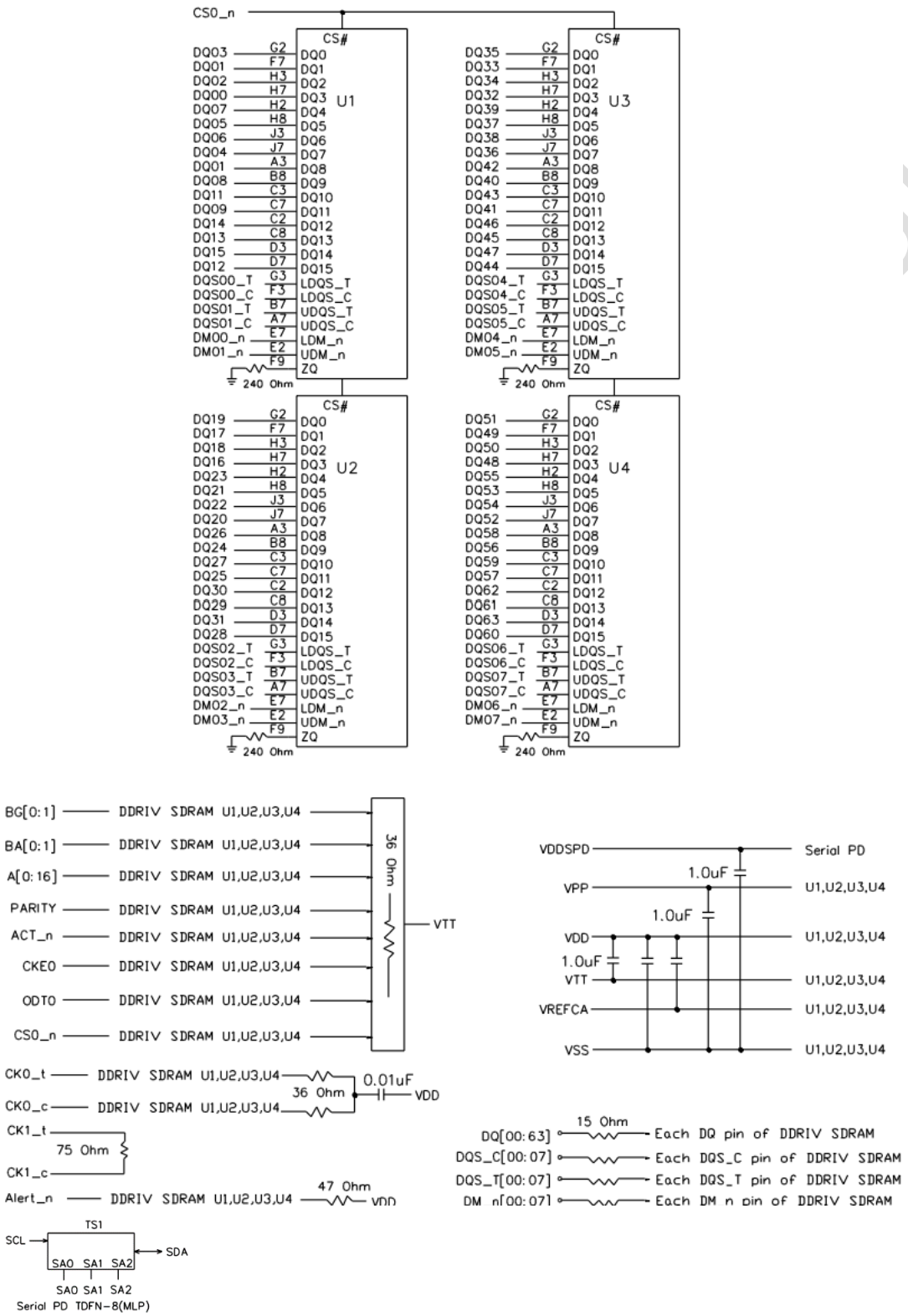
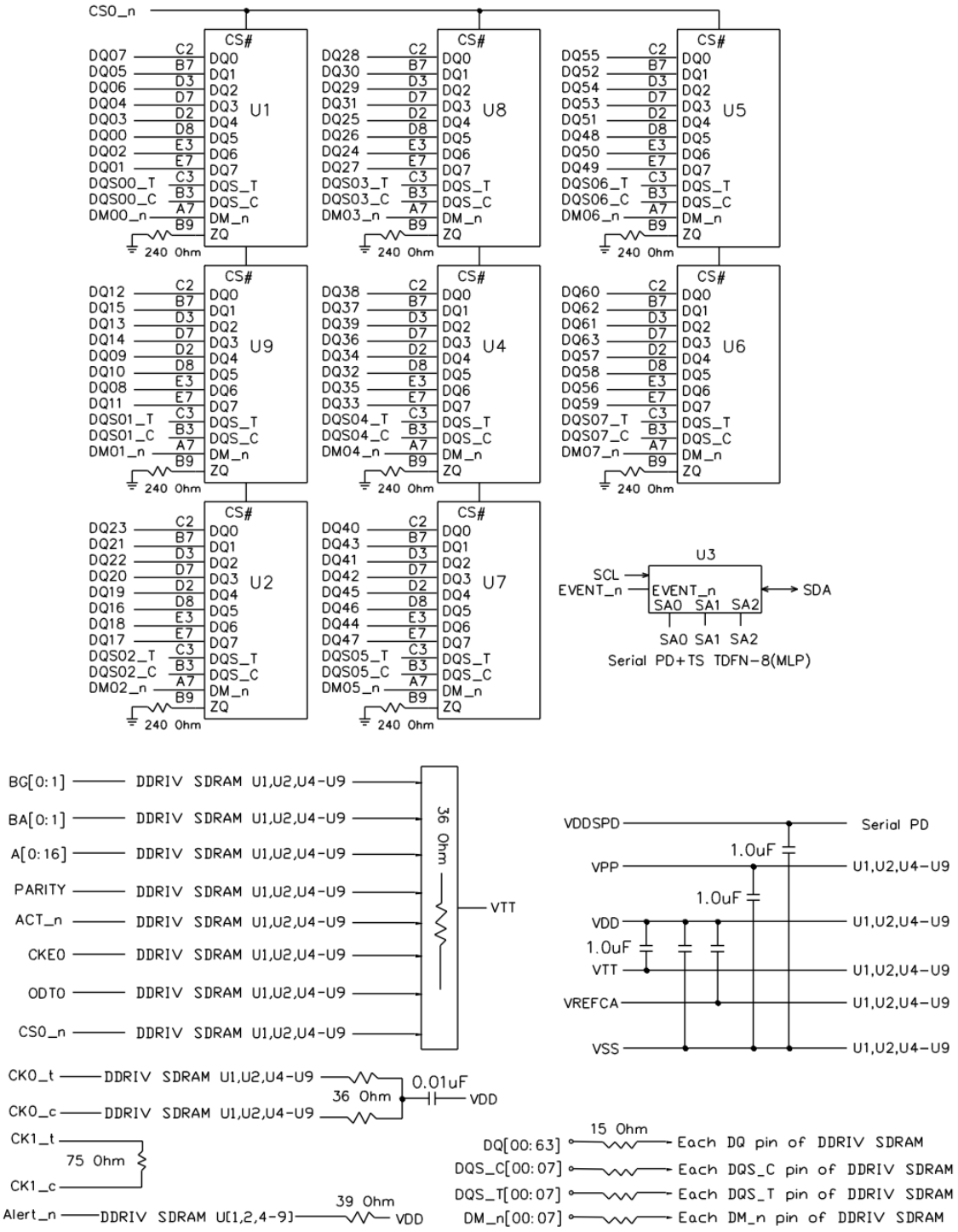


**Figure 2: FD4AS3200C8GZH**



# 15. PCB Specifications

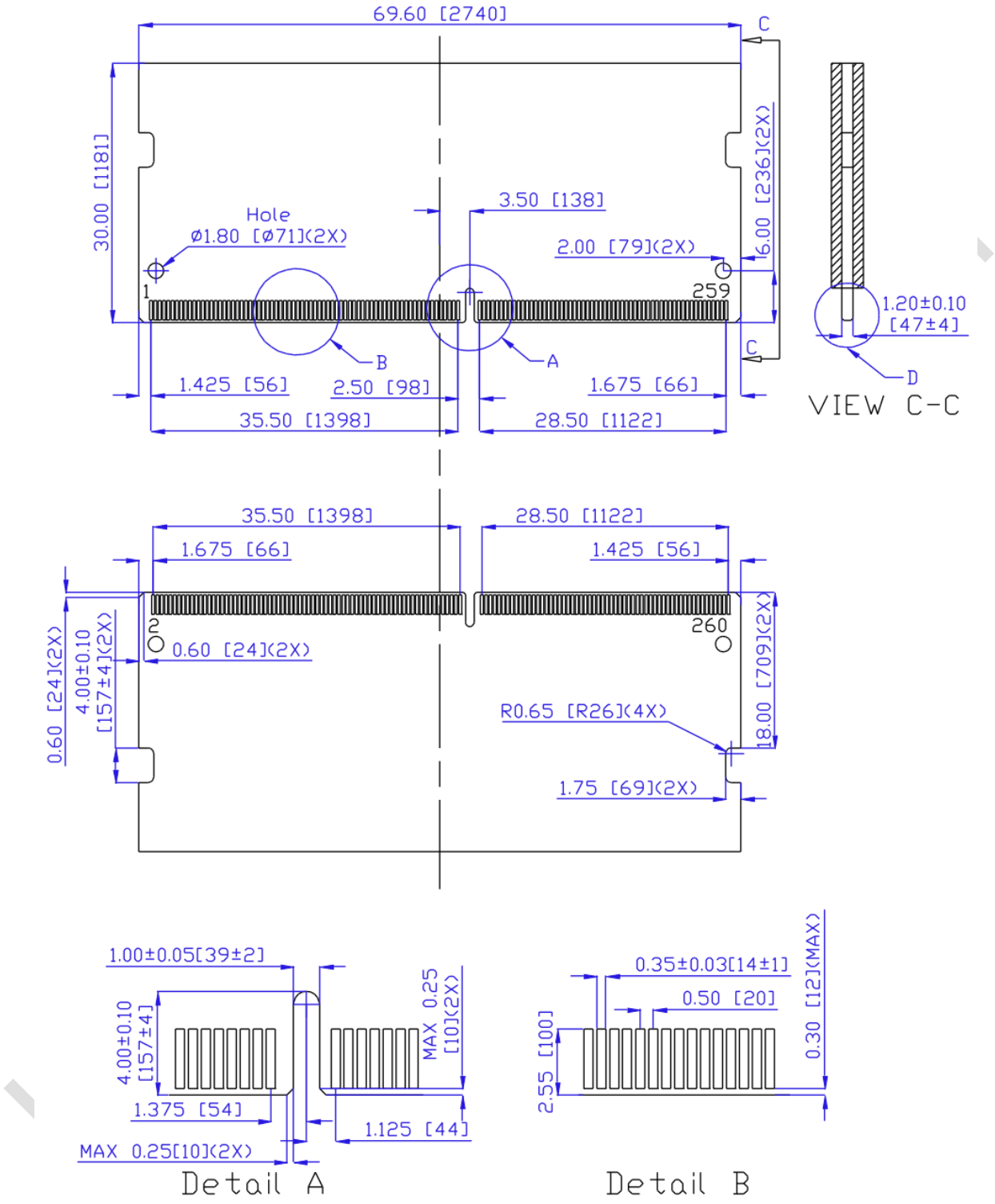
### General

1. Board size：69.6 x 30 mm ± 0.15 mm
2. Thickness：1.2 ± 0.1 mm
3. Pin count：260 PIN

### PCB Material

1. RoHS
2. Glass Epoxy FR4, .UL 94V-0

# 16. Module Dimensions




Units: millimeters

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