FORESEE 8GB DDR4 3200 UDIMM Datasheet

Version: 1.0

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Revision History

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1. Description

FORESEE Unbuffered DDR4 SDRAM DIMMs (Unbuffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered DIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

2. Features

- 288-Pin Unbuffered DDR4 SDRAM memory modules.
- VDD = VDDQ = 1.2V ± 60mV
- 16 Banks (4 Bank Groups)
- 8-bit pre-fetch
- On Die Termination using ODT pin
- (Data Bus Inversion)
- CRC (Cyclic Redundancy Check) for Read/Write data security
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- capabilityPPR and sPPR is supported
- All of Lead-Free products are compliant for RoHS

3. Ordering Information

Part Number	Density	Speed	Component Composition	# of ranks
FD4AU3200C8GSE	8GB	DDR4 3200	1Gx8*8	1

4. Key Parameters

Grade	Speed (Mbps)	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
3200AA	3200	0.625	22	13.75	13.75	32	45.75	22-22-22

5. Address Table

	1G*8
Number of Bank Groups	4
Bank group Address	BG0~BG1
Bank Address in a BG	BA0~BA1
Row Address	A0~A15
Column Address	A0~A9
Page size	1 KB

F D4 A U 3200 C 8G SE

F=FORESEE

DDR3=D3
DDR4=D4
DDR5=D5

A=1.2V
B=1.35V
C=1.5V

U=UDIMM
S=SO-DIMM
E=ECC DIMM
R=Register DIMM
⋮

1600=1600Mbps
2400=2400Mbps
2666=2666Mbps
2933=2933Mbps
3200=3200Mbps
⋮

C= 0-85℃
I =-25-85℃
W=-40-85℃

4G=4GB
8G=8GB
QG=16GB
WG=32GB

SE=SAMSUNG

6. DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units
T_{OPER}	Normal Operating Temperature Range	0 to 85	℃

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85℃ under all operating conditions.

7. Absolute Maximum Ratings

Symbol	Parameter	Rating	Max	Units
VDD	Voltage on VDD pin relative to Vss	-0.3	1.5	V
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3	1.5	V
VPP	Voltage on VPP pin relative to Vss	-0.3	3.0	V
V_{IN}, V_{OUT}	Voltage on any relative to VSS	-0.3	1.5	V

Notes:

1. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV.
2. VPP must be equal or greater than VDD/VDDQ at all times.

8. Supply Operating Conditions

Recommended Supply Operating Conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
VDD	Supply Voltage	1.14	1.2	1.26	V
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V
VPP	Word line supply voltage	2.375	2.5	2.75	V

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

9. x8 Package Pinout (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n/DBI_n /TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	NC	ODT				CK_t	CK_c	VDD	F
G	VSS	NC	CKE				CS_n	NC	TEN	G
H	VDD	WE_n/A14	ACT_n				CAS_n/A15	RAS_n	VSS	H
J	VREFCA	BG0	A10/AP				A12/BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

10. Pin Descriptions

Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address input	SCL	I²C serial bus clock for SPD/TS and register
BA0, BA1	SDRAM bank select input	SDA	I²C serial data line for SPD/TS and register
BG0, BG1	Regsiter bank group select input	SA0–SA2	I²C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power
WE_n[4]	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t TDQS17_t TDQS_c TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

Notes:

1. Address A17 is only valid for 16Gbx4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

11. Input/Output Functional Descriptions

Symbol	Type	Function
CK0/#CK0 CK1/#CK1	IN	Clock: CK_t and CK_c are differential clock inputs. All address and control inputsignals are sampled on the
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.CS2_n and CS3_n are not used on UDIMMs.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. Not used on UDIMMs.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15 and A14.

RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example,for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table.
Symbol	**Type**	**Function**
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations.TDQS is not valid for UDIMMs.
BG0, BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessedduring a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0.
BA0, BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bankan Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additionalfunctions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 SDRAM configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If onlyone bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC isenabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may

		indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
Symbol	**Type**	**Function**
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, toprovide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c are not valid for UDIMMs.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on-going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input.Using this signal or not is dependent on the system.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD1	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VTT	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
12 V	Supply	12 V supply not used on UDIMMs.
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE.
VREFCA	Supply	Reference voltage for CA

Note:

1. Input pins (BG0-BG1,BA0-BA1,A0-A17,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14, CS_n,CKE,ODT,and RESET_n) do not supply termination.

12. Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Lable	Pin	Back Side Pin Label
1	12V	145	12V	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS	KEY			
6	VSS	150	DQ1				
7	DM0_n,DBI_n DQS9_t,TDQS9_t	151	VSS	78	EVENT_n	222	PARITY
8	DQS9_c,TDQS9_c	152	DQS0_c	79	A0	223	VDD
9	VSS	153	DQS0_t	80	VDD	224	BA1
10	DQ6	154	VSS	81	BA0	225	A10/AP
11	VSS	155	DQ7	82	RAS_n/A16	226	VDD
12	DQ2	156	VSS	83	VDD	227	RFU
13	VSS	157	DQ3	84	CS0_n	228	WE_n/A14
14	DQ12	158	VSS	85	VDD	229	VDD
15	VSS	159	DQ13	86	CAS_n/A15	230	NC
16	DQ8	160	VSS	87	ODT0	231	VDD
17	VSS	161	DQ9	88	VDD	232	A13
18	DM1_n,DBI1_n DQS10_t,TDQS10_t	162	VSS	89	CS1_n	233	VDD
19	DQS10_c,TDQS10_c	163	DQS1_c	90	VDD	234	NC
20	VSS	164	DQS1_t	91	ODT1	235	NC
21	DQ14	165	VSS	92	VDD	236	VDD
22	VSS	166	DQ15	93	S2_n,C[0]	237	NC,CS3_n,C1
23	DQ10	167	VSS	94	VSS	238	SA2
24	VSS	168	DQ11	95	DQ36	239	VSS
25	DQ20	169	VSS	96	VSS	240	DQ37
26	VSS	170	DQ21	97	DQ32	241	VSS
27	DQ16	171	VSS	98	VSS	242	DQ33

28	VSS	172	DQ17	99	DM4_n,DBI4_n DQS13_t,TDQS13_t	243	VSS
29	DM2_n,DBI2_n DQS11_t,TDQS11_t	173	VSS	100	DQS13_c,TDQS13_c	244	DQS4_c
30	DQS11_c,TDQS11_c	174	DQS2_c	101	VSS	245	DQS4_t
31	VSS	175	DQS2_t	102	DQ38	246	VSS
32	DQ22	176	VSS	103	VSS	247	DQ39
33	VSS	177	DQ23	104	DQ34	248	VSS
Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Lable	Pin	Back Side Pin Label
34	DQ18	178	VSS	105	VSS	249	DQ35
35	VSS	179	DQ19	106	DQ44	250	VSS
36	DQ28	180	VSS	107	VSS	251	DQ45
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41
39	VSS	183	DQ25	110	DM5_n,DBI5_n DQS14_t,TDQS14_t	254	VSS
40	DM3_n,DBI3_n DQS12_t,TDQS12_t	184	VSS	111	DQS14_c,TDQS14_c	255	DQS5_c
41	DQS12_c,TDQS12_c	185	DQS3_c	112	VSS	256	DQS3_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4,NC	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5,NC	119	DQ48	263	VSS
49	CB0,NC	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1,NC	121	DM6_n,DBI6_n DQS15_t,TDQS15_t	265	VSS
51	DM8_n,DBI_n DQS17_t,TDQS17_t	195	VSS	122	DQS15_c,TDQS15_c	266	DQS6_c
52	DQS17_c,TDQS17_c	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6,NC	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7,NC	126	DQ50	270	VSS
56	CB2,NC	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3,NC	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1	130	DQ56	274	VSS
60	ACT_n	204	VDD	131	VSS	275	DQ57

61	VDD	205	RFU	132	DM7_n,DBI7_n DQS16_t,TDQS16_t	276	VSS
62	ACT_n	206	VDD	133	DQS16_c,TDQS16_c	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Lable	Pin	Back Side Pin Label
68	A8	212	VDD	139	SA0	283	VSS
69	A6	213	A5	140	SA1	284	VDDSPD
70	VDD	214	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

13. DDR4-3200 Speed Bins and Operations

Speed Bin		DDR4-3200V		Unit
CL-nRCD-nRP		22-22-22		ns
Parameter	Symbol	min	max	ns
Internal READ command to first data	tAA	13.75	18.00	ns
Internal READ command to first data with read DBI enabled	tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns
ACT to internal READ or WRITE delay time	tRCD	13.75	-	ns
PRE command period	tRP	13.75	-	ns
ACT to PRE command Period	tRAS	32	9 x tREFI	ns
ACT to ACT or REF command period	tRC	45.75	-	ns

14. Trouble shooting Guide

Description: DDRIV SDRAM, Single-Rank, x8-FBGA 78-Ball-based, x64 Unbuffered, 288-pin UDIMM

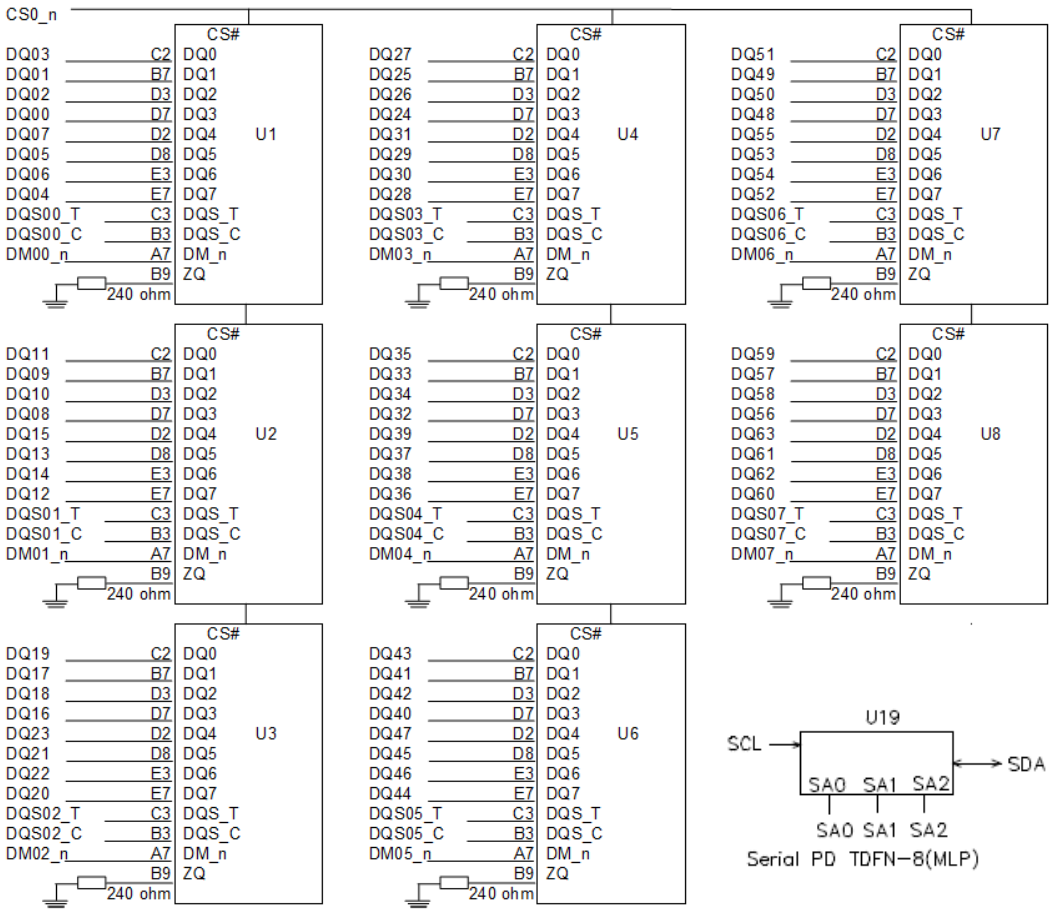
Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ	Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ
5	0	RN1(2-3)	U1	3	16	8	RN7(2-3)	U2	3
150	1	RN3(1-4)		1	161	9	RN5(1-4)		1
12	2	RN2(2-3)		2	23	10	RN8(2-3)		2
157	3	RN4(1-4)		0	168	11	RN6(1-4)		0
3	4	RN1(1-4)		7	14	12	RN7(1-4)		7
148	5	RN3(2-3)		5	159	13	RN5(2-3)		5
10	6	RN2(1-4)		6	21	14	RN8(1-4)		6
155	7	RN4(2-3)		4	166	15	RN6(2-3)		4
27	16	RN9(2-3)	U3	3	38	24	RN15(2-3)	U4	3
172	17	RN11(1-4)		1	183	25	RN13(1-4)		1
34	18	RN12(2-3)		2	45	26	RN14(2-3)		2
179	19	RN10(1-4)		0	190	27	RN16(1-4)		0
25	20	RN9(1-4)		7	36	28	RN15(1-4)		7
170	21	RN11(2-3)		5	181	29	RN13(2-3)		5
32	22	RN12(1-4)		6	43	30	RN14(1-4)		6
177	23	RN10(2-3)		4	188	31	RN16(2-3)		4
97	32	RN17(2-3)	U5	3	108	40	RN21(2-3)	U6	3
242	33	RN19(1-4)		1	253	41	RN23(1-4)		1
104	34	RN20(2-3)		2	115	42	RN24(2-3)		2
249	35	RN18(1-4)		0	260	43	RN22(1-4)		0
95	36	RN17(1-4)		7	106	44	RN21(1-4)		7
240	37	RN19(2-3)		5	251	45	RN23(2-3)		5
102	38	RN20(1-4)		6	113	46	RN24(1-4)		6
247	39	RN18(2-3)		4	258	47	RN22(2-3)		4
119	48	RN26(2-3)	U7	3	130	56	RN28(2-3)	U8	3

264	49	RN25(1-4)		1	275	57	RN30(1-4)		1
126	50	RN45(2-3)		2	137	58	RN29(2-3)		2
271	51	RN27(1-4)		0	282	59	RN31(1-4)		0
117	52	RN26(1-4)		7	128	60	RN28(1-4)		7
262	53	RN25(2-3)		5	273	61	RN30(2-3)		5
124	54	RN45(1-4)		6	135	62	RN29(1-4)		6
269	55	RN27(2-3)		4	280	63	RN31(2-3)		4

First check the SPD data and EEPROM. Then check the following components for other problem.

	Clock loading	Boot failure
1-RANK	R24, RN47	SPD data, U19

15. Functional Diagram



16. PCB Specifications

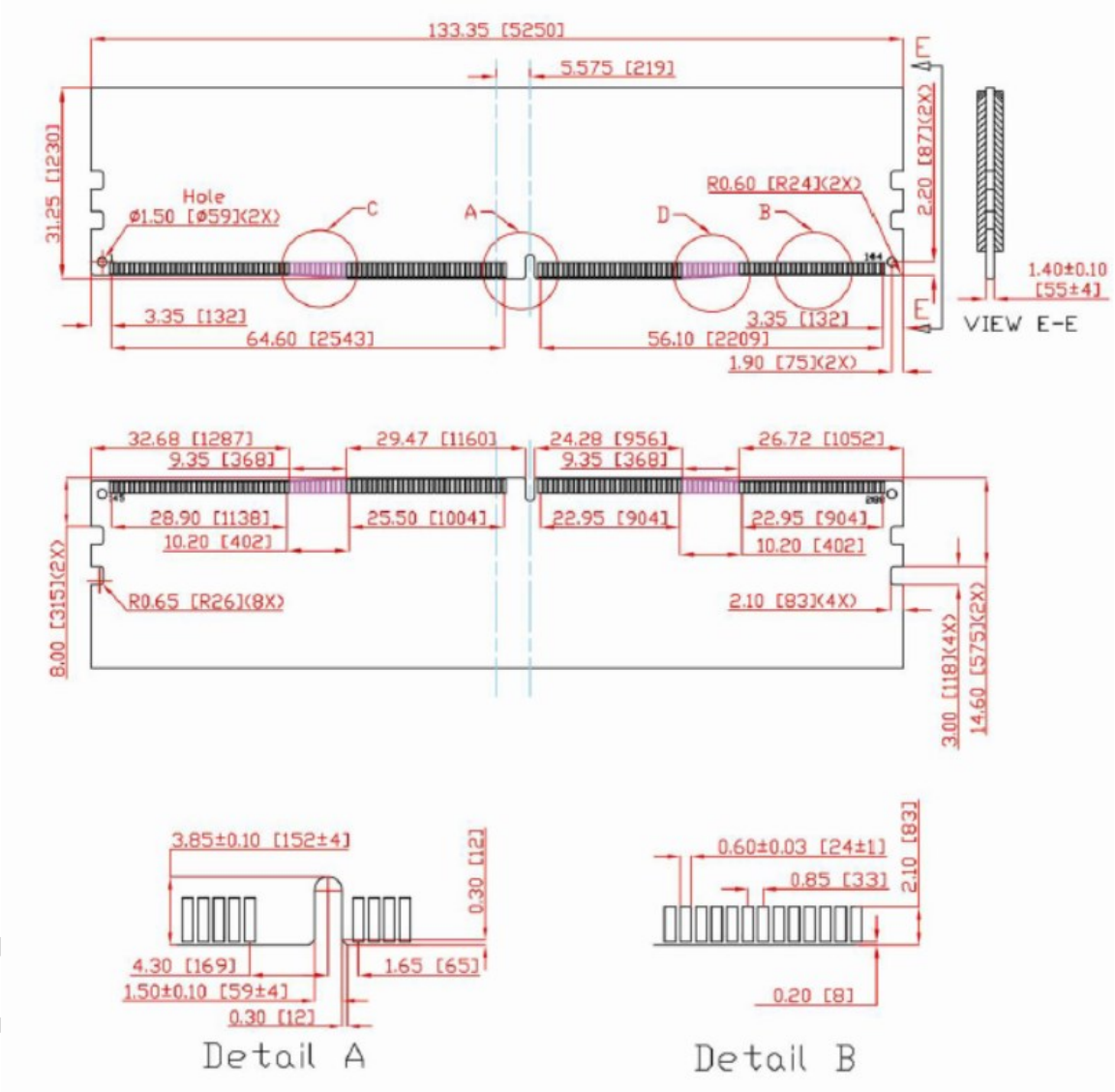
General

1. Board size：133.35 x 31.25 mm ± 0.15 mm
2. Thickness：1.4 ± 0.1 mm
3. Pin count：288 PIN

PCB Material

1. RoHS
2. Glass Epoxy FR4, .UL 94V-0, BP ML or BP 4M-1

17. Module Dimensions



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