FORESEE®

FSNAND Datasheet

FS33ND01GS1
Series

Rev 2.0

2018-07

Revision History:

Rev.	Date	Change	Remark
A0	2017/06	Basic spec and architecture	
A1	2017/07	Revise some descriptions	
1.0	2017/09	Revise some descriptions	
1.1	2017/10	Revise some descriptions	NOP=1
2.0	2018/07	Revise some descriptions	Add Marketing Part Number Chart

Contents

1. INTRODUCTION

1.1. General Description

The FORESEE FSNAND is offered in 3.3 VCC with x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state application market. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.

1.2. Flash ID

Product Family	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle
FS33ND01GS1	ECh	F1h	00h	95h	42h

1.3. Device Features

Voltage Supply
- V_{CC}: 3.3V (2.7V ~ 3.6V)

Organization
- Memory Cell Array : (128M + 4M) Byte
- Page Size : (2K + 64) Byte
- Data Register : (2K + 64) Byte
- Block Erase : (128K + 4K) Byte

Automatic Program and Erase
- Page Program : (2K + 64) Byte

Page Read Operation
- Random Read: 25μs(Max.)
- Serial Access : 25ns(Min.)
- Data Transfer Rate : SDR 40Mhz (40MB/s)

Fast Write Cycle Time
- Page Program time : 400μs(Typ.)
- Block Erase Time : 4.5ms(Typ.)

Command/Address/Data Multiplexed I/O Port

Hardware Data Protection
- Program/Erase Lockout During Power Transitions

Command Driven Operation

Operation Temperature
- -40℃~85℃

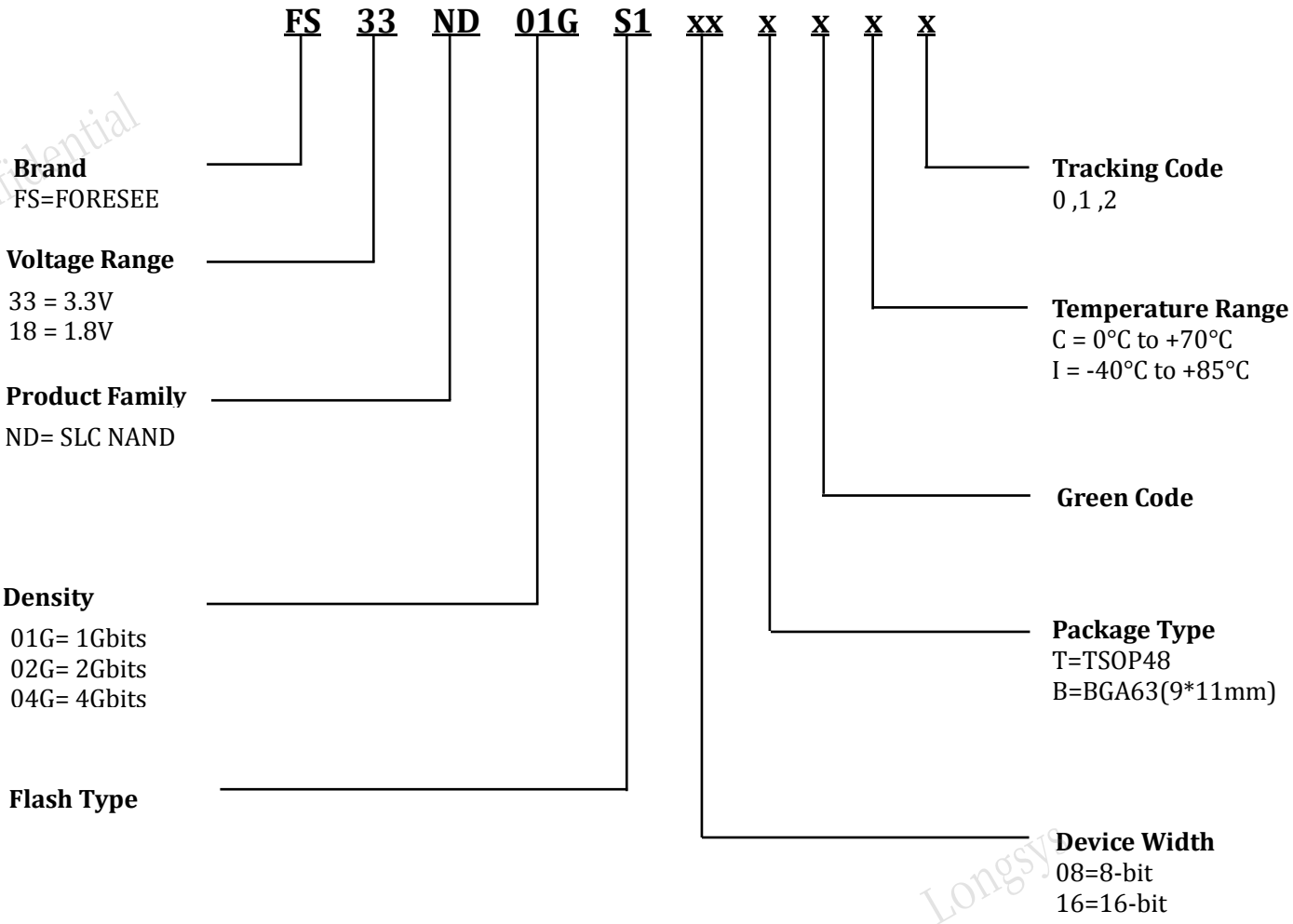
Reliability
- Up to 100,000 P/E Cycle
- 10 Year Data retention (Typ.)

1.4. Product List

[Table 1] Product List

Part Number	Density	Package Type	Organization	Package Size(mm)	VCC Range
FS33ND01GS108TFI0	1Gb	TSOP 48	x8	12*20	2.7V ~ 3.6V
FS33ND01GS108BFI0	1Gb	BGA 63	x8	9*11	2.7V ~ 3.6V

Marketing Part Number Chart



1.5. Connection Diagram

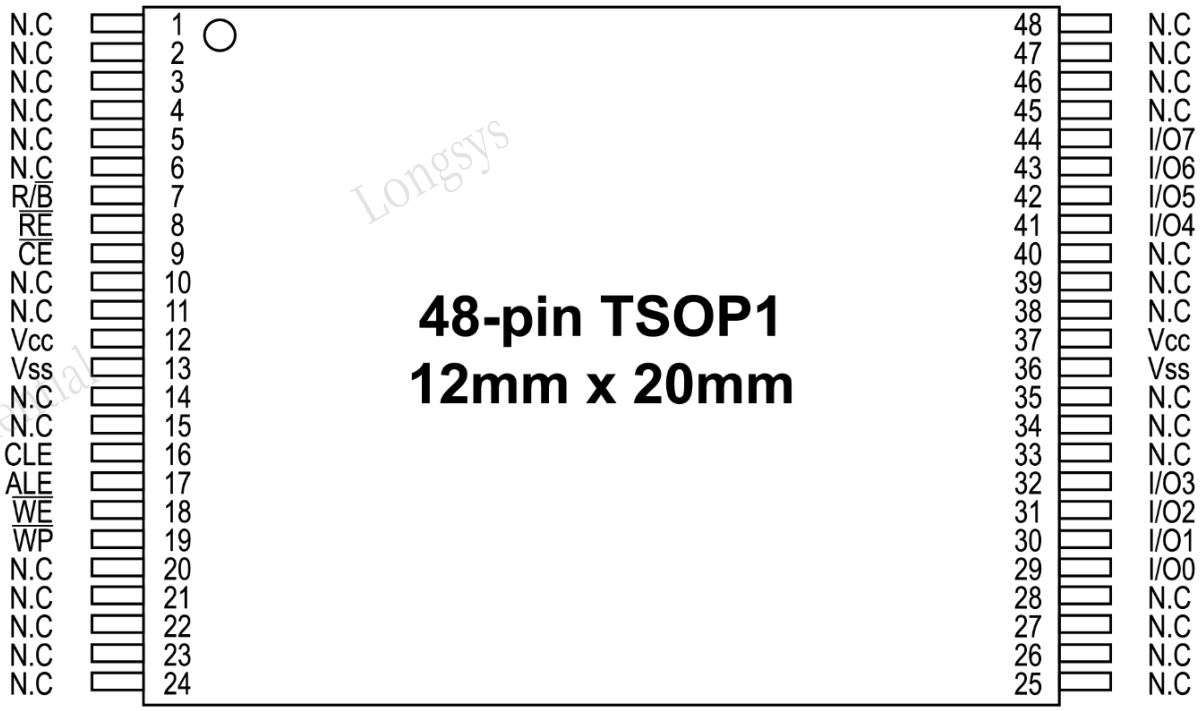


Figure 1 48-Pin TSOP1 Contact x8 Device

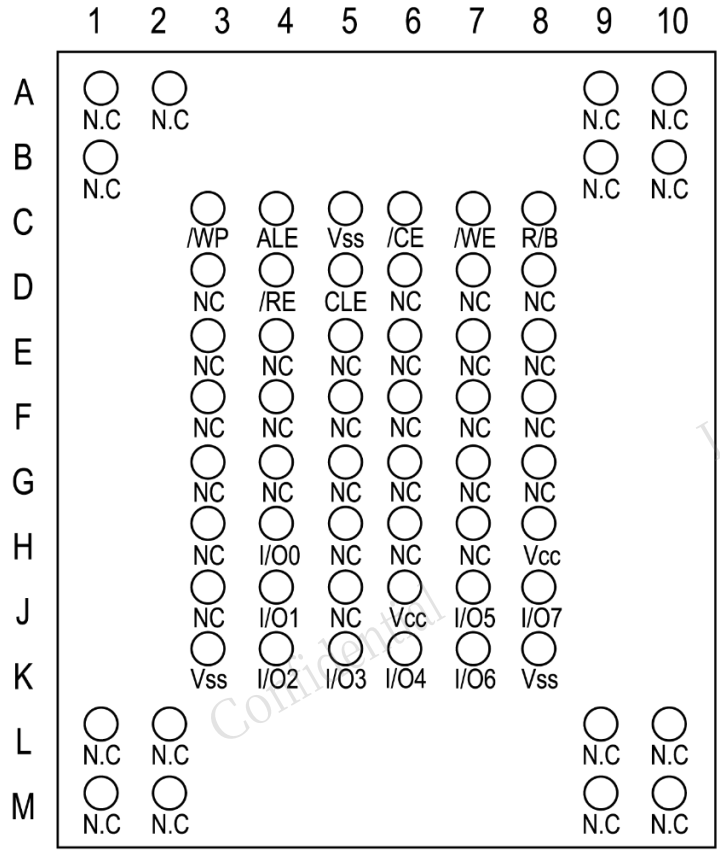


Figure 2 63-BGA Contact, x8 Device (Top View)

1.6. Pin Description

[Table 2] Pin Description

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE# signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE# with ALE high.
CE#	**CHIP ENABLE** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WE#	**WRITE ENABLE** The WE# input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	**WRITE PROTECT** The WP# pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	**READY/BUSY OUTPUT** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**
NC	**NO CONNECTION**

NOTE:
Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.

1.7. System Block Diagram

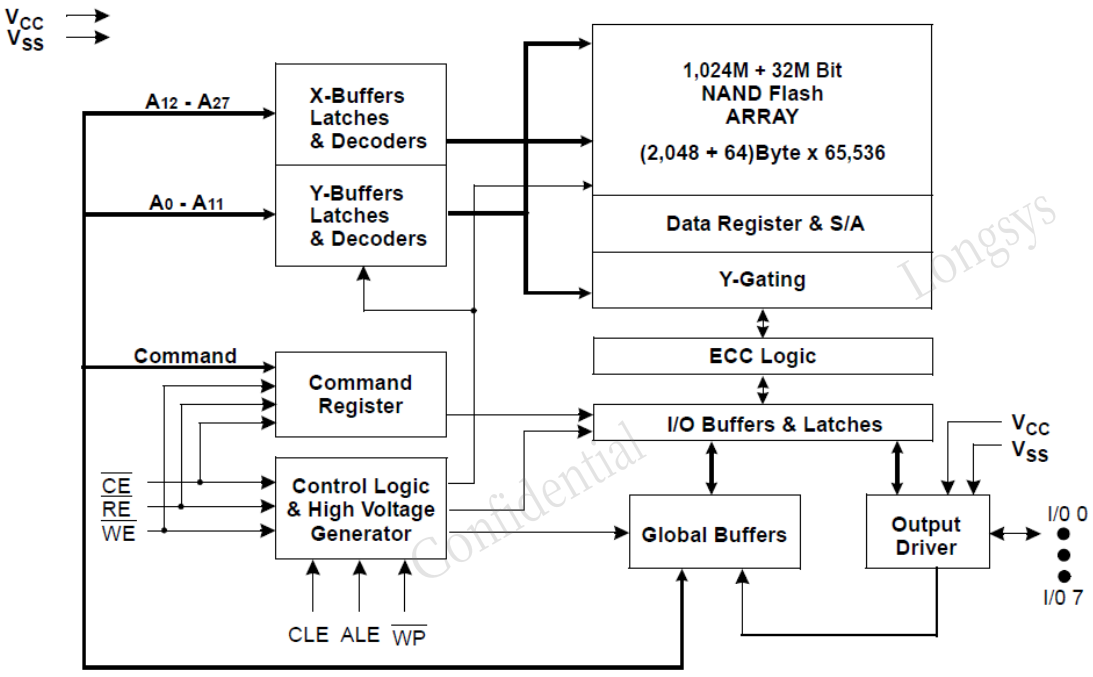


Figure 3 FSNAND Functional Block Diagram

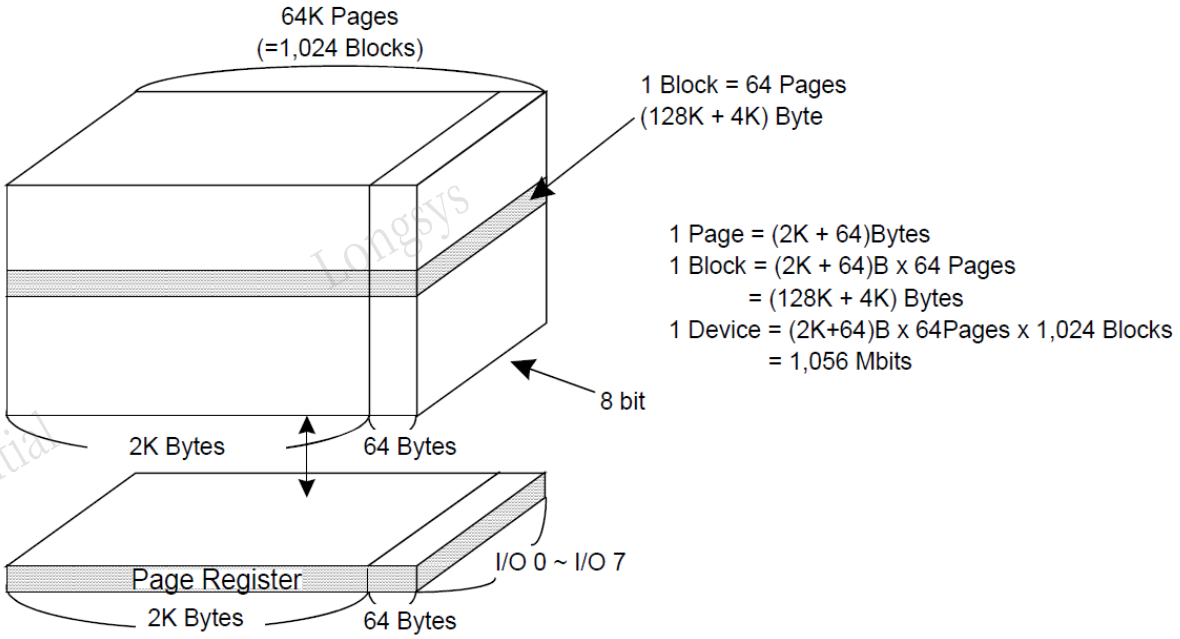


Figure 4 FSNAND Array Organization

1.8. Addressing

[Table 3] Address Cycle Map

Bus cycle	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	L	L	L	L	
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	

NOTE :
Column Address : Starting Address of the Register.
L must be set to "Low".
The device ignores any additional input of address cycles than required.

2. DEVICE OPERATION

2.1. Command Sets

[Table 4] Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input[1)]	85h	-	
Random Data Output[1)]	05h	E0h	
Read Status	70h	-	O
ECC Read Status	7Ah		

NOTE :
1) Random Data Input/Output can be executed in a page.

2.2. Reset Operation

The reset command FFh resets the read/program/erase operation and clear the status register to be C0h (when WP# is high). The reset command during the program/erase operation will result in the content of the selected locations(perform programming/erasing) might be partially programmed/erased. If the Flash memory has already been set to reset stage with reset command, the additional new reset command is invalid.

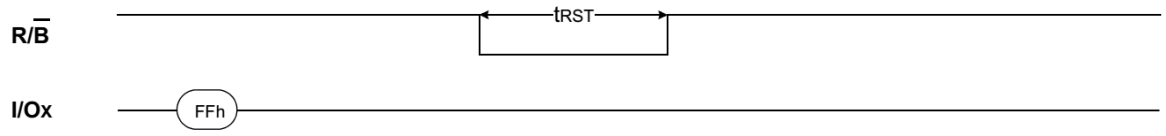


Figure 5 Reset Sequence

2.3. Read ID

The device contains a product identification mode, initiated by wrSiting 90h to the command register, followed by an address input of 00h.
For the FORESEE device, five read cycles sequentially output the 1st Cycle, and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it.

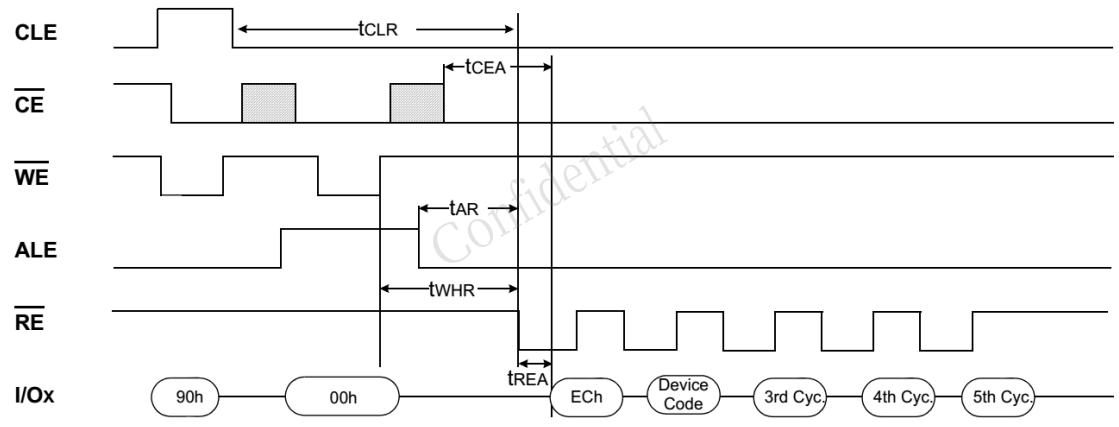


Figure 6 Read ID Sequence

[Table 5]00h Address ID cycle

Part Number	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle
FS33ND01GS1	ECh	F1h	00h	95h	42h

[Table 6]3rd ID Data

	Description	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between multiple chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

[Table 7]4th ID Data

	Description	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Redundant Area Size (byte/512byte)	8 16						0 1		
Organization	x8 x16		0 1						
Serial Access Minimum	50ns/30ns 25ns Reserved Reserved	0 1 0 1				0 0 1 1			

[Table 8]5th ID Data

	Description	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Plane Size (w/o redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Proccess	21nm 1ynm reserved reserved							0 1 0 1	1 0 0 1
Reserved		0						0	0

2.4. Page Read Operation

The device array is accessed in Page of 2,112 bytes. External reads begins after the R/B# pin goes to READY.
The Read operation may also be initiated by writing the 00h command and giving the address (column and row address) and being confirmed by the 30h command, the device begins the internal read operation and the chip enters busy state. The data can be read out in sequence after the chip is ready.
The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

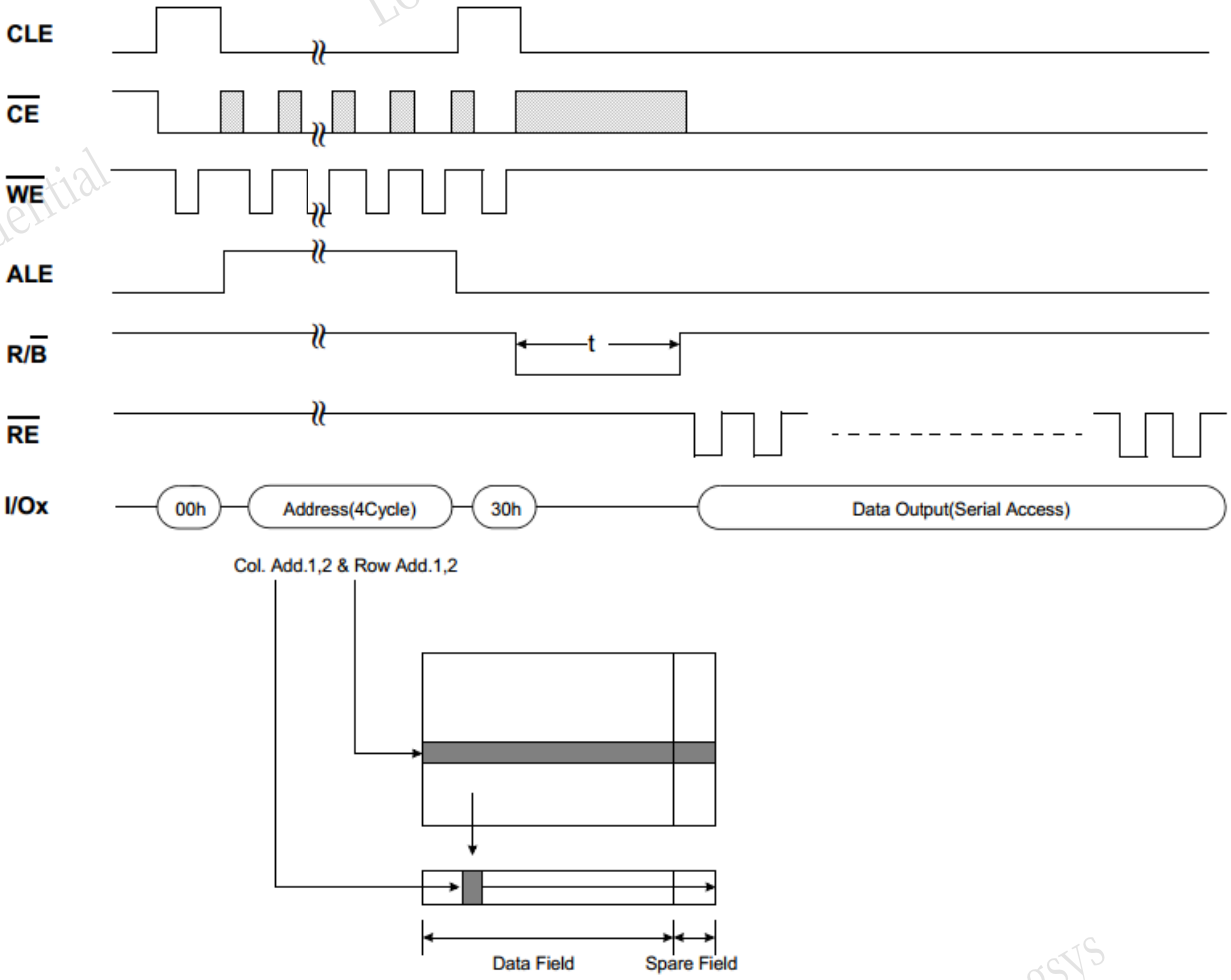


Figure 7 Page Read Sequence

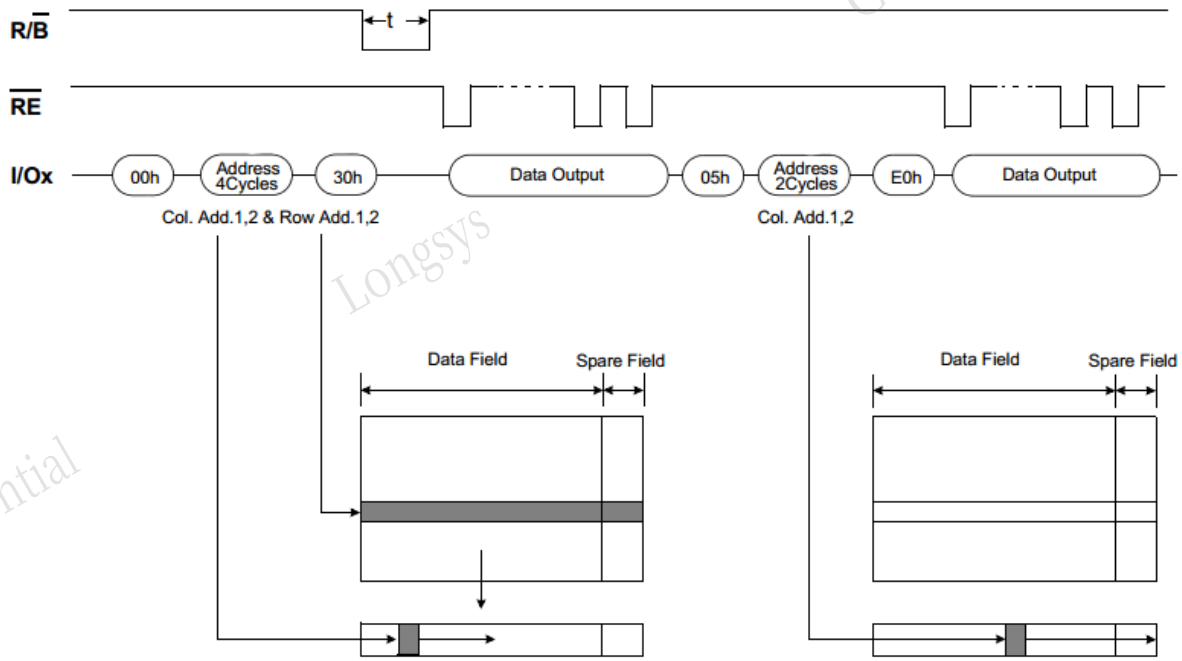


Figure 8 Page Read with Random Data Output Sequence

2.5. Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased.
The memory is programmed by page, which is 2,112 bytes. After Program load command (80h) is issued and the row and column address is given, the data will be loaded into the chip sequentially. Random Data Input command (85h) allows multiple data load in non-sequential address. After data load is complete, program confirm command (10h) is issued to start the page program operation. The page program operation in a block should start from the low address to high address.
Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Page Program is complete, the Write Status Bit (I/O0) may be checked (Figure 9). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.
During the Page Program progressing, only the read status register command and reset command are accepted, others are ignored.

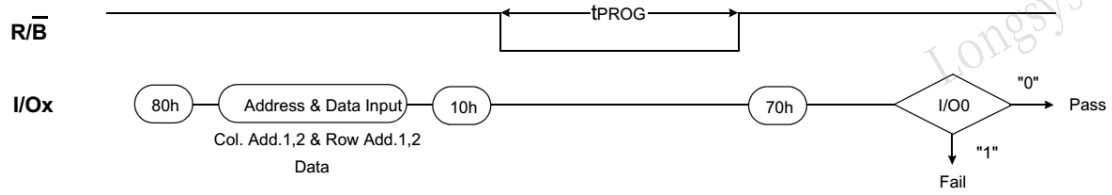


Figure 9 Page Program Sequence

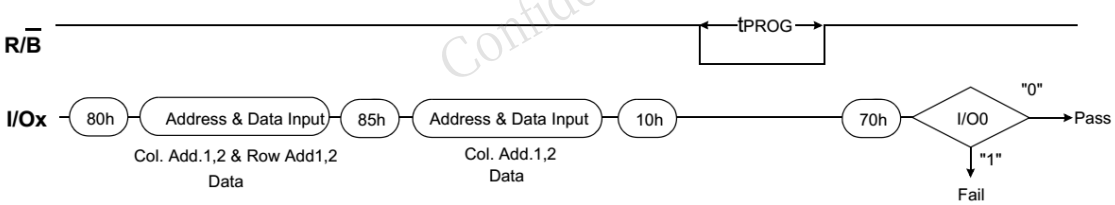


Figure 10 Program Operation with Random Data Input Sequence

2.6. Copy-Back Program Operation

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit(I/O6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O0) may be checked(Figure 11). The command register remains in Read Status command mode until another valid command is written to the command register.
During copy-back program, data modification is possible using random data input command (85h) as shown in Figure 11.

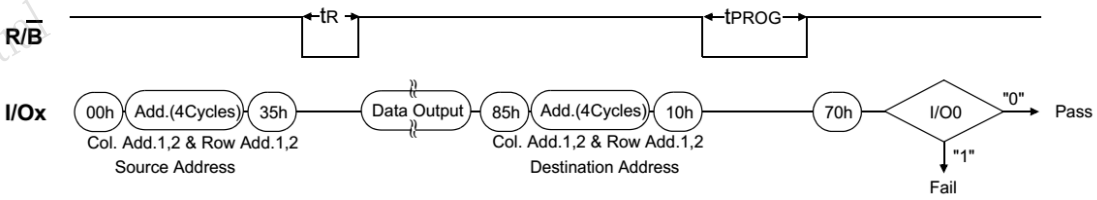


Figure 11 Copy-Back Program Sequence

NOTE :
Copy-Back Program operation is allowed only within the same memory plane.

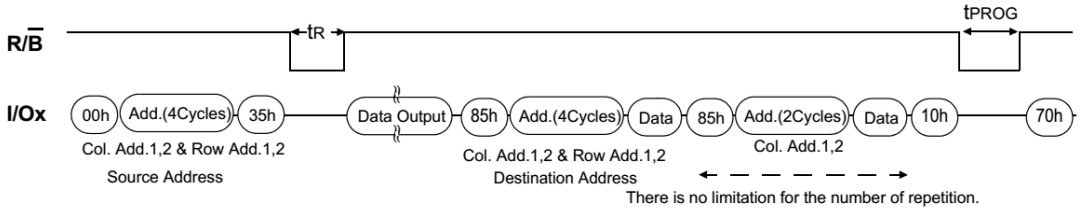


Figure 12 Copy-Back Program with Random Data Input Sequence

2.7. Block Erase Operation

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A18 to A27 is valid while A12 to A17 is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
The completion of the erase operation can be detected by R/B# pin or Status register bit (IO6). Recommend to check the status register bit IO0 after the erase operation completes.
During the erasing process, only the read status register command and reset command can be accepted,others are ignored.

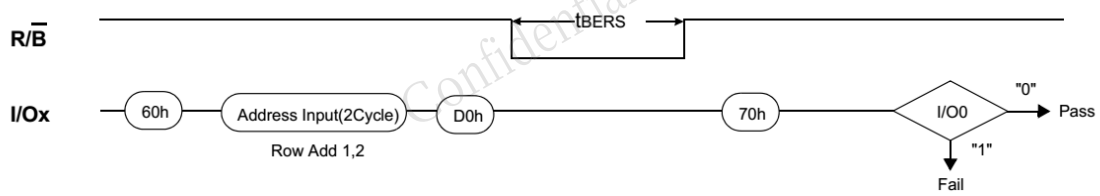


Figure 13 Block Erase Sequence

2.8. Read Status

The device provides a status register that outputs the device status by writing a command code 70h, and then the IO pins output the status at the falling edge of CE# or RE# which occurs last. Even though when multiple flash devices are connecting in system and the R/B# pins are common-wired, the two lines of CE# and RE# may be checked for individual devices status separately. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

[Table 9] Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Not use	Don't -cared
I/O 2	Not use	Not use	Not use	Don't -cared
I/O 3	Not use	Not use	Normal or uncorrectable / Recommended to rewrite	Chip Read Status Normal or uncorrectable : 0 Recommended to rewrite : 1
I/O 4	Not use	Not use	Not use	Don't -cared
I/O 5	Not use	Not use	Not use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :
I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

2.9. ECC Read Status

Using the ECC Read Status function, the Error Correction Status can be identified. ECC is performed on the NAND Flash main and spare areas.
The ECC Read Status function also shows the number of errors in a sector as identified from a ECC check during a read operation.

[Table 10] ECC Status Bytes

I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Sector Information				ECC Status			

[Table 11] ECC Status

I/O3 to I/O0	ECC Status
0000	No Error
0001	1bit error (Correctable)
0010	2bit error (Correctable)
0011	3bit error (Correctable)
0100	4bit error (Correctable)
Others	Reserve

[Table 12]Sector Information

I/O7 to I/O4	Sector Information
0000	1st Sector (Main and Spare area)
0001	2nd Sector (Main and Spare area)
0010	3rd Sector (Main and Spare area)
0011	4th Sector (Main and Spare area)
Others	Reserved

2.10. ECC Sector Information

ECC is generated by internal ECC logic during program operation.
During Read operation, the device automatically executes ECC. After read operation is executed, read status command can be issued to identify the read status the read status remains unmodified until other valid commands are executed.

[Table 13] 2KByte Page Assignment

1'st Main	2'nd Main	3'rd Main	4'th Main	1'st Spare	2'nd Spare	3'rd Spare	4'th Spare
512B	512B	512B	512B	16B	16B	16B	16B

[Table 14]Definition of 528Byte Sector

Sector	Column Address (Byte)	
	Main Field	Spare Field
1'st Sector	0 ~ 511	2,048 ~ 2,063
2'nd Sector	512 ~ 1,023	2,064 ~ 2,079
3'rd Sector	1,024 ~ 1,535	2,080 ~ 2,095
4'th Sector	1,536 ~ 2,047	2,096 ~ 2,111

NOTE :
The Internal ECC manages all data of Main area and Spare area.
A sector is the minimum unit for program operation and the number of program per page must not exceed 1.

2.11. Ready/Busy

The R/B# is an open-drain output pin and a pull-up resistor is necessary to add on the R/B# pin. The R/B# outputs the ready/busy status of read/program/ erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

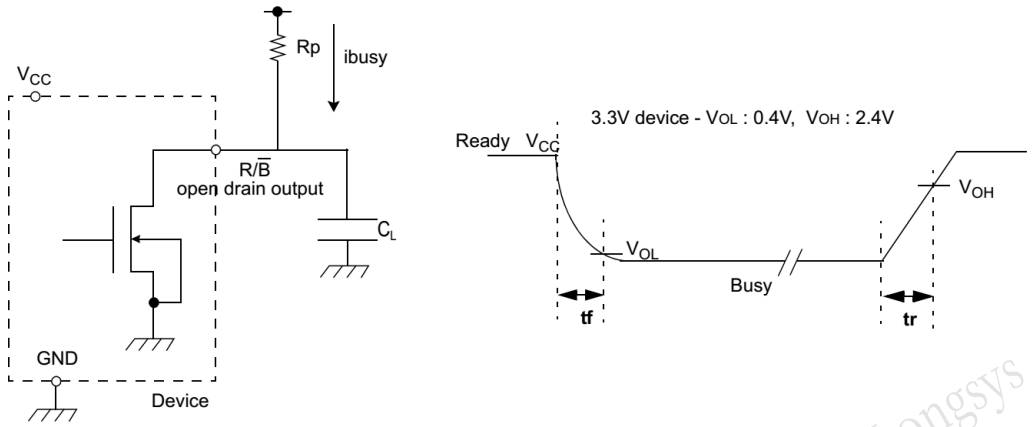


Figure 15 Rp vs tr, tf & Rp vs ibusy

Rp Value Guidence
The rise time of the R/B# signal depends on the combination of Rp and capacitive loading of the R/B# circuit.
It is approximately two times constants (Tc) between the 10% and 90% points on the R/B# waveform.
$T_C = R \times C$
Where R = Rp (Resistance of pull-up resistor), and C = C_L (Total capacitive load)
The fall time of the R/B# signal majorly depends on the output impedance of the R/B# signal and the total load capacitance.

$$\text{Rp (Min.)} = \frac{Vcc\ (Max.) - VOL\ (Max.)}{IOL + \Sigma IL}$$

Notes:
Considering of the variation of device-by-device, the above data is for reference to decide the resistor value.
Rp maximum value depends on the maximum permissible limit of tr.
IL is the total sum of the input currents of all devices tied to the R/B pin.

3. Electrical Characteristic

3.1. Valid Block

[Table 15] The Number of Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
FS33ND01GS1	NVB	1,004	-	1,024	Blocks

3.2. Recommended Operating Conditions

[Table 16] Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	VCC	2.7	3.3	3.6	V
Ground Supply Voltage	VSS	0	0	0	V

3.3. Absolute Maximum DC Ratings

[Table 17] Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	VCC	-0.6 to + 4.6	V
	VIN	-0.6 to + 4.6	
	VI/O	-0.6 to VCC + 0.3 (< 4.6V)	
Temperature Under Bias	TBIAS	-40 to +85	℃

NOTE :
Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet.
Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.4. DC Operating Characteristics

[Table 18] DC & Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Access Operation Current	ICC1	tRC=25ns CE#=VIL, IOUT=0mA	-	15	30	mA
Program Operation Current	ICC2	-	-			
Erase Operation Current	ICC3	-	-			
Stand-by Current (TTL)	ISB1	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)	ISB2	CE#=VCC-0.2, WP#=0V/VCC	-	10	70	µA
Input Leakage Current	ILI	VIN=0 to VCC(max)	-	-	±10	
Output Leakage Current	ILO	VOUT=0 to VCC(max)	-	-	±10	
Input High Voltage	VIH1)	-	0.8xVCC	-	VCC+0.3	V
Input Low Voltage, All inputs	VIL1)	-	-0.3	-	0.2xVCC	
Output High Voltage Level	VOH	IOH=-400µA	2.4	-	-	
Output Low Voltage Level	VOL	IOL=2.1mA	-	-	0.4	
Output Low Current (R/B#)	IOL(R/B#)	VOL=0.4V	8	10	-	mA

NOTE :
VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20ns or less.
Typical value is measured at VCC=3.3V, TA=25℃. Not 100% tested.

3.5. Input / Output Capacitance (TA=25℃, VCC=3.3V, f=1.0Mhz)

[Table 19] Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	pF

NOTE :
Capacitance is periodically sampled and not 100% tested.

3.6. Read / Program / Erase Characteristics

[Table 20] NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	tR	-		25	µs
Program Time	tPROG	-	400	900	µs
Number of Partial Program Cycles	Nop	-	-	1	cycles
Block Erase Time	tBERS	-	4.5	16	ms

NOTE :
Typical value is measured at VCC=3.3V, T_A=25℃. Not 100% tested.
Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V VCC and 25℃ temperature.

3.7. AC Timing Parameters Table

[Table 21] AC Timing Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS[1)]	12	-	ns
CLE Hold Time	tCLH	5	-	ns
CE# Setup Time	tCS[1)]	20	-	ns
CE# Hold Time	tCH	5	-	ns
WE# Pulse Width	tWP	12	-	ns
ALE Setup Time	tALS[1)]	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time	tDS[1)]	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
WE# High Hold Time	tWH	10	-	ns
Address to Data Loading Time	tADL[2)]	100	-	ns
ALE toRE# Delay	tAR	10	-	ns
CLE to RE# Delay	tCLR	10	-	ns
Ready to RE# Low	tRR	20	-	ns
RE# Pulse Width	tRP	12	-	ns
WE# High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	25	-	ns
RE# Access Time	tREA	-	20	ns
CE# Access Time	tCEA	-	25	ns
RE# High to Output Hi-Z	tRHZ	-	100	ns
CE# High to Output Hi-Z	tCHZ	-	30	ns
CE# High to ALE or CLE Don't Care	tCSD	0	-	ns
RE# High to Output Hold	tRHOH	15	-	ns
Data Hold Time after CE# Disable	tCOH	15	-	ns
RE# High Hold Time	tREH	10	-	ns
Output Hi-Z to RE# Low	tIR	0	-	ns
RE# High to WE# Low	tRHW	100	-	ns
WE# High to RE# Low	tWHR	60	-	ns
Device Resetting Time (Read/Program/Erase)	tRST	-	5/10/500 [1)]	µs

NOTE :
1) The transition of the corresponding control pins must occur only once while WE# is held low.
2) t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.
3) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5µs.

4. NAND FLASH TECHNICAL NOTES

4.1. Initial Invalid Block(s)

The initial invalid blocks are included in the device while it gets shipped called. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. During the time of using the device, the additional invalid blocks might be increasing; therefore, it is recommended to check the invalid block marks and avoid using the invalid blocks. Furthermore, please read out the initial invalid block and the increased invalid block information before any erase operation since it may be cleared by any erase operation.

4.2. Identifying Initial Invalid Block(s)

While the device is shipped, the value of all data bytes of the good blocks are FFh. The initial invalid block(s) status is defined by the 1st byte in the spare area. Longsys makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048.
Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart (Figure 16). The erase operation at the invalid block is not recommended.

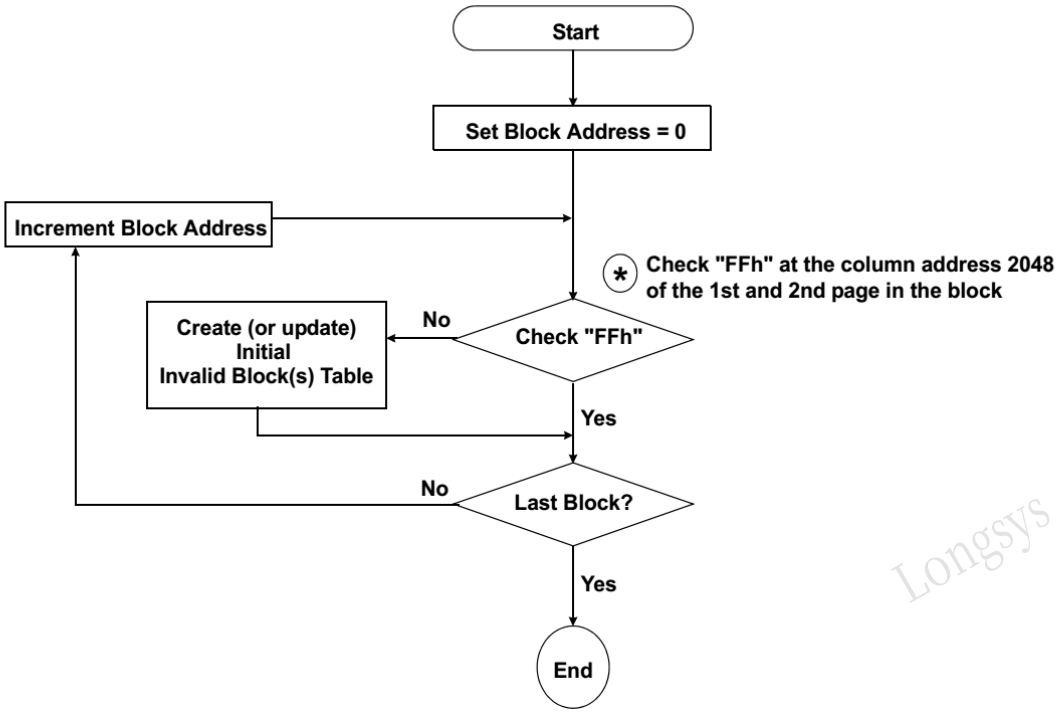


Figure 16 Flow Chart to Create Initial Invalid Block Table

4.3. Error in Write or Read Operation

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system.Block replacement should be done while status read failure after erase or program. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

[Table 22] Failure Cases

	Failure Mode	Detection and Countermeasure Sequence
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

ECC:

Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

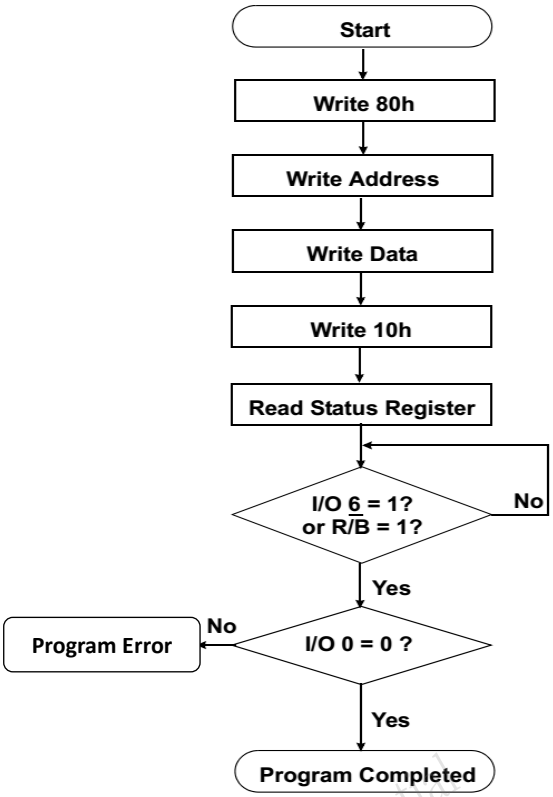
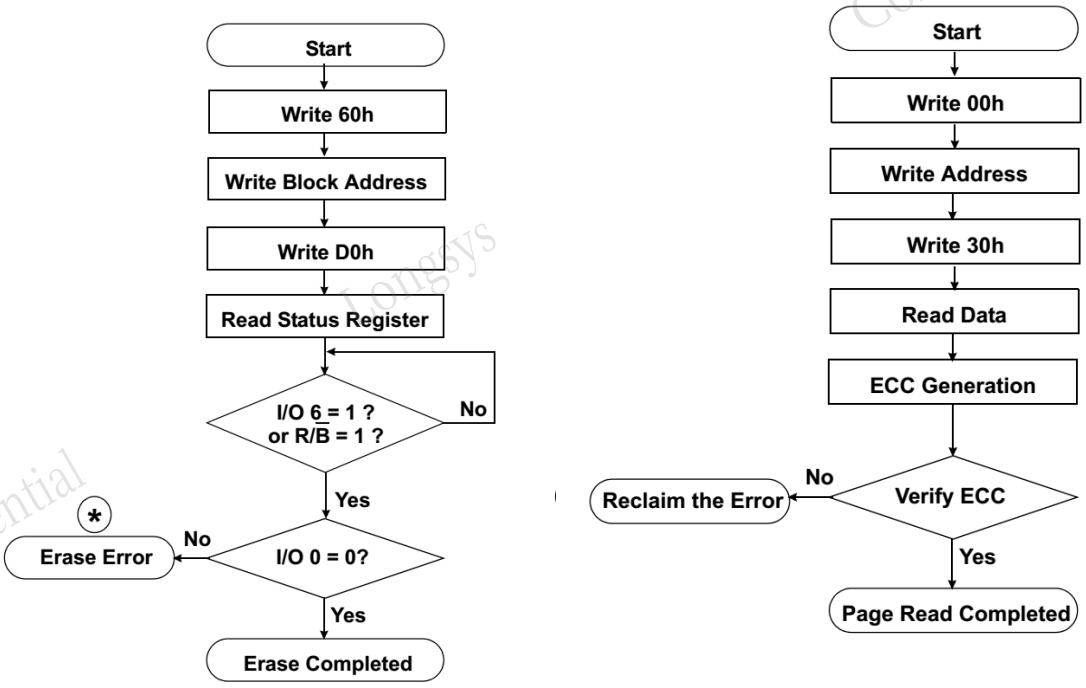


Figure 17 Program Flow Chart

If program operation results in an error, map out the block including the page in error and copy the target data to another block.



*If erase operation results in an error, map out the failing block and replace it with another block.

Figure 18 Erase Flow Chart& Read Flow Chart

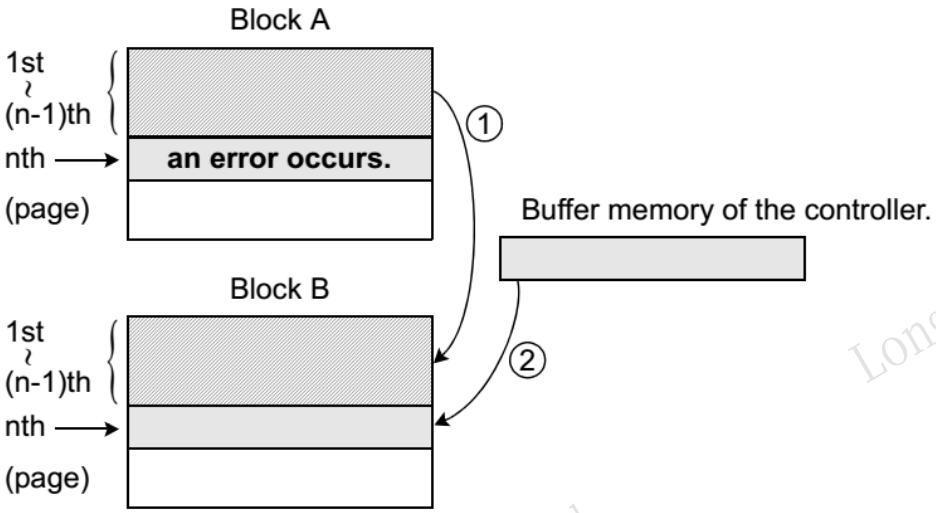


Figure 19 Block Replacement

1.When an error happens in the nth page of the Block 'A' during erase or program operation.
2.Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block'B')
3. Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block'B'.
4. Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

4.4. Addressing for Program Operation

Within a block, The page program operation in a block should start from the low address to high address. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.

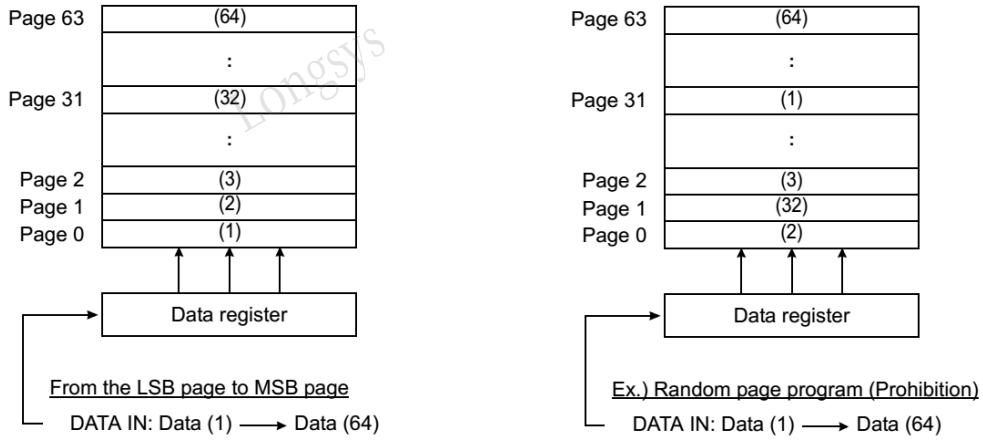


Figure 20

[Table 23]Address Information

Device	I/O	DATA	ADDRESS			
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2
FS30ND01GS108BF10	$I/O_0 \sim I/O_7$	2112Byte	A0~A7	A8~A11	A12~A19	A20~A27
FS30ND01GS108BF10	$I/O_0 \sim I/O_7$	2112Byte	A0~A7	A8~A11	A12~A19	A20~A27

4.5. System Interface Using CE# Don't-Care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 2,112 byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ-seconds, deactivating CE# during the data-loading and serial access would provide significant savings in power consumption.

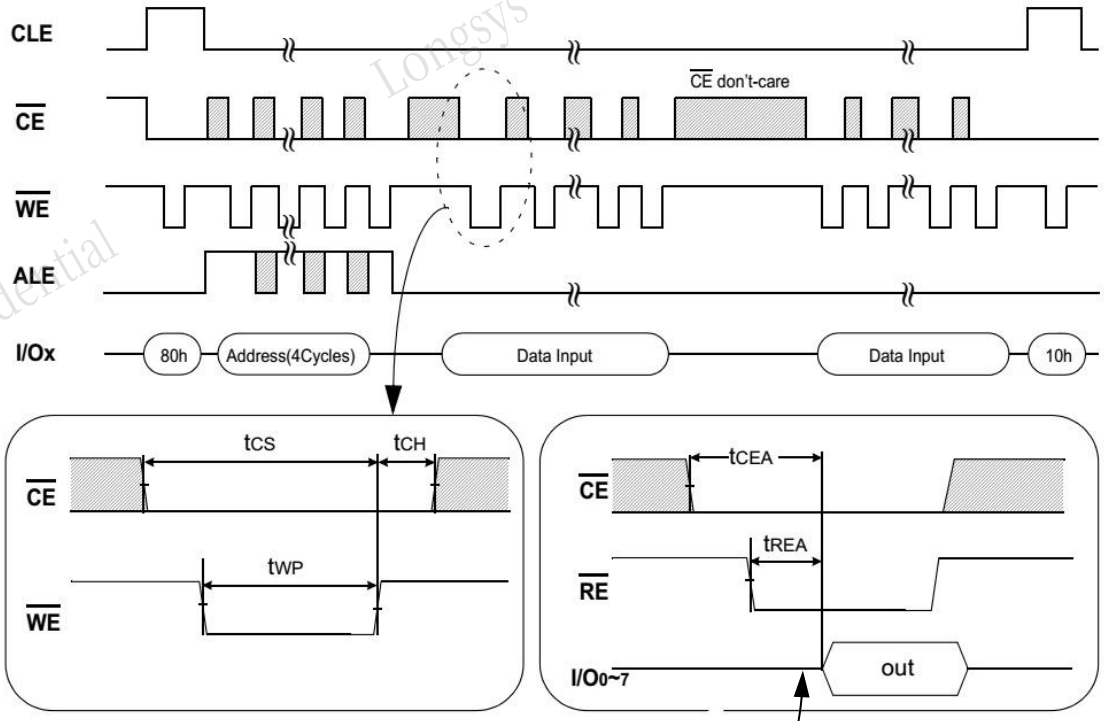


Figure 21 Program Operation with CE# don't-care

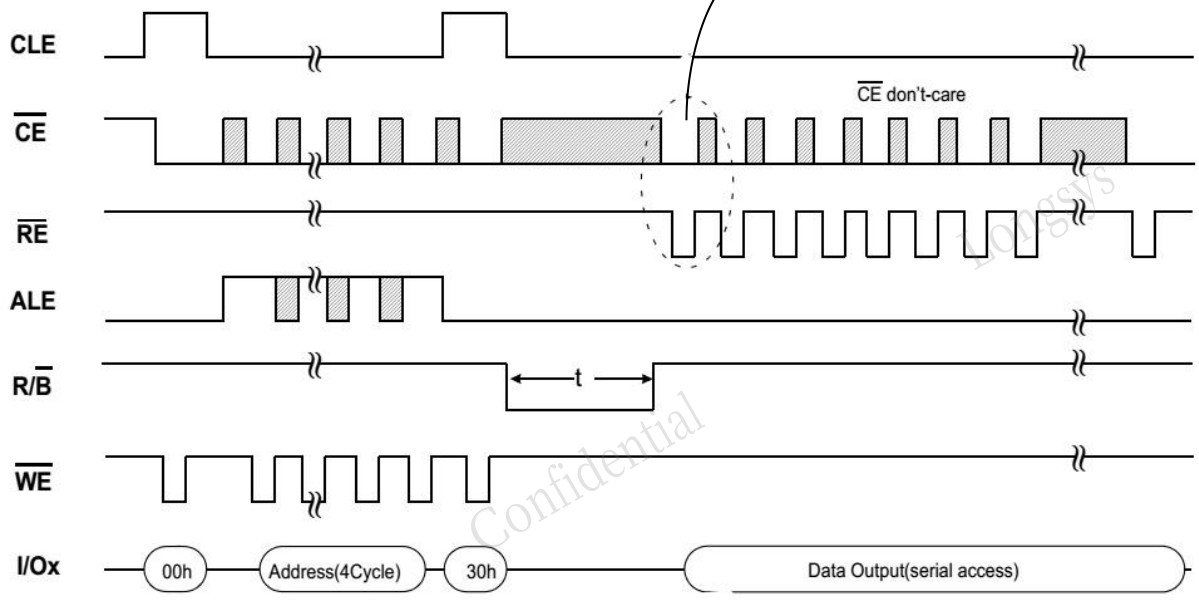


Figure 22 Read Operation with CE# don't-care

5. Timing

5.1. Data Protection & Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 2V(3.3V device). WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences as shown in Figure 23. The two step command sequence for program/erase provides additional software protection.

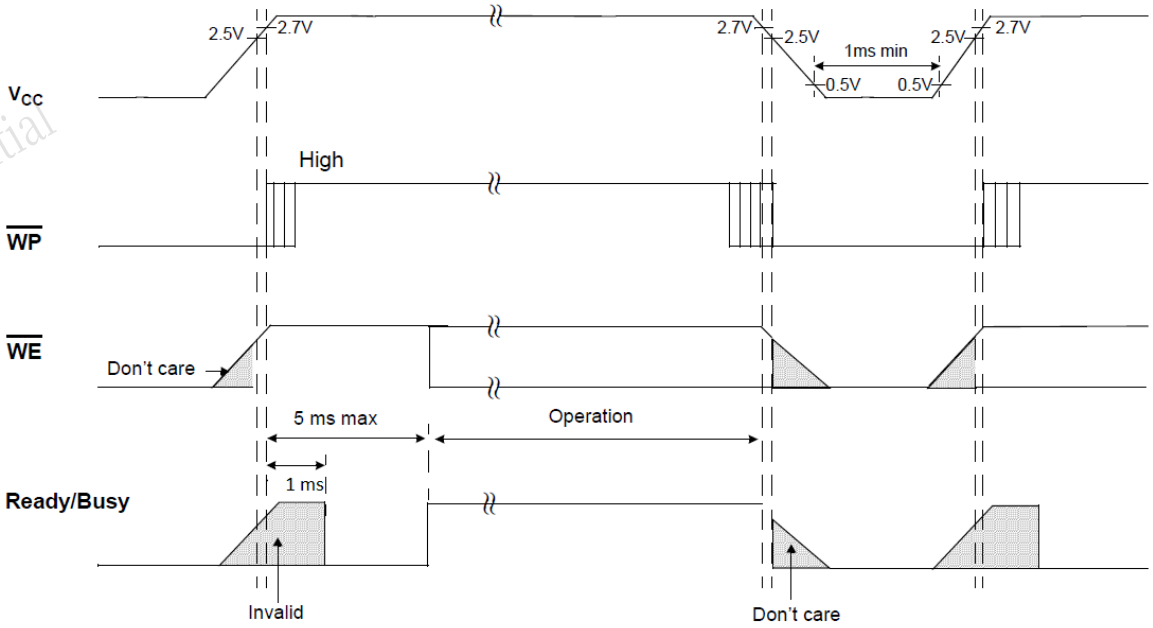


Figure 23 AC Waveforms for Power Transition

NOTE :
1) During the initialization, the device consumes a maximum current of 30mA (ICC1).
2) Once Vcc drops under 2.5V, Vcc is recommended that it should be driven down to 0.5V and stay low under 0.5V for at least 1ms before Vcc power up.

5.2. Mode Selection

[Table 24]Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(4cycles)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(4cycles)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X[1)]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/VCC[2)]	Stand-by	

NOTE :
1) X can be VIL or VIH.
2) WP should be biased to CMOS high or CMOS low for standby.

5.3. Command Latch Cycle

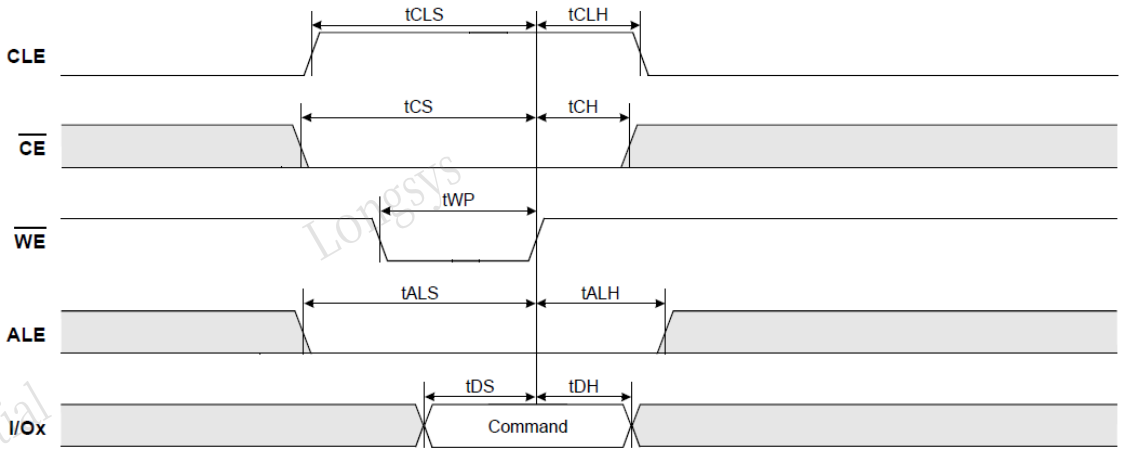


Figure 24 Command Latch Cycle

5.4. Address Latch Cycle

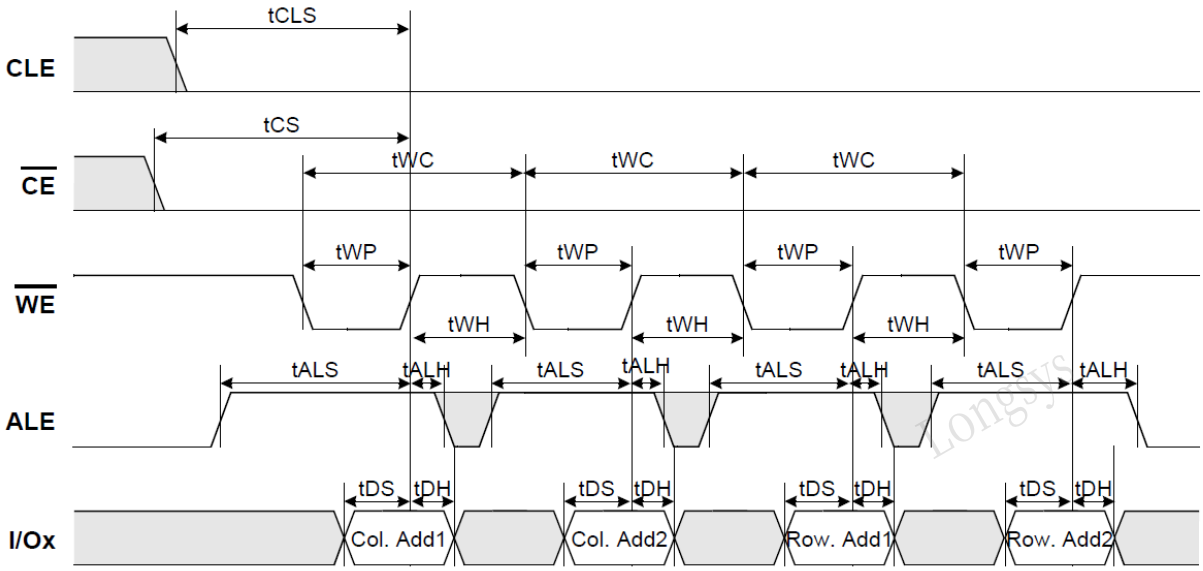


Figure 25 Address Latch Cycle

5.5. Input Data Latch Cycle

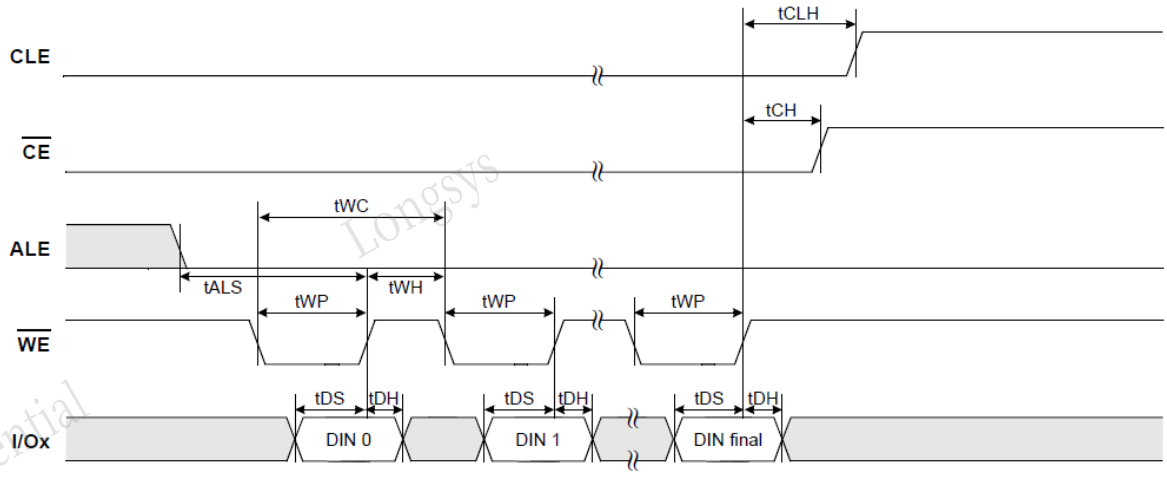


Figure 26 Input Data Latch Cycle

5.6. Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

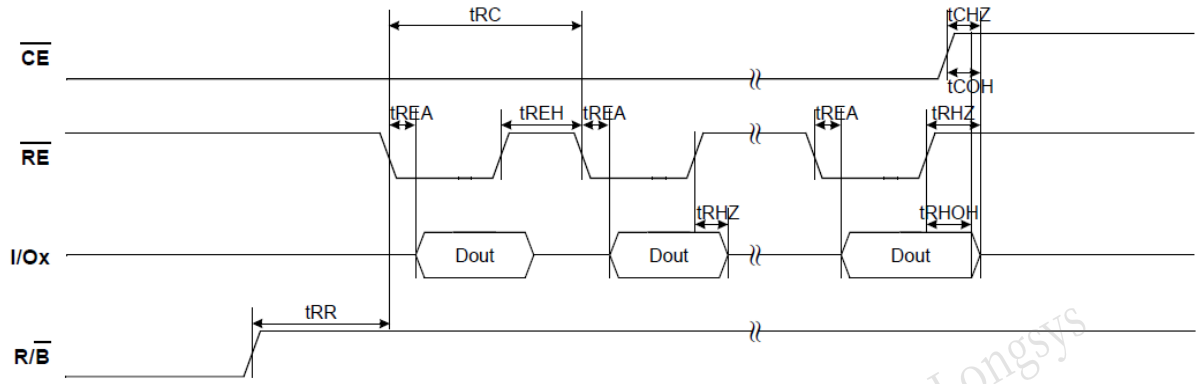


Figure 27 Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

NOTE :
1) Transition is measured at 200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
2) tRHOH starts to be valid when frequency is lower than 20Mhz.

5.7. Read Status Cycle

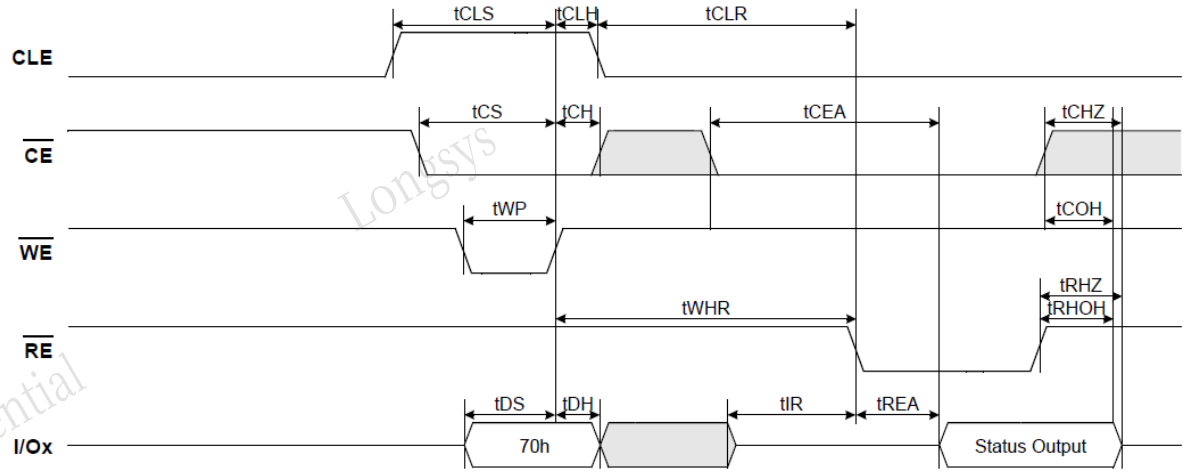


Figure 28 Read Status Cycle

5.8. ECC Read Status Cycle

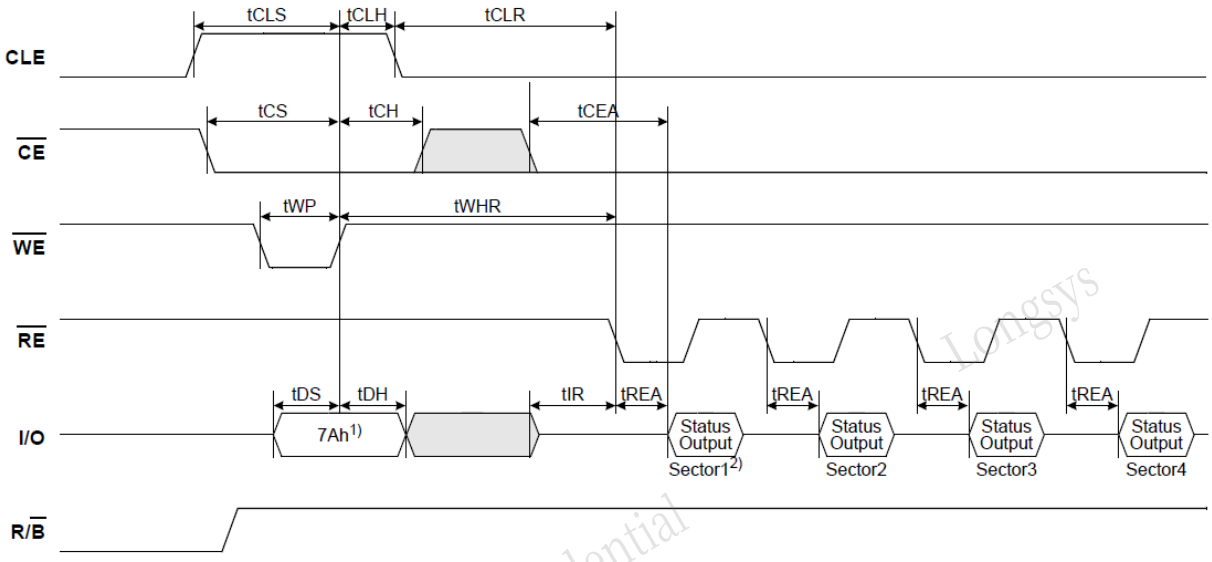


Figure 29 ECC Read Status Cycle

NOTE :
1) ECC Read Status output should include all 4 sector information.

5.9. Read Operation

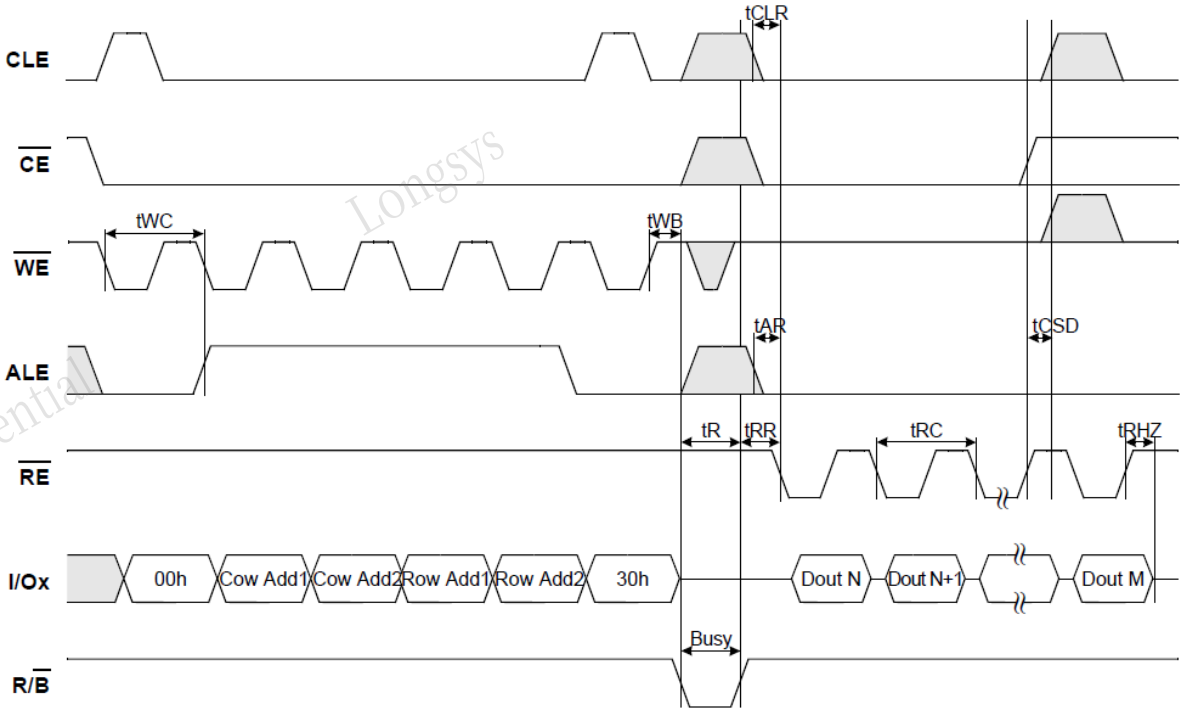


Figure 30 Read Operation

5.10. Page Program Operation

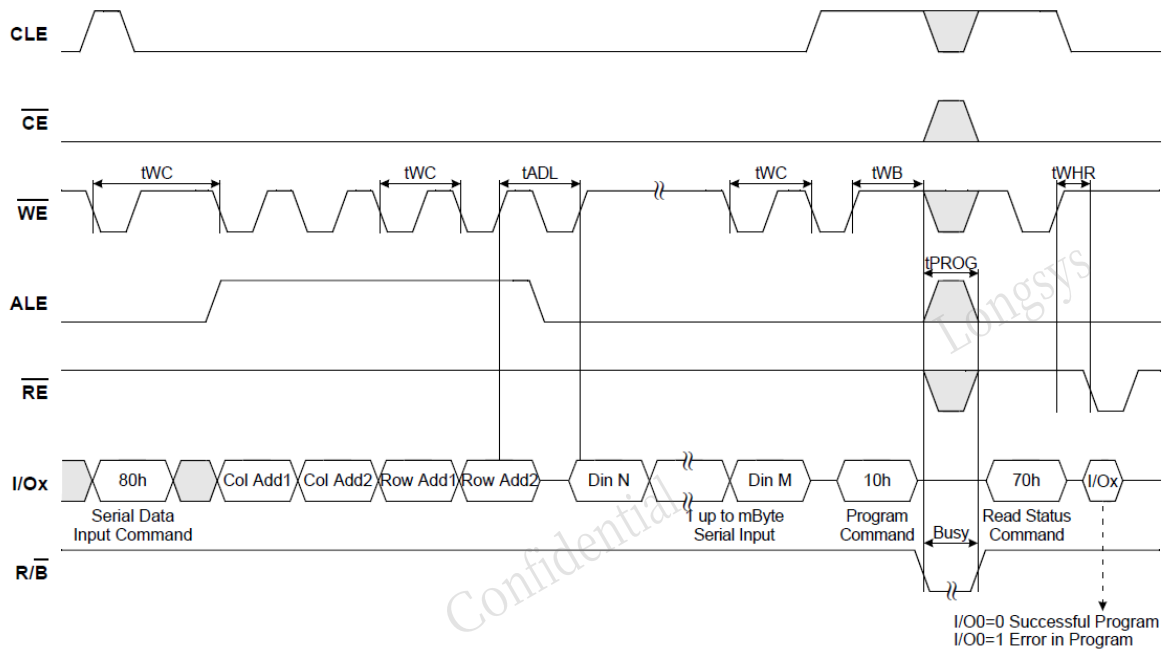


Figure 31 Page Program Operation

NOTE :
tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

5.11. Read Operation (Intercepted by CE#)

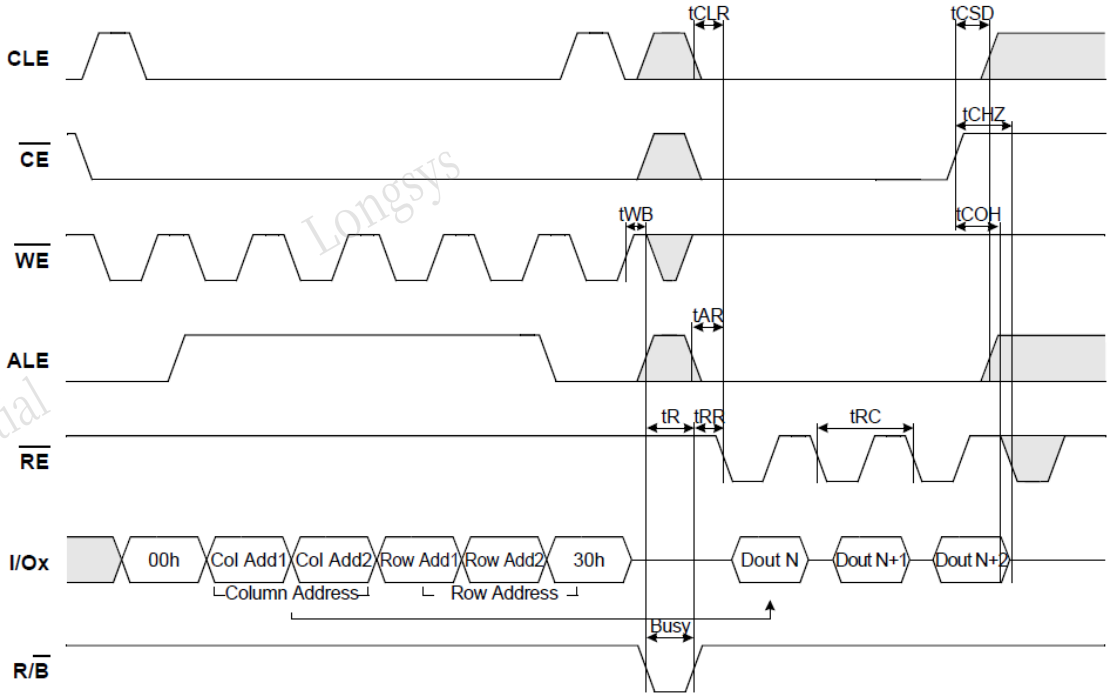


Figure 32 Read Operation (Intercepted by CE#)

5.12. Random Data Output In a Page Operation

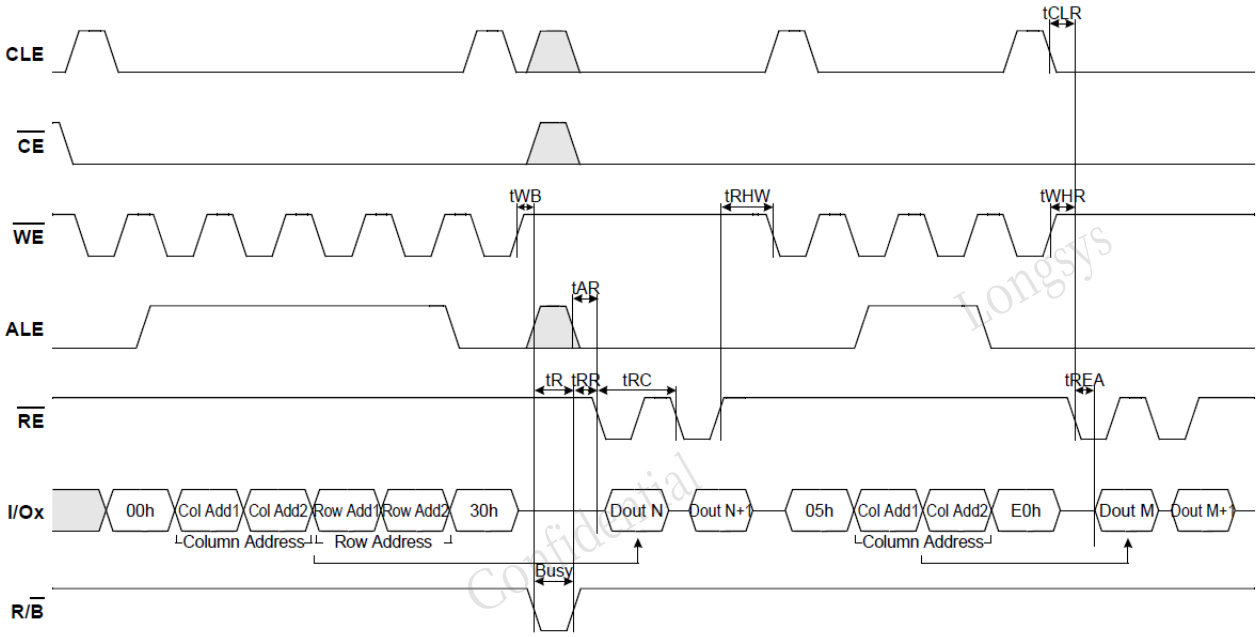


Figure 33 Random Data Output In a Page Operation

5.13. Page Program Operation with Random Data Input Operation

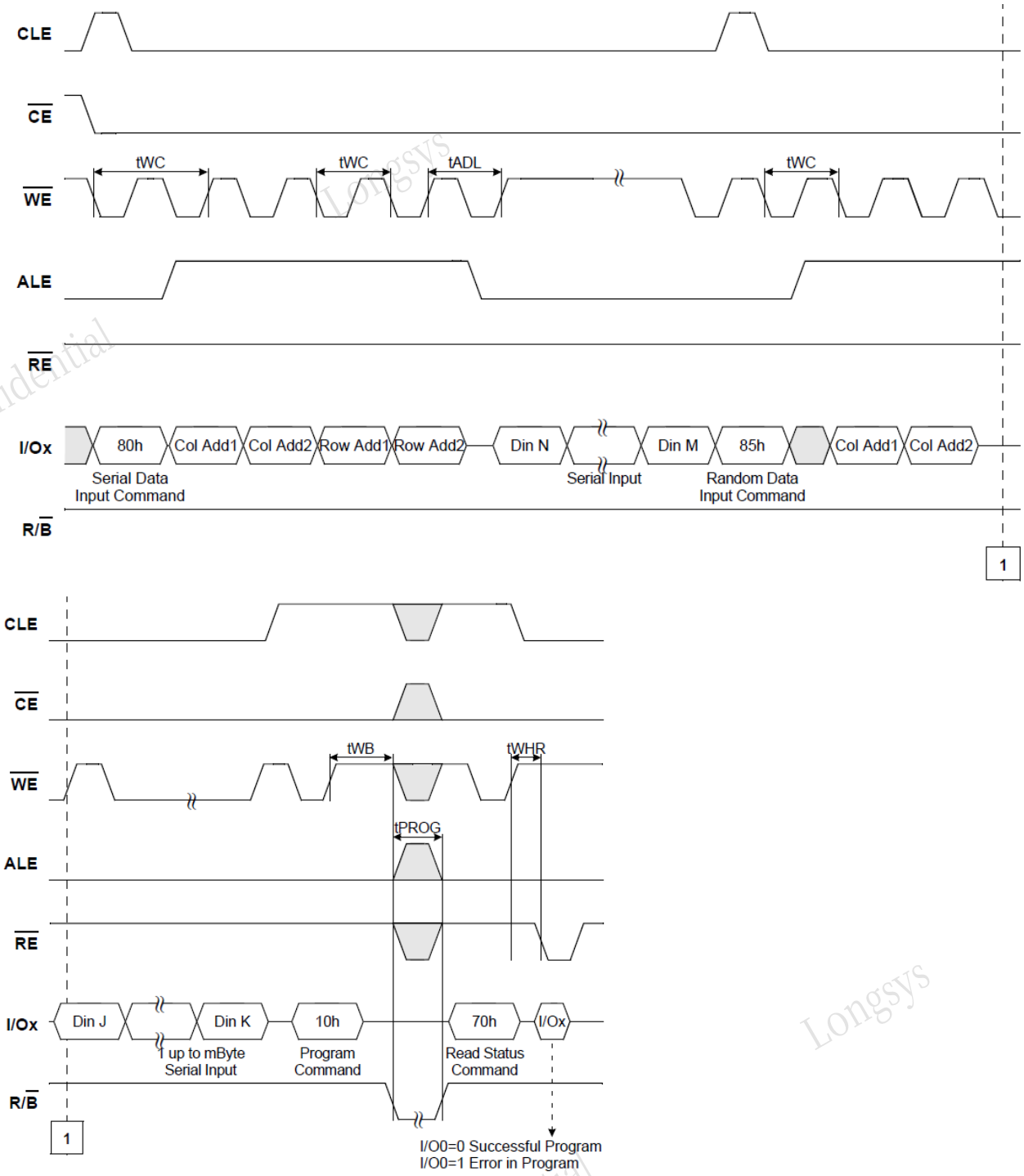


Figure 34 Page Program Operation with Random Data Input Operation

5.14. Copy-Back Program Operation

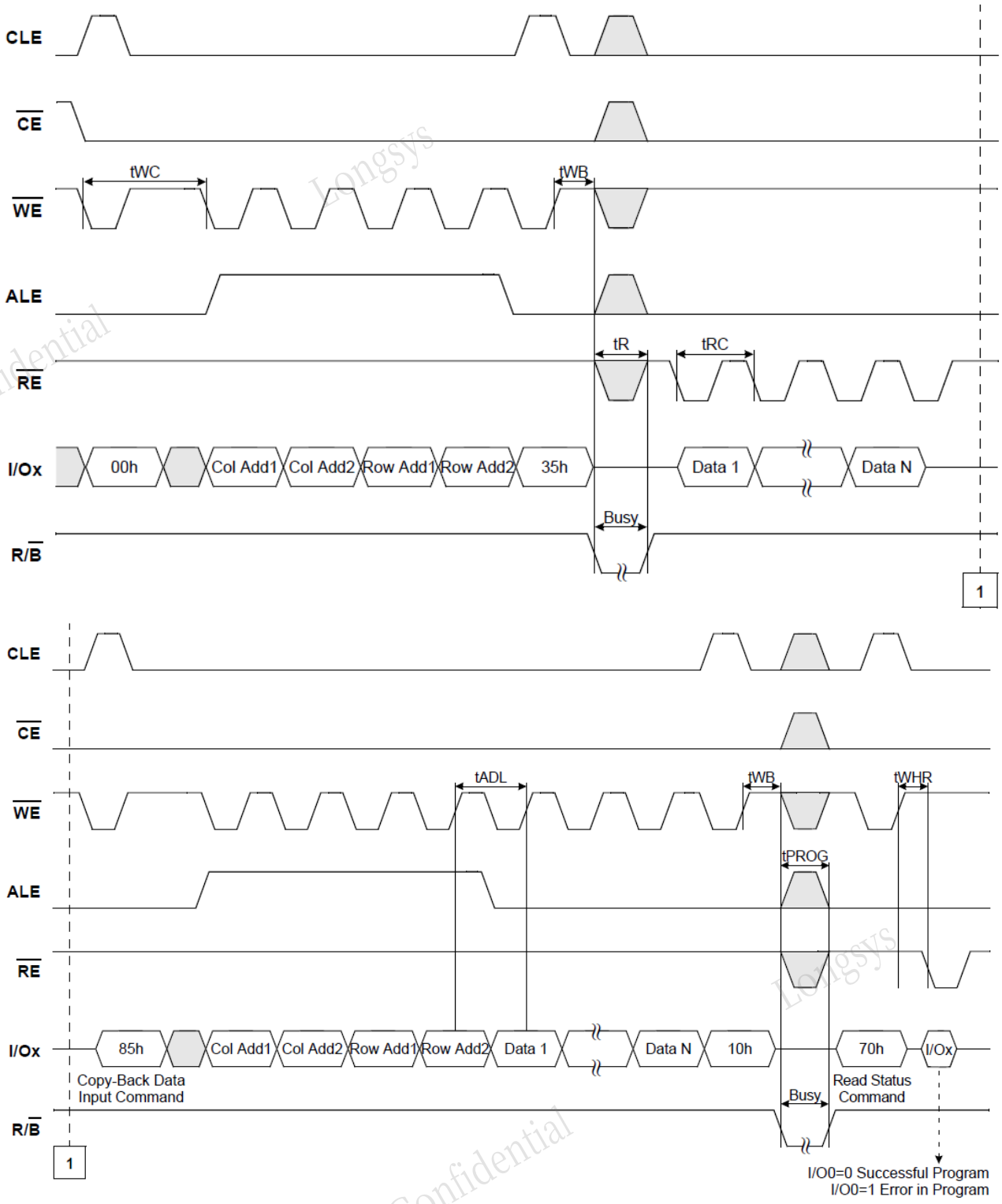


Figure 35 Copy-Back Program Operation

5.15. Copy-Back Program Operation with Random Data Input Operation

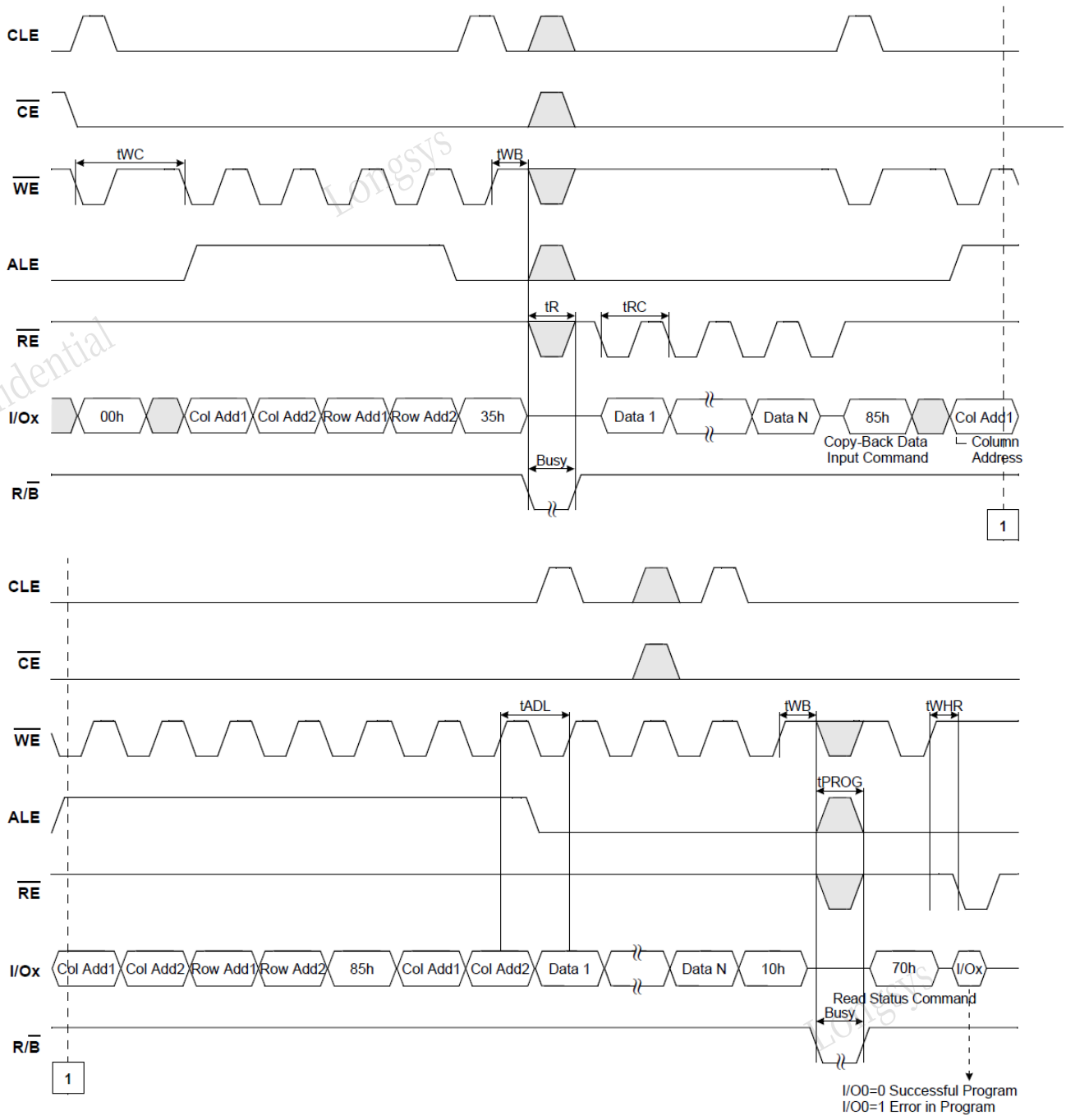


Figure 36 Copy-Back Program Operation with Random Data Input Operation

NOTE :
1) tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.
2)Copy-Back Program operation is allowed only within the same memory plane.

5.16. Block Erase Operation

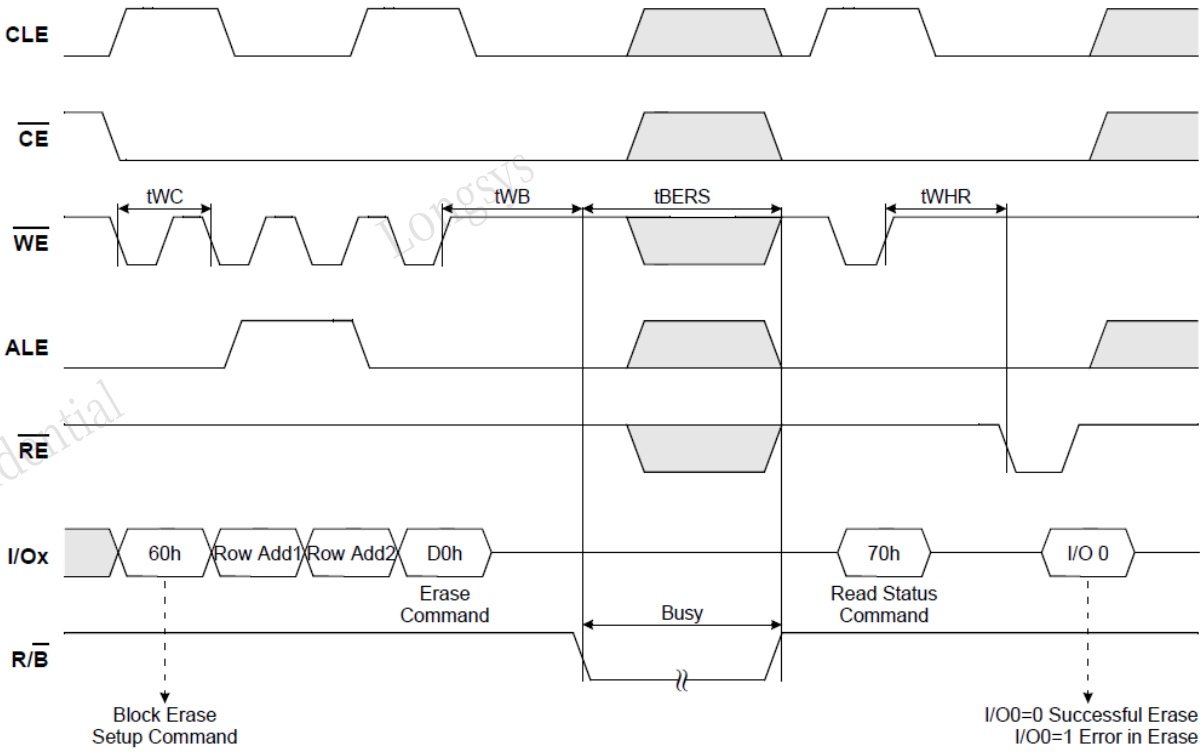


Figure 37 Block Erase Operation

5.17. Read ID Operation

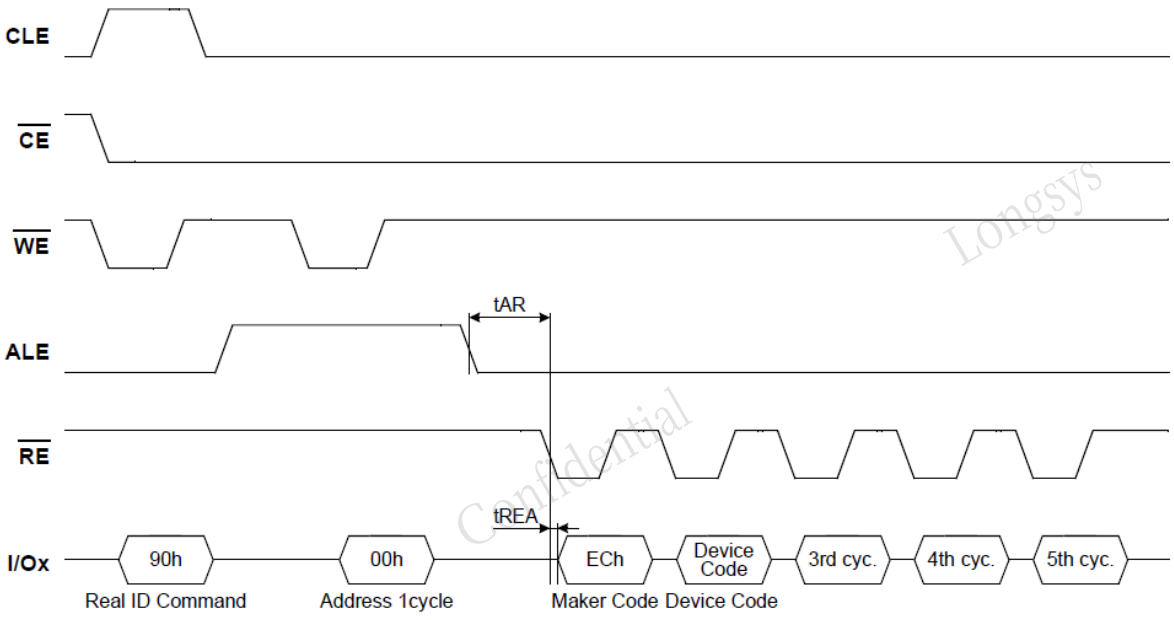


Figure 38 Read ID Operation

6. Physical Diagram

6.1. 48-Pin Thin Small Outline Package(TSOP)

Unit :mm/Inch

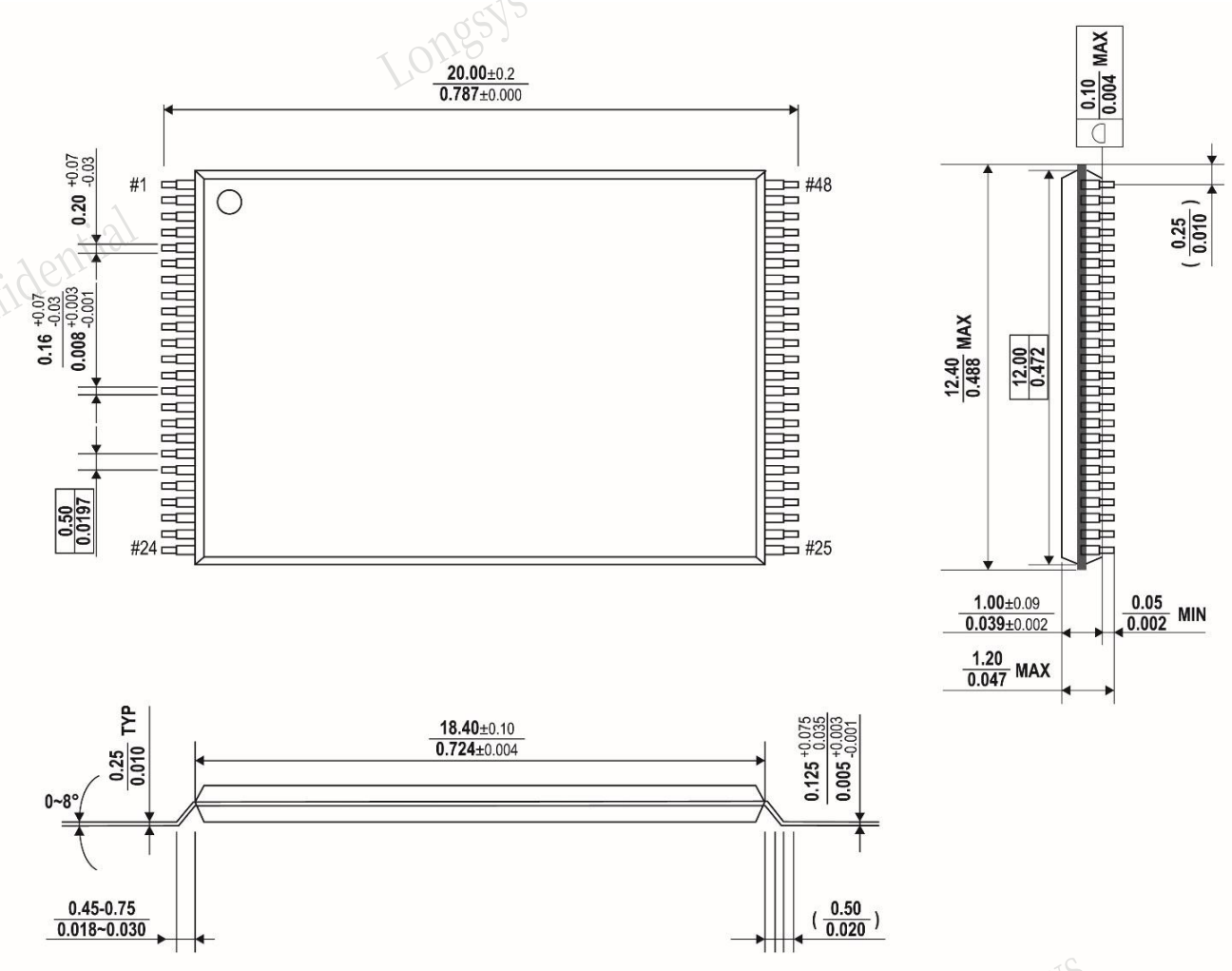


Figure 39 48-Pin Thin Small Outline Package

6.2. 63-Pin Ball Grid Array (BGA)

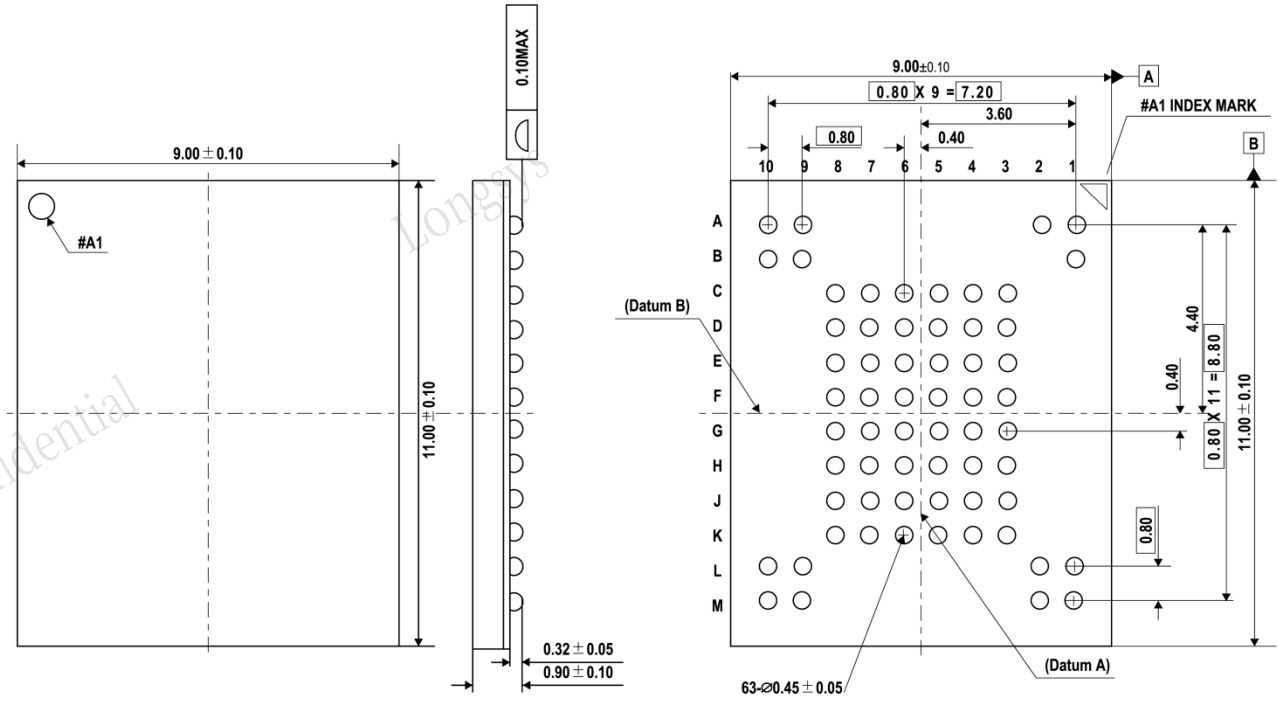


Figure 40 63-Pin Ball Grid Array

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