FORESEE®

2Gbit SLC NAND Flash

FSNS8A002G

Datasheet

LM-00008

Rev 1.2

Revision History

Rev.	Date	Changes	Editor
1.0	2021/01/15	1. Initial release.	Alex
1.1	2021/11/08	1. Revise descriptions in 4, 10.1, 10.4, 12.5, 14.	Alex
1.2	2021/12/01	1. Add chapter 15.	Alex

Content

1 General Description

The FSNS8A002G is a 2G-bit (256Mx8bit) NAND Flash Memory with spare 64M-bit. The device operates on a single 3.3V VCC. A program operation can be performed in typical 350µs on the (2K+64) Byte page and an erase operation can be performed in typical 2ms on a (128K+4K) Byte block. Data in the page buffer can be read out at 25ns cycle time per Byte. The FSNS8A002G is an optimum solution for large nonvolatile storage applications such as solid-state file storage and other portable applications requiring non-volatility.

The FSNS8A002G supports the standard NAND flash memory interface using the multiplexed 8-bit bus to transfer data, addresses, and command instructions. The five control signals, CLE, ALE, CE#, RE# and WE# handle the bus interface protocol. Also, the device has two other signal pins, the WP# and the R/B# for monitoring the device status.

2 Features

Voltage Supply
- VCC: 2.7V ~ 3.6V

Organization
- Memory Cell Array: (256M + 8M) Byte
- Page Size: (2k + 64) Byte
- Block Size: 64 pages, (128k + 4k) Byte
- Plane Size: 1,024 Blocks

High Performance
- Random Read: 25µs
- Sequential Read: 25ns
- Page Program Time: 350µs (Typ.)
- Block Erase Time: 2ms (Typ.)

Low Power
- Standby: 10µA (Typ.)
- Read: 10mA (Typ.)
- Program/Erase: 15mA (Typ.)

Advanced Features
- Hardware WP# write protect
- Software block protect
- Unique ID
- One 2kB parameter page
- Sixty-two 2kB OTP Pages
- Promised golden block0

High Reliability
- Endurance: typical 100k cycles (1)
- Data Retention: 10 years (1)

Package
- 48-TSOP (20x12mm)
- 63-TFBGA (11x9mm)

Note:

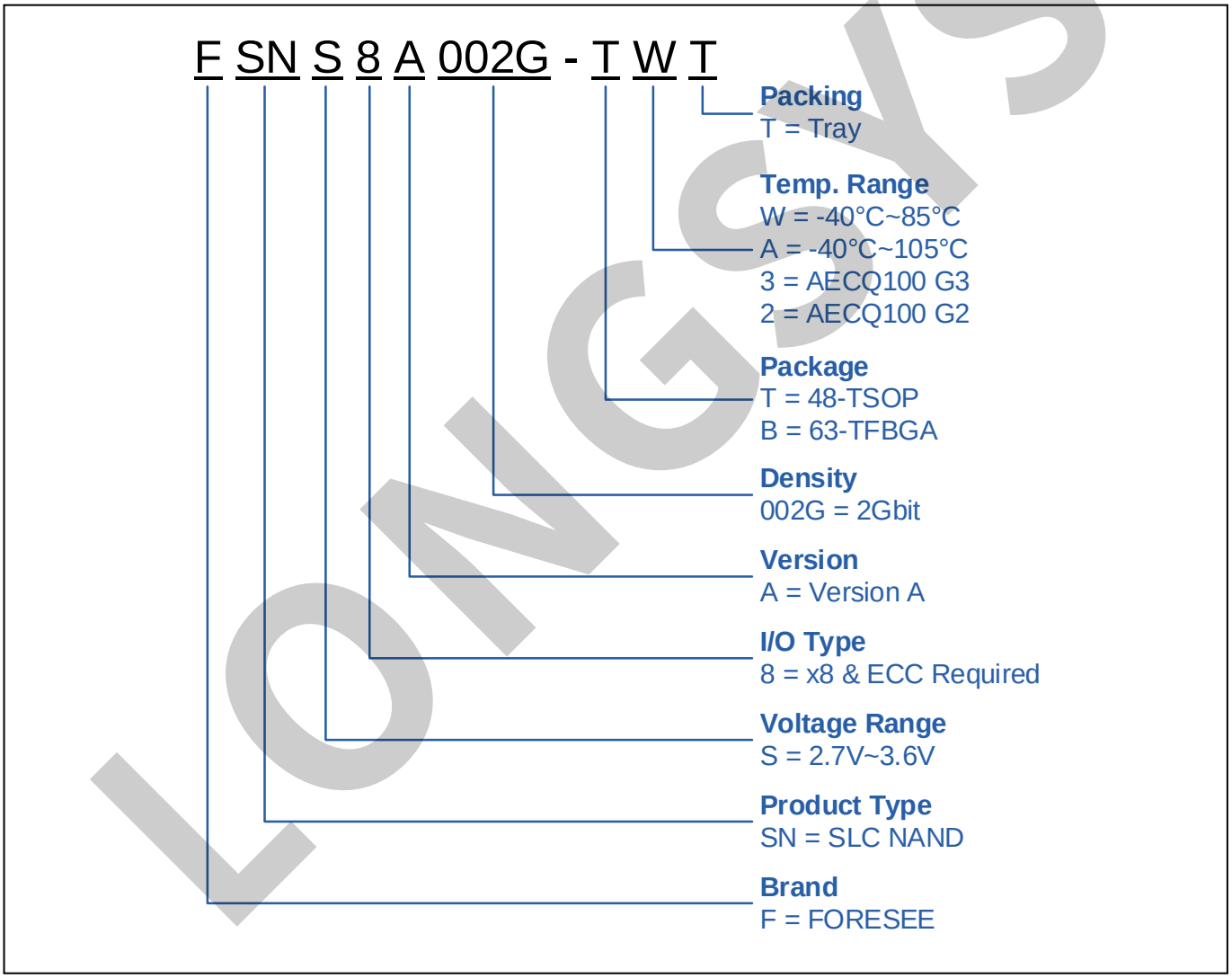
(1) Endurance and Data Retention specification is based on 1bit / 528Byte ECC

3 Product List

Table 1 Product List

Part Number	Density	I/O Type	Voltage Range	Package	Temp. Range	Packing
FSNS8A002G-TWT	2Gb	x8	2.7V ~ 3.6V	48-TSOP	-40°C ~ 85°C	Tray
FSNS8A002G-TAT	2Gb	x8	2.7V ~ 3.6V	48-TSOP	-40°C ~ 105°C	Tray
FSNS8A002G-BWT	2Gb	x8	2.7V ~ 3.6V	63-TFBGA	-40°C ~ 85°C	Tray
FSNS8A002G-BAT	2Gb	x8	2.7V ~ 3.6V	63-TFBGA	-40°C ~ 105°C	Tray

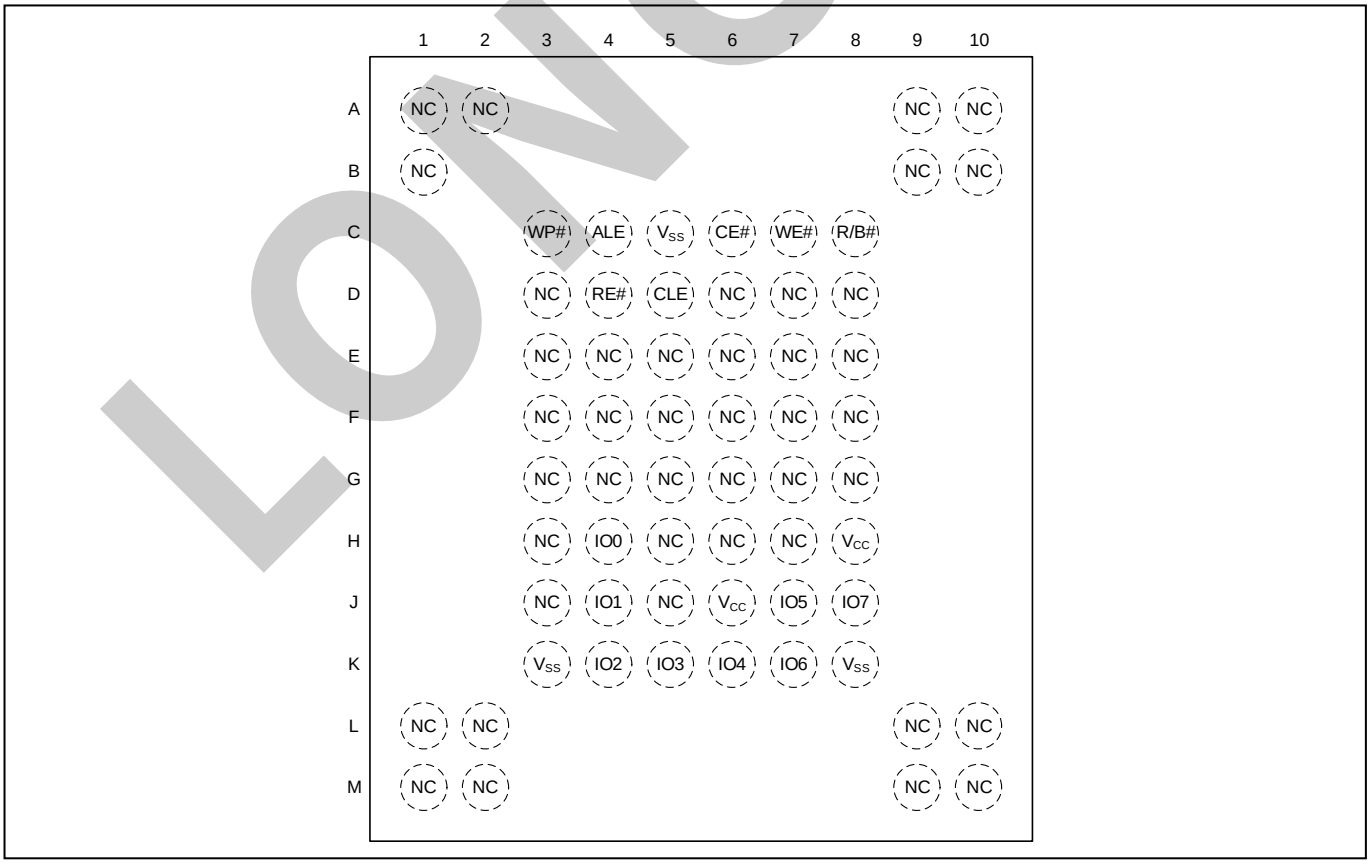
Figure 1 Marketing Part Numbering Chart



4 Package Types and Pin Configurations

Figure 2 Pin Configuration 48-TSOP

Figure 3 Pin Configuration 63-TFBGA



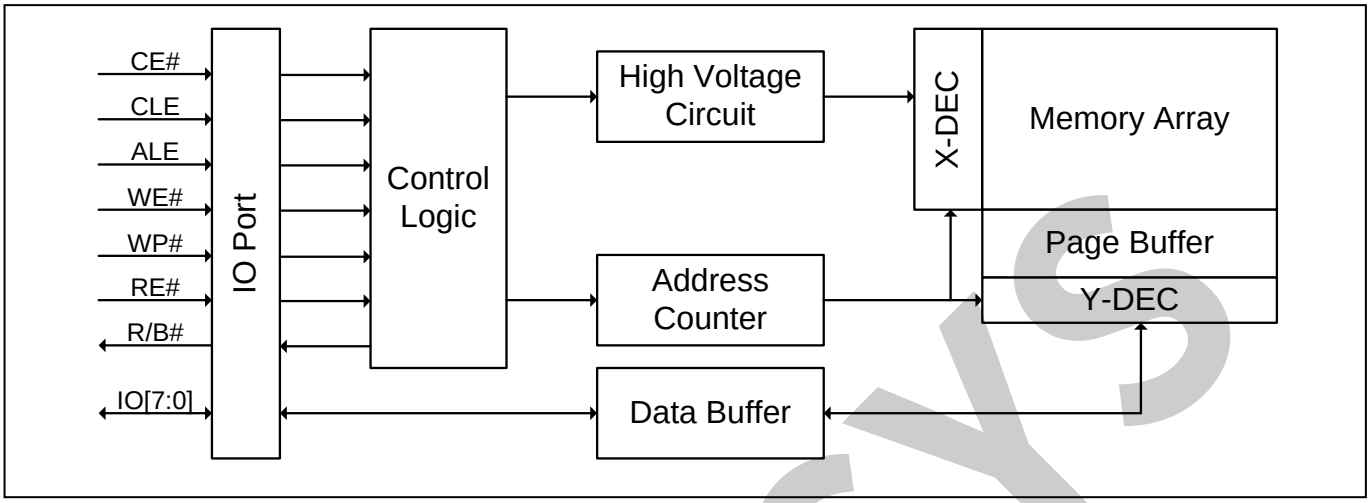
5 Pin Descriptions

Table 2 Pin Description

Pin Name	Pin Functions
CE#	**Chip Enable** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation.
RE#	**Read Enable** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WE#	**Write Enable** The WE# input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse.
CLE	**Command Latch Enable** The CLE input controls the activating path for commands sent to the command register. Commands are latched on the rising edge of WE# with CLE high.
ALE	**Address Latch Enable** The ALE input controls the activating path for address sent to the address registers. Addresses are latched on the rising edge of WE# with ALE high.
WP#	**Write Protect** The WP# input can be used to prevent the inadvertent program / erase to the device. All program / erase operations are disabled when WP# is active low.
R/B#	**Ready / Busy Output** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
IO7 - IO0	**Data Inputs / Outputs** The IO pins are used to input command, address and data and to output data during read operations. The IO pins float to high-z when the chip is deselected or when the outputs are disabled.
VSS	**Ground**
VCC	**Power Supply**
NC	**No Connection**

6 Block Diagram

Figure 4 Block Diagram



7 Array Organization and Mapping

Figure 5 Array Organization

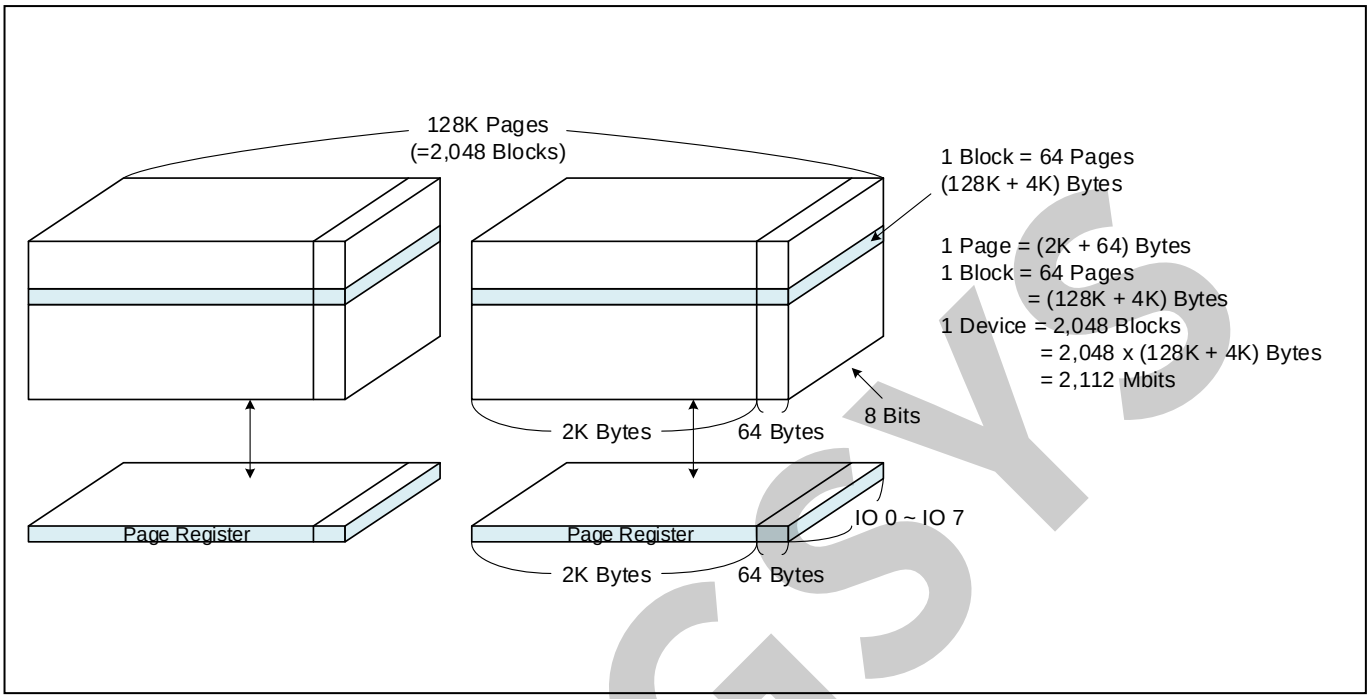


Table 3 Addressing

		IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Column Address	1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
	2nd cycle	L	L	L	A12	A11	A10	A9	A8
Row Address	3rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
	4th cycle	A27	A26	A25	A24	A23	A22	A21	A20
	5th cycle	L	L	L	L	L	L	L	A28

Note

(1) L: A low condition, which must be held during the address cycle to insure correct processing.

(2) A17~A12 are page addresses, A28~A18 are block addresses.

8 Mode Selection

Table 4 Mode Selection

Mode		CLE	ALE	CE#	WE#	RE#	WP#
Read	Command Input	H	L	L		H	X
	Address Input (5 cycles)	L	H	L		H	X
Write	Command Input	H	L	L		H	H
	Address Input (5 cycles)	L	H	L		H	H
Data Input		L	L	L		H	H
Data Output		L	L	L	H		X
During Read (Busy)		X	X	X	X	H	X
During Program (Busy)		X	X	X	X	X	H
During Erase (Busy)		X	X	X	X	X	H
Write Protect		X	X	X	X	X	L
Stand-by		X	X	H	X	X	0V / V_{CC}

Note

(1) “H” indicates a HIGH input level, “L” indicates a LOW input level, and “X” can be V_{IL} or V_{IH}.

9 Command Set

Table 5 Command Table

Command	1st Cycle	2nd Cycle	Acceptable While Busy
Reset	FFh	-	Yes
Page Read	00h	30h	
Random Data Output	05h	E0h	
Read Status	70h	-	Yes
Read ID	90h	-	
Read Parameter Page	ECh	-	
Read Unique ID	EDh	-	
Page Program	80h	10h	
Random Data Input	85h	-	
Copy Back Read	00h	35h	
Copy Back Program	85h	10h	
Block Erase	60h	D0h	
Get Feature	EEh	-	
Set Feature	EFh	-	

Note

(1) Random Data Input and Random Data Output command is only to be used within a page.

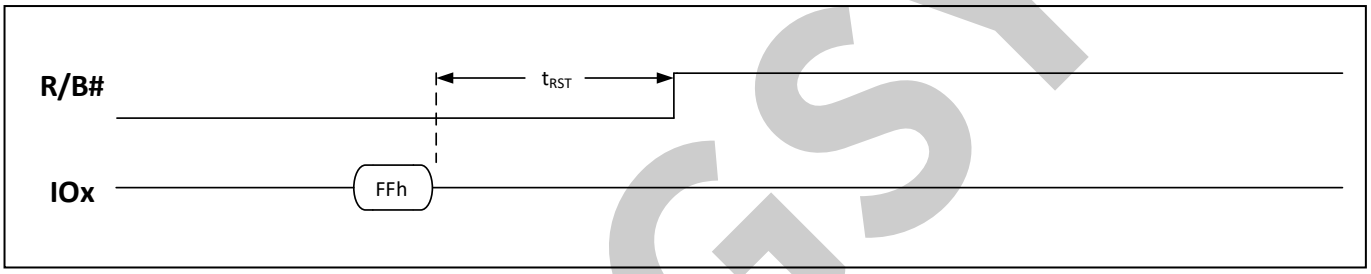
(2) Any commands not in the above table are considered as undefined and are prohibited as inputs.

10 Device Operation

10.1 Reset (FFh)

The device offers a reset operation, executed by writing FFh to the command register. When the device is in busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP# is high. If the device is already in reset state a new reset command will be accepted by the command register, and the device is reset instantly, but the R/B# pin will not change to low.

Figure 6 Reset Sequence



10.2 Read Operation

10.2.1 Page Read (00h-30h)

The FSNS8A002G array is accessed in page of 2,112 bytes. When the device powers on, 00h command is latched to command register. Therefore, system only issues five address cycles and 30h command for initial read from the device. This operation can also be entered by writing 00h command to the command register, and then write five address cycles, followed by writing 30h command. After writing 30h command, the data is transferred from NAND array to page buffer during t_R.

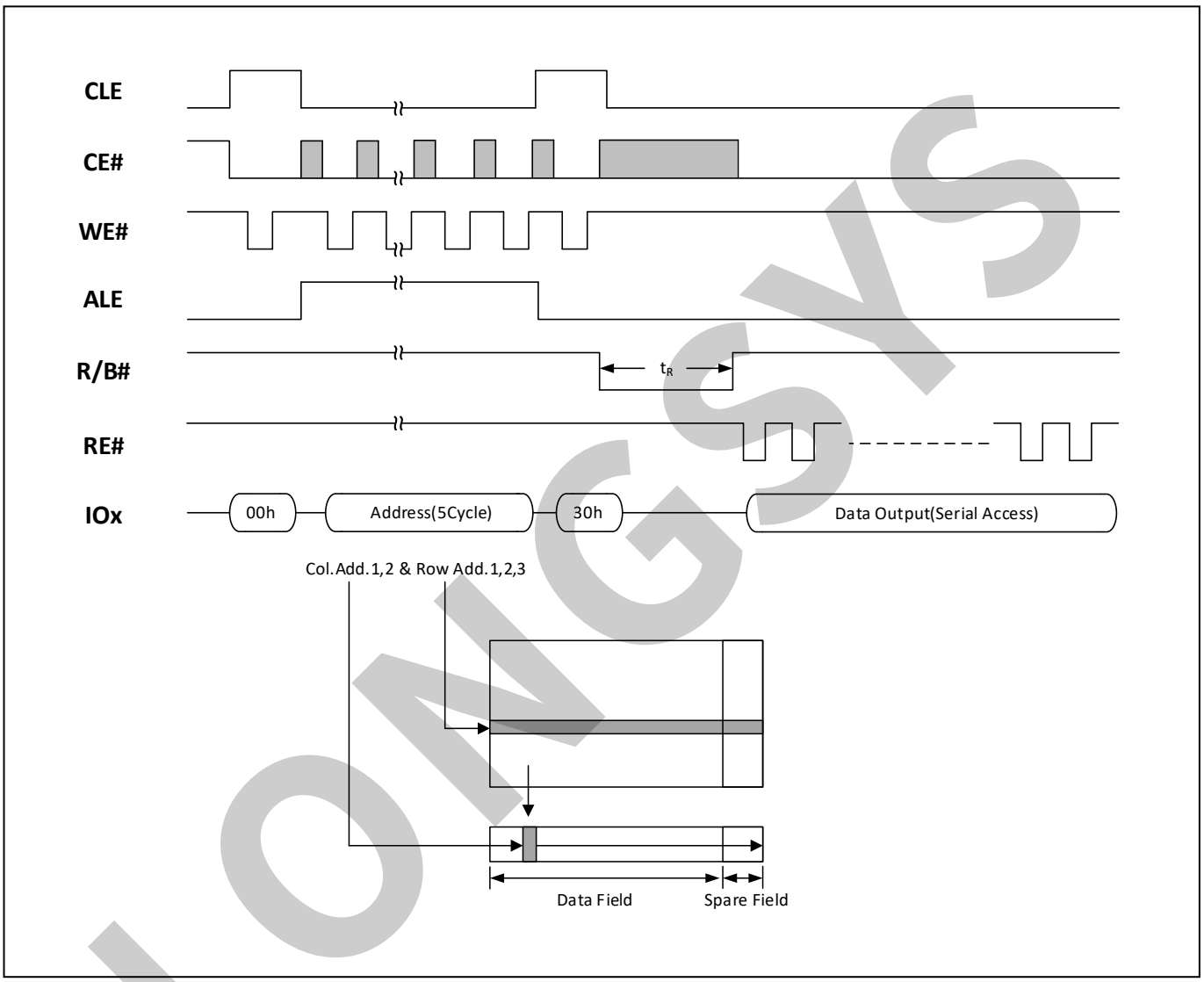
Data transfer progress can be done by monitoring the status of the R/B# signal output. R/B# signal will be LOW during data transfer. Also, there is an alternate method by using the Read Status command. If the Read Status command is issued during read operation, the Page Read command must be re-issued to read out the data from page buffer.

Once the data in a page is loaded into the page buffer, R/B# signal goes high, and the data can be read from Page buffer by toggling RE#. Read is sequential from initial column address to the end of the page.

If the host side uses a sequential access time (t_{RC}) of less than 30ns, the data can be latched on the next falling edge of RE# as the waveform of EDO mode.

The device may output random data in a page instead of the consecutive sequential data by writing Random Data Output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

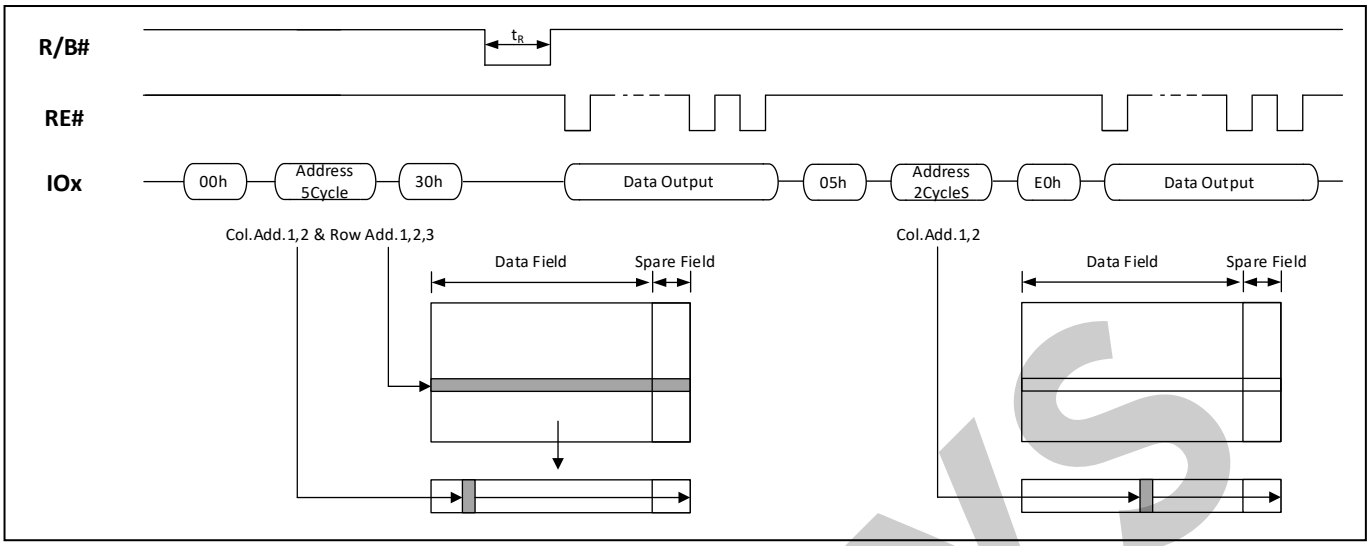
Figure 7 Page Read Sequence



10.2.2 Random Data Output (05h-E0h)

The Random Data Output command allows the selection of random column addresses to read out data from a single or multiple of addresses. The use of the Random Data Output command is available after the Page Read (00h-30h) sequence by writing the 05h command following by the two cycles column address and then the E0h command. Toggling RE# will output data sequentially. The Random Data Output command can be issued multiple times, but limited to the current loaded page.

Figure 8 Page Read with Random Data Output Sequence



10.2.3 Read Status (70h)

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to **Table 6** for specific Status Register definitions.

The command register remains in Read Status mode until another command is issued. Therefore, if the status register is read during a random read cycle, the Page Read command should be given before starting read cycles.

Figure 9 Read Status Sequence

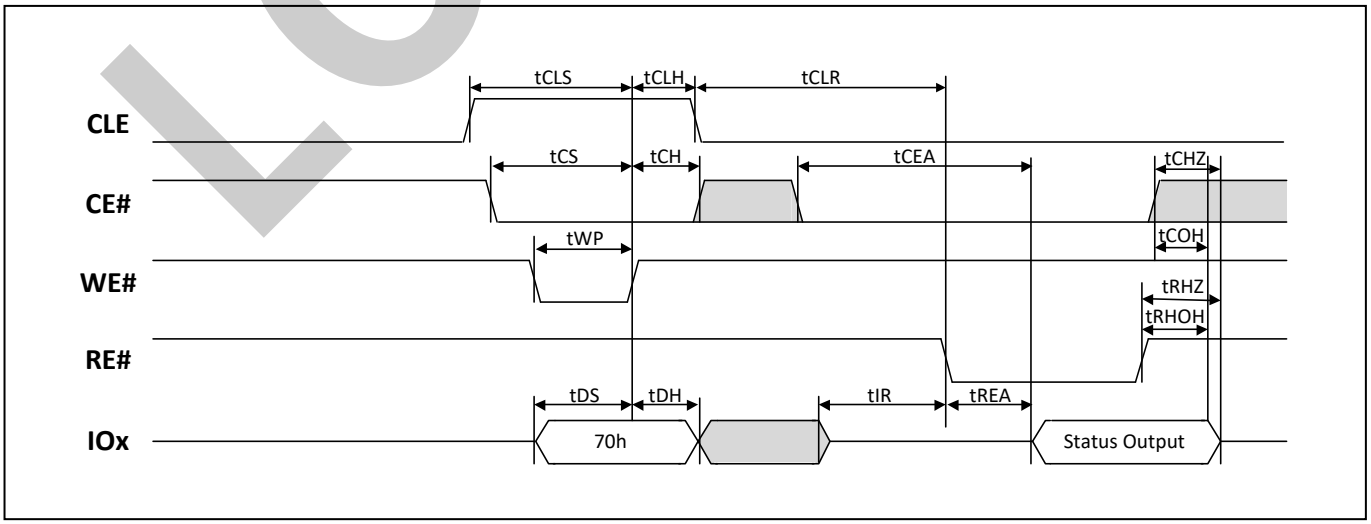


Table 6 Status Register Definition

SR Bits	Page Program	Block Erase	Read	Definition
IO 0	Pass / Fail	Pass / Fail	Not use	0 = Pass, 1 = Fail
IO 1	Not use	Not use	Not use	Don't -care
IO 2	Not use	Not use	Not use	Don't -care
IO 3	Not use	Not use	Not use	Don't -care
IO 4	Not use	Not use	Not use	Don't -care
IO 5	Not Use	Not Use	Not Use	Don't -care
IO 6	Ready / Busy	Ready / Busy	Ready/Busy	0 = Busy, 1 = Ready
IO 7	Write Protect	Write Protect	Write Protect	0 = Protected, 1 = Unprotected

Note

(1) IOs defined 'Not use' are recommended to be masked out when Read Status is being executed.

10.2.4 Read ID (90h)

Read ID command is comprised of two modes determined by the input address, device (00h) or ONFI (20h) identification information. To enter the Read ID mode, write 90h command following by a 00h address cycle, then toggle RE# for 5 single byte cycles. The pre-programmed code includes the Manufacturer ID, Device ID, and Product-Specific Information (See **Table 8**). If the Read ID command is followed by 20h address, the output code includes 4 single byte cycles of ONFI identifying information. The device remains in the Read ID mode until the next valid command is issued.

Figure 10 Read ID Sequence

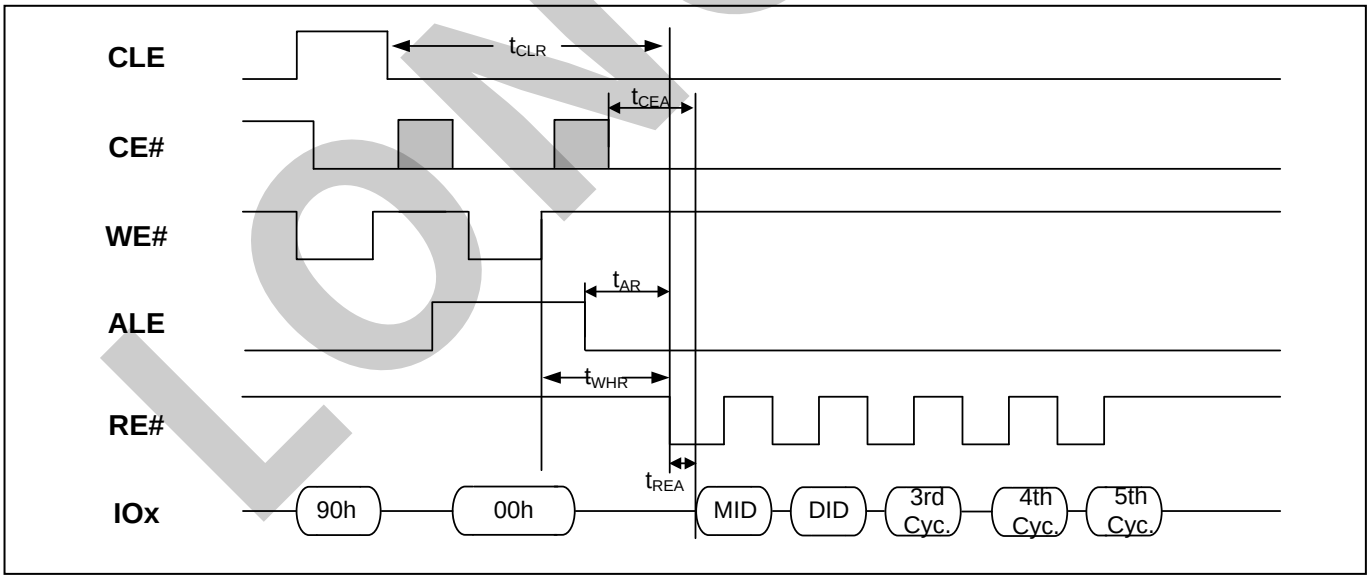


Table 7 Device and ONFI identification information

Address	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle	5th Byte/Cycle
00h	CDh Manufacturer ID	DAh Device ID	00h	95h	44h
20h	4Fh	4Eh	46h	49h	-

Table 8 Product-Specific Information

Terms	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
3rd Byte		**00h**							
Cache Program	0 = Not supported	0							
Multiple die operation	0 = Not supported		0						
Simultaneously Programmed page number	00 = 1			0	0				
Cell type	00 = SLC					0	0		
Die number per CE	00 = 1							0	0
4th Byte		**95h**							
Sequential access min	10 = 25ns	1				0			
Organization	0 = x8		0						
Block size (without spare)	01 = 128kB			0	1				
Spare size per 512B	1 = 16						1		
Page size	01 = 2kB							0	1
5th Byte		**44h**							
Internal ECC	0 = Not supported	0							
Plane size	100 = 1Gb		1	0	0				
Plane number per CE	01 = 2					0	1		
ECC requirement	00 = 1bit / 528B							0	0

10.2.5 Read Parameter Page (ECh)

Read Parameter Page can read out the device's parameter data structure, such as, manufacturer information, device organization, timing parameters, key features, and other pertinent device parameters. The data structure is stored with at least three copies in the device's parameter page. The Random Data Output command is supported during data output.

Figure 11 Read Parameter Page Sequence

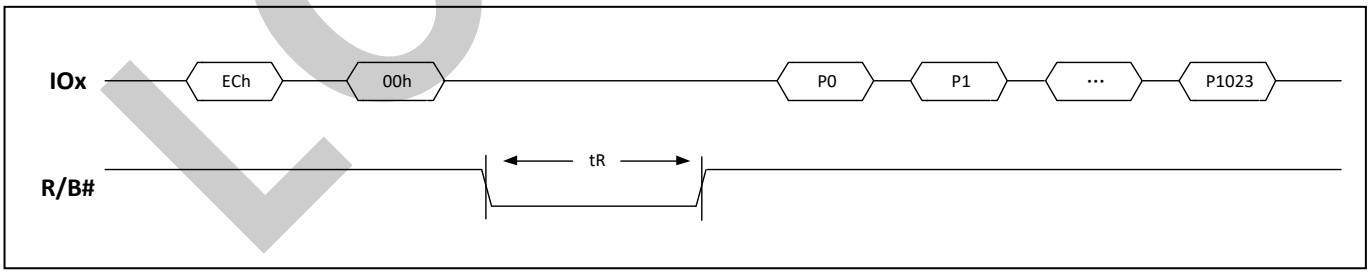


Table 9 Parameter Definition

Byte Number	Descriptions	Values
0~3	Parameter Page Signature, "ONFI" ASCII characters	4Fh 4Eh 46h 49h
4~5	Revision Number	02h 00h

Byte Number	Descriptions	Values
6~7	Feature Supported b6-b15 reserved (0) b5 1 = supports source synchronous b4 1 = supports odd to even page Copy-back b3 1 = supports interleaved operations b2 1 = supports non-sequential page programming b1 1 = supports multiple LUN operations b0 1 = supports 16-bit data bus width	10h 00h
8~9	Optional Command Supported b6-b15 reserved (0) b5 1 = supports Read Unique ID b4 1 = supports Copyback b3 1 = supports Read Status Enhanced b2 1 = supports Get Features and Set Features b1 1 = supports Read Cache commands b0 1 = supports Page Cache Program command	34h 00h
10~31	Reserved (0)	all 00h
32~43	Device manufacturer, 12 ASCII characters	46h 4Fh 52h 45h 53h 45h 45h 20h 20h 20h 20h 20h
44-63	Device Model, 20 ASCII characters	46h 53h 4Eh 53h 38h 41h 30h 30h 32h 47h 20h 20h 20h 20h 20h 20h 20h 20h 20h 20h
64	JEDEC MID	CDh
65-66	Date Code	00h 00h
67-79	Reserved (0)	all 00h
80-83	Number of Data Bytes per Page	00h 08h 00h 00h
84-85	Number of Spare Bytes per Page	40h 00h
86-89	Number of Data Bytes per Partial Page	00h 02h 00h 00h
90-91	Number of Spare Bytes per Partial Page	10h 00h
92-95	Number of Pages per Block	40h 00h 00h 00h
96-99	Number of Block per Logic Unit	00h 08h 00h 00h
100	Number of Logic Units	01h
101	Number of Address Bytes b4-b7 column address cycles b0-b3 row address cycles	23h
102	Number of Bits per Cell	01h
103-104	Bad Blocks Maximum per Logic Unit	28h 00h
105-106	Block Endurance	01h 05h
107	Guaranteed Valid Blocks at Beginning of Target	01h
108-109	Block Endurance for Guaranteed Valid Blocks	01h 03h

Byte Number	Descriptions	Values
110	Number of Programs per Page	04h
111	Partial Programming Attributes b5-b7 reserved (0) b4 1 = partial page layout is partial page data followed by partial page spare b1-b3 reserved (0) b0 1 = partial page programming has constraints	00h
112	Number of ECC Bits Correctability	01h
113	Number of Interleaved Address Bits b4-b7 reserved (0) b0-b3 number of interleaved address bits	00h
114	Interleaved Operation Attributes b4-b7 reserved (0) b3 address restrictions for program cache b2 1 = program cache supported b1 1 = no block address restrictions b0 overlapped / concurrent interleaving support	00h
115-127	Reserved (0)	all 00h
128	I/O Pin Capacitance, Maximum	08h
129-130	Asynchronous Timing Mode Support b6-b15 reserved (0) b5 1 = supports timing mode 5 b4 1 = supports timing mode 4 b3 1 = supports timing mode 3 b2 1 = supports timing mode 2 b1 1 = supports timing mode 1 b0 1 = supports timing mode 0, shall be 1	1Fh 00h
131-132	Asynchronous Program Cache Timing Mode Support b6-b15 reserved (0) b5 1 = supports timing mode 5 b4 1 = supports timing mode 4 b3 1 = supports timing mode 3 b2 1 = supports timing mode 2 b1 1 = supports timing mode 1 b0 1 = supports timing mode 0, shall be 1	00h 00h
133-134	t_{PROG} Maximum Page Program Time (us)	BCh 02h
135-136	t_{BERS} Maximum Block Erase Time (us)	10h 27h
137-138	t_R Maximum Page read Time (us)	19h 00h
139~140	t_{CCS} Minimum Change Column Setup Time (ns)	3Ch 00h
141-163	Reserved (0)	all 00h
164-165	Vendor Specific Revision Number	00h 00h
166-253	Vendor Specific	all 00h
254-255	Integrity CRC	85h B3h

Byte Number	Descriptions	Values
256-511	Value of Bytes 0-255	
512-767	Value of Bytes 0-255	
768+	Additional Redundant Parameter Pages	

Note:

(1) The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details. The CRC shall be calculated using the following 16-bit generator polynomial: G(X) = X16 + X15 +X2 + 1

10.2.6 Read Unique ID (EDH)

The unique ID is 32-byte and with 16 copies for back-up purpose. After writing the Unique ID read command and following the one address byte (00h), the host may read out the unique ID data. The host need to XOR the 1st 16-byte unique data and the 2nd 16-byte complement data to get the result, if the result is FFh, the unique ID data is correct; otherwise, host need to repeat the XOR with the next copy of Unique ID data.

Once sending the EDh command, the NAND device will remain in the Unique ID read mode until next valid command is sent. The Random Data Output command is supported during data output.

The Read Status command can be used to check the completion. To continue the read operation, a following read command (00h) to re-enable the data out is necessary.

Figure 12 Read Unique ID Sequence

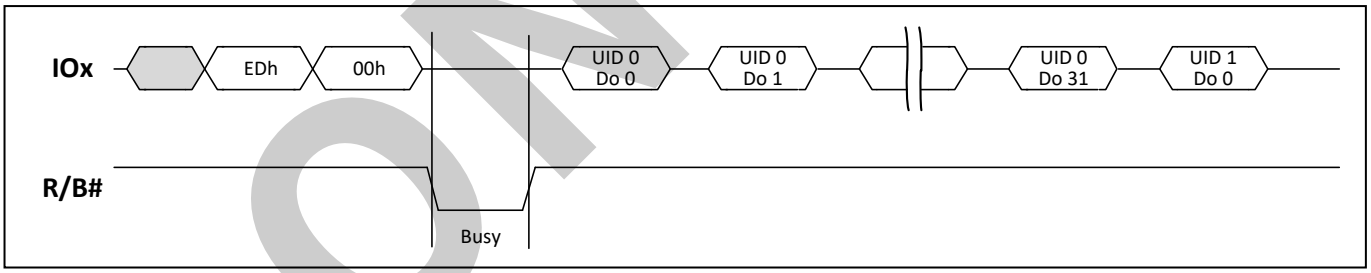
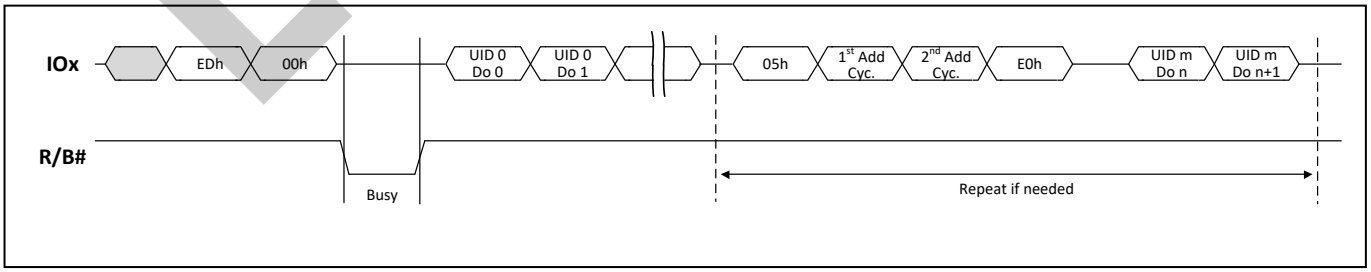


Figure 13 Read Unique ID Sequence with Random Data Output



10.3 Program Operation

10.3.1 Page Program (80h-10h)

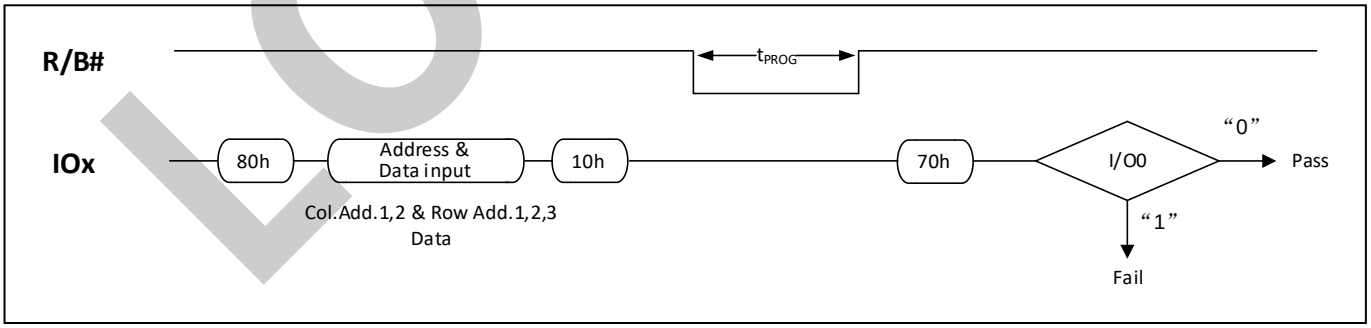
The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 2,112 in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must NOT exceed 4 times for a single page. The addressing should be done in sequential order in a block.

A page program cycle consists of a serial data loading period in which up to 2,112-bytes of data may be loaded into the page buffer, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the 80h command, followed by the five cycle address inputs and then serial data loading. The bytes other than those to be programmed do not need to be loaded. The 10h command initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process.

The internal write state controller automatically exe-cutes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (IO6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status bit (IO 0) may be checked (See **Figure 14**). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

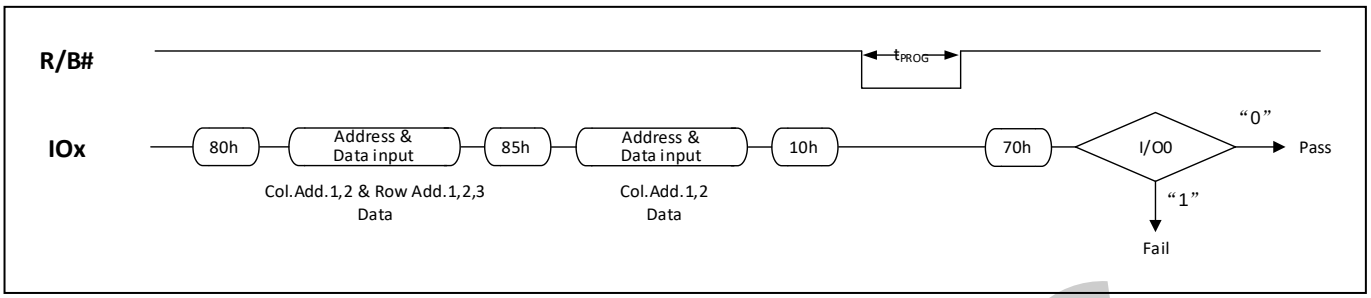
Figure 14 Page Program Sequence



10.3.2 Random Data Input (85h)

After the Page Program 80h command execution of the initial data has been loaded into the page buffer, if the need for additional writing of data is required, using the Random Data Input command can perform this function to a new column address prior to the 10h command. The Random Data Input may be operated multiple times regardless of how many times it is done in a page.

Figure 15 Page Program with Random Data Input Sequence



10.4 Copy Back Operation

Copy Back operations can quickly and efficiently rewrite data stored in one page. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. The operations require two sequential command sets. Issue a Copy Back Read command first, then the Copy Back Program command.

Since Copy Back operations do not use external memory and the data of source page might include a bit errors, a competent ECC scheme should be developed to check the data before programming data to a new destination page.

Note: Copy Back Operation can only be used to copy even page to even page or to copy odd page to odd page.

10.4.1 Copy Back Read (00h-35h)

The Copy Back Read command is used together with the Copy Back Program command. To start execution, 00h command is written to the command register, followed by the five cycles of the source page address. To start the transfer of the selected page data from the memory array to the page buffer, write the 35h command to the command register.

After execution of the Copy Back Read command sequence and R/B# returns to HIGH marking the completion of the operation, the transferred data from the source page into the page buffer may be read out by toggling RE#. Data is output sequentially from the column address that was originally specified with the Copy Back Read command (See **Figure 16**).

The Random Data Output commands can be issued multiple times without any limitation after Copy Back Read command has been executed.

10.4.2 Copy Back Program (85h-10h)

After the Copy Back Read command operation has been completed and R/B# goes HIGH, the Copy Back Program command can be written to the Command Register.

The operation is initiated by issuing 85h command with destination page address. Actual programming operation begins after 10h command is issued. Once the program process starts, the Read Status command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (IO6) of the Status Register. When the copy back program is complete, the Write Status Bit (IO0) may be checked (See **Figure 16**). The command register remains in Read Status command mode until another valid command is written to the command register.

During copy-back program, data modification is possible using Random Data Input command with multiple times (see **Figure 17**).

Note: Copy back program operation is allowed only within the same memory plane, which means the address A28 of destination page must be the same as that of source page.

Figure 16 Copy Back Read and Copy Back Program Sequence

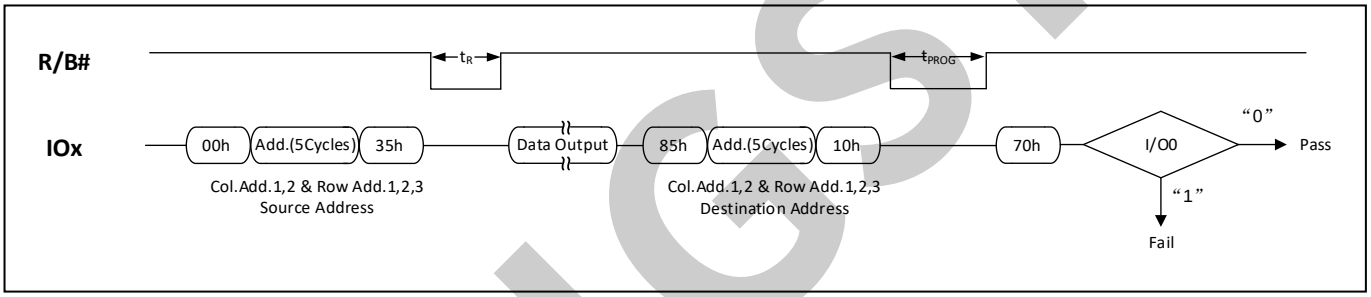
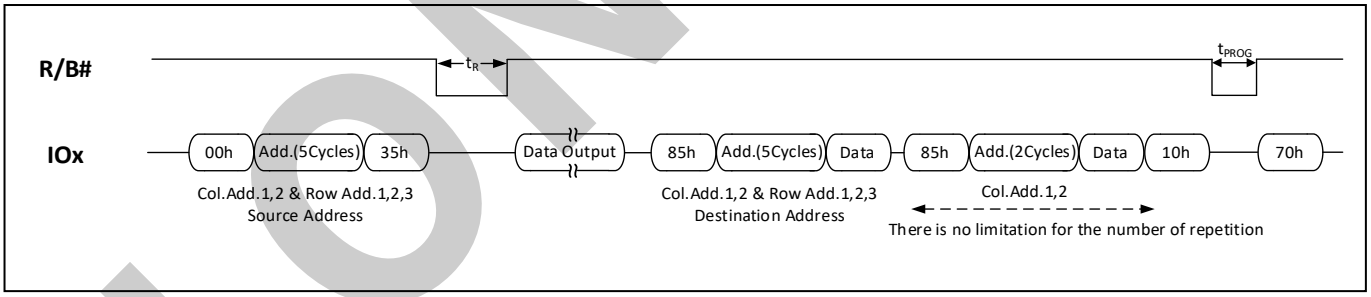


Figure 17 Copy Back Program with Random Data Input Sequence



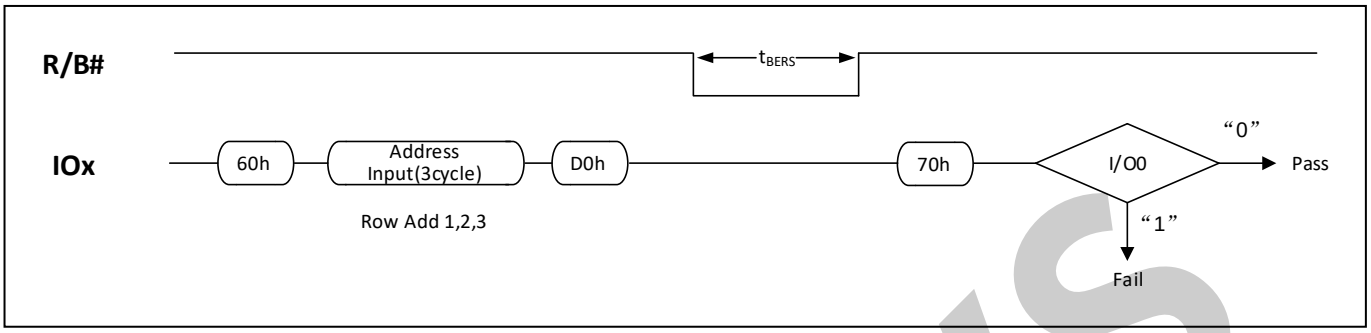
10.5 Block Erase (60h-D0h)

The erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by 60h command. Only address A18 to A28 is valid while A12 to A17 is ignored. The D0h command following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. The system controller can detect the completion of an erase cycle by monitoring

the R/B# output, or the Status bit (IO6) of the Status Register. When the block erase operation is complete, the Write Status Bit (IO0) may be checked.

Figure 18 Block Erase Sequence



10.6 Feature Operation

The Feature Set operation is to change the default power-on feature sets by using the Set Feature and Get Feature command and writing the specific parameter data (P1-P4) on the specific feature addresses. The NAND device may remain the current feature set until next power cycle since the feature set data is volatile. However, the reset command cannot reset the current feature set.

10.6.1 Feature Register

Table 10 Feature Register

Feature Register	Address	Parameter	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	Description
Operation Mode	90h	P1	0	0	0	0	0	0	0	0	Normal Mode, default value after power cycle.
			0	0	0	0	0	0	0	1	OTP Operation Mode. See **10.7.1** for detail information
			0	0	0	0	0	0	1	1	OTP Lock Mode. See **10.7.2** for detail information
		P2	Reserved (0)								
		P3	Reserved (0)								
		P4	Reserved (0)								
Block Protection	A0h	P1	R	BP3	BP2	BP1	BP0	TB	0	SP	Default value after power cycle is 00000000 (00h). See **10.8** for detail information
		P2	Reserved (0)								
		P3	Reserved (0)								
		P4	Reserved (0)								

Note:

(1) R: Reserved Bit and has no function. They may be read out as a "0" or "1". It is recommended to ignore the values of those

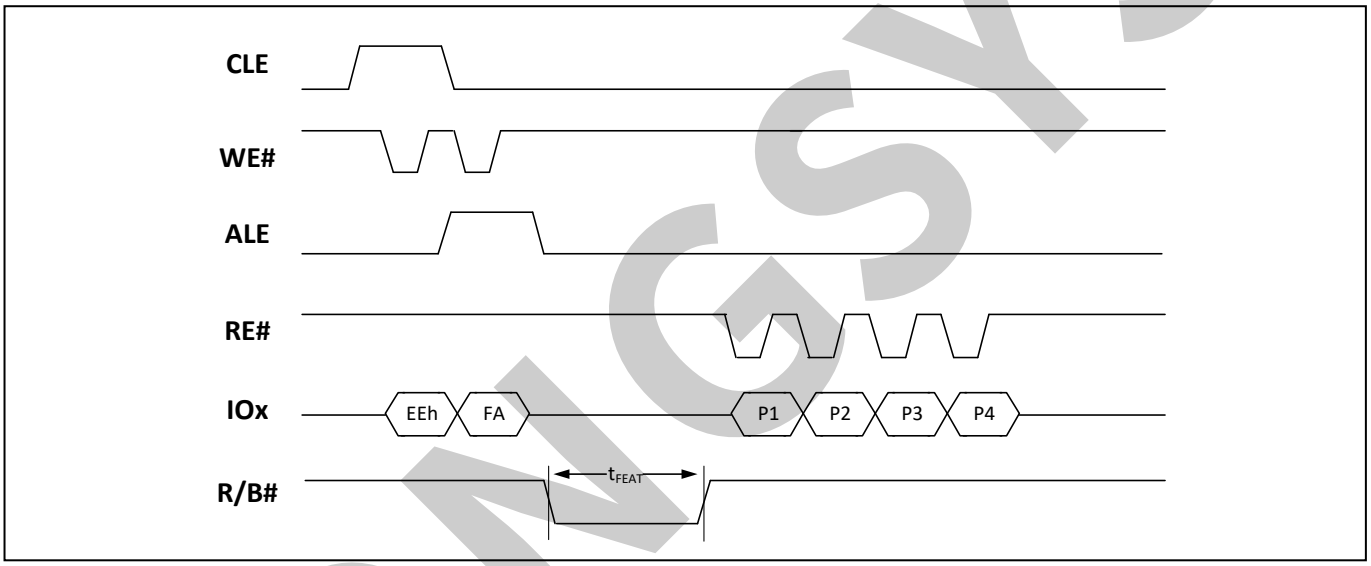
bits. During a Set Feature command, the Reserved Bits can be written as “0”, but there will not be any effects.

10.6.2 Get Feature (EEh)

The Get Feature command is to read feature parameter. After sending the Get Feature command and following register address, the host may read out the P1-P4 sub-feature parameter data. Once sending the EEh command, the NAND device will remain in the Get Feature mode until next valid command is sent.

The Status Read command can be used to check the completion. To continue the read operation, a following 00h command to re-enable the data out is necessary.

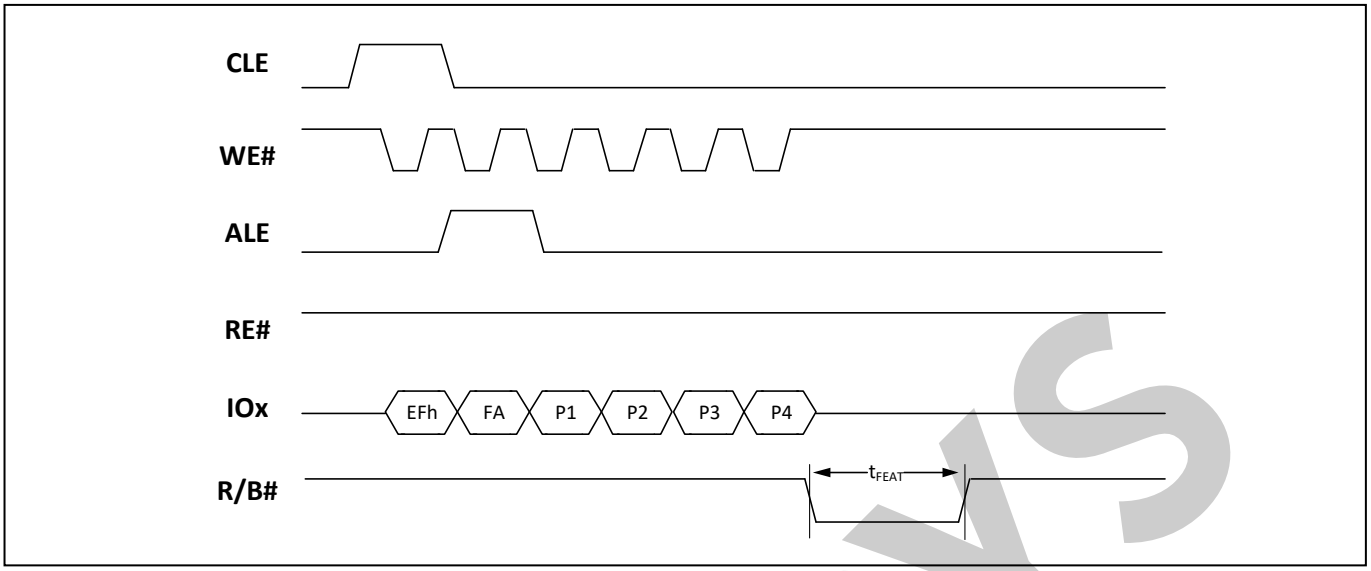
Figure 19 Get Feature Sequence



10.6.3 Set Feature (EFh)

The Set Feature command is to change the power-on default feature set. After sending the Set Feature command and following register address and then input the P1-P4 parameter data to change the feature set. Once sending the EFh command, the NAND device will remain in the Set Feature mode until next valid command is sent. The Status Read command may check the completion of the Set Feature.

Figure 20 Set Feature Sequence



10.7 OTP Operation

The OTP area has 62 pages (62 x 2,112-byte). It is a non-erasable and one-time programmable area, which is default to “1” and allows whole page or partial page program to be “0”. Once the OTP protection mode is set, the OTP area becomes read-only and cannot be programmed again.

The OTP operation is operated by the Set Feature / Get Feature operation to access the OTP Operation Mode and OTP Lock Mode.

To check the NAND device is ready or busy in the OTP operation mode, either checking the R/B# or using the Read Status command to check the status.

To exit the OTP operation or protect mode, it can be done by writing 00h to P1 at feature address 90h.

10.7.1 OTP Read / Program Operation

To enter the OTP Operation Mode, it is by using the Set Feature command and followed by the feature address 90h and then input the 01h to P1 and 00h to P2-P4 of sub-Feature Parameter data (see **Table 10 Feature Register**).

After enter the OTP Operation Mode, the OTP area can be read or programmed like non-OTP area. The address of OTP is located on the 000002h-00003Fh of page address.

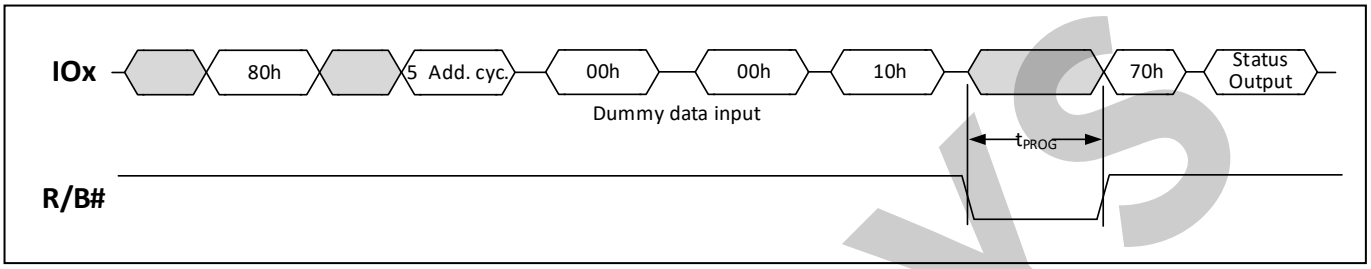
10.7.2 OTP Lock Operation

To prevent the further OTP data to be changed, the OTP lock operation is necessary. To enter the OTP Lock Mode, it can be done by using the Set Feature command and followed by the feature address 90h

and then input the 03h to P1 and 00h to P2-P4 of sub-Feature Parameter data (see **Table 10 Feature Register**). And then the normal Page Program command with the address 00h before the 10h command is required.

The OTP lock operation is operated on the whole OTP area instead of individual OTP page. Once the OTP protection mode is set, the OTP area can NOT be programmed or unprotected again.

Figure 21 OTP Lock Operation Sequence



10.8 Block Protection

The block protect operation can protect the whole chip or selected blocks from erasing or programming. When program or erase attempt at a protected block is happened, the R/B# keeps low for the time of t_{PBSY}, and the Status Read command may get the 41h result.

At power-on, all the blocks are default to be un-protected. The Set Feature command with feature address A0h followed by the destined protection bits with data “1” is necessary to protect those selected blocks. After the selected blocks are protected, those protected blocks can be un-protected again by reset Block Protection Bit to “0” if required.

The “solid-protection” feature can be set by writing the Set Feature command with feature address A0h and the “SP” solid protection bit as “1” (see **Table 10 Feature Register**), after that, the selected block is solid-protected and cannot be up-protected until next power cycle.

Table 11 Block Protection Bits

TB	BP3	BP2	BP1	BP0	Protected Block(s)	Protected Page Address PA[16:0]	Protected Density	Protected Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	2047	1FFC0h – 1FFFFh	128KB	Upper 1/2048
0	0	0	1	0	2046 & 2047	1FF80h – 1FFFFh	256KB	Upper 1/1024
0	0	0	1	1	2044 thru 2047	1FF00h – 1FFFFh	512KB	Upper 1/512
0	0	1	0	0	2040 thru 2047	1FE00h – 1FFFFh	1MB	Upper 1/256
0	0	1	0	1	2032 thru 2047	1FC00h – 1FFFFh	2MB	Upper 1/128
0	0	1	1	0	2016 thru 2047	1F800h – 1FFFFh	4MB	Upper 1/64
0	0	1	1	1	1984 thru 2047	1F000h – 1FFFFh	8MB	Upper 1/32
0	1	0	0	0	1920 thru 2047	1E000h – 1FFFFh	16MB	Upper 1/16

0	1	0	0	1	1792 thru 2047	1C000h – 1FFFFh	32MB	Upper 1/8
0	1	0	1	0	1536 thru 2047	18000h – 1FFFFh	64MB	Upper 1/4
0	1	0	1	1	1024 thru 2047	10000h – 1FFFFh	128MB	Upper 1/2
1	0	0	0	1	0	00000h – 0003Fh	128KB	Lower 1/2048
1	0	0	1	0	0 & 1	00000h – 0007Fh	256KB	Lower 1/1024
1	0	0	1	1	0 thru 3	00000h – 000FFh	512KB	Lower 1/512
1	0	1	0	0	0 thru 7	00000h – 001FFh	1MB	Lower 1/256
1	0	1	0	1	0 thru 15	00000h – 003FFh	2MB	Lower 1/128
1	0	1	1	0	0 thru 31	00000h – 007FFh	4MB	Lower 1/64
1	0	1	1	1	0 thru 63	00000h – 00FFFh	8MB	Lower 1/32
1	1	0	0	0	0 thru 127	00000h – 01FFFh	16MB	Lower 1/16
1	1	0	0	1	0 thru 255	00000h – 03FFFh	32MB	Lower 1/8
1	1	0	1	0	0 thru 511	00000h – 07FFFh	64MB	Lower 1/4
1	1	0	1	1	0 thru 1023	00000h – 0FFFFh	128MB	Lower 1/2
X	1	1	X	X	0 thru 2047	00000h – 1FFFFh	256MB	ALL

10.9 Write Protect

WP# pin can enable or disable program and erase commands preventing or allowing program and erase operations. **Figure 22** to **Figure 27** shows the enabling or disabling timing with WP# setup time (t_{WW}) that is from rising or falling edge of WP# to latch the first commands. After first command is latched, WP# pin must not toggle until the command operation is complete and the device is in the ready state. (Status Register Bit6 (IO6) equal 1).

Figure 22 Erase Enable

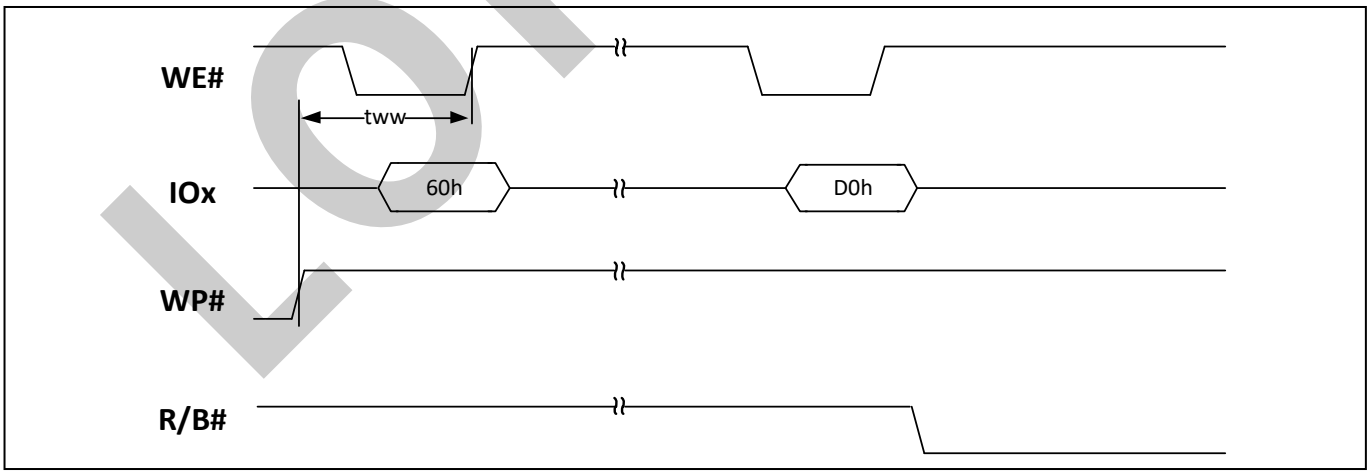


Figure 23 Erase Disable

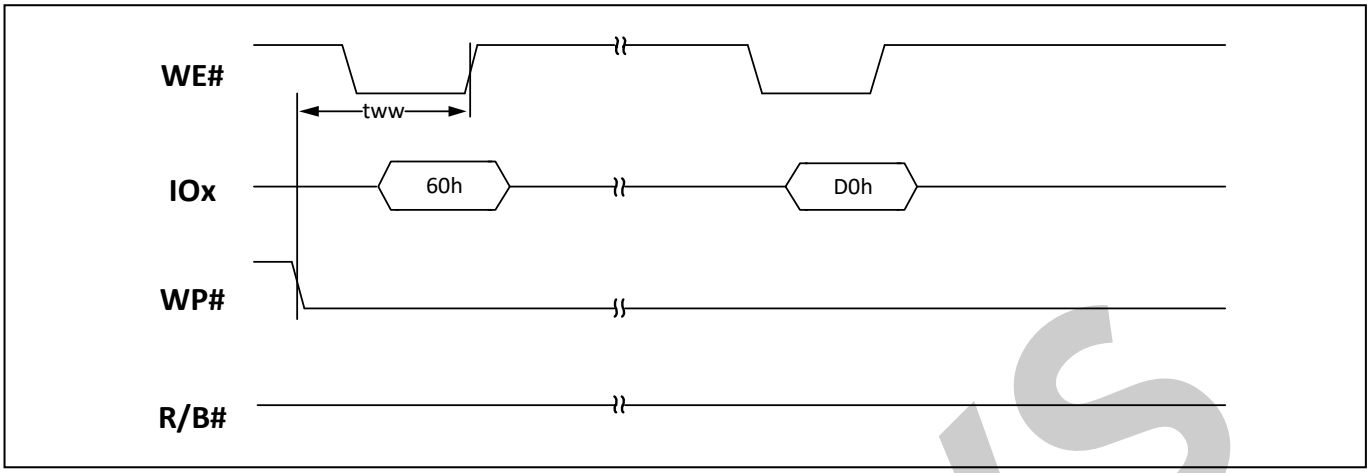


Figure 24 Program Enable

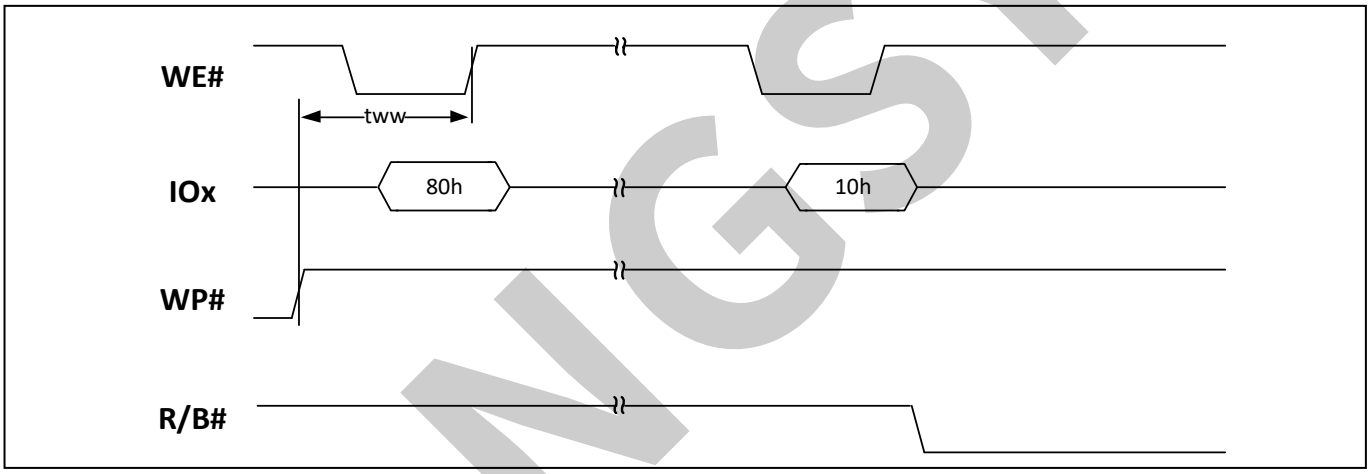


Figure 25 Program Disable

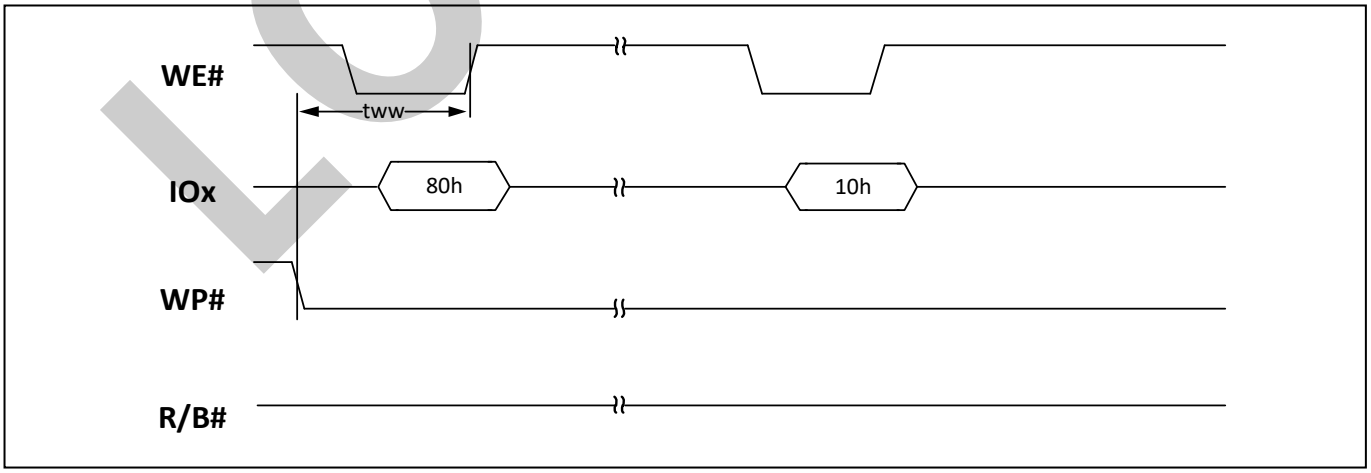


Figure 26 Program for Copy-Back Enable

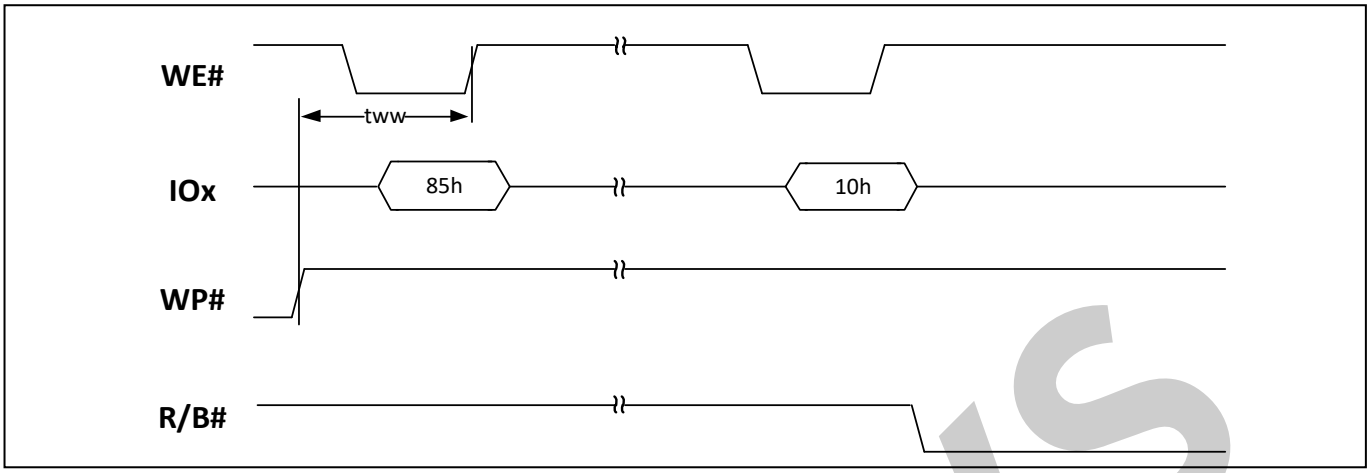
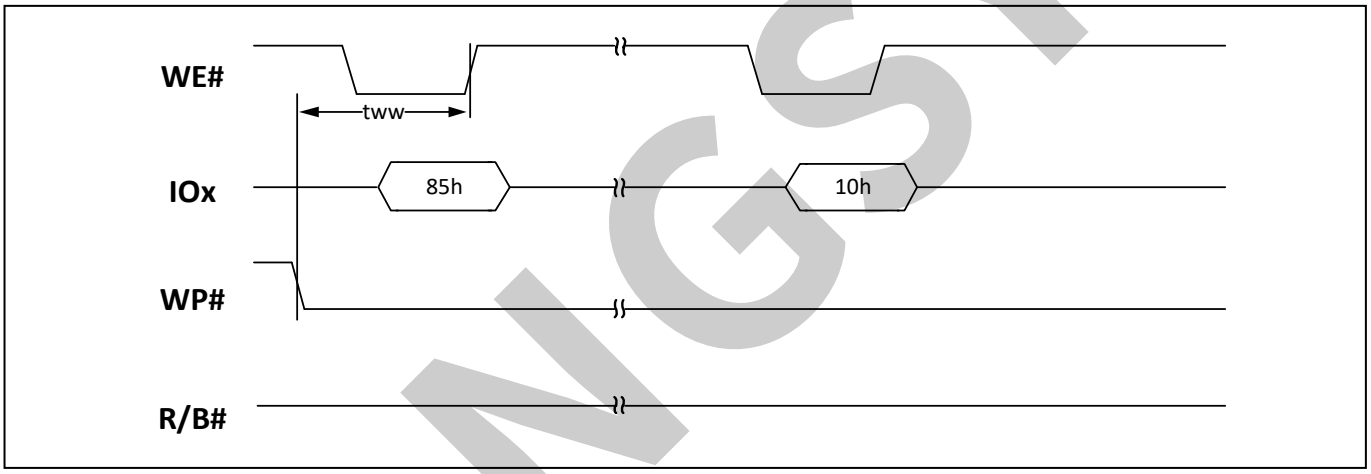


Figure 27 Program for Copy-Back Disable



11 Software Algorithm

11.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same electrical characteristics. An initial invalid block(s) does not affect the performance of valid block(s). The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

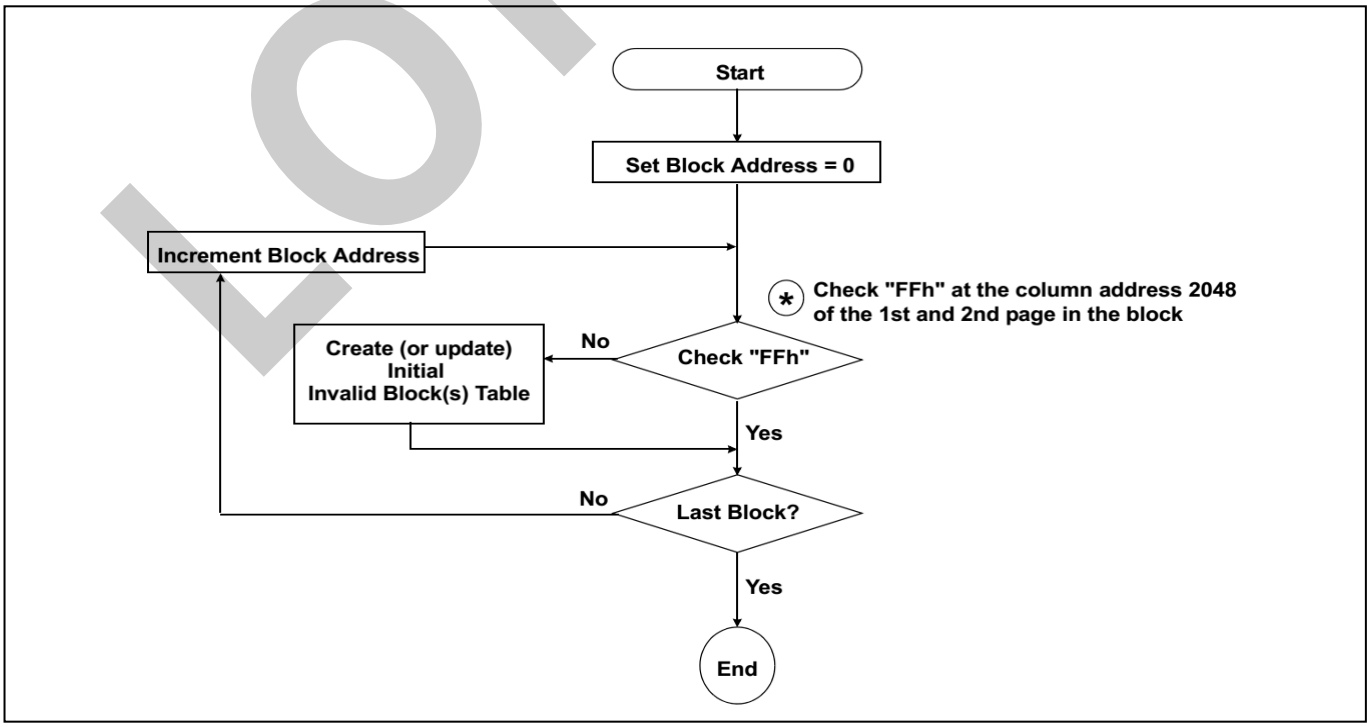
Table 12 Valid Block Number

Parameter	Symbol	Min	Max	Unit
Valid block number	N_{VB}	2008	2048	Blocks

11.2 Identifying Initial Invalid Block(s)

All device locations are erased (FFh) except locations where the initial invalid block(s) information is written prior to shipping. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the suggested flow (**Figure 28**). Any intentional erasure of the original initial invalid block information is prohibited.

Figure 28 Flow to Create Initial Invalid Block Table



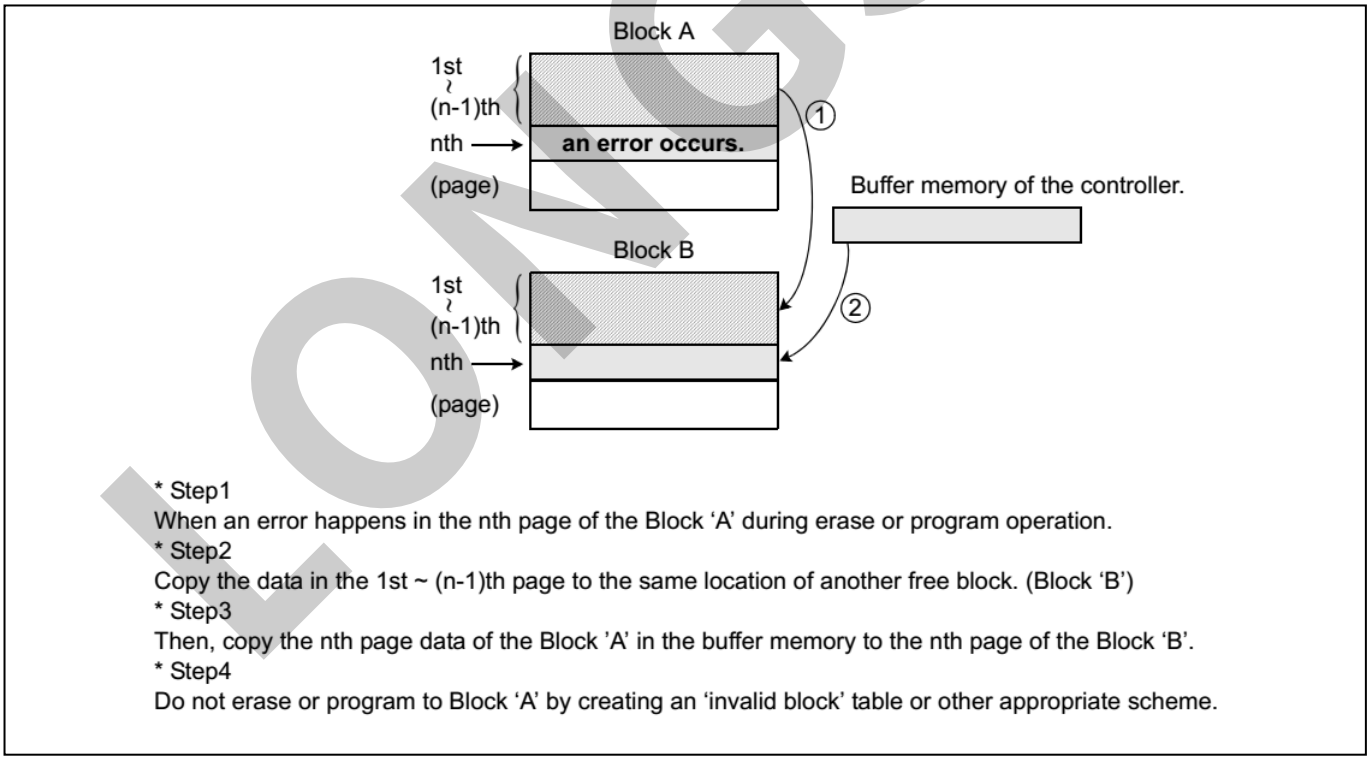
11.3 Error in Operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Table 13 Failure Modes

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction

Figure 29 Bad Block Replacement

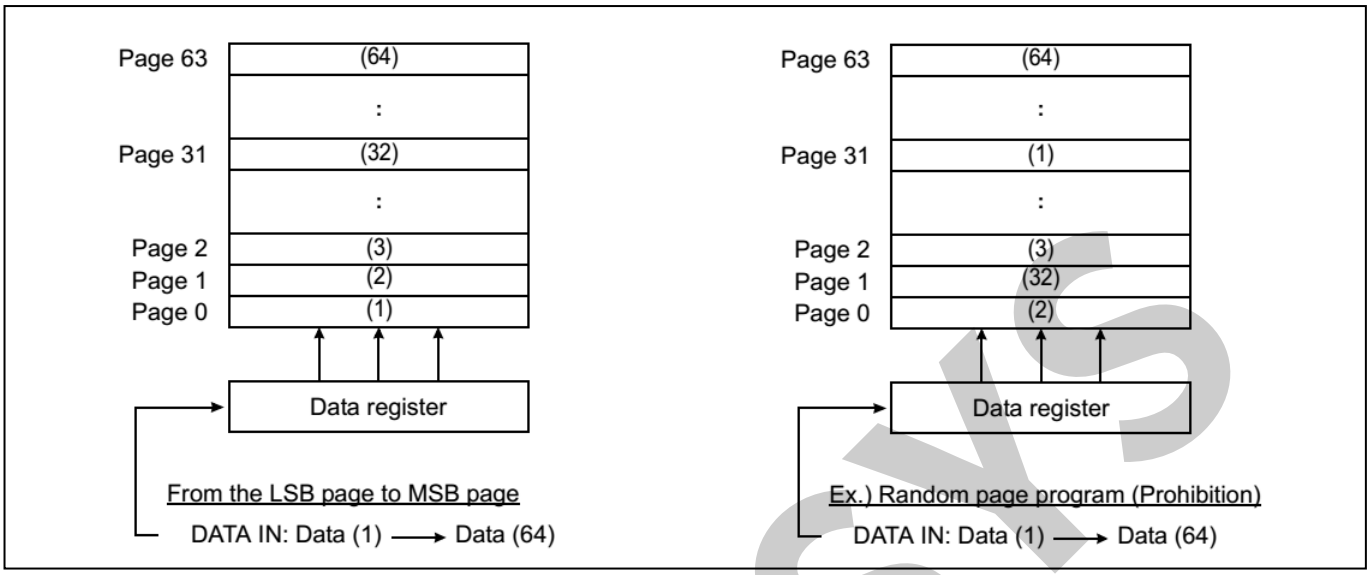


11.4 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB(least significant bit) page of the block to the MSB(most significant bit) pages of the block. The LSB page is defined as the start page among the pages to be programmed, does not need to be page 0 in the block. Random page address

programming is prohibited.

Figure 30 Addressing for Program Operation



11.5 System Interface Using CE# Don't-Care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 2,112 bytes data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of µ-seconds, de-activating CE# during the data-loading and serial access would provide significant savings in power consumption.

Figure 31 Program Operation with CE# don't-care

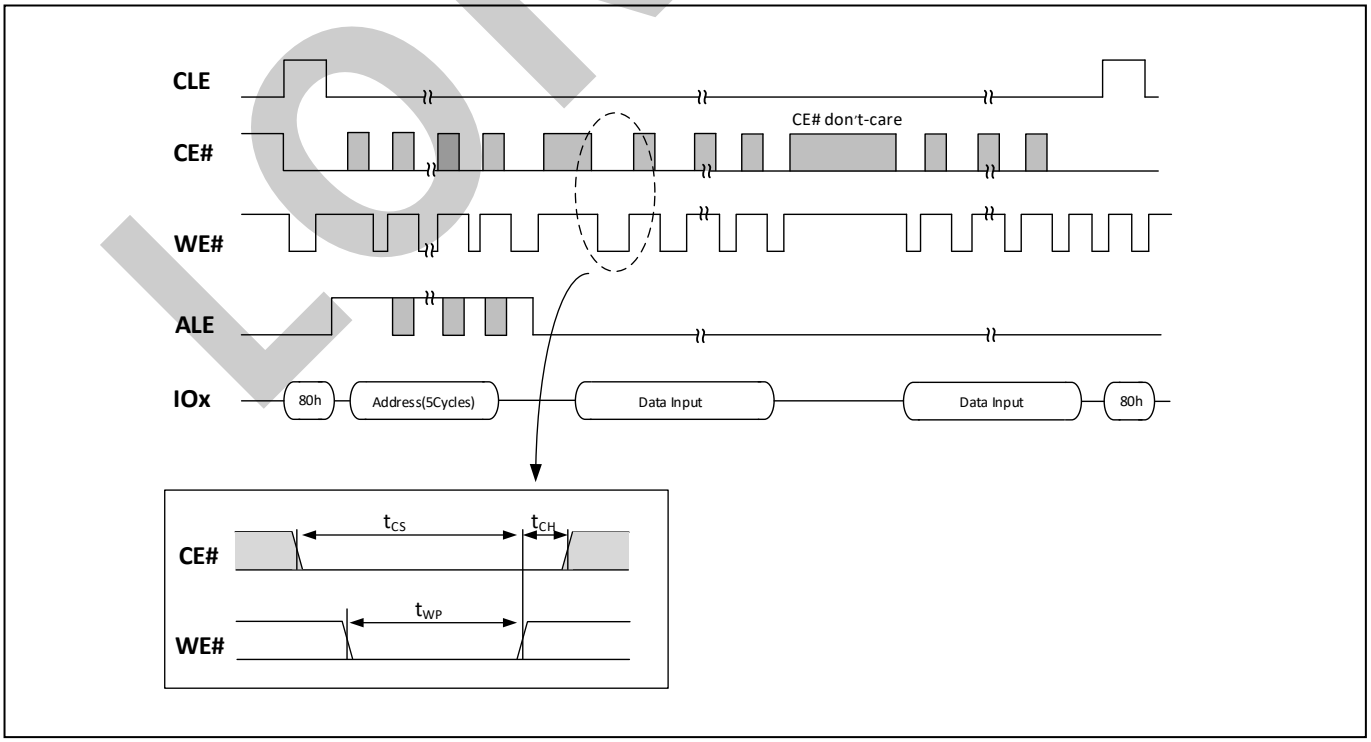
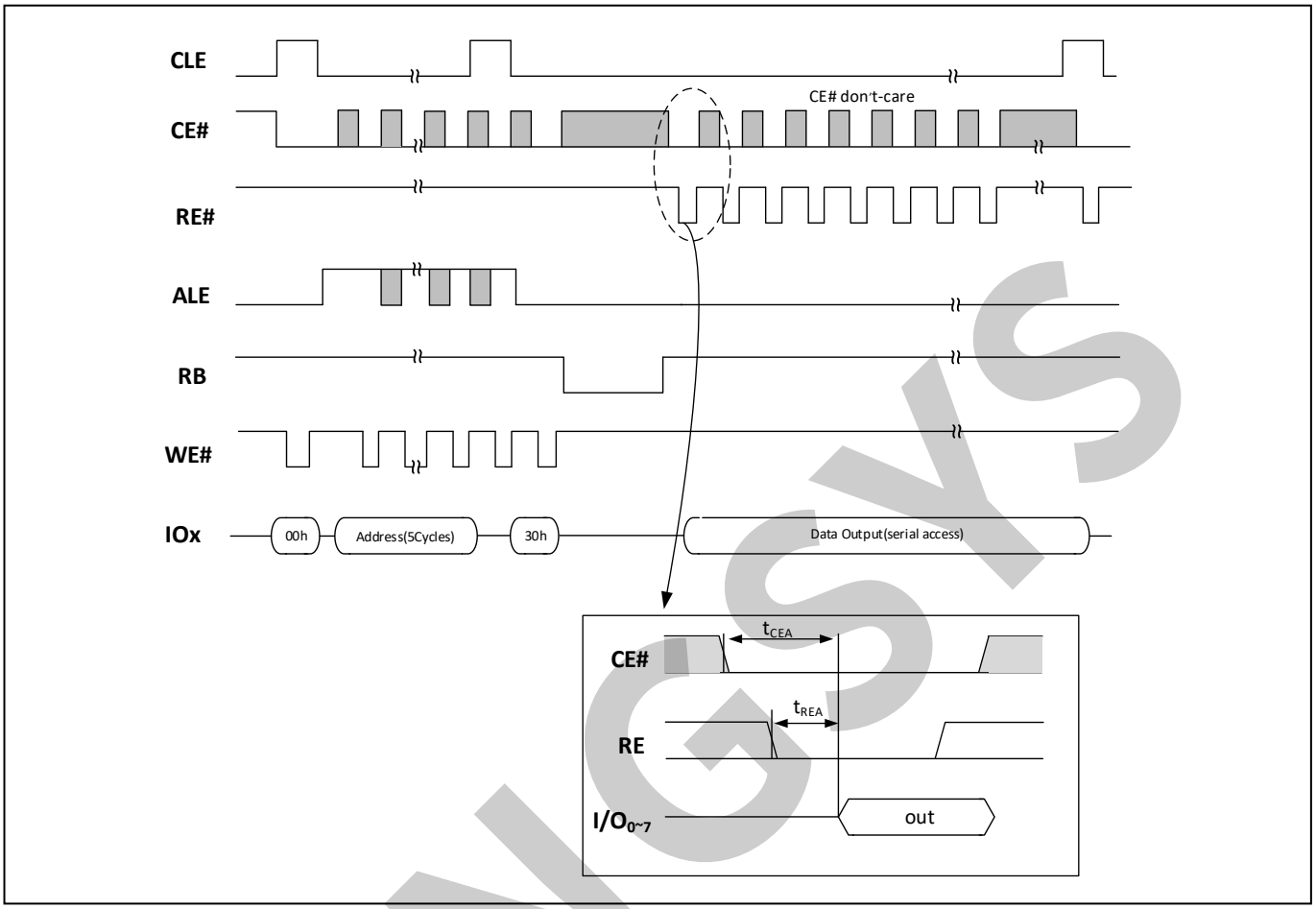


Figure 32 Read Operation with CE# don't-care



12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Table 14 Absolute Maximum Rating

Parameters	Symbol	Range	Unit
Supply Voltage	V_{CC}	–0.6 to +4.6	V
Voltage Applied to Any Pin	V_{IO}	–0.6 to V_{CC}+0.4	V
Temperature under Bias	T_{BIAS}	–40 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Short circuit output current, I/Os	I_{OS}	5	mA

Note:

(1) Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.

(2) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

12.2 Operating Ranges

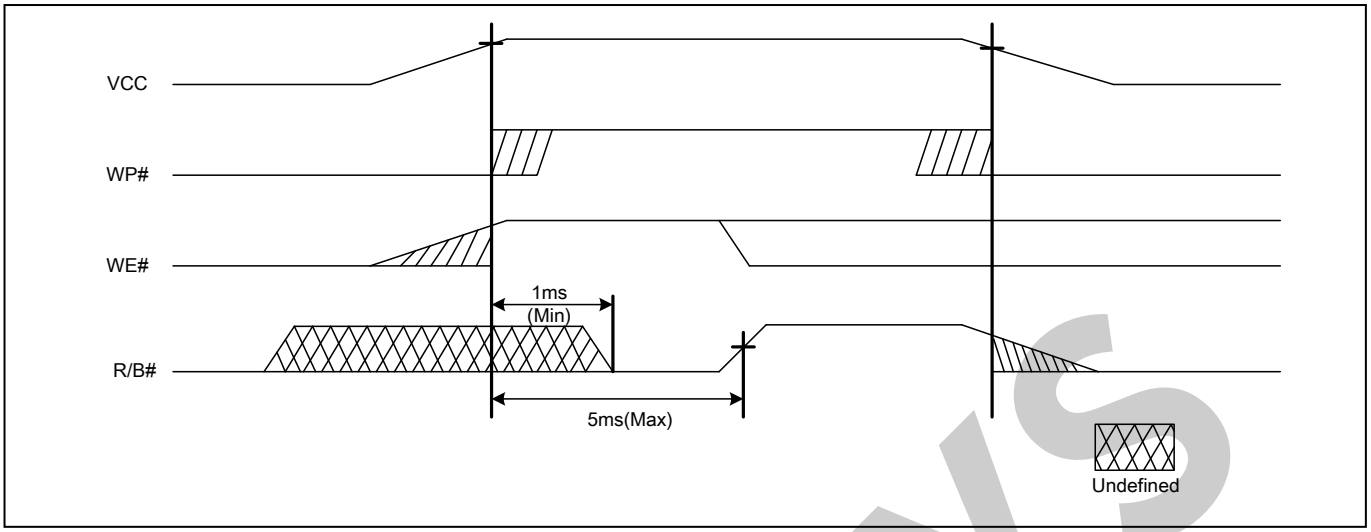
Table 15 Operating Ranges

Parameters	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{CC}		2.7	3.6	V
Ambient Temperature	T_A	Industrial	-40	+85	°C
		Industrial plus	-40	+105	°C

12.3 Power-up Timing

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 2V. WP# pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences as shown in **Figure 33**.

Figure 33 Power-up Timing



12.4 Pin Capacitance

Table 16 Pin Capacitance

Parameters	Symbol	Min	Max	Unit
Input / Output Capacitance	C_{IO}		8	pF
Input Capacitance	C_{IN}		8	pF

Note:

(1) Test conditions: TA=25°C, F=1MHz, V_{IN}=0V, V_{CC}=3V

(2) These parameters are characterized only.

12.5 DC Electrical Characteristics

Table 17 DC Electrical Characteristics

Parameters	Symbol	Conditions	SPEC(1)			Unit
			Min	Typ	Max	
Standby Current (CMOS)	I_{SB}	CE# = V_{CC} – 0.2V, All Input Pin = 0V/V_{CC}		10	50	µA
Page Read Current	I_{CC1}			10	25	mA
Program Current	I_{CC2}			15	25	mA
Erase Current	I_{CC3}			15	25	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V/V_{CC}			±10	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0V/V_{CC}			±10	µA
Output Low Current (R/B#)	$I_{OL(R/B\#)}$	V_{OL} = 0.4V	8	10		mA
Input Low Voltage	V_{IL}		-0.3		0.2V_{CC}	V
Input High Voltage	V_{IH}		0.8V_{CC}		V_{CC}+0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -400µA	2.4			V

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 2.7V to 3.6V, unless otherwise noted.

12.6 AC Measurement Conditions

Table 18 AC Measurement Conditions

Parameters	Symbol	Min	Max	Unit
Load Capacitance	C_L		30	pF
Input Rise Time	t_{Rise}		5	ns
Input Fall Time	t_{Fall}		5	ns
Input Pulse Voltages	V_{IN}	0 to V_{CC}		V
Input Timing Reference Voltages	IN	$0.5V_{CC}$		V
Output Timing Reference Voltages	OUT	$0.5V_{CC}$		V

12.7 AC Electrical Characteristics

Table 19 AC Electrical Characteristics for Command, Address and Data Input

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
Address to Data Loading Time	t_{ADL}(2)	70			ns
ALE Setup Time	t_{ALS}(3)	12			ns
ALE Hold Time	t_{ALH}	5			ns
CE# Setup Time	t_{CS}(3)	20			ns
CE# Hold Time	t_{CH}	5			ns
CLE Setup Time	t_{CLS}(3)	12			ns
CLE Hold Time	t_{CLH}	5			ns
Data Setup Time	t_{DS}(3)	12			ns
Data Hold Time	t_{DH}	5			ns
Write Cycle Time	t_{WC}	25			ns
WE# Pulse Width	t_{WP}	12			ns
WE# High Hold Time	t_{WH}	10			ns
WP# Setup Time (to WE# high)	t_{WW}	100			ns

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 2.7V to 3.6V, unless otherwise noted.

(2) t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

(3) The transition of the corresponding control pins must occur only once while WE# is held low.

Table 20 AC Electrical Characteristics for Operation

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
ALE to RE# Delay	t_{AR}	10		-	ns
CE# Access Time	t_{CEA}	-		25	ns
CE# High to Output Hi-Z	t_{CHZ}	-		50	ns
CE# High to ALE or CLE Don't Care	t_{CSD}	0		-	ns

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
CLE to RE# Delay	t_{CLR}	10		-	ns
Data Hold Time after CE# Disable	t_{COH}	15		-	ns
Output Hi-Z to RE# Low	t_{IR}	0		-	ns
Read Cycle Time	t_{RC}	25		-	ns
RE# Access Time	t_{REA}	-		20	ns
RE# High Hold Time	t_{REH}	10		-	ns
RE# High to Output Hold (EDO)	t_{RHOH}	15		-	ns
RE# High to WE# Low	t_{RHW}	100		-	ns
RE# High to Output Hi-Z	t_{RHZ}	-		100	ns
RE# Low to Output Hold (EDO)	t_{RLOH}	5		-	ns
RE# Pulse Width	t_{RP}	12		-	ns
Ready to RE# Low	t_{RR}	20		-	ns
WE# High to Busy	t_{WB}	-		100	ns
WE# High to RE# Lo	t_{WHR}	60			ns
Device reset time (Read/Program/Erase)	t_{RST}(2)			5/20/200	µs

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 2.7V to 3.6V, unless otherwise noted.

(2) If Reset command (FFh) is written at Ready state, the device is reset instantly. These parameters are characterized only.

12.8 Read / Program / Erase Characteristics

Table 21 Read / Program / Erase Characteristics

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
Data Transfer from Cell to Page buffer	t_R			25	µs
Program Time	t_{PROG}(2)		350	700	µs
Block Erase Time	t_{BERS}		2	10	ms
The busy time for program / erase at protected block	t_{PBSY}			3	µs
The busy time for Set Feature / Get Feature	t_{FEAT}			1	µs
Number of Partial Program Cycles	NOP			4	cycles

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 2.7V to 3.6V, unless otherwise noted.

(2) Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V and 25°C.

13 Timing Diagram

Figure 34 Command Input Cycle

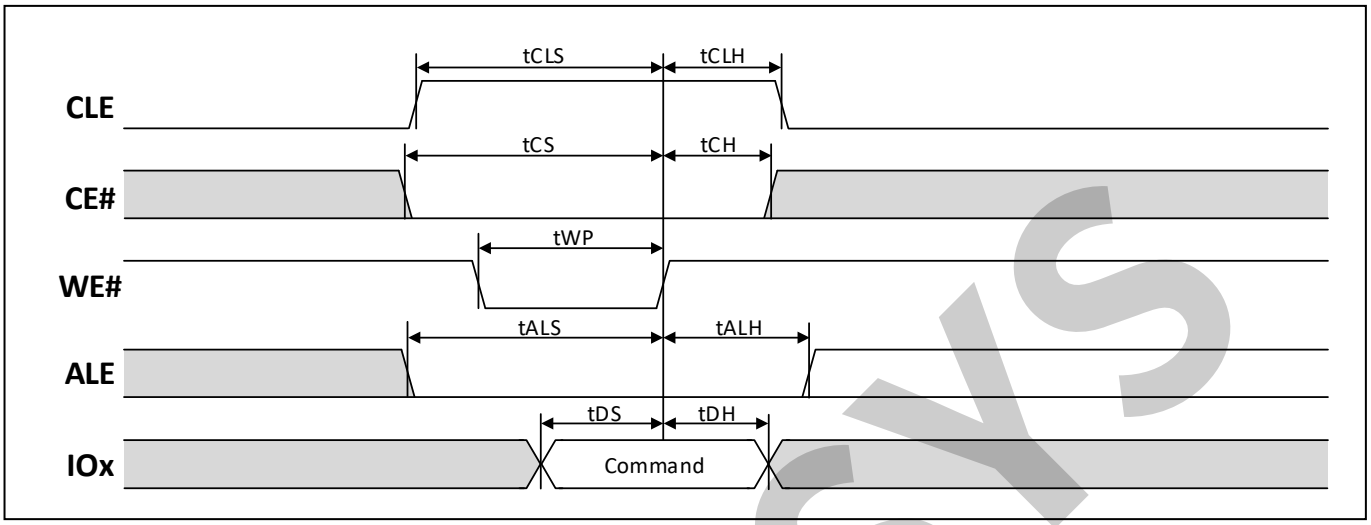


Figure 35 Address Input Cycle

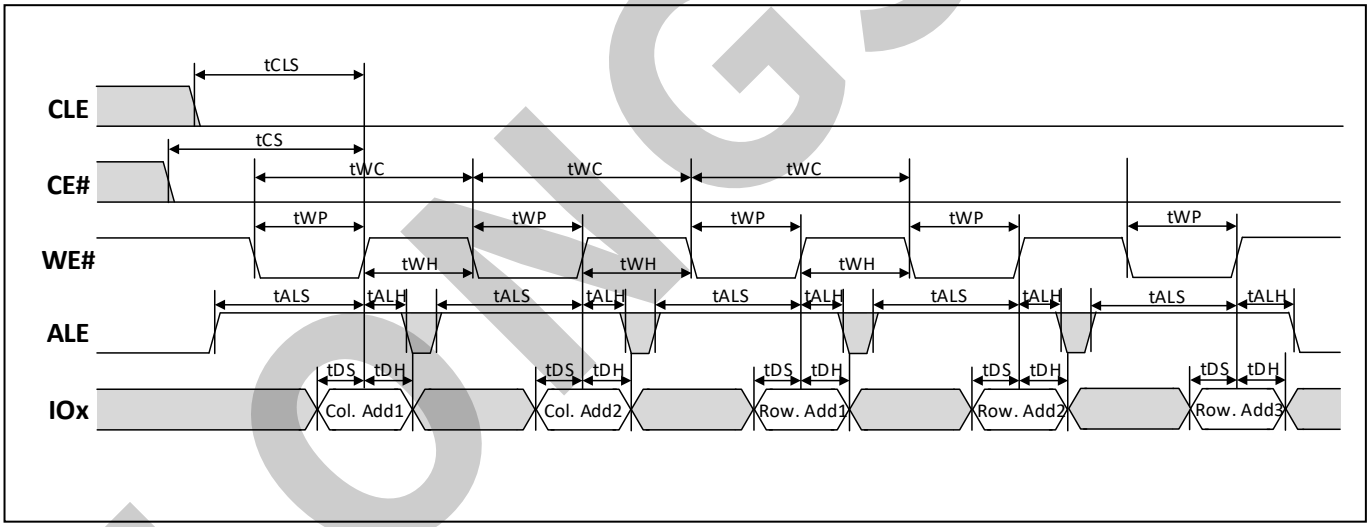


Figure 36 Data Input Cycle

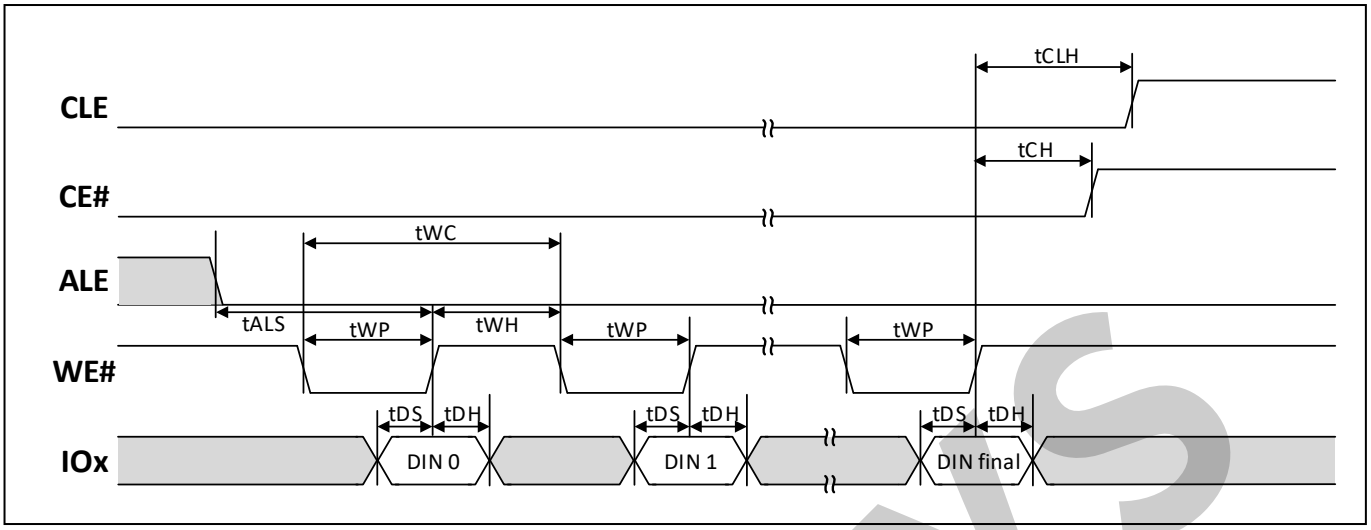


Figure 37 Serial Access Cycle after Read (CLE = L, ALE = L, WE# = H)

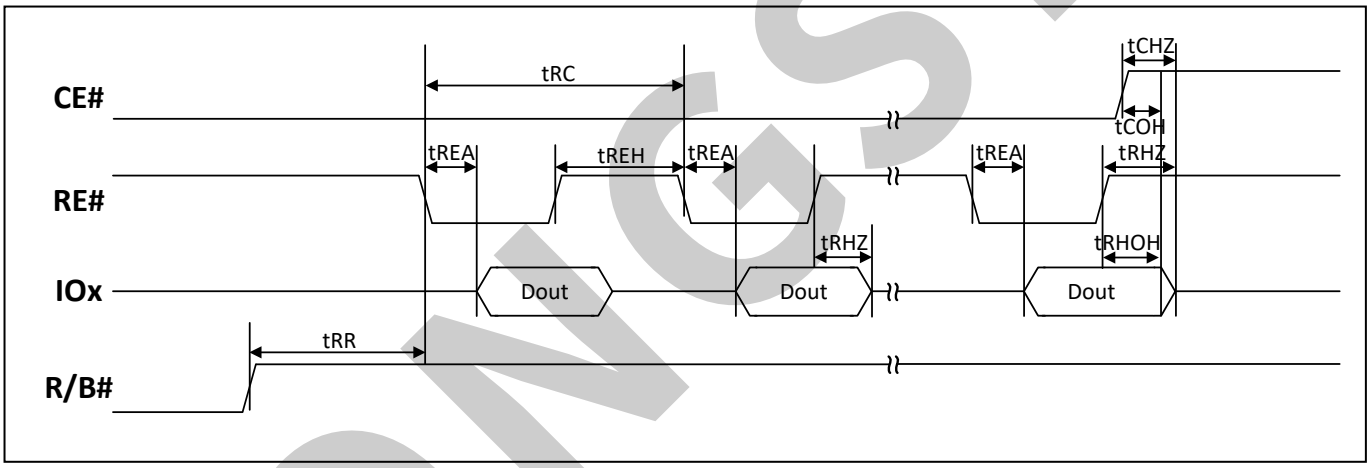


Figure 38 Serial Access Cycle after Read (EDO Type, CLE = L, ALE = L, WE# = H)

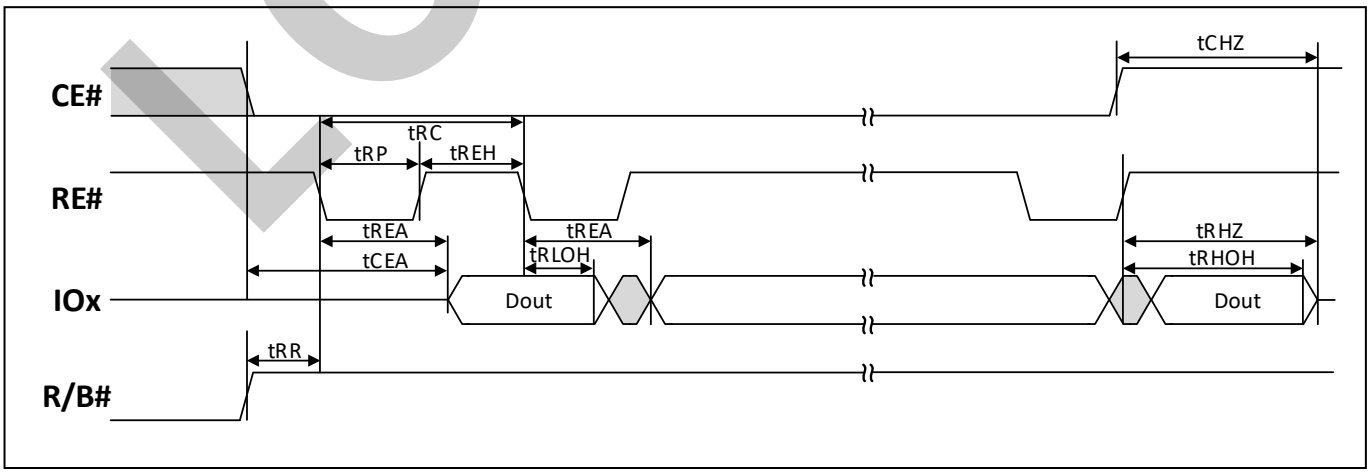


Figure 39 Read Status

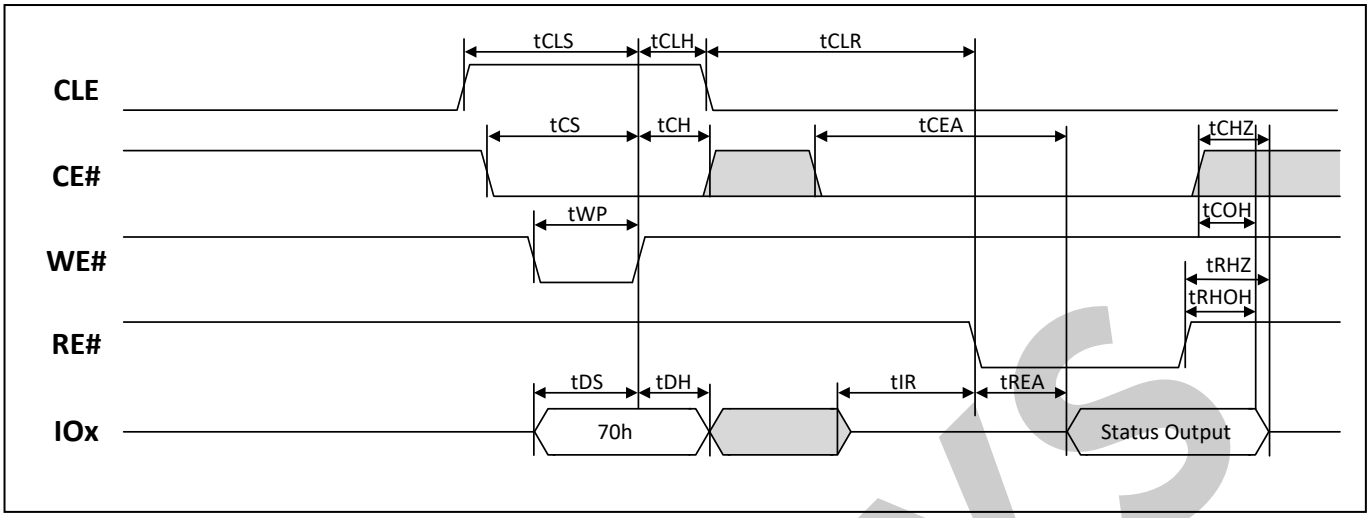


Figure 40 Page Read

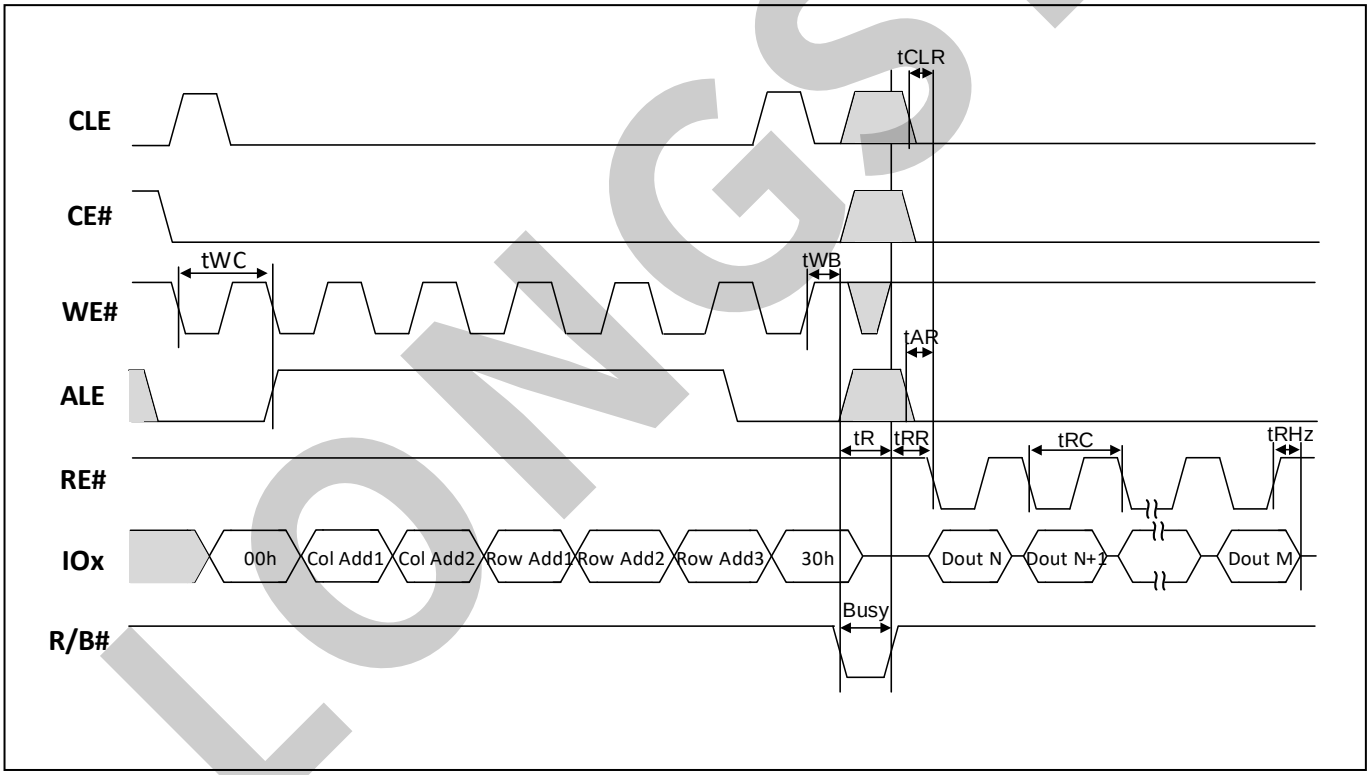


Figure 41 Page Read Intercepted by CE#

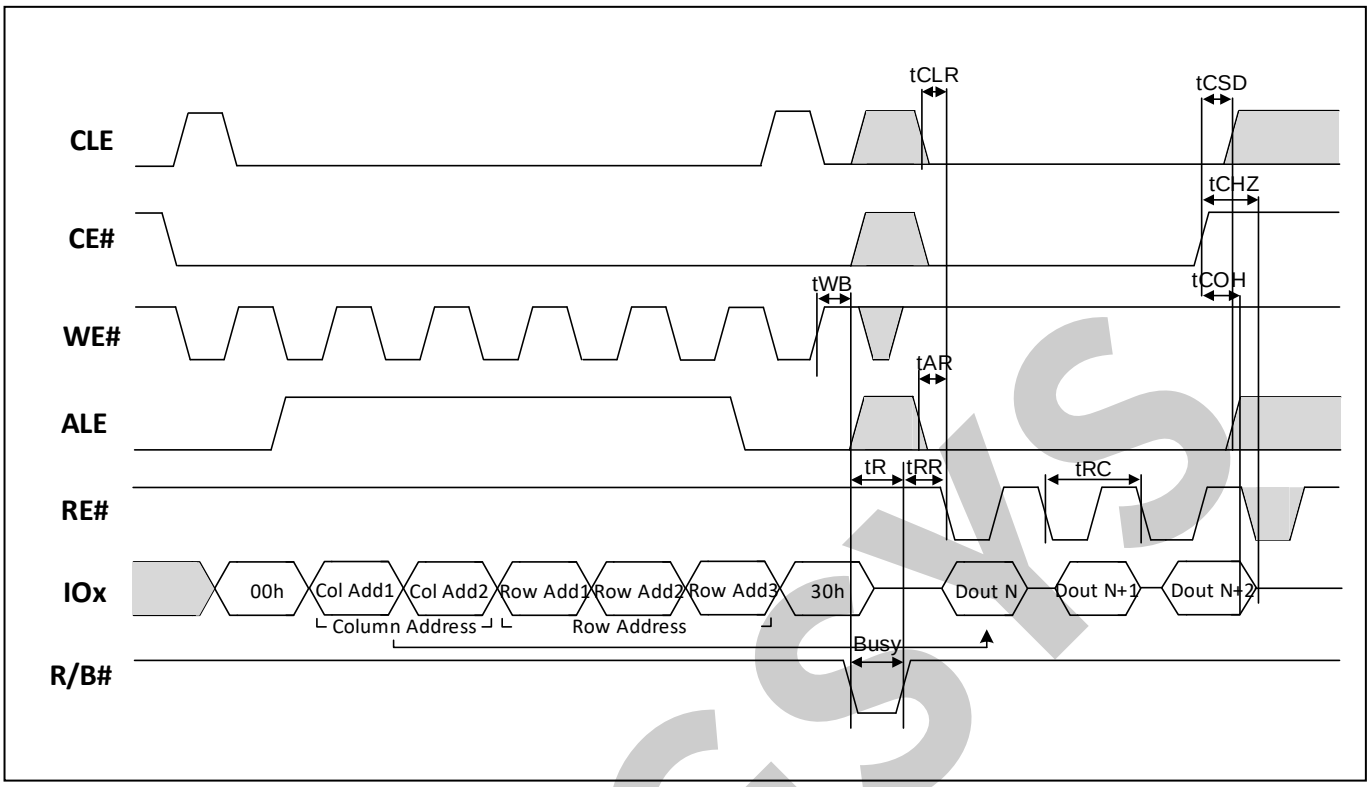


Figure 42 Random Data Output

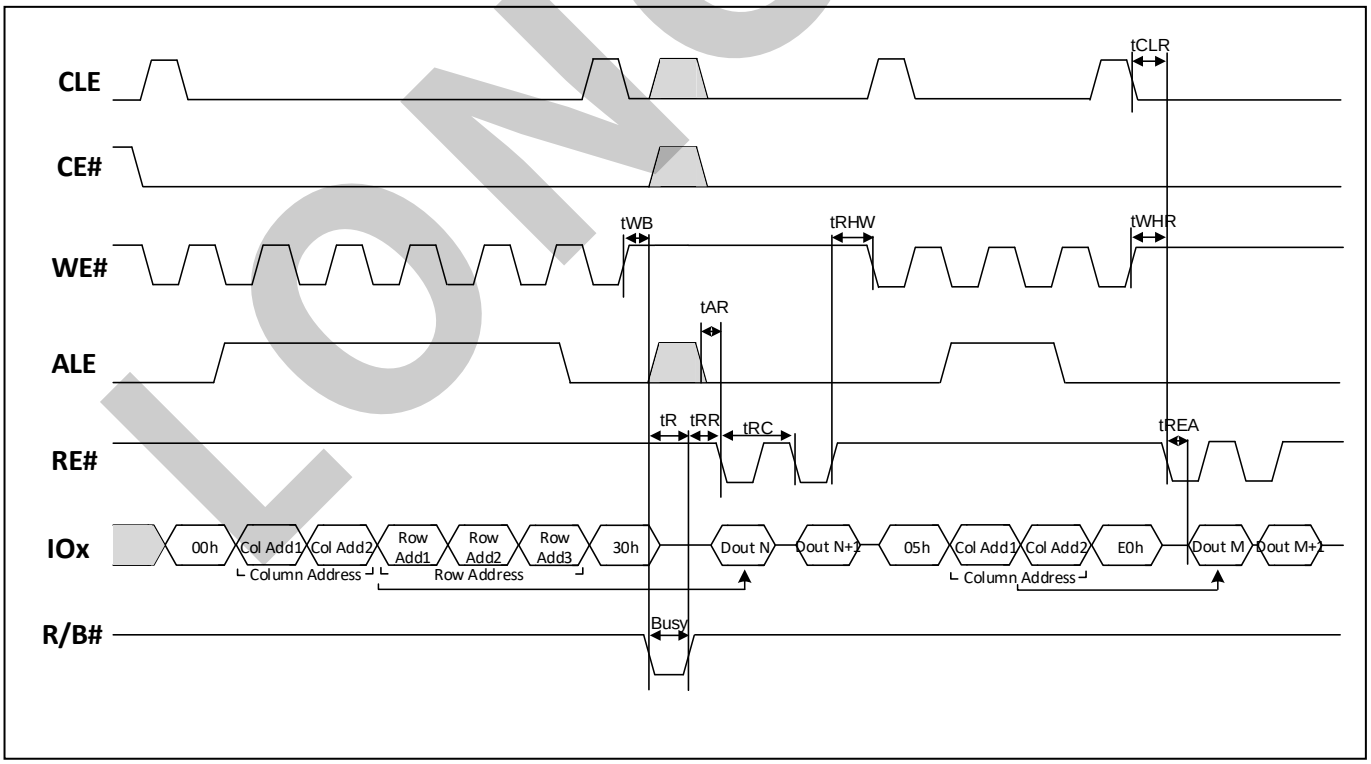


Figure 43 Page Program

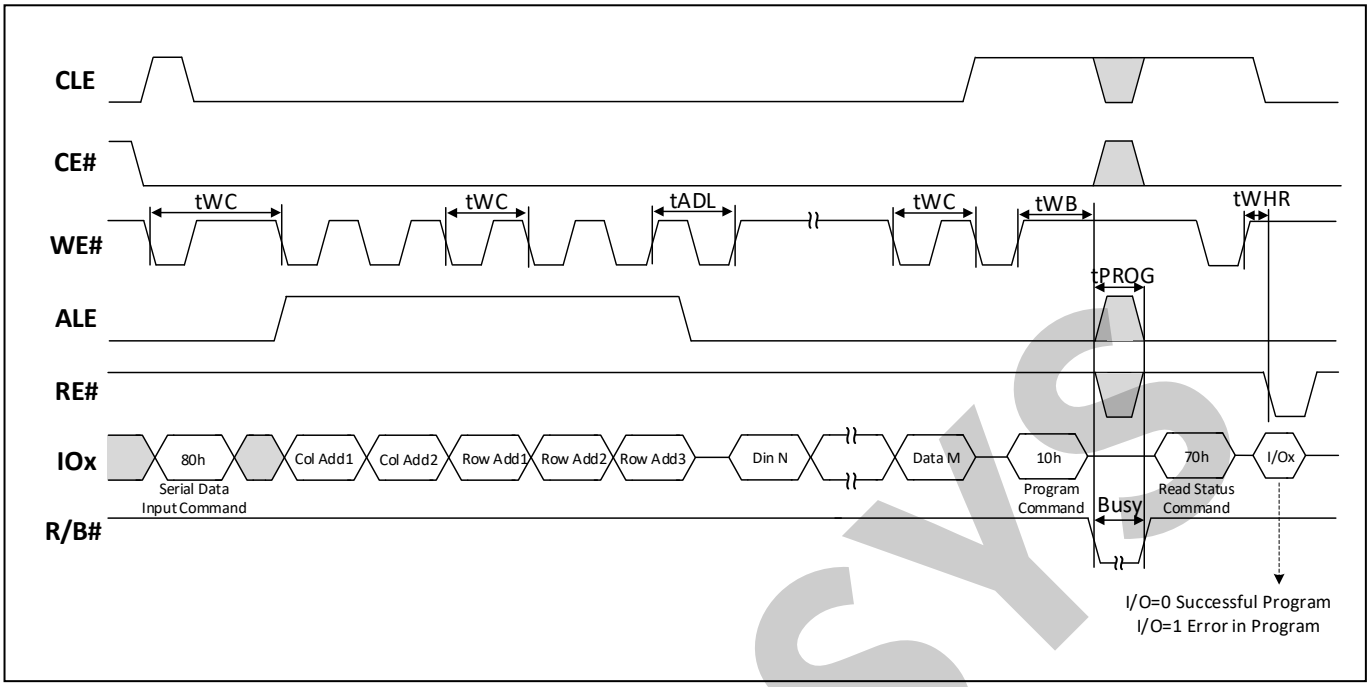


Figure 44 Copy-Back Program

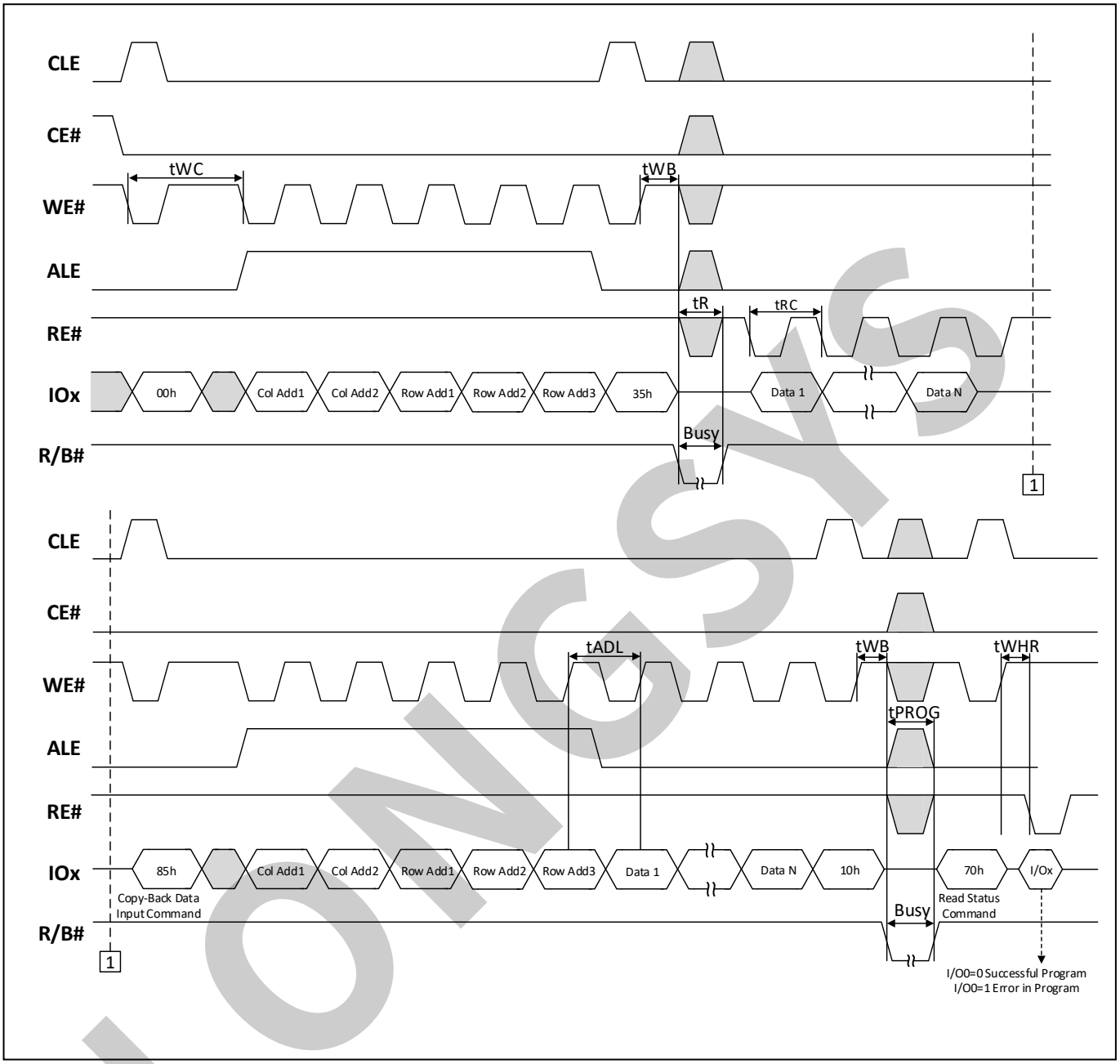


Figure 45 Copy-Back Program with Random Data Input

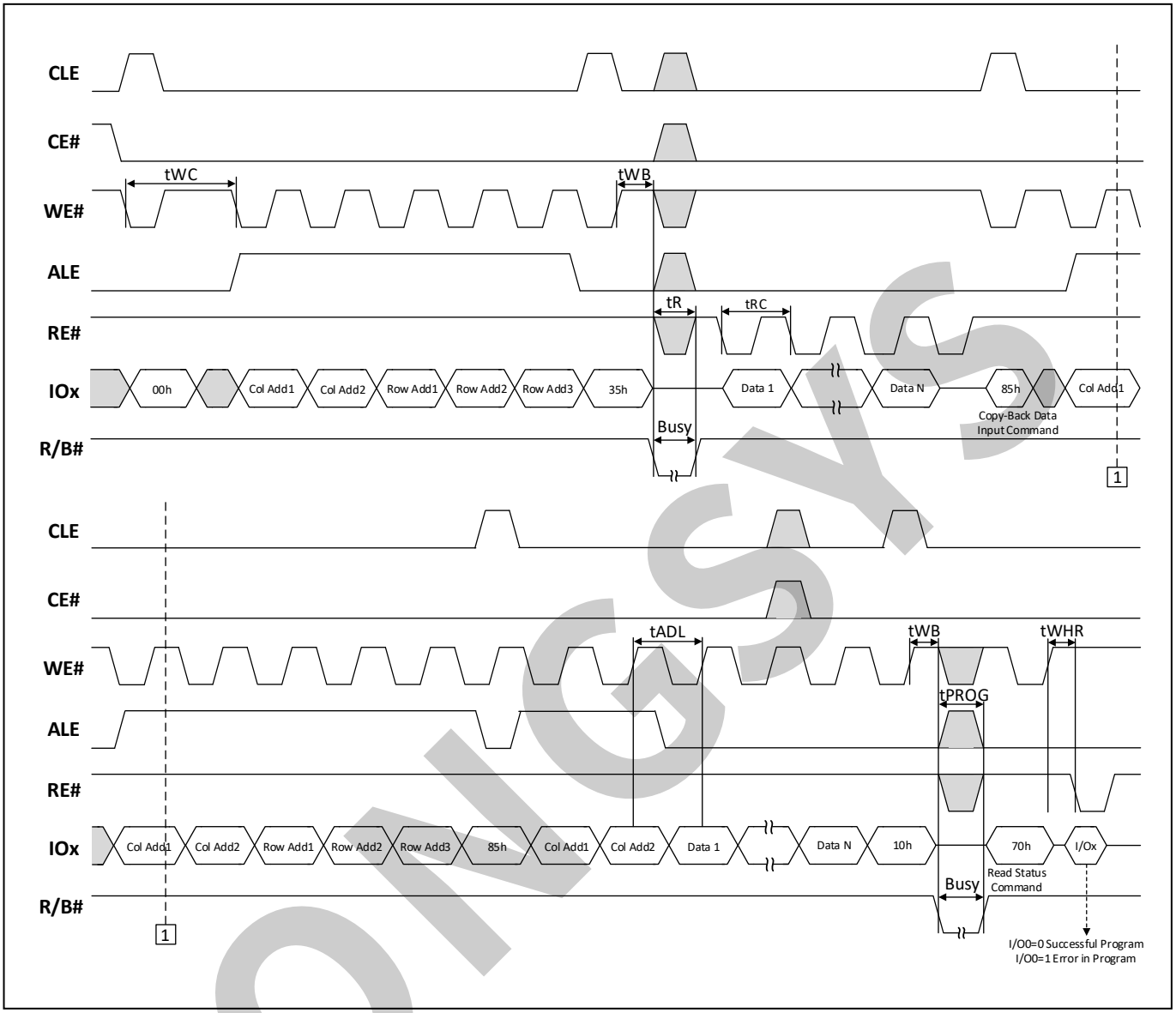


Figure 46 Page Program with Random Data Input

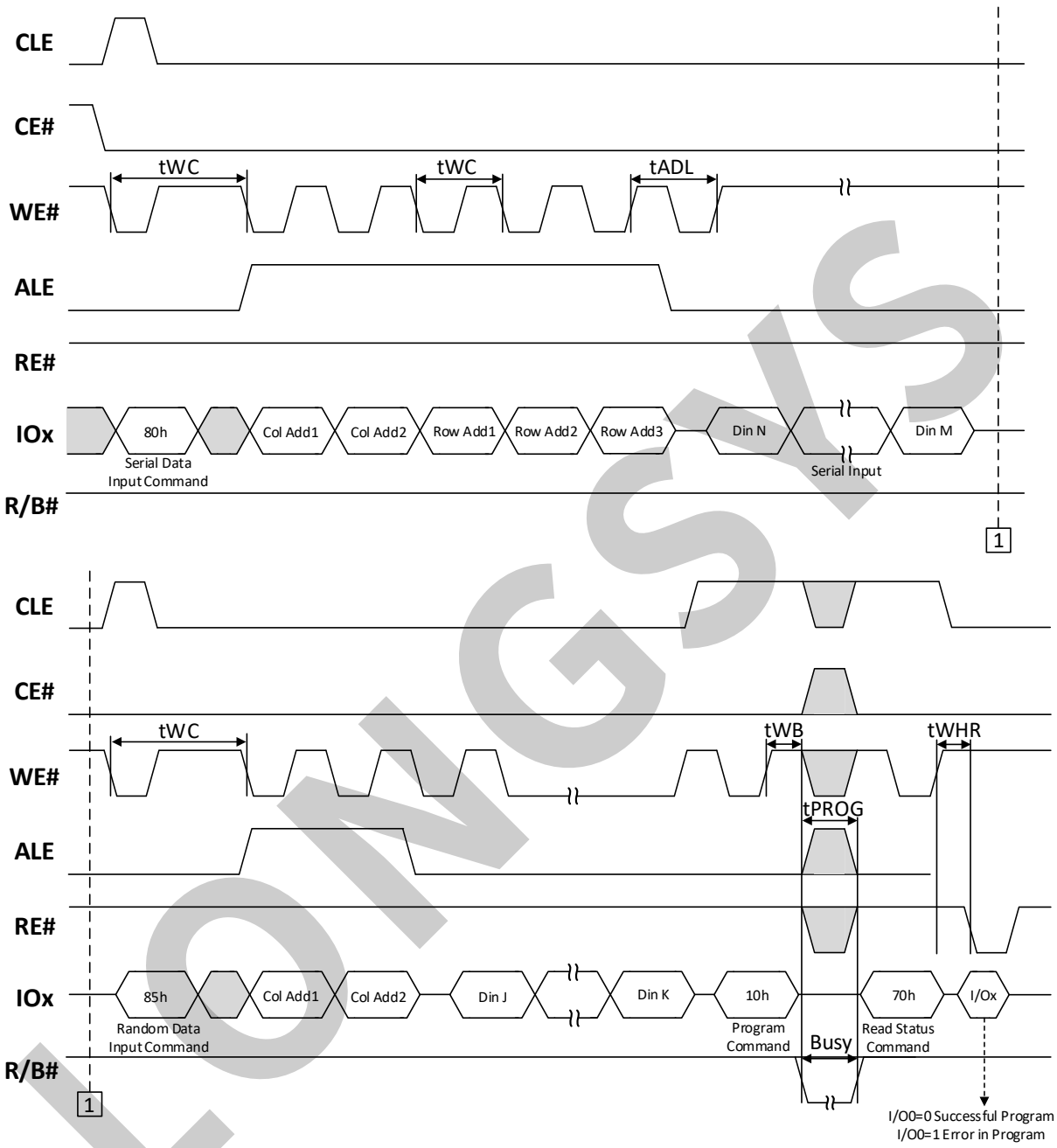


Figure 47 Block Erase

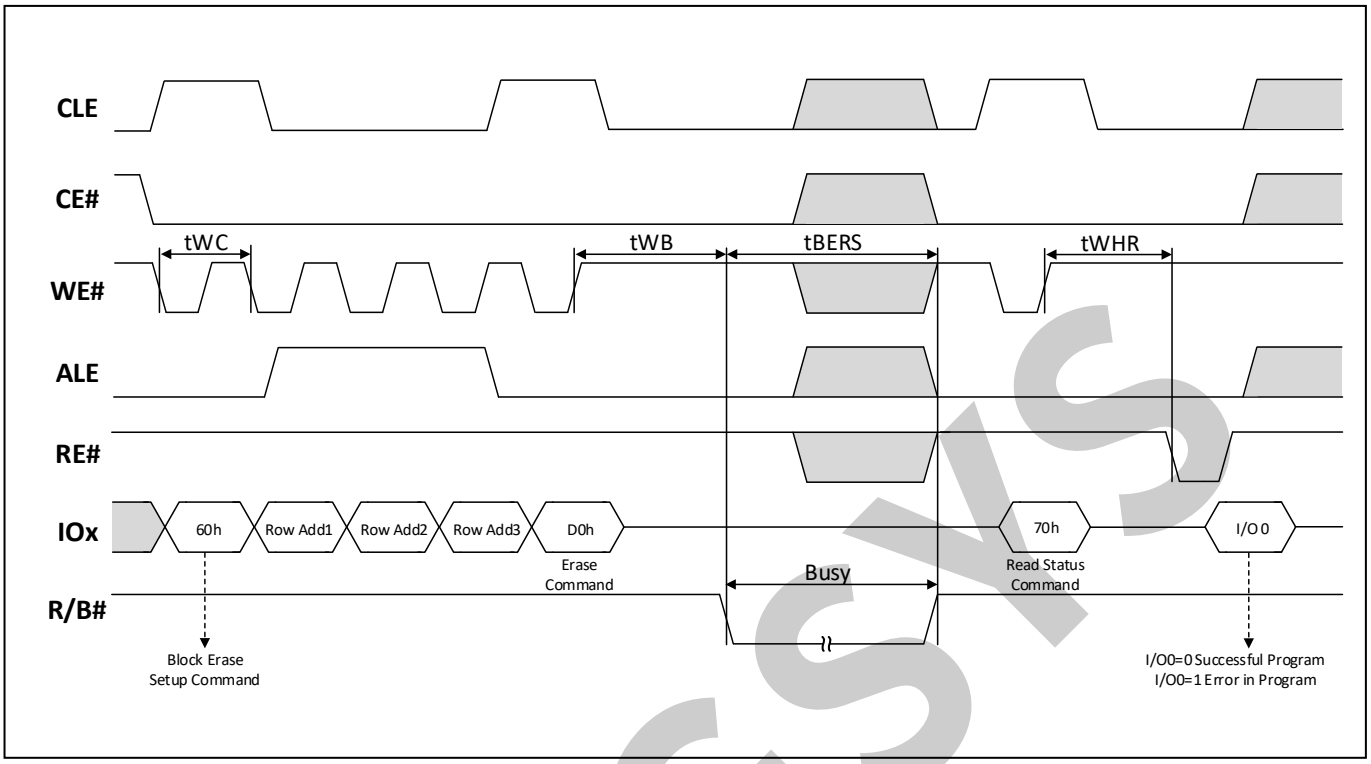
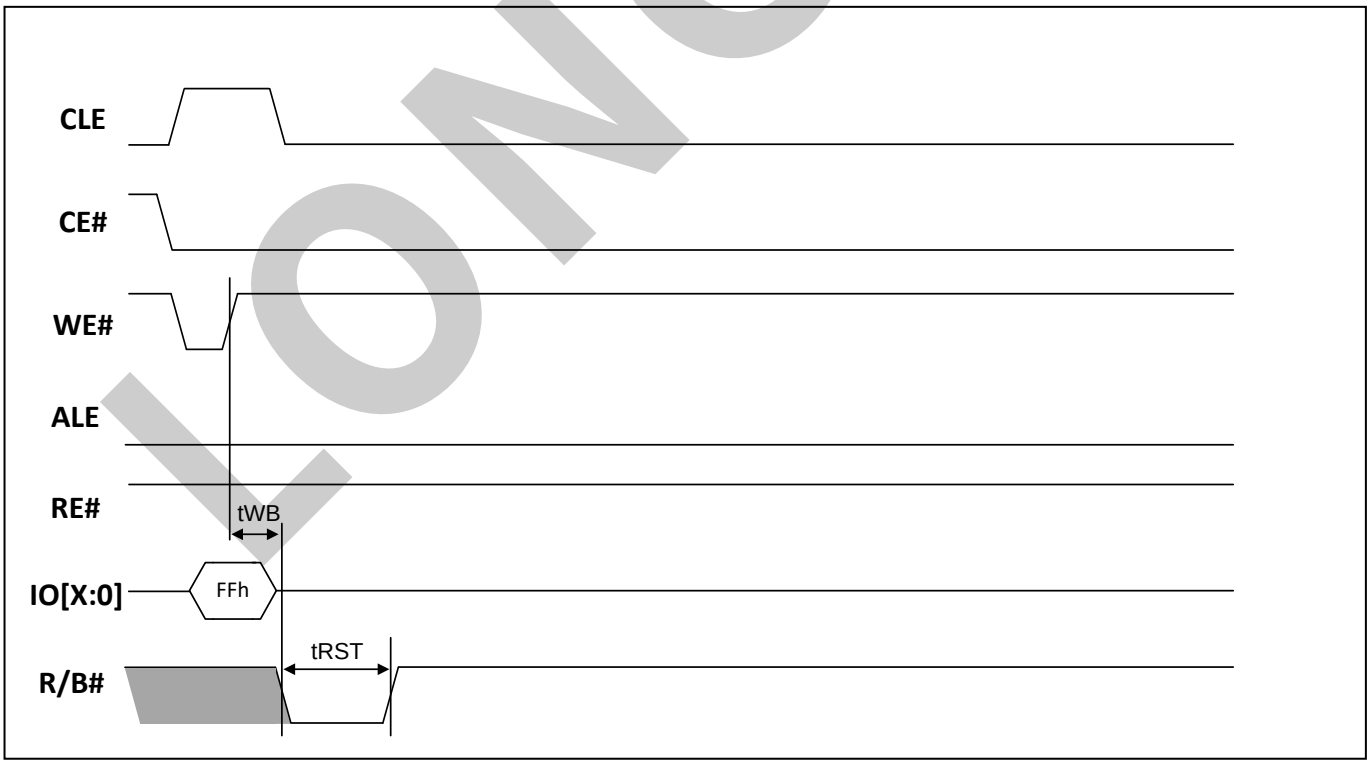


Figure 48 Reset



14 Packaging Information

14.1 48-TSOP (20x12mm)

Figure 49 48-TSOP (20x12mm) Package Information

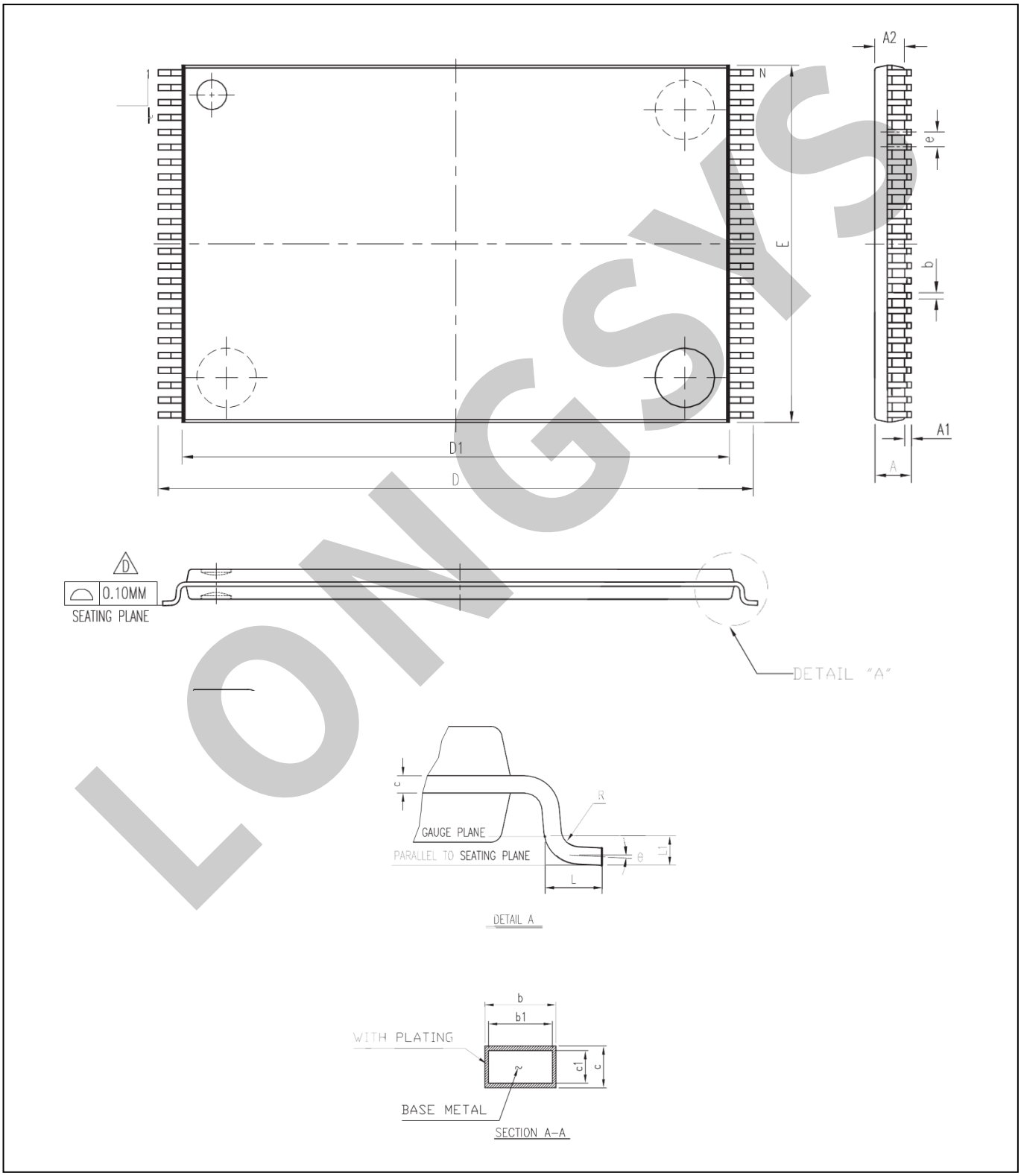


Table 22 48-TSOP Package Information

SYMBOL	Min. (mm)	Nom. (mm)	Max. (mm)
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.10		0.21
c1	0.10		0.16
e		0.50 BASIC	
L	0.50	0.60	0.70
L1	0.24	0.25	0.26
R	0.08		0.35
Θ	0°	5°	8°

14.2 63-TFBGA (11x9mm)

Figure 50 63-TFBGA (11x9mm) Package Information

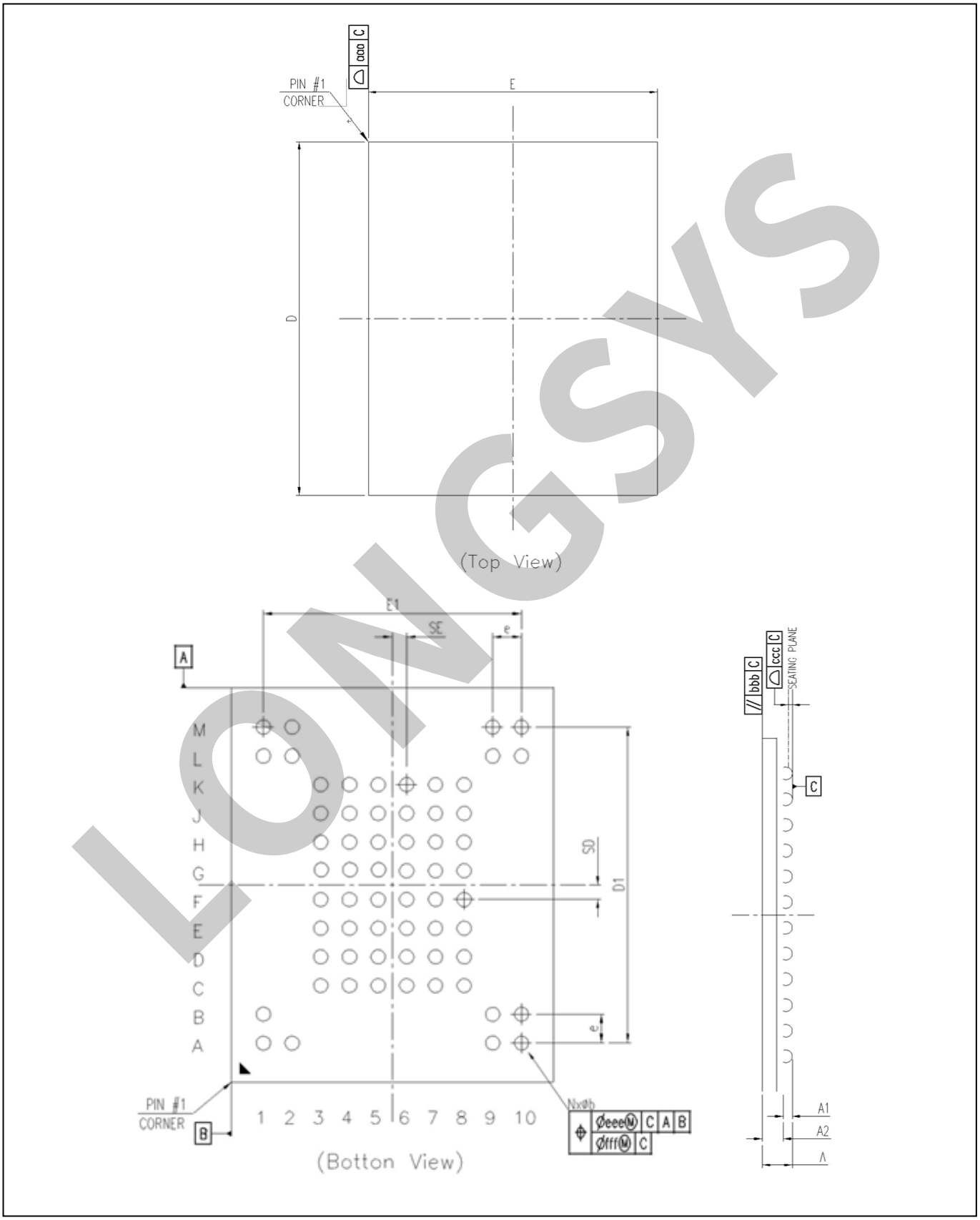
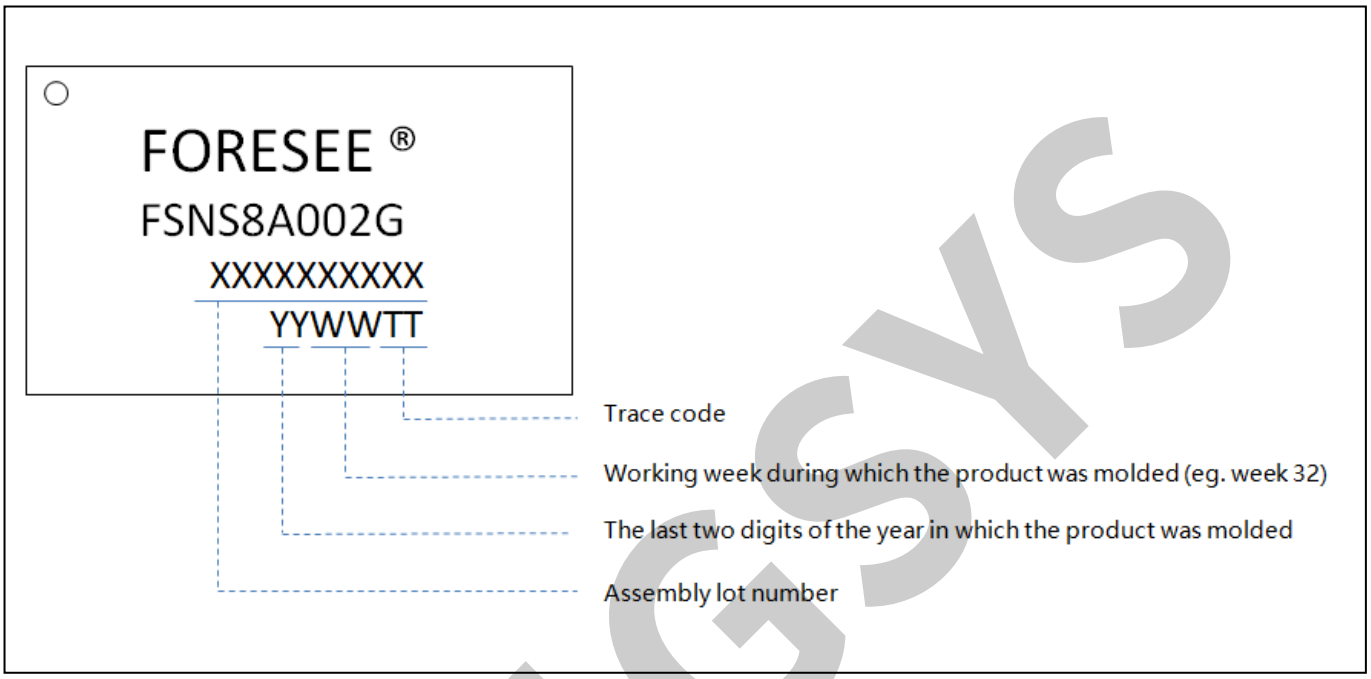


Table 23 63-TFBGA (11x9mm) Package Information

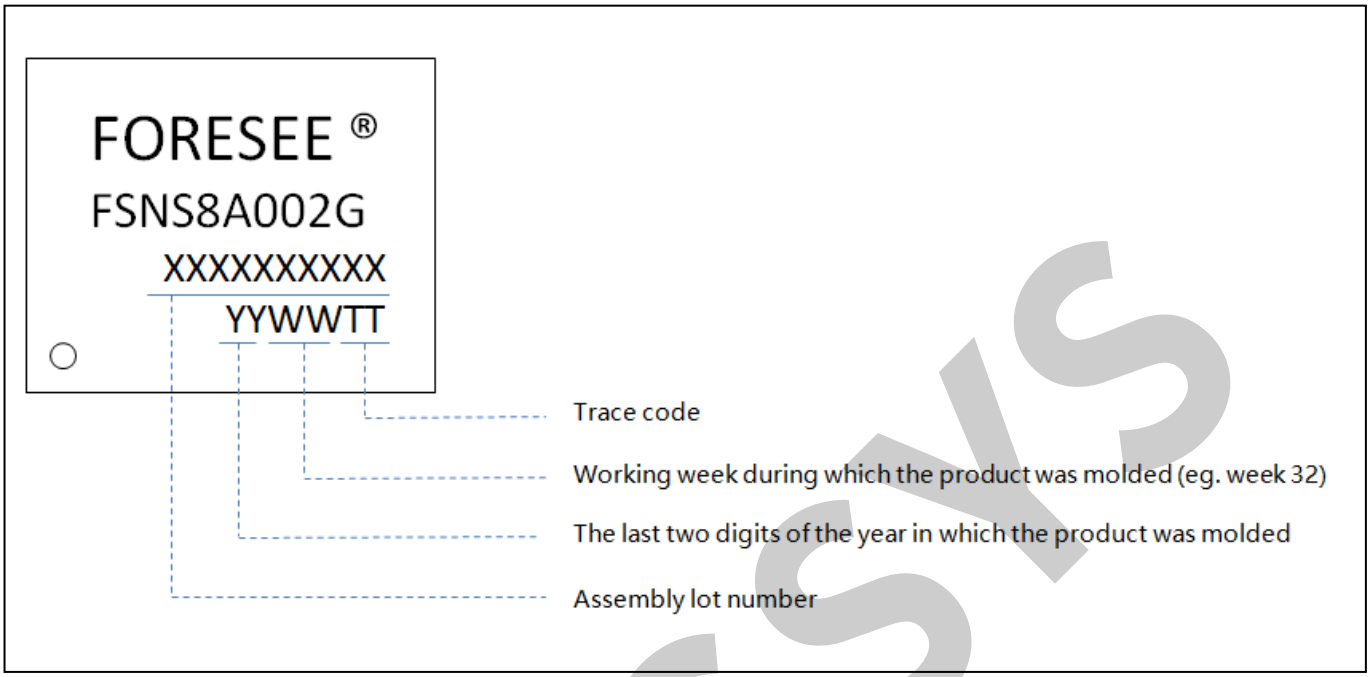
SYMBOL	Min. (mm)	Nom. (mm)	Max. (mm)
A			1.00
A1	0.25		0.31
A2		0.65	-
b	0.35	0.40	0.45
D	10.90	11.00	11.10
D1	8.80 BASIC		
SD	0.40 BASIC		
E	8.90	9.00	9.10
E1	7.20 BASIC		
SE	0.40 BASIC		
e	0.80 BASIC		
aaa	0.10		
bbb	0.20		
ccc	0.12		
eee	0.15		
fff	0.08		

15 Part Marking Scheme

15.1 48-TSOP (20x12mm)



15.2 63-TFBGA (11x9mm)



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