

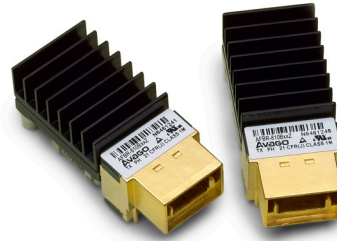
AFBR-810BxxxZ and AFBR-820BxxxZ

Twelve-Channel Transmitter and Receiver

Pluggable, Parallel-Fiber-Optic Modules



Data Sheet



Description

The AFBR-810B Twelve-Channel, Pluggable, Parallel-Fiber-Optic Transmitter and AFBR-820B Twelve-Channel, Pluggable, Parallel-Fiber-Optic Receiver are high performance fiber optic modules for short-range parallel multi-lane data communication and interconnect applications. These 12-channel devices are capable of 10.0 Gbps per channel, 120 Gbps raw aggregate operation. The modules are designed to operate over multimode fiber systems using a nominal wavelength of 850 nm. The electrical interface uses a 10x10 MEG-Array[®] low-profile mezzanine connector. The optical interface uses a MTP[®] (MPO) 1x12 ribbon cable connector. The thermal interface can be a factory installed heatsink for air-cooled systems or thermal seating plane for user flexibility. The modules incorporate high performance, highly reliable, short wavelength optical devices coupled with proven circuit technology to provide long life and consistent service.

Applications

- High Performance and High Productivity computer interconnects
- InfiniBand QDR SX interconnects
- Datacom switch and router backplane connections
- Telecom switch and router backplane connections

Part Number Ordering Options

Transmitter Part Numbers

| | |
|--------------|---------------------------------------|
| AFBR-810BZ | With Fin heat sink / no EMI nose clip |
| AFBR-810BEZ | With Fin heat sink / EMI nose clip |
| AFBR-810BPZ | With Pin heat sink / no EMI nose clip |
| AFBR-810BEPZ | With Pin heat sink / EMI nose clip |
| AFBR-810BHZ | With no heat sink / no EMI nose clip |
| AFBR-810BEHZ | With no heat sink/ EMI nose clip |

Receiver Part Numbers

| | |
|--------------|---------------------------------------|
| AFBR-820BZ | With Fin heat sink / no EMI nose clip |
| AFBR-820BEZ | With Fin heat sink / EMI nose clip |
| AFBR-820BPZ | With Pin heat sink / no EMI nose clip |
| AFBR-820BEPZ | With Pin heat sink / EMI nose clip |
| AFBR-820BHZ | With no heat sink / no EMI nose clip |
| AFBR-820BEHZ | With no heat sink/ EMI nose clip |

Features

- High Channel Capacity: 120 Gbps per module
- High port density: 19 mm lateral port pitch; < 0.51 mm/ Gbps for Tx–Rx pair
- Low power consumption per Gbps: < 42 mW/Gb/s for Tx–Rx pair
- Based on industry-standard, pluggable, SNAP12 form factor with upgraded pinout for improved signal integrity and keyed to prevent mis-plugging with first generation SNAP12 devices
- Twelve independent channels per module
- Separate transmitter and receiver modules
- 850 nm VCSEL array in transmitter; PIN array in receiver
- Operates up to 10 Gbps with 8b/10b compatible coded data
- Links up to 50 m at 10 Gbps with 2000 MHz-km 50 um MMF
- Two power supplies, 2.5 V and 3.3 V, for low power consumption
- Dedicated signals for module address, module reset and host interrupt.
- Two Wire Serial (TWS) interface with maskable interrupt for expanded functionality including:
 - Individual channel functions: disable, squelch disable, lane polarity inversion, margin
 - Programmable equalization integrated with DC blocking caps at transmitter data input
 - Programmable receiver output swing and de-emphasis level
 - A/D readback: module temperature and supply voltages, per channel laser current and laser power, or received power
 - Status: per channel Tx fault, electrical (transmitter) or optical (receiver) LOS, and alarm flags
- 0 to 70°C case temperature operating range

Transmitter Module

The optical transmitter module (see Figure 1) incorporates a 12-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 12-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. The transmitter is designed for IEC-60825 and CDRH eye safety compliance; Class 1M out of the module. The Tx Input Buffer provides CML compatible differential inputs (presenting a nominal differential input impedance of 100 Ohms and a nominal common mode impedance to signal ground of 25 Ohms) for the high speed electrical interface that can operate over a wide common mode range without requiring DC blocking capacitors. For module control and interrogation, the control interface (LVTTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for VCSEL bias, light output (LOP), temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential inputs, de-activate channels, place channels into margin mode,

disable the squelch function and program input equalization levels to reduce the effect of long PCB traces. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. The optical output will squelch for loss of input signal unless squelch is disabled. Fault detection or channel deactivation through the TWS interface will disable the channel. Status, alarm and fault information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm, LOS and/or Tx fault.

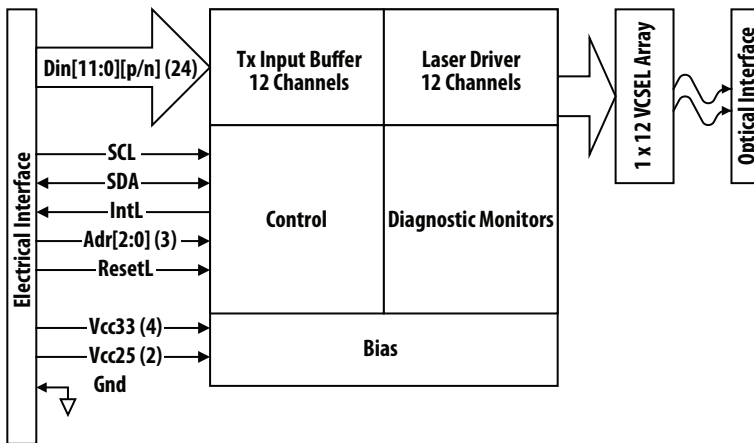


Figure 1. Transmitter Block Diagram

Receiver Module

The optical receiver module (see Figure 2) incorporates a 12-channel PIN photodiode array, a 12-channel pre-amplifier and output buffer, diagnostic monitors, control and bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ohms to AC ground and 100 Ohms differentially that should be differentially terminated with 100 Ohms. DC blocking capacitors may be required. For module control and interrogation, the control interface (LVTTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals and dedicated signals for host interrupt, module address setting and module reset. Diagnostic monitors for optical input power, temperature, both supply voltages and elapsed operating time are implemented and results are available through the TWS interface.

Over the TWS interface, the user can, for individual channels, control (flip) polarity of the differential outputs, de-activate channels, disable the squelch function,

program output signal amplitude and de-emphasis and change receiver bandwidth. A reset for the control registers is available. Serial ID information and alarm thresholds are provided. To reduce the need for polling, the TWS interface is augmented with an interrupt signal for the host.

Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of optical input signal (LOS). All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. Status and alarm information are available via the TWS interface. The interrupt signal (selectable via the TWS interface as a pulse or static level) is provided to inform hosts of an assertion of an alarm and/or LOS.

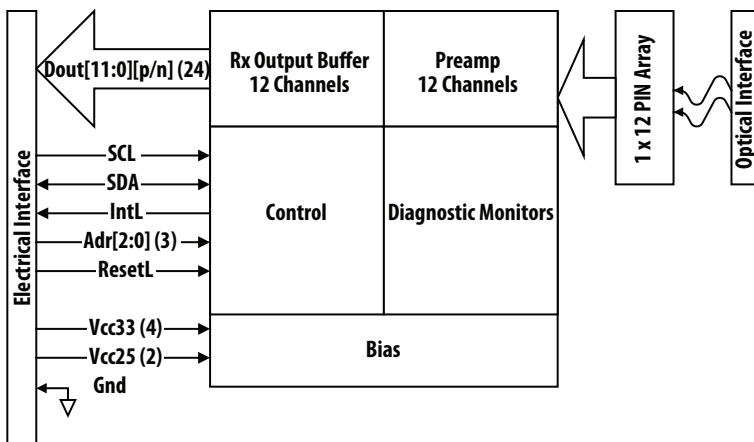


Figure 2. Receiver Block Diagram

High Speed Signal Interface

Figure 3 shows the interface between an ASIC/SerDes and the fiber Optic modules. For simplicity, only one channel is shown. As shown in the Figure 3, the compliance points are on the host board side of the electrical connectors. Sets of s-parameters are defined for the transmitter and receiver interfaces. The transmitter and receiver are designed, when operating within Recommended Operating Conditions, to provide a robust eye-opening at the receiver outputs. See the Recommended Operating Conditions and the Receiver Electrical Characteristics for details.

Unused inputs and outputs should be terminated with $100\ \Omega$ differential loads.

The transmitter inputs support a wide common mode range and DC blocking capacitors may not be needed – none are shown in Figure 3. Depending on the common mode range tolerance of the ASIC/SerDes inputs, DC blocking capacitors may be required in series with the receiver. Differential impedances are nominally $100\ \Omega$. The common mode output impedance for the receiver is nominally $25\ \Omega$ while the nominal common mode input impedance of the transmitter is $25\ \Omega$.

Transmitter Input Equalization

Transmitter inputs can be programmed for one of several levels of equalization. See Figure 4. Different levels of compensation can be selected to equalize skin-effect losses across the host circuit board. See Tx Memory Map 01h Upper Page section addresses 228 - 233 for programming details.

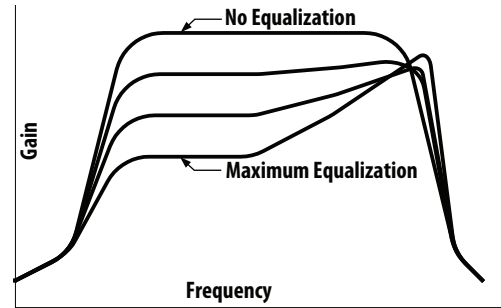


Figure 4. Input Equalization

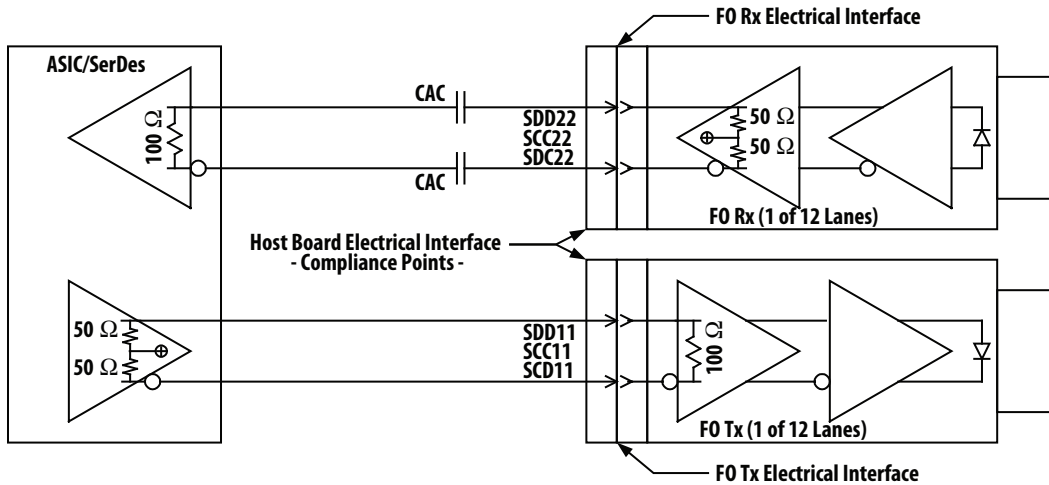


Figure 3. Application Reference Diagram

Receiver Output Amplitude and De-emphasis

Receiver outputs can be programmed to provide several levels of amplitude and de-emphasis. See Figure 5 for de-emphasis definition. The user can program for peak-to-peak amplitude and then a de-emphasis level. If zero de-emphasis is selected, then the signal steady state equals the peak-to-peak level. For other levels of de-emphasis the selected de-emphasis reduces the steady-state from the peak-to-peak level. The change from peak-to-peak level to steady-state occurs within a bit time. See Rx Memory Map 01h Upper Page section addresses 228 - 233 for amplitude programming details and addresses 234 - 239 for de-emphasis programming details. **For optimal performance at 10 Gb/s, lowering the De-Emphasis setting below the default value of 4 is not recommended.**

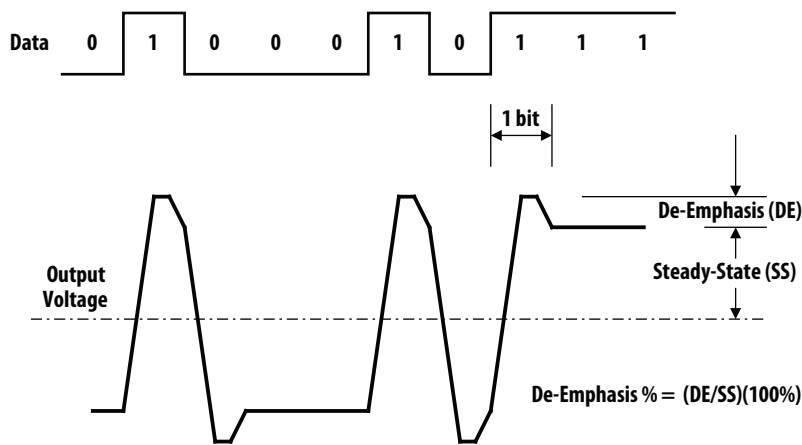


Figure 5. Definition of De-emphasis and Steady State

Control Signal Interface

The control interface includes dedicated signals for address inputs, interrupt output and reset input and bidirectional clock and data lines for a two-wire serial access (TWS interface) to control and status and information registers. The TWS interface is compatible with industry standard two-wire serial protocol scaled for 3.3 volt LVTTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface & Memory Map sections.

The registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Regulatory & Compliance Issues

Various standard and regulations apply to the modules. These include eye-safety, EMC, ESD and RoHS. See the Regulatory Section for details regarding these and component recognition. Please note the transmitter module is a Class 1M laser product – DO NOT VIEW RADIATION DIRECTLY WITH OPTICAL INSTRUMENTS. See Regulatory Compliance Table for details. When released, the AFBR- will support this table.

Package Outline

The module is designed to meet the package outline defined in the PPOD MSA. This MSA follows the outline of the SNAP12 MSA except for the position of the MEG-Array® connector and pin assignments. See the package outline and host board footprint figures (Figures 23 -26) for details.

Handling and Cleaning

The transmitter and receiver modules can be damaged by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Each module is supplied with an inserted port plug for protection of the optical ports. This plug should always be in place whenever a fiber cable is not inserted.

The optical connector includes recessed elements that are exposed whenever a cable or port plug is not inserted. Prior to insertion of a fiber optic cable, it is recommended that the cable end be cleaned to avoid contamination from the cable plug. The port plug ensures the Optic remain clean and no addition cleaning should be needed. In the event of contamination, dry nitrogen or clean dry air at less than 20 psi can be used to dislodge the contamination. The optical port features (e.g. guide pins) preclude use of a solid instrument. Liquids are also not advised.

Link Model and Reference Channel

Performance specifications for the AFBR-810 Transmitter and AFBR-820 Receiver are based on a reference channel model. A reference channel model provides the basis for inter-operability between independently produced transmitter and receiver modules. The reference model used for the AFBR-810 Transmitter and AFBR-820 Receiver is based on the industry standard 10GbE link model (10GEPBud3_1_16a.xls available at the IEEE P802.3ae 10Gb/s Ethernet Task Force Serial PMD Documents website http://www.ieee802.org/3/ae/public/adhoc/serial_pmd/documents/).

As shown in Figure 6, a channel for a fiber optic link comprises a transmitter, receiver and cable plant with inputs at test point TP1 and outputs at test point TP4. The test points TP1 and TP4 coincide with the compliance points defined in Figure 3. The cable plant here assumes a point to point link and does not include any inline connectors.

A reference channel permits the effect of various channel attributes to be referred to different points in the channel and accumulated. For example, in the GbE (All_1250.xls available at the IEEE website http://grouper.ieee.org/groups/802/3/10G_study/public/email_attach/All_1250.xls) and 10 GbE models all signal impairments are captured and translated into power penalties. Also, the effect of transmitter and fiber attributes are also captured and referred to TP3 to define stressed receiver test criteria. Similarly, all effects upstream of TP4 can be captured and referred to TP4 and combined at this point into a figure of merit. Since the signal at TP4 is electrical and not optical there are advantages for this.

To ensure inter-operability among independently produced transmitters and receivers, definition of acceptable devices is required. This can be accomplished on an individual parameter basis by setting min/max limits or with aggregates of attributes by establishing a figure of merit. Referring again to the 10GbE link model, the entity 'margin at target distance' is an aggregate figure of merit of all link attributes. There a set of link attributes will yield a specific

link margin and a worst case set of link attributes can be defined for a minimum level of performance. Instead of placing a maximum or minimum limit on each attribute, it is possible to allow elements in the set to shift (i.e. tradeoff with others within the set) as long as the desired margin is achieved. Further, if 'margin at target distance' can be translated into eye opening at TP4, the aggregate figure of merit is directly measurable. To preserve independence for transmitter, receiver and fibers, it is required that transmitter attributes only trade-off with other transmitter attributes and, similarly, receiver attributes can only trade-off with other receiver attributes.

In this data sheet, a minimum eye width at TP4 for a specified maximum BER is the figure of merit used to define acceptable link performance. Additional inputs and calculations have been added to the 10GbE link model to calculate eye closure and the effects of all impairments are referred to TP4 and combined as elements of eye closure. The minimum eye width at TP4 is included in tables, Transmitter Optical Characteristics and Receiver Electrical Characteristics, as minimum "Reference Link Output Eye Width". *The Recommended Operating Conditions table and those for transmitter and receiver characteristics provide the necessary attributes to define the worst case set for the reference channel. Various elements of this worst case set are labeled 'Informative' and are allowed to range outside the maximum or minimum limit for the individual element when there is a compensating improvement in others of the worst case subset. Transmitter attribute tradeoffs are limited to the transmitter subset and receiver tradeoffs are limited to the receiver subset.*

The following two tables summarizes the practical trade-offs between different informative transmitter parameters, as well as different informative receiver parameters, respectively. Although the wavelength and spectral width can also trade off with each other, they are not included here for interoperability reason.

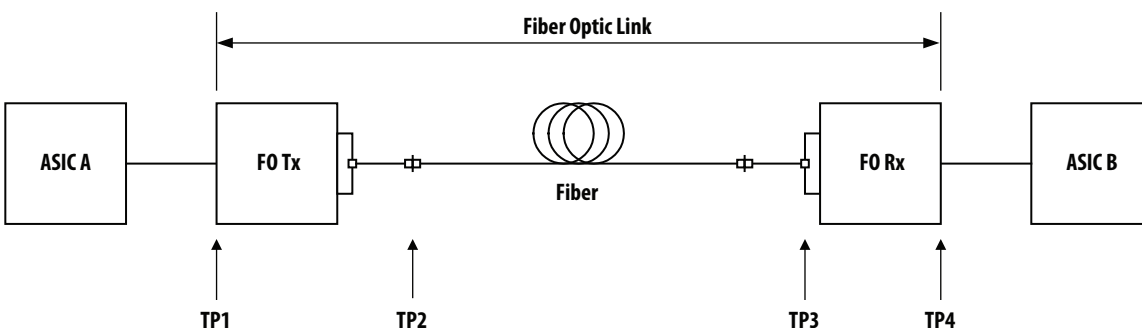


Figure 6. Fiber Optic Link

Informative TX parameters trading off each other while guaranteeing TP2 & TP4 performance

| Parameter | Symbol |
|---|-----------------------|
| Extinction Ratio | ER |
| Output Optical Modulation Amplitude | OMA |
| Output Rise/Fall Time | |
| Relative Intensity Noise OMA | RIN ₁₂ OMA |
| Contributed Portion of Accumulated Deterministic Jitter | |
| Contributed Portion of Accumulated Total Jitter | |

Informative RX parameters trading off each other while guaranteeing TP4 performance

| Parameter | Symbol |
|---|--------|
| Receiver Bandwidth (BW) | |
| Input Optical Power Sensitivity (OMA) | |
| Contributed Portion of Accumulated Deterministic Jitter | |
| Contributed Portion of Accumulated Total Jitter | |

The reference model for testing transmitters consists of a pattern generator, fiber optic test cable, attenuator, test receiver and BERT. See Figure 7 for the evolution of a reference channel to a transmitter test channel. Differences between the worst case values for attributes in the reference model and those in the test equipment set can be compensated by an added attenuator (note that the 10GbE model translates all impairments into power penalties) and adjustments in TJ criteria at TP4. Differences in the TP1 input jitter between the defined conditions, TJ_r and DJ_r, for the reference channel and actually provided in the test channel, TJ_t and DJ_t, can also be accommodated by adjustments to TP4 test criteria (TJ_r becomes TJ_t). The extended 10GbE Link model is used to determine the compensating attenuation and TP4 criteria adjustments.

The reference for testing receivers consists of a pattern generator, test transmitter, fiber optic test cable, attenuator and BERT. See Figure 8 for the evolution of a reference channel to a receiver test channel. In a similar manner as with the transmitter, all differences between the test equipment and worst case channel are compensated with an attenuator and adjustments in the TP4 criteria.

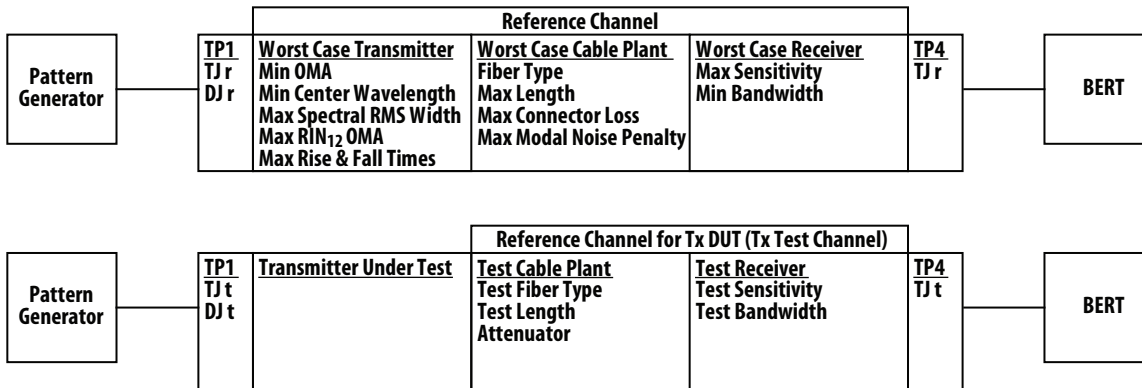


Figure 7. Reference and Test Channels for Transmitter

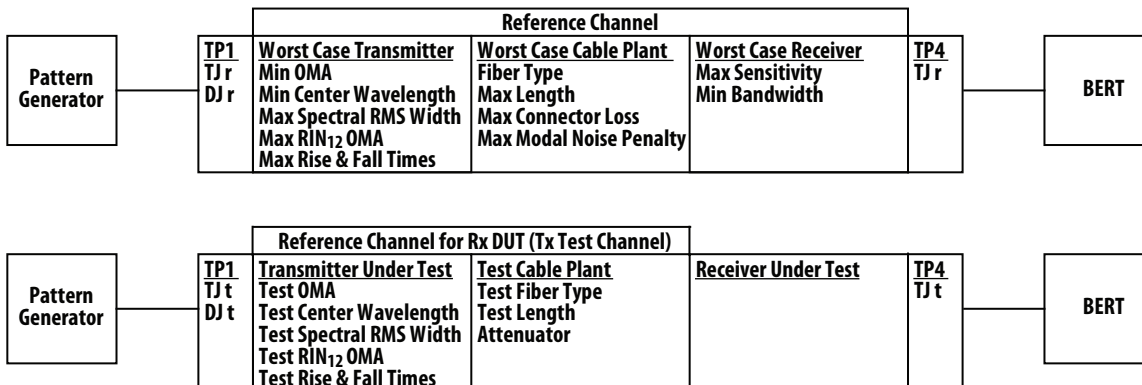


Figure 8. Reference and Test Channels for Receiver

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operation Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

| Parameter | Symbol | Min | Max | Units | Notes |
|-----------------------------------|-------------------------------------|------|--|-------|-------|
| Storage Temperature | T _S | -40 | 100 | °C | |
| Case Temperature – Operating | T _{C AMR} | -20 | 90 | °C | 1 |
| 2.5 V Power Supply Voltage | V _{CC25} | -0.5 | 3.0 | V | |
| 3.3 V Power Supply Voltage | V _{CC33} | -0.5 | 3.6 | V | |
| Data Input Voltage – Single Ended | | -0.5 | V _{CC33+0.5} , V _{CC25+0.5} | V | 2 |
| Data Input Voltage – Differential | V _{DIP} - V _{DIN} | | 1.0 | V | 3 |
| Control Input Voltage | V _i | -0.5 | V _{CC33+0.5} , 3.6 | V | 4 |
| Control Output Current | I _o | -20 | 20 | mA | |
| Relative Humidity | RH | 5 | 95 | % | |

Notes:

1. The position for case temperature measurement is shown in Figure 11. Operation at or above the maximum Absolute Maximum Case Temperature for extended periods may adversely affect reliability. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions.
2. The maximum limit is the lesser of V_{CC33} + 0.5 V or V_{CC25} + 0.5 V.
3. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry.
4. The maximum limit is the lesser of V_{CC33} + 0.5 V or 3.6 V.

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

| Parameter | Symbol | Min | Typ | Max | Units | Reference |
|--|---------------------|-------|-----|-----------------|-------|----------------------|
| Case Temperature | T_C | 0 | 40 | 70 | °C | 1 |
| 2.5 V Power Supply Voltage | V_{CC25} | 2.375 | 2.5 | 2.625 | V | Figures 12, 13 |
| 3.3 V Power Supply Voltage | V_{CC33} | 3.135 | 3.3 | 3.465 | V | Figures 12, 13 |
| Signal Rate per Channel | | 2.5 | | 10 | GBd | 2 |
| Data Input Differential Peak-to-Peak Voltage Swing | $\Delta V_{DI\ pp}$ | 175 | | 1400 | mVpp | 3, Figure 14 |
| Data Input Common Mode Voltage | $V_{DI\ CM}$ | 0.35 | | $V_{CC33}-0.35$ | V | 4 |
| Data Input Rise & Fall Times (20% - 80%) | | 30 | | 48 | ps | |
| Data Input Deterministic Jitter | | | | 15 | ps | 5 |
| Data Input Total Jitter | | | | 30 | ps | 6 |
| Control* Input Voltage High | V_{ih} | 2 | | V_{CC33} | V | |
| Control* Input Voltage Low | V_{il} | GND | | 0.8 | V | |
| Two Wire Serial Interface Clock Rate | | | | 400 | kHz | Figure 17 |
| Two Wire Serial Interface Write Cycle Time | T_{Wr} | 40 | | | mS | |
| Reset Pulse Width | $t_{RSTL\ PW}$ | 10 | | | µs | Figure 19 |
| Power Supply Noise | | | | 100 | mVpp | 7, 500 Hz to 2.7 GHz |
| Receiver Differential Data Output Load | | | 100 | | Ohms | Figure 3 |
| AC Coupling Capacitors – Receiver Data Outputs | C_{ac} | | 0.1 | | µF | 8, Figure 3 |
| Fiber Length: 2000 MHz-km 50µm MMF | | 0.5 | | 50 | m | 9 |

Notes:

* Control signals, LVTTTL (3.3 V) compatible, include Adr[2:0], IntL, ResetL, SCL and SDA.

- The position for case temperature measurement is shown in Figure 11. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability. Modules will function (degraded performance may result) where operated with case temperatures below the minimum Recommended Operating Case Temperature.
- While operation for various codes, e.g. 8b10b and 64b66b, are supported, certain parameters, jitter and sensitivity, are defined for specific operating conditions of 10 GBd and 8b/10b equivalent test patterns. The receiver has a low frequency -3dB (electrical) corner near 100 kHz.
- Data inputs are CML compatible. Minimum input requirement holds for default input equalization settings. Data Input Differential Peak to Peak Voltage Swing is defined as follows: $\Delta V_{DI\ pp} = \Delta V_{DIH} - \Delta V_{DIL}$ where ΔV_{DIH} = High State Differential Data Input Voltage and ΔV_{DIL} = Low State Differential Data Input Voltage.
- Data Input Common Mode Voltage is defined as follows: $V_{DI\ CM} = (V_{Dinp} + V_{Dinn})/2$.
- Deterministic Jitter, DJ, conforms to the dual-Dirac model where $TJ(BER) = DJ + 2Q(BER)RJ_{rms}$ and RJ_{rms} is the width of the Gaussian component. Here $BER = 10^{-12}$. DJ is measured with the same conditions as TJ. Effects of impairments in the test signal due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
- Total Jitter, TJ, defined for a BER of 10^{-12} , is measured at the 50% signal level using test pattern 2 defined in IEEE P802.3ae clause 52.9.1, or equivalent, operating at 10 GBd. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
- Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figures 12 and 13 for recommended power supply filters.
- For data patterns with restricted run lengths and disparity, e.g. 8b10b, smaller value capacitors may provide acceptable results.
- Channel insertion loss includes 3.5 dB/km attenuation, 0 dB connector loss and 0.3 dB modal noise penalty allocations.

Transmitter Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for $T_c = 40^\circ\text{C}$, $V_{cc33} = 3.3\text{ V}$ and $V_{cc25} = 2.5\text{ V}$.

| Parameter | Symbols | Min | Typ | Max | Units | Reference |
|--|--------------------------|-----|-----|-----|----------|--------------|
| Power Consumption | | | | 2.4 | W | |
| Power Supply Current – Vcc25 | | | | 380 | mA | 1 |
| Power Supply Current – Vcc33 | | | | 425 | mA | 12 |
| Differential Input Impedance | | 80 | | 120 | Ω | Informative |
| Differential Input Reflection Coefficient | S_{DD11} | | -8 | | dB | 3, Figure 3 |
| Common Mode Input Reflection Coefficient | S_{CC11} | | -6 | | dB | 4, Figure 3 |
| Differential to CM Input Reflection Coefficient | S_{CD11} | | -35 | | dB | 5, Figure 3 |
| LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing | $\Delta V_{DI\ PP\ LOS}$ | 58 | 120 | 156 | mVpp | |
| LOS Hysteresis: Tx Data Input | | 1 | | 4 | dB | 6 |
| Power On Initialization Time | $t_{PWR\ INIT}$ | | | 500 | ms | 7, Figure 18 |

Notes:

* For control signal timing including $Adr[2:0]$, $IntL$, $ResetL$, SCL and SDA see Control Characteristics: Transmitter/Receiver.

1. Supply current includes that of all V_{cc25} contacts.
2. Supply current includes that of all V_{cc33} contacts.
3. Measured over the range 100 MHz to 3.75 GHz with reference differential impedance of $100\ \Omega$
4. Measured over the range 100 MHz to 3.75 GHz with reference common mode impedance of $25\ \Omega$
5. Measured over the range 100 MHz to 3.75 GHz with reference differential impedance of $100\ \Omega$
6. LOS Hysteresis is defined as $20\ \text{Log}(\text{LOS De-assert Level} / \text{LOS Assert Level})$.
7. Power On Initialization Time is the time from when the supply voltages reach and remain above the minimum Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.

Receiver Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for $T_c = 40^\circ\text{C}$, $V_{cc33} = 3.3\text{ V}$ and $V_{cc25} = 2.5\text{ V}$.

| Parameter | Symbol | Min | Typ | Max | Units | Reference |
|--|----------------------|-------|-----|------------|---------------|--|
| Power Consumption | | | | 2 | W | 1 |
| Power Supply Current (V_{cc25}) | | | | 670 | mA | 2 |
| Power Supply Current (V_{cc33}) | | | | 200 | mA | 3 |
| Data Output Differential Peak-to-Peak Voltage Swing (Zero De-emphasis) | $\Delta V_{DO\ pp}$ | 775 | 850 | 925 | mVpp | 4, Figure 14, 100 Ω Load Full Scale Setting |
| | | 415 | 490 | 565 | | Default Amplitude Setting |
| Data Output Common Mode Voltage | $V_{DO\ CM}$ | 1.785 | | 2.540 | V | 5, Figure 14, Over Amplitude Setting Range |
| Data Output Off State Differential Voltage | $\Delta V_{DO\ OFF}$ | | | 20 | mVpp | |
| Data Output Off Common Mode Voltage | $V_{DO\ OFF\ CM}$ | | | V_{cc25} | V | |
| Output Rise/Fall time (20-80%) | | | | 80 | ps | 6 |
| LOS to Data Output Squelch Assert Time | $t_{SQ\ ON}$ | | | 80 | μs | 7, Figure 22 |
| Data Output Squelch De-assert Time | $t_{SQ\ OFF}$ | | | 300 | μs | 8, Figure 22 |
| Reference Link Output Deterministic Jitter | | | | 35 | ps | 9, Informative |
| Reference Link Output Total Jitter | | | | 70 | ps | 10 |
| Reference Link Output Eye Width | $t_{EYE\ LINK}$ | 30 | | | ps | 11 |
| Differential Output Impedance | | 80 | | 120 | Ω | Informative |
| Differential Output Reflection Coefficient | S_{DD22} | | -10 | | dB | 12, Figure 3 |
| Common Mode Output Reflection Coefficient | S_{CC22} | | -8 | | dB | 13, Figure 3 |
| CM to Differential Output Reflection Coefficient | S_{DC22} | | -35 | | dB | 14, Figure 3 |
| Power On Initialization Time | $t_{PWR\ INIT}$ | | | 500 | ms | 15, Figure 18 |
| Inter-channel Skew | | | | 150 | ps | 16 |
| Rx Input-Output Latency | | | | 600 | ps | Informative |

Notes:

- * For control signal timing including $Adr[2:0]$, $IntL$, $ResetL$, SCL and SDA see Control Characteristics: Transmitter/Receiver.
- 1. Max conditions include default output amplitude and de-emphasis programming.
- 2. Supply current includes that of all V_{cc25} contacts. Max conditions include maximum output amplitude and de-emphasis programming.
- 3. Supply current includes that of all V_{cc33} contacts. Max conditions include maximum output amplitude and de-emphasis programming.
- 4. Data outputs are CML compatible. Data Output Differential Peak to Peak Voltage Swing is defined as follows: $\Delta V_{DO\ pp} = \Delta V_{DOH} - \Delta V_{DOL}$ where ΔV_{DOH} = High State Differential Data Output Voltage and ΔV_{DOL} = Low State Differential Data Output Voltage. Impairments in measurements due to the test system are removed.
- 5. Data Output Common Mode Voltage is defined as follows: $V_{DO\ CM} = (V_{Doutp} + V_{Doutn})/2$.
- 6. These are unfiltered rise and fall times without de-emphasis measured between the 20% and 80% levels using a 500 MHz square wave test pattern. Impairments in measurements due to the test system are removed.
- 7. This is the module response time from fall of Rx input to less than Rx input LOS threshold to squelch of Rx outputs.
- 8. This is the module response time from rise of Rx input to greater than Rx input LOS threshold to resumption of Rx outputs.
- 9. Deterministic Jitter, DJ, conforms to the dual-Dirac model where $TJ(BER) = DJ + 2Q(BER)R_{Jrms}$ and R_{Jrms} is the width of the Gaussian component. Here $BER = 10^{-12}$. DJ is measured with the same conditions as TJ. The receiver output is measured with default de-emphasis. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns at an input signal 6 dB above maximum Receiver Sensitivity.
- 10. Total Jitter, TJ, defined for BER of 10^{-12} , is measured at the 50% signal level using test pattern 2 defined in IEEE P802.3ae clause 52.9.1, or equivalent, operating at 10 Gb/s with characteristics that are equivalent to that of an AFBR 810B transmitter module and maximum cable length operating per the Recommended Operation Conditions as the test source. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
- 11. Eye Opening is defined as the unit interval less TJ for the same test pattern and conditions as TJ.
- 12. Measured over the range 100 MHz to 3.75 GHz with reference differential impedance of 100 Ω
- 13. Measured over the range 100 MHz to 3.75 GHz with reference common mode impedance 25 Ω
- 14. Measured over the range 100 MHz to 3.75 GHz with reference differential impedance 100 Ω
- 15. Power On Initialization Time is the time from when the supply voltages reach and remain within Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.
- 16. Inter-Channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.

Control Characteristics: Transmitter/Receiver

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for $T_c = 40^\circ\text{C}$, $V_{cc33} = 3.3\text{ V}$ and $V_{cc25} = 2.5\text{ V}$.

| Parameter | Symbol | Min | Typ | Max | Units | Reference |
|--|-----------------------|------|-----|------|-------|--|
| Control* Input Voltage Hysteresis LVTTTL | V _{hys} | | 0.4 | | V | |
| Control* Input Current LVTTTL | I _{in} | -125 | | 125 | μA | 0 V < V _{in} < V _{cc33} |
| Control* Output Voltage Low LVTTTL | V _{ol} | | | 0.4 | V | I _{ol} = 2mA |
| Control* Output Current High-Z | I _{oh} | -10 | | 10 | μA | 0 V < V _{in} < V _{cc33} |
| Address Assert Time | | | | 100 | ms | 1 |
| Interrupt Assert Time | t _{INTL ON} | | | 200 | ms | 2, Figure 20 |
| Interrupt Pulse Width | t _{INTL PW} | 5 | | | μs | 3, Figure 20 |
| Interrupt De-assert Time | t _{INTL OFF} | | | 500 | μs | 4, Figure 20 |
| Reset Assert Time | t _{RSTL ON} | | | 100 | μs | 5, Figure 19 |
| Reset De-assert Time | t _{RSTL OFF} | | | 500 | ms | 6, Figure 19 |
| Initialization Time TWS Interfaces | | | | 500 | ms | Figure 18 |
| TWS Data In Set Up Time | t _{SU:SDA} | | | 0.10 | μs | 7, Figure 17 |
| TWS Data In Hold Time | t _{HD:SDA} | | | 0 | μs | 8, Figure 17 |
| TWS Clock Low to Data Out Valid | t _{AA} | 0.10 | | 0.90 | μs | 9, Figure 17 |
| TWS Data Out Hold Time | t _{DH} | 50 | | | ns | 10, Figure 17 |
| TWS Data Output Rise Time | t _{r SDA} | | | 0.30 | μs | Figure 17, Measured between 0.8V and 2.0V |
| TWS Data Output Fall Time | t _{f SDA} | | | 0.30 | μs | Figure 17, Measured between 0.8V and 2.0V |
| TWS Interface Timing | | | | | | See Atmel Two-Wire Serial EEPROM, e.g. AT24C01A |
| TWS Write Cycle Time | t _{wr} | 40ms | | | | |

Notes:

* Control signals include ADR[2:0], INTL, RESETL, SCL and SDA.

1. This is the module response time from a change in module address, ADR[2:0], to response to TWS communication using the new address.
2. This is the module response time from occurrence of interrupt generating event to INTL assertion, V_{out:INTL} = V_{ol}.
3. Pulse or static level can be selected for INTL. Pulse mode is default. See Memory Map.
4. This is the module response time from clear on read operation, measured from falling SCL edge after stop bit of read transaction, until V_{out:INTL} = V_{oh} where INTL is in static mode.
5. Assertion of RESETL activates a complete module reset, i.e. module returns to factory default and non-volatile control settings. While RESETL is Low, Tx and Rx outputs are disabled and the module does not respond to the TWS interface.
6. This is the response time from RESETL de-assertion to resumption of operation.
7. Data In Set Up Time is measured from V_{il(max)SDA} or V_{ih(min)SDA} to V_{il(max)SCL}.
8. Data In Hold Time is measured from V_{il(max)SCL} to V_{il(max)SDA} or V_{ih(min)SDA}.
9. Clock Low to Data Out Time is measured from V_{il(max)SCL} to V_{ol(max)SDA} or V_{oh(min)SDA}.
10. Data Out Hold Time is measured from V_{il(max)SCL} to V_{ol(max)SDA} or V_{oh(min)SDA}.

Transmitter Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for $T_c = 40^\circ\text{C}$, $V_{cc33} = 3.3\text{ V}$ and $V_{cc25} = 2.5\text{ V}$.

| Parameter | Symbol | Min | Typ | Max | Units | Reference |
|---|-----------------|-------|-----|------|---------------|----------------|
| Output Optical Power: Average | $P_{O\ AVE}$ | | | -1.5 | dBm | |
| Output Optical Power: Disabled | $P_{O\ OFF}$ | | | -30 | dBm | |
| Extinction Ratio | ER | 3 | | | dB | Informative |
| Output Optical Modulation Amplitude | OMA | -5.25 | | | dBm | Informative |
| Output OMA: Squelched | | | | -27 | dBm | |
| Encircled Flux | | | | | | 1 |
| Center Wavelength | | 830 | | 860 | nm | |
| Spectral Width - rms | | | | 0.85 | nm | |
| Output Rise/Fall Time | | | | 50 | ps | 2, Informative |
| Power On Initialization Time Tx Outputs | $t_{PWR\ INIT}$ | | | 500 | ms | Figure 18 |
| Reset Assert Time Tx Outputs | $t_{RSTL\ ON}$ | | | 500 | ms | Figure 19 |
| Reset De-assert Re-initialization Time Tx Outputs | $t_{RSTL\ OFF}$ | | | 500 | ms | Figure 19 |
| Output Disable Assert Time for Fault | $t_{DIS\ ON}$ | | | 100 | ms | Figure 21 |
| Output Squelch Assert Time for LOS | $t_{SQ\ ON}$ | | | 80 | μs | Figure 22 |
| Output Squelch De-assert Time for LOS | $t_{SQ\ OFF}$ | | | 80 | μs | Figure 22 |
| Inter-channel Skew | | | | 150 | ps | 3 |
| Channel Latency | | | 400 | | ps | Informative |
| Relative Intensity Noise OMA | $RIN_{12\ OMA}$ | | | -124 | dB/Hz | Informative |
| Accumulated Deterministic Jitter | | | | 30 | ps | 4, Informative |
| Accumulated Total Jitter | | | | 60 | ps | 5, Informative |
| Reference Link Output Eye Width | $t_{EYE\ REF}$ | 40 | | | ps | 6 |

Notes:

1. The transmitter launch condition meets the requirements of 10 Gigabit Ethernet multimode fiber as detailed in TIA 492AAC.
2. These are unfiltered rise and fall times measured between the 20% and 80% levels using a 500 MHz square wave test pattern. Impairments in measurements due to the test system are removed.
3. Inter-Channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.
4. Deterministic Jitter, DJ, conforms to the dual-Dirac model where $TJ(BER) = DJ + 2Q(BER)RJ_{rms}$ and RJ_{rms} is the width of the Gaussian component. Here $BER = 10^{-12}$. DJ is measured with the same conditions as TJ. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
5. Total Jitter, TJ, defined for BER of 10^{-12} , is measured at the 50% signal level using test pattern 2 defined in IEEE P802.3ae clause 52.9.1, or equivalent, operating at 10 GbD with test source characteristics per the Recommended Operation Conditions. Effects of impairments in the test signals due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns.
6. Eye Opening is defined as the unit interval less TJ for the same test pattern and conditions as TJ. Measurement is made at the output, TP4, of the Reference Channel. See Link Model and Reference Channel section and Receiver Electrical Characteristics.

Receiver Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for $T_c = ^\circ\text{C}$, $V_{cc33} = 3.3\text{ V}$ and $V_{cc25} = 2.5\text{ V}$.

| Parameter | Symbol | Min | Typ | Max | Units | Reference |
|---------------------------------------|----------------|------|-----|-----|-------|-------------------------------------|
| Input Optical Power Sensitivity (OMA) | | | | -11 | dBm | 1, Informative, Default Signal Rate |
| Input Optical Power Saturation | $P_{SAT\ AVE}$ | -1.0 | | | dBm | 2 |
| Operating Center Wavelength | | 830 | | 860 | nm | |
| Return Loss | | 12 | | | dB | |
| LOS Asserted Threshold – OMA | $P_{LOS\ OMA}$ | -26 | -19 | | dBm | |
| LOS De-asserted – OMA | | | -17 | -12 | dBm | |
| LOS Hysteresis | | 0.5 | 2 | | dB | 3 |

Notes:

- Sensitivity is defined as the input OMA needed to produce a BER $\leq 10^{-12}$ at the center of the signal period using test pattern 2 defined in IEEE P802.3ae clause 52.9.1, or equivalent, operating at 10 GBd. Effects of impairments in the test signal due to the test system are removed from the measurement. All channels not under test are operating with similar test patterns and input signals 6 dB above $P_{IN\ MIN}$.
- Saturation is defined as the average input power (ER = 6 dB) that at the receiver output produces an eye width less than the Reference Link Output Eye Width Minimum ($t_{EYE\ LINK}$) for a BER $\leq 10^{-12}$ using test pattern 2 defined in IEEE P802.3ae clause 52.9.1, or equivalent, operating at 10 GBd. Effects of impairments in the test signal due to the test system are removed from the measurement.
- Signal Detect Hysteresis is defined as 10 Log(LOS De-assert Level / LOS Assert Level).

Regulatory Compliance Table (When released, the AFBR-810BxxZ and AFBR-820xxxZ will support this table.)

| Feature | Test Method | Performance |
|---|---|---|
| Electrostatic Discharge (ESD) to the Electrical Contacts | JEDEC Human Body Model (HBM) (JESD22-A114-B) | Transmitter module withstands minimum 2000 V Receiver module withstands minimum 2000 V |
| | JEDEC Machine Model (MM) (JESD22-A115-A) | Transmitter module withstands minimum 100 V Receiver module withstands minimum 100 V |
| Electrostatic Discharge (ESD) to Optical Connector Receptacle | Variation of IEC 61000-4-2 | Typically withstands at least 6 kV air discharge with module biased |
| Electromagnetic Interference (EMI) | FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1 | Typically passes with 10 dB margin. Actual performance dependent on enclosure design. |
| Immunity | Variation of IEC 61000-4-3 | Typically minimal effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure. |
| Laser Eye Safety and Equipment Type Testing | IEC 60825-1 Amendment 2 CFR 21 Section 1040 | Pout: IEC AEL & US FDA CDRH Class 1M CDRH Accession Number: 9720151-074 TUV Certificate Number: 72060862 |
| Component Recognition | Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment | UL File Number: E173874 |
| RoHS Compliance | | Less than 100 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters. |

Transmitter Module Contact Assignment and Signal Description

Optical Connector Side

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|--------|-------|-------|-------|-------|-------|-------|--------|--------|-------|
| A | Adr2 | GND | GND | GND | GND | GND | GND | GND | GND | IntL |
| B | Adr1 | GND | Din1p | GND | Din4p | GND | Din8n | GND | Din11n | GND |
| C | Adr0 | GND | Din1n | GND | Din4n | GND | Din8p | GND | Din11p | GND |
| D | GND | Din0p | GND | Din3p | GND | Din6n | GND | Din10n | GND | SDA |
| E | GND | Din0n | GND | Din3n | GND | Din6p | GND | Din10p | GND | SCL |
| F | ResetL | GND | Din2p | GND | Din5n | GND | Din7n | GND | Din9p | GND |
| G | DNC | GND | Din2n | GND | Din5p | GND | Din7p | GND | Din9n | GND |
| H | DNC | DNC | GND | DNC | GND | DNC | GND | DNC | GND | DNC |
| J | GND | GND | GND | DNC | DNC | DNC | DNC | GND | GND | GND |
| K | Vcc25 | Vcc33 | Vcc33 | DNC | DNC | DNC | DNC | Vcc33 | Vcc33 | Vcc25 |

Figure 9. Host Board Pattern for Transmitter Connector – Top View

| Signal Name | Signal Description | I/O | Type |
|-------------|--|-----|--|
| Adr[2:0] | TWS Module Bus Address bits: Address has the form 0101hjkx where Adr2, Adr1 & Adr0 correspond to h, j & k respectively and x corresponds to the R/W command. | I | 3.3V LVTTTL |
| Din[11:0]p | Transmitter Data Non-inverting Input for channels 11 through 0 | I | CML |
| Din[11:0]n | Transmitter Data Inverting Input for channels 11 through 0 | I | CML |
| DNC | Reserved – Do Not Connect to any electrical potential on Host PCB | | |
| GND | Signal Common: All module voltages are referenced to this potential unless otherwise stated. Connect these pins directly to the host board signal ground plane. | | |
| IntL | Interrupt signal to Host, Asserted Low: An interrupt is generated in response to any Tx Fault condition, loss of input signal or assertion of any monitor Flag. It may be programmed through the TWS interface to generate either a pulse or static level with static mode as default. This output presents a High-Z condition when IntL is de-asserted and requires a pull-up on the Host board. Pull-up to the Host 3.3 V supply is recommended. | O | 3.3V LVTTTL, high-Z or driven to 0 level |
| ResetL | Reset signal to module, Asserted Low: When asserted the optical outputs are disabled, TWS interface commands are inhibited, and the module returns to default and non-volatile settings. An internal pullup biases the input High if the input is open. | I | 3.3V LVTTTL |
| SDA | TWS interface data signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is recommended. | I/O | 3.3V LVTTTL/ Open-Drain |
| SCL | TWS interface clock signal I: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is recommended. | I | 3.3V LVTTTL |
| Vcc25 | 2.5V Power supply, External common connection of pins required – not common internally | | |
| Vcc33 | 3.3 V Power supply, External common connection of pins required – not common internally | | |
| Case Common | Not accessible in connector. Case common incorporates exposed conductive surfaces including threaded bosses and is electrically isolated from signal common, i.e. GND. Connect as appropriate for EMI shield integrity. See EMI clip and bezel cutout recommendation. | | |

Receiver Module Contact Assignment and Signal Description

Optical Connector Side

| | | | | | | | | | | | |
|--|--------|--------|--------|--------|--------|--------|--------|---------|---------|-------|---|
| | Adr2 | GND | GND | GND | GND | GND | GND | GND | GND | IntL | K |
| | Adr1 | GND | Dout1p | GND | Dout4p | GND | Dout8n | GND | Dout11r | GND | J |
| | Adr0 | GND | Dout1n | GND | Dout4n | GND | Dout8p | GND | Dout11p | GND | H |
| | GND | Dout0p | GND | Dout3p | GND | Dout6n | GND | Dout10r | GND | SDA | G |
| | GND | Dout0n | GND | Dout3n | GND | Dout6p | GND | Dout10p | GND | SCL | F |
| | ResetL | GND | Dout2p | GND | Dout5n | GND | Dout7n | GND | Dout9p | GND | E |
| | DNC | GND | Dout2n | GND | Dout5p | GND | Dout7p | GND | Dout9n | GND | D |
| | DNC | DNC | GND | DNC | GND | DNC | GND | DNC | GND | DNC | C |
| | GND | GND | GND | DNC | DNC | DNC | DNC | GND | GND | GND | B |
| | Vcc25 | Vcc33 | Vcc33 | DNC | DNC | DNC | DNC | Vcc33 | Vcc33 | Vcc25 | A |
| | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

Figure 10. Host Board Pattern for Receiver Connector – Top View

| PIN name | Functional descriptions | I/O | Type |
|-------------|--|-----|--|
| Adr[2:0] | TWS Module Bus Address bits: Address has the form 0101hjkx where Adr2, Adr1 & Adr0 correspond to h, j & k respectively and x corresponds to the R/W command. | I | 3.3V LVTTTL |
| Dout[11:0]p | Receiver Data Non-inverting Output for channels 11 through 0 | O | CML |
| Dout[11:0]n | Receiver Data Inverting Output for channels 11 through 0 | O | CML |
| DNC | Reserved – Do Not Connect to any electrical potential on Host PCB | | |
| GND | Signal Common: All module voltages are referenced to this potential unless otherwise stated. Connect these pins directly to the host board signal ground plane. | | |
| IntL | Interrupt signal to Host, Asserted Low: An interrupt is generated in response to loss of input signal or assertion of any monitor Flag. It may be programmed through the TWS interface to generate either a pulse or static level with static mode as default. This output presents a High-Z condition when IntL is de-asserted and requires a pull-up on the Host board. Pull-up to the Host 3.3 V supply is recommended. | O | 3.3V LVTTTL, high-Z or driven to 0 level |
| ResetL | Reset signal to module, Asserted Low: When asserted the data outputs, Dout[11:0]p/n are squelched, TWS interface commands are inhibited, and the module returns to default and non-volatile settings. An internal pullup biases the input High if the input is open. | I | 3.3V LVTTTL |
| SDA | TWS interface data signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is recommended. | I/O | 3.3V LVTTTL/ Open-Drain |
| SCL | TWS interface clock signal: Pull-up with a 2.0 kΩ to 8.0 kΩ resistor to the Host 3.3 V supply is recommended. | I | 3.3V LVTTTL |
| Vcc25 | 2.5V Power supply, External common connection of pins required – not common internally | P | |
| Vcc33 | 3.3 V Power supply, External common connection of pins required – not common internally | P | |
| Case Common | Not accessible in connector. Case common incorporates exposed conductive surfaces including threaded bosses and is electrically isolated from signal common, i.e. GND. Connect as appropriate for EMI shield integrity. See EMI clip and bezel cutout recommendation. | | |

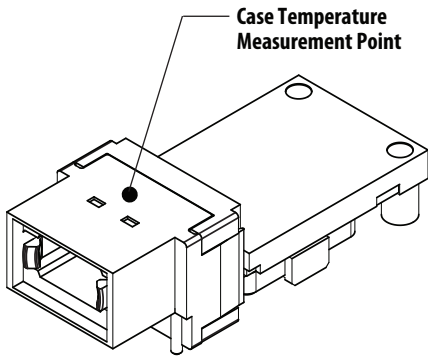


Figure 11. Case Temperature Measurement Point

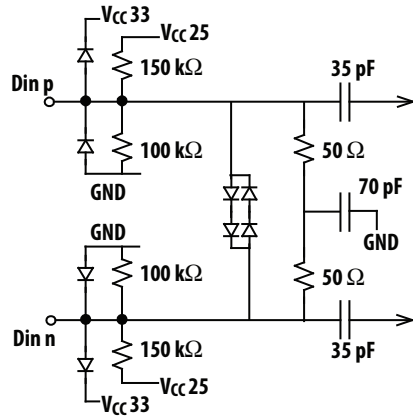


Figure 15. Transmitter Data Input Equivalent Circuit

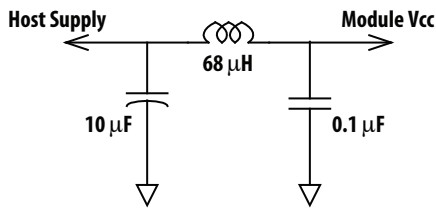


Figure 12. Recommended Tx Power Supply Filter

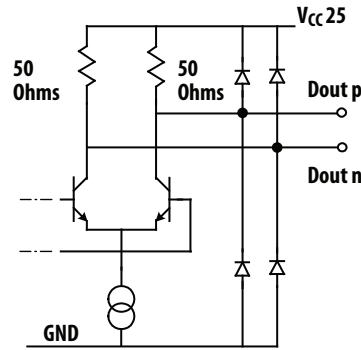


Figure 16. Receiver Data Output Equivalent Circuit

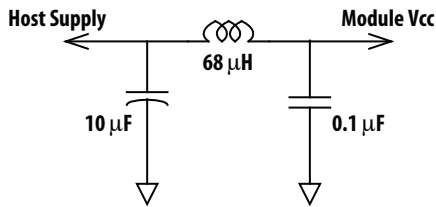


Figure 13. Recommended Rx Power Supply Filter

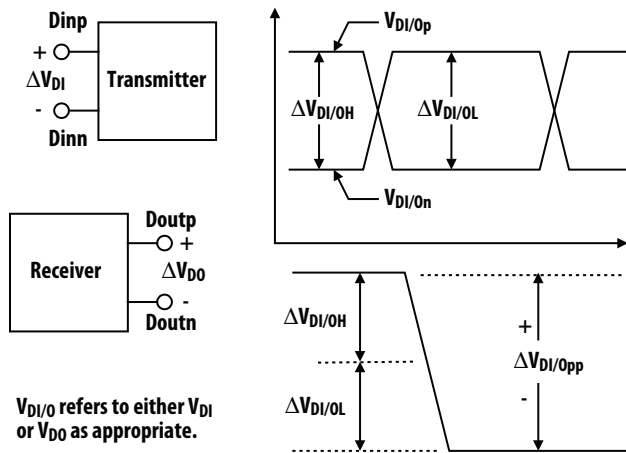


Figure 14. Differential Signal Definitions

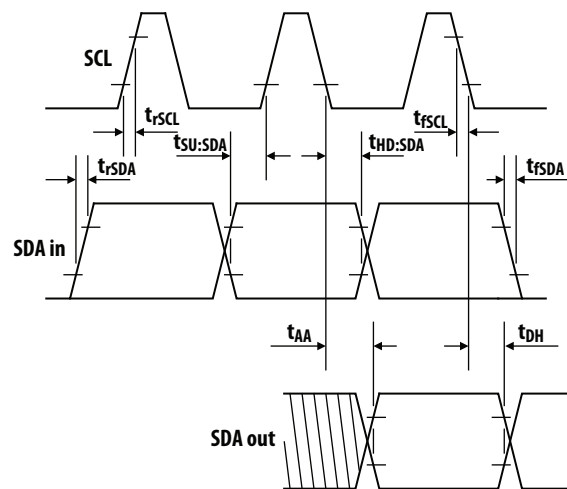


Figure 17. TWS Interface Bus Timing

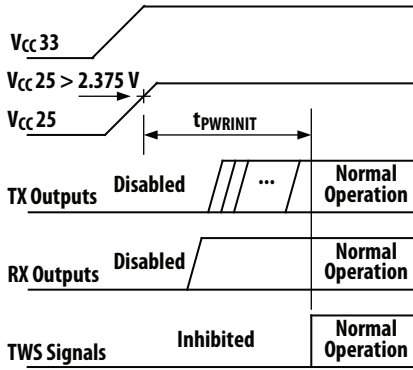


Figure 18. Power-up Sequence

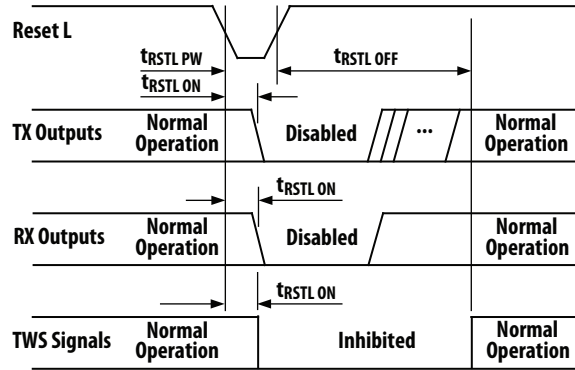


Figure 19. ResetL Sequence

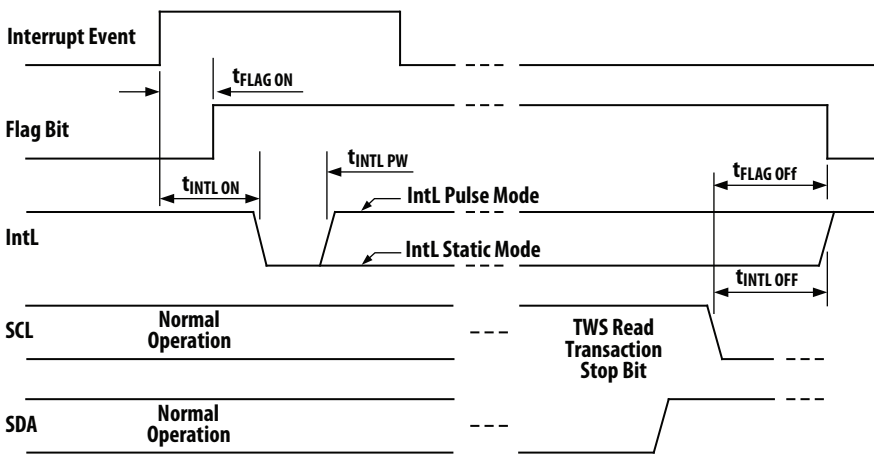


Figure 20. Interrupt Sequence

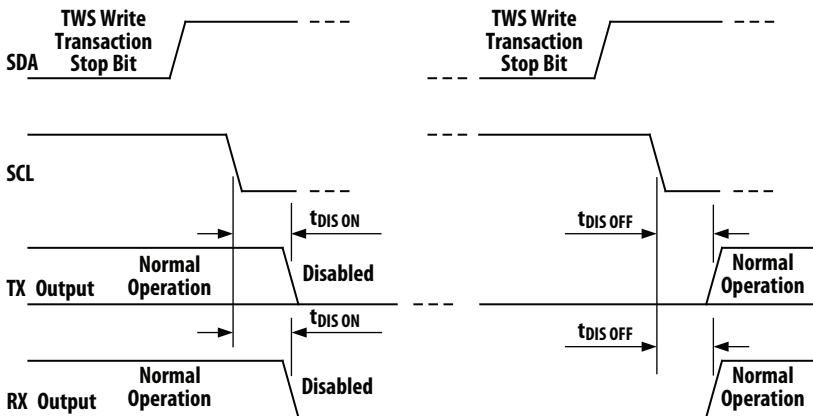


Figure 21. Channel Disable Sequence

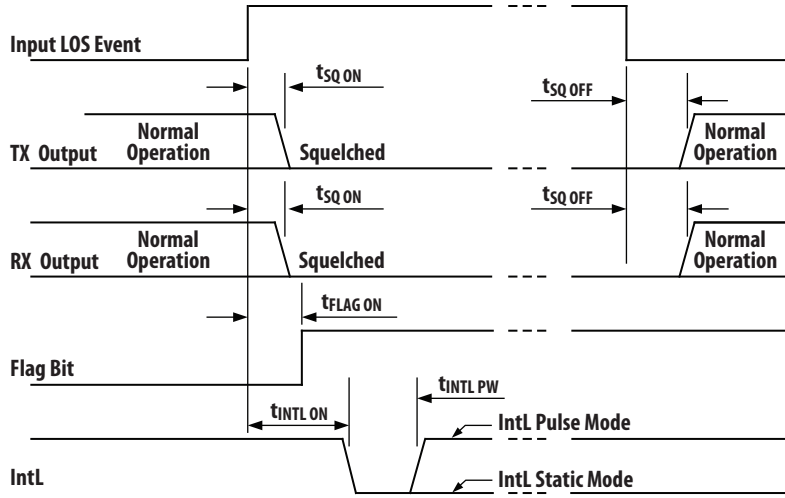


Figure 22. LOS Squelch Sequence

Package Outline, Host PCB Footprint and Panel Cutout

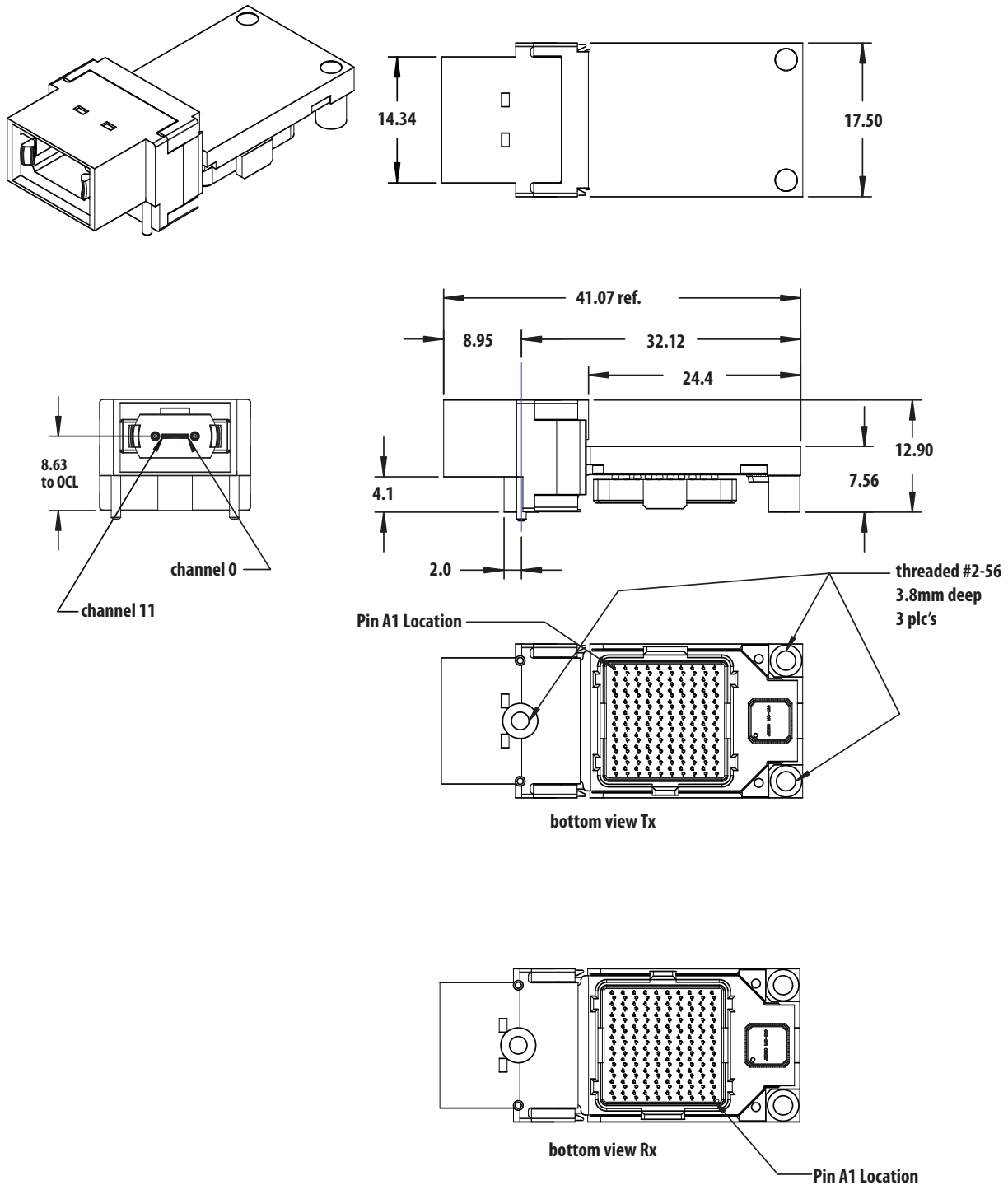


Figure 23. Package Outline AFBR-810BHZ and AFBR-820BHZ

Package outline dimensions are nominal expressed in mm unless otherwise stated. The mating host PCB mounted electrical connector is a 100 position FCI MEG-Array® Plug (FCI PN: 84512-102) or equivalent.

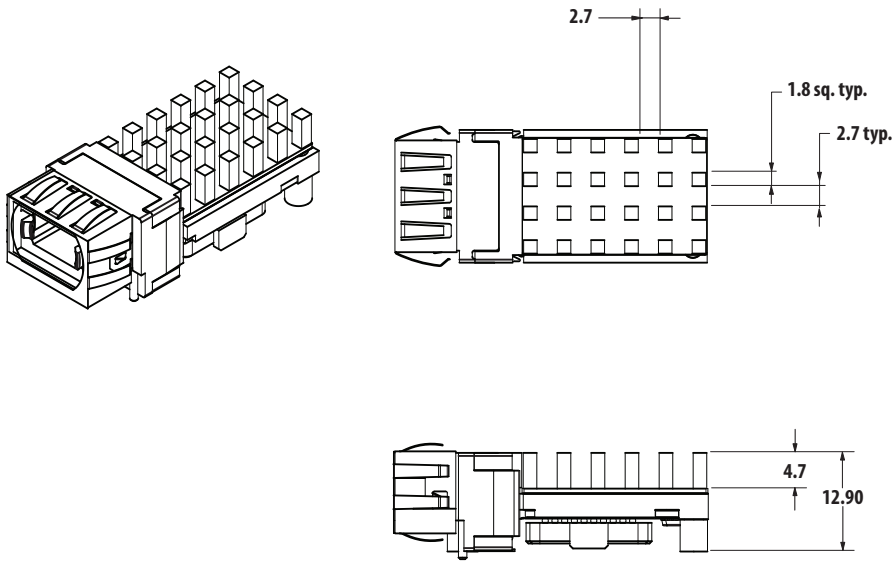


Figure 24. Package Outline AFBR-810BEPZ and AFBR-820BEPZ

Package outline dimensions are nominal expressed in mm unless otherwise stated. The mating host PCB mounted electrical connector is a 100 position FCI MEG-Array® Plug (FCI PN: 84512-102) or equivalent.

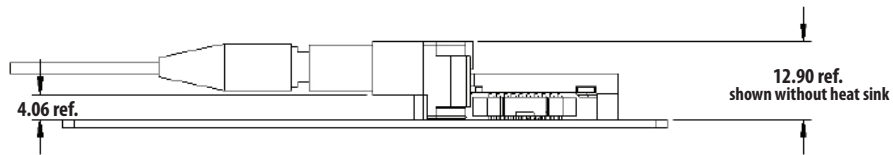
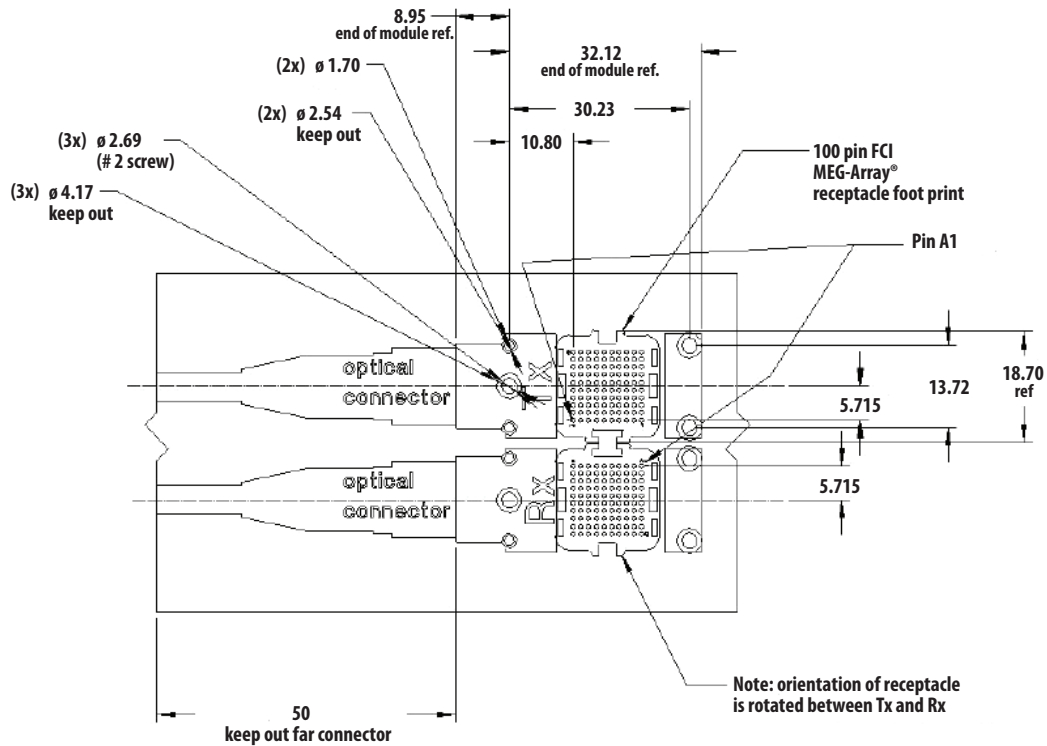


Figure 25. Host Board Module Footprint (Top View) and Module (Side View) – Mid-Plane Mount

Dimensions are nominal expressed in mm unless otherwise stated. The mating host PCB mounted electrical connector is a 100 position FCI MEG-Array® Plug (FCI PN: 84512-102) or equivalent.

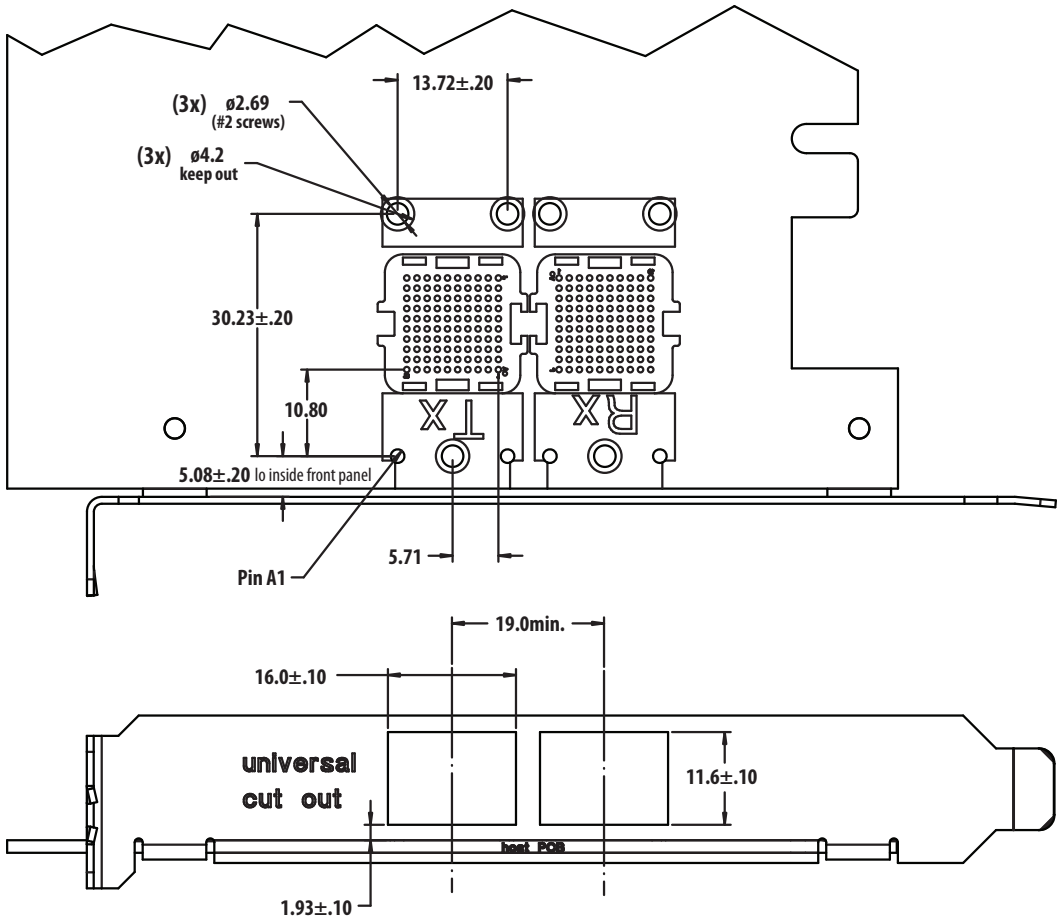


Figure 26. Host Board Module Footprint (Top and Side Views) – Panel Mount

Dimensions are nominal expressed in mm unless otherwise stated. The mating host PCB mounted electrical connector is a 100 position FCI MEG-Array® Plug (FCI PN: 84512-102) or equivalent.

Control Interface & Memory Map

The control interface combines dedicated signal lines for address inputs, $\text{Adr}[2:0]$, interrupt output, IntL , and reset input, ResetL , with two-wire serial, TWS, interface clock, SCL , and data, SDA , signals to provide users rich functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. It is scaled for 3.3 volt LVTTTL. Outputs are high-z in the high state to support busing of these signals. Signal and timing characteristics are further defined in the Control I/O Characteristics section. In general, TWS bus timing and protocols follow the implementation popularized in Atmel Two-wire Serial EEPROMs. For additional details see, e.g., Atmel AT24C01A.

The address signals, Adr_2 , Adr_1 and Adr_0 , provide the ability to program the TWS bus address of the module. The module address has the binary form 0101hjkx , where h , j and k correspond to Adr_2 , Adr_1 and Adr_0 , respectively and x corresponds to the Read/Write command bit. Modules will respond to TWS bus addresses in the range of 50h^1 to 5Fh (hereafter 5ih) depending upon the state of Adr_2 , Adr_1 and Adr_0 . The address $\text{B0}(\text{h})$ should be avoided on the TWS bus where these modules are used.

An interrupt signal, IntL , is used to alert the host of a loss of input signal (LOS), transmitter fault conditions and/or assertion of any monitor flag. This reduces the need for dedicated status signal lines and polling the status and monitor registers while maintaining timely alerts to significant events. IntL can be programmed (page 01h byte 225 bit 0) to either pulse or static mode with pulse as the default mode.

A dedicated module reset signal, ResetL , is provided in case the TWS interface becomes dysfunctional. When ResetL is asserted, the outputs are disabled, TWS interface commands are inhibited and the module returns to factory default settings except Non-volatile Read-Write (RWn) registers which retain the last write. A module register (memory map except the non-volatile registers) reset can also be initiated over the TWS interface (page 5ih byte 91 , bit 0). A TWS reset can be initiated by nine SLA clock cycles with SDA high in each cycle and creating a start condition.

With the TWS interface the user can read a status register (page 5ih byte 2) to see if data is available in the monitor registers, if the module has generated an IntL that has not been cleared and global status reports for loss of signal and fault conditions

LOS, Tx fault and/or monitor flag registers can be accessed to check the status of individual channels or which channel may have generated a recent IntL . LOS, Tx fault and flag bits

remain set (latched) after assertion even in the event the condition changes and operation resumes until cleared by the read operation of the associated registers or reset by ResetL or the TWS module reset function.

The user can read the present value of the various monitors. For transmitters and receivers, internal module temperature and supply voltages are reported. For transmitters, monitors provide for each channel laser bias current and laser light output power (LOP) information. For receivers, input power (Pave) is monitored for each channel. In addition, elapsed operating time is reported. All monitor items are two-byte fields and to maintain coherency, the host must access these with single two-byte read sequences. For each monitored item, alarm thresholds are established. If an item moves past a threshold, a flag is set, and, provided the item is not masked, IntL is asserted. The threshold settings are available in the upper memory page, 01h .

The user can select either a pulse or static mode for the interrupt signal IntL and initiate a module register reset. The user is provided the ability to disable individual channels. For transmitters, equalization levels can be independently set for individual channels. For receivers, output signal amplitude, de-emphasis levels and rate select can be independently set for individual channels. In the upper page, 01h , control field the user can invert the truth of the differential inputs for individual transmitter channel and for the differential outputs of individual receiver channels. In addition, the user can disable the output squelch function on an individual channel basis for both transmitters and receivers. For transmitters the user can, on an individual channel basis, activate a margin mode that reduces the output optical modulation amplitude for the channel.

All non-volatile control registers are located in the upper page $01(\text{h})$. Non-volatile functions include the IntL mode selection bit, input and output polarity flip bits, transmitter equalization control bits, receiver output amplitude control and receiver output de-emphasis control. Entries into these registers will retain the last write for supply voltage cycles and for ResetL and module register resets. Volatile functions include module register reset, channel disable, squelch disable and margin activation.

A mask bit that can be set to prevent assertion of IntL for the individual item exists for every LOS, Tx fault and monitor flag. Mask fields for LOS, Tx fault and module monitors are in the lower memory page, 5ih , and the mask field for the channel monitors are in the upper page 01h . Entries in the mask fields are volatile.

Page 00h , based on the Serial ID pages of XFP and QSFP, provides module identity and information regarding the capabilities of the module.

1. In terms $\#\#\text{h}$, the h indicates that $\#\#$ is hexadecimal, if $\#\#\text{b}$, b indicates binary and if $\#\#$, then decimal.

1. Memory Map Overview

The memory is structured as a single address, multiple page approach after that in the XFP MSA and adapted by QSFP MSA for multi-channel transceivers. Figure 27 presents an overview of the memory structure showing a lower page (5ih) and two upper pages (00h and 01h). As with XFP and QSFP, time sensitive, dynamic and/or high interest information are contained in the base, i.e. lower, page. Here the upper page 00h contains the serial id

information, again following the style of XFP and QSFP. The 01h upper table contains static threshold information, configuration controls and flag masks.

Unless otherwise stated all reserved bytes are coded 00h and all reserved bits are coded 0b. Non-volatile read-write bits are labeled RWn and volatile read-write bits are labeled RWv.

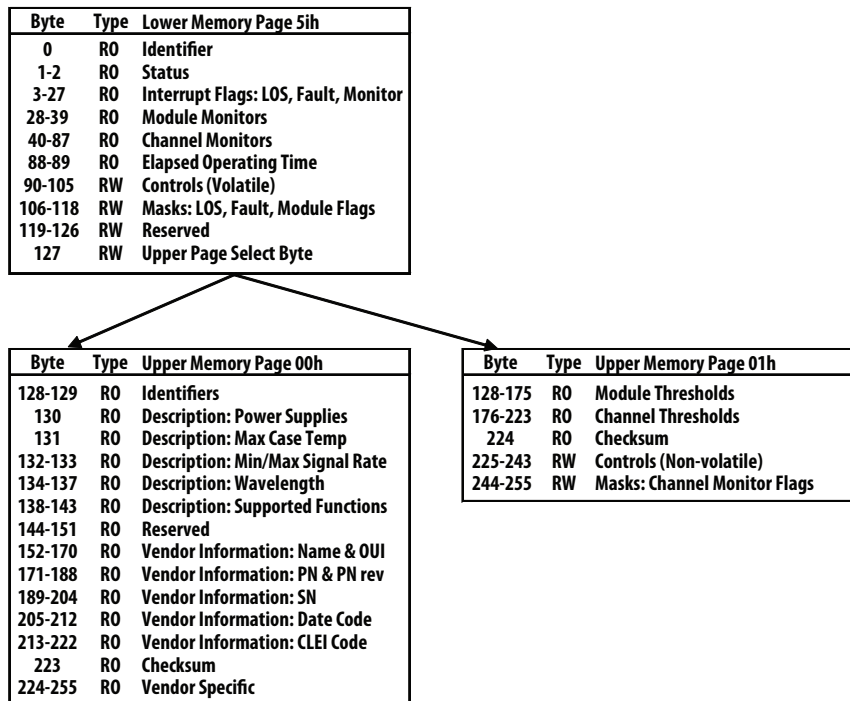


Figure 27. Two-Wire Serial Address 5ih Page Structure

2. Memory Map Timing Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for $T_c = 40^\circ\text{C}$, $V_{cc33} = 3.3\text{ V}$ and $V_{cc25} = 2.5\text{ V}$.

| Parameter | Symbol | Min | Typ | Max ¹ | Units | Reference |
|--|-----------------------|-----|-----|------------------|---------------|--|
| Flag (including Tx Fault & LOS) Assert Time ² | $t_{\text{FLAG ON}}$ | | | 100 | ms | Figure 20, Time from occurrence of condition to IntL assertion, $V_{\text{out:IntL}} = V_{\text{ol}}$ |
| Flag (including Tx Fault & LOS) Clear Time ² | $t_{\text{FLAG OFF}}$ | | | 100 | ms | Figure 20, Time for clear on read operation, measured from falling SCL edge after stop bit of read transaction, until $V_{\text{out:IntL}} = V_{\text{oh}}$, where IntL is in static mode |
| Channel Disable Assert Time | $t_{\text{DIS ON}}$ | | | 100 | ms | Figure 21, Time from write operation, measured from falling edge of SCL after stop bit of write transaction, until channel output falls below 10% of nominal |
| Channel Disable De-assert Time | $t_{\text{DIS OFF}}$ | | | 300 | ms | Figure 21, Time from write operation, measured from falling edge of SCL after stop bit of write transaction, until channel output rises above 90% of nominal |
| Mask Assert Time | | | | 100 | ms | Time from write operation, measured from falling edge of SCL after stop bit of write transaction, until associated IntL is inhibited |
| Mask De-assert Time | | | | 100 | ms | Time from write operation, measured from falling edge of SCL after stop bit of write transaction, until associated IntL resumes |
| Volatile Control Assert Time (except Channel Disable) | $t_{\text{CNTL ON}}$ | | | 100 | ms | Time from write operation, measured from falling edge of SCL after stop bit of write transaction, until associated control is activated |
| Volatile Control De-assert Time (except Channel Disable) | | | | 100 | ms | Time from write operation, measured from falling edge of SCL after stop bit of write transaction, until associated control is de-activated |
| Control Transition Period | $t_{\text{CNTL XP}}$ | | 10 | | μs | Time during the control assert time when signal integrity may be impaired |
| Non-Volatile Control Assert Time | | | | 150 | ms | Time from up to two byte write operation, measured from falling edge of SCL after stop bit of write transaction, until associated control is activated |
| Non-Volatile Control De-assert Time | | | | 150 | ms | Time from up to two byte write operation, measured from falling edge of SCL after stop bit of write transaction, until associated control is de-activated |
| Non-Volatile Control Assert Time | | | | 300 | ms | Time from up to six byte write operation, measured from falling edge of SCL after stop bit of write transaction, until associated control is activated |
| Non-Volatile Control De-assert Time | | | | 300 | ms | Time from up to six byte write operation, measured from falling edge of SCL after stop bit of write transaction, until associated control is de-activated |
| Module Reset Assert Time | | | | 100 | ms | Time from write operation, measured from falling edge of SCL after stop bit of write transaction, until associated reset begins |
| Module Reset De-assert Time | | | | 500 | ms | Time from write operation, measured from falling edge of SCL after stop bit of write transaction, until associated reset is completed and normal operation resumes |

Notes:

1. Max values are valid where competing TWS traffic is absent.
2. The outputs of affected channels are disabled for incidences of Tx Fault and squelched for Tx LOS and/or Rx LOS. Timing for output fault and squelch assertion and de-assertion are found in the Receiver Electrical and Transmitter Optical Characteristics sections.

3. Tx Memory Map 5ih Lower Page

Details of the base or lower page of the memory map for a transmitter follow.

| Address | Type | Field Name/Description |
|---------|------|---|
| Byte | Bit | |
| 0 | all | RO Type Identifier: Coded 00h for unspecified |
| 1 | all | RO Reserved: Coded 00h |
| 2 | 7-4 | RO Reserved: Coded 0000b |
| 2 | 3 | RO Fault Status: Coded 1 when a Fault flag (bytes 11 and 12 of this page) is asserted for any channel, else 0. Clears when Fault flags are cleared. |
| 2 | 2 | RO LOS Status: Coded 1 when a LOS flag (bytes 9 and 10 of this page) is asserted for any channel, else 0. Clears when LOS flags are cleared. |
| 2 | 1 | RO IntL Status: Coded 1 for asserted IntL. Clears to 0 when all flags including LOS and Fault are cleared. |
| 2 | 0 | RO Data Not Ready: Coded 1 until data is available in monitor registers. Coded 0 in normal operation. |
| 3 - 7 | all | RO Reserved: Coded 00h |
| 8 | 0 | Module Ready Interrupt. Coded 1 when asserted and module is Ready to respond to TWS commands, Latched, Clears on Read. |
| 9 | 7-4 | RO Reserved: Coded 0000b |
| 9 | 3 | RO LOS Latched Tx Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 9 | 2 | RO LOS Latched Tx Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 9 | 1 | RO LOS Latched Tx Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 9 | 0 | RO LOS Latched Tx Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 7 | RO LOS Latched Tx Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 6 | RO LOS Latched Tx Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 5 | RO LOS Latched Tx Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 4 | RO LOS Latched Tx Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 3 | RO LOS Latched Tx Channel 3: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 2 | RO LOS Latched Tx Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 1 | RO LOS Latched Tx Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 0 | RO LOS Latched Tx Channel 0: Coded 1 when asserted, Latched, Clears on Read. |
| 11 | 7-4 | RO Reserved: Coded 0000b |
| 11 | 3 | RO Fault Latched Tx Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 11 | 2 | RO Fault Latched Tx Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 11 | 1 | RO Fault Latched Tx Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 11 | 0 | RO Fault Latched Tx Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 12 | 7 | RO Fault Latched Tx Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 12 | 6 | RO Fault Latched Tx Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 12 | 5 | RO Fault Latched Tx Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 12 | 4 | RO Fault Latched Tx Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 12 | 3 | RO Fault Latched Tx Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 12 | 2 | RO Fault Latched Tx Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 12 | 1 | RO Fault Latched Tx Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 12 | 0 | RO Fault Latched Tx Channel 0: Coded 1 when asserted, Latched, Clears on Read. |
| 13 | 7 | RO High Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 13 | 6 | RO Low Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 13 | 5-0 | RO Reserved |
| 14 | 7 | RO High Internal 3.3 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 14 | 6 | RO Low Internal 3.3 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 14 | 5-4 | RO Reserved |
| 14 | 3 | RO High Internal 2.5 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 14 | 2 | RO Low Internal 2.5 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 14 | 1-0 | RO Reserved |

| Address | Type | Field Name/Description |
|---------|------|---|
| Byte | Bit | |
| 15 | all | RO Reserved: Coded 00h |
| 16 | 7 | RO High Tx Bias Current Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 16 | 6 | RO Low Tx Bias Current Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 16 | 5-4 | RO Reserved |
| 16 | 3 | RO High Tx Bias Current Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 16 | 2 | RO Low Tx Bias Current Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 16 | 1-0 | RO Reserved |
| 17 | 7 | RO High Tx Bias Current Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 17 | 6 | RO Low Tx Bias Current Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 17 | 5-4 | RO Reserved |
| 17 | 3 | RO High Tx Bias Current Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 17 | 2 | RO Low Tx Bias Current Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 17 | 1-0 | RO Reserved |
| 18 | 7 | RO High Tx Bias Current Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 18 | 6 | RO Low Tx Bias Current Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 18 | 5-4 | RO Reserved |
| 18 | 3 | RO High Tx Bias Current Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 18 | 2 | RO Low Tx Bias Current Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 18 | 1-0 | RO Reserved |
| 19 | 7 | RO High Tx Bias Current Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 19 | 6 | RO Low Tx Bias Current Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 19 | 5-4 | RO Reserved |
| 19 | 3 | RO High Tx Bias Current Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 19 | 2 | RO Low Tx Bias Current Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 19 | 1-0 | RO Reserved |
| 20 | 7 | RO High Tx Bias Current Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read. |
| 20 | 6 | RO Low Tx Bias Current Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read. |
| 20 | 5-4 | RO Reserved |
| 20 | 3 | RO High Tx Bias Current Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 20 | 2 | RO Low Tx Bias Current Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 20 | 1-0 | RO Reserved |
| 21 | 7 | RO High Tx Bias Current Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 21 | 6 | RO Low Tx Bias Current Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 21 | 5-4 | RO Reserved |
| 21 | 3 | RO High Tx Bias Current Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read. |
| 21 | 2 | RO Low Tx Bias Current Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read. |
| 21 | 1-0 | RO Reserved |
| 22 | 7 | RO High Tx Power Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 22 | 6 | RO Low Tx Power Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 22 | 5-4 | RO Reserved |
| 22 | 3 | RO High Tx Power Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 22 | 2 | RO Low Tx Power Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 22 | 1-0 | RO Reserved |
| 23 | 7 | RO High Tx Power Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 23 | 6 | RO Low Tx Power Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 23 | 5-4 | RO Reserved |
| 23 | 3 | RO High Tx Power Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 23 | 2 | RO Low Tx Power Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 23 | 1-0 | RO Reserved |

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 24 | 7 | RO High Tx Power Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 24 | 6 | RO Low Tx Power Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 24 | 5-4 | RO Reserved |
| 24 | 3 | RO High Tx Power Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 24 | 2 | RO Low Tx Power Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 24 | 1-0 | RO Reserved |
| 25 | 7 | RO High Tx Power Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 25 | 6 | RO Low Tx Power Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 25 | 5-4 | RO Reserved |
| 25 | 3 | RO High Tx Power Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 25 | 2 | RO Low Tx Power Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 25 | 1-0 | RO Reserved |
| 26 | 7 | RO High Tx Power Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read. |
| 26 | 6 | RO Low Tx Power Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read. |
| 26 | 5-4 | RO Reserved |
| 26 | 3 | RO High Tx Power Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 26 | 2 | RO Low Tx Power Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 26 | 1-0 | RO Reserved |
| 27 | 7 | RO High Tx Power Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 27 | 6 | RO Low Tx Power Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 27 | 5-4 | RO Reserved |
| 27 | 3 | RO High Tx Power Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read. |
| 27 | 2 | RO Low Tx Power Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read. |
| 27 | 1-0 | RO Reserved |
| 28 | all | RO Internal Temperature Monitor MSB: Integer part coded in signed 2's complement. Tolerance is $\pm 3^{\circ}\text{C}$. |
| 29 | all | RO Internal Temperature Monitor LSB: Fractional part in units of $1^{\circ}/256$ coded in binary. |
| 30-31 | all | RO Reserved: Coded 00h |
| 32-33 | all | RO Internal 3.3 Vcc Monitor: Voltage in 100 μV units coded as 16 bit unsigned integer, Byte 32 is MSB. Tolerance is $\pm 0.150\text{V}$. |
| 34-35 | all | RO Internal 2.5 Vcc Monitor: Voltage in 100 μV units coded as 16 bit unsigned integer, Byte 34 is MSB. Tolerance is $\pm 0.150\text{V}$. |
| 36-39 | all | RO Reserved: Coded 00h |
| 40-41 | all | RO Tx Bias Current Monitor Channel 11: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 40 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 42-43 | all | RO Tx Bias Current Monitor Channel 10: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 42 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 44-45 | all | RO Tx Bias Current Monitor Channel 9: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 44 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 46-47 | all | RO Tx Bias Current Monitor Channel 8: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 46 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 48-49 | all | RO Tx Bias Current Monitor Channel 7: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 48 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 50-51 | all | RO Tx Bias Current Monitor Channel 6: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 50 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 52-53 | all | RO Tx Bias Current Monitor Channel 5: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 52 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 54-55 | all | RO Tx Bias Current Monitor Channel 4: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 54 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 56-57 | all | RO Tx Bias Current Monitor Channel 3: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 56 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |
| 58-59 | all | RO Tx Bias Current Monitor Channel 2: Bias current in 2 μA units coded as 16 bit unsigned integer, Byte 58 is MSB. Tolerance is $\pm 0.50\text{ mA}$. |

| Address | Type | Field Name/Description |
|---------|------|---|
| Byte | Bit | |
| 60-61 | all | RO Tx Bias Current Monitor Channel 1: Bias current in 2 μ A units coded as 16 bit unsigned integer, Byte 60 is MSB. Tolerance is \pm 0.50 mA. |
| 62-63 | all | RO Tx Bias Current Monitor Channel 0: Bias current in 2 μ A units coded as 16 bit unsigned integer, Byte 62 is MSB. Tolerance is \pm 0.50 mA. |
| 64-65 | all | RO Tx Light Output Monitor Channel 11: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 64 is MSB. Tolerance is \pm 3dB. |
| 66-67 | all | RO Tx Light Output Monitor Channel 10: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 66 is MSB. Tolerance is \pm 3dB. |
| 68-69 | all | RO Tx Light Output Monitor Channel 9: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 68 is MSB. Tolerance is \pm 3dB. |
| 70-71 | all | RO Tx Light Output Monitor Channel 8: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 70 is MSB. Tolerance is \pm 3dB. |
| 72-73 | all | RO Tx Light Output Monitor Channel 7: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 72 is MSB. Tolerance is \pm 3dB. |
| 74-75 | all | RO Tx Light Output Monitor Channel 6: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 74 is MSB. Tolerance is \pm 3dB. |
| 76-77 | all | RO Tx Light Output Monitor Channel 5: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 76 is MSB. Tolerance is \pm 3dB. |
| 78-79 | all | RO Tx Light Output Monitor Channel 4: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 78 is MSB. Tolerance is \pm 3dB. |
| 80-81 | all | RO Tx Light Output Monitor Channel 3: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 80 is MSB. Tolerance is \pm 3dB. |
| 82-83 | all | RO Tx Light Output Monitor Channel 2: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 82 is MSB. Tolerance is \pm 3dB. |
| 84-85 | all | RO Tx Light Output Monitor Channel 1: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 84 is MSB. Tolerance is \pm 3dB. |
| 86-87 | all | RO Tx Light Output Monitor Channel 0: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 86 is MSB. Tolerance is \pm 3dB. |
| 88-89 | all | RO Elapsed (Power-on) Operating Time: Elapsed time in 2 hour units coded as 16 bit unsigned integer, Byte 88 is MSB, Tolerance is \pm 10% |
| 90 | all | RWv Reserved: Coded 00h |
| 91 | 7-1 | RWv Reserved: Coded 0000000b |
| 91 | 0 | RWv Transmitter Reset: Writing 1 return all registers except non-volatile RW to factory default values. Reads 0 after operation. |
| 92 | 7-4 | RWv Reserved: Coded 0000b |
| 92 | 3 | RWv Tx Channel 11 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 92 | 2 | RWv Tx Channel 10 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 92 | 1 | RWv Tx Channel 9 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 92 | 0 | RWv Tx Channel 8 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 93 | 7 | RWv Tx Channel 7 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 93 | 6 | RWv Tx Channel 6 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 93 | 5 | RWv Tx Channel 5 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 93 | 4 | RWv Tx Channel 4 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 93 | 3 | RWv Tx Channel 3 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 93 | 2 | RWv Tx Channel 2 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 93 | 1 | RWv Tx Channel 1 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 93 | 0 | RWv Tx Channel 0 Disable: Writing 1 deactivates the optical output, Default is 0. |
| 94 | 7-4 | RWv Reserved: Coded 0000b |
| 94 | 3 | RWv Squelch Disable Channel 11: Writing 1 inhibits squelch for the channel, Default is 0. |
| 94 | 2 | RWv Squelch Disable Channel 10: Writing 1 inhibits squelch for the channel, Default is 0. |
| 94 | 1 | RWv Squelch Disable Channel 9: Writing 1 inhibits squelch for the channel, Default is 0. |
| 94 | 0 | RWv Squelch Disable Channel 8: Writing 1 inhibits squelch for the channel, Default is 0. |

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 95 | 7 | RWv Squelch Disable Channel 7: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 6 | RWv Squelch Disable Channel 6: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 5 | RWv Squelch Disable Channel 5: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 4 | RWv Squelch Disable Channel 4: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 3 | RWv Squelch Disable Channel 3: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 2 | RWv Squelch Disable Channel 2: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 1 | RWv Squelch Disable Channel 1: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 0 | RWv Squelch Disable Channel 0: Writing 1 inhibits squelch for the channel, Default is 0. |
| 96-98 | all | RWv Reserved: Coded 00h |
| 99 | 7-4 | RWv Reserved: Coded 0000b |
| 99 | 3 | RWv Margin Activation Channel 11: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 99 | 2 | RWv Margin Activation Channel 10: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 99 | 1 | RWv Margin Activation Channel 9: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 0 | RWv Margin Activation Channel 8: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 7 | RWv Margin Activation Channel 7: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 6 | RWv Margin Activation Channel 6: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 5 | RWv Margin Activation Channel 5: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 4 | RWv Margin Activation Channel 4: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 3 | RWv Margin Activation Channel 3: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 2 | RWv Margin Activation Channel 2: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 1 | RWv Margin Activation Channel 1: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 100 | 0 | RWv Margin Activation Channel 0: Writing 1 places channel into Margin mode (Reduces OMA by 1 dB), Default is 0. |
| 101-105 | all | RWv Reserved: Coded 00h |
| 106-111 | all | RWv Reserved: Coded 00h |
| 112 | 7-4 | RWv Reserved: Coded 0000b |
| 112 | 3 | RWv Mask LOS Tx Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 112 | 2 | RWv Mask LOS Tx Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 112 | 1 | RWv Mask LOS Tx Channel 9: Writing 1 Prevents IntL generation, Default = 0 |
| 112 | 0 | RWv Mask LOS Tx Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 7 | RWv Mask LOS Tx Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 6 | RWv Mask LOS Tx Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 5 | RWv Mask LOS Tx Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 4 | RWv Mask LOS Tx Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 3 | RWv Mask LOS Tx Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 2 | RWv Mask LOS Tx Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 1 | RWv Mask LOS Tx Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 0 | RWv Mask LOS Tx Channel 0: Writing 1 Prevents IntL generation, Default = 0 |
| 114 | 7-4 | RWv Reserved: Coded 0000b |
| 114 | 3 | RWv Mask Fault Tx Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 114 | 2 | RWv Mask Fault Tx Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 114 | 1 | RWv Mask Fault Tx Channel 9: Writing 1 Prevents IntL generation, Default = 0 |
| 114 | 0 | RWv Mask Fault Tx Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 115 | 7 | RWv Mask Fault Tx Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 115 | 6 | RWv Mask Fault Tx Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 115 | 5 | RWv Mask Fault Tx Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 115 | 4 | RWv Mask Fault Tx Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 115 | 3 | RWv Mask Fault Tx Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 115 | 2 | RWv Mask Fault Tx Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 115 | 1 | RWv Mask Fault Tx Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 115 | 0 | RWv Mask Fault Tx Channel 0: Writing 1 Prevents IntL generation, Default = 0 |

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 116 | 7 | RWv Mask High Internal Temperature Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 116 | 6 | RWv Mask Low Internal Temperature Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 116 | 5-0 | RWv Reserved |
| 117 | 7 | RWv Mask High Internal 3.3 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 117 | 6 | RWv Mask Low Internal 3.3 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 117 | 5-4 | RWv Reserved |
| 117 | 3 | RWv Mask High Internal 2.5 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 117 | 2 | RWv Mask Low Internal 2.5 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 117 | 1-0 | RWv Reserved |
| 118 | all | RWv TX output power alarm level select. Custom=01h, Factory Default=0 |
| 119-120 | all | RW Tx Optical Power All Channels Custom High Alarm Threshold: Optical power in 0.1 uW units coded as 16 bit unsigned integer, low address is MSB |
| 121-122 | all | RW TX Optical Power All Channels Custom Low Alarm Threshold: Optical power in 0.1 uW units coded as 16 bit unsigned integer, low address is MSB |
| 123-126 | all | RW Reserved: Coded 00h |
| 127 | all | RWv Page Select Byte |

4. Tx Memory Map 00h Upper Page

Transmitter serial id page 00h entries follow. Description of the registers can be found in Section 9 below.

| Address | Contents | | Type | Field Name/Description |
|---------|----------|--|------|---|
| | Byte | Bit Code | | |
| 128 | all | 00h | RO | Type Identifier: Coded 00h for unspecified. See SFF-8472 for reference |
| 129 | all | 10000010b | RO | Module Description: Coded for < 2.5 W max, Controlled Launch |
| 130 | all | 11000000b | RO | Required Power Supplies: Coded for 3.3V & 2.5V supplies |
| 131 | all | 01010000b | RO | Max Recommended Operating Case Temperature in Degrees C: Coded for 80°C |
| 132 | all | 00011001b | RO | Min Bit Rate in 100 Mb/s units: Coded for 2500 Mb/s |
| 133 | all | 01100100b | RO | Max Bit Rate in 100 Mb/s units: Coded for 10000 Mb/s |
| 134-135 | all | 42h 04h | RO | Nominal Laser Wavelength (Wavelength in nm = value / 20): Coded for 845 nm |
| 136-137 | all | 0Bh BBh | RO | Wavelength deviation from nominal (Wavelength tolerance in nm = +/- value / 200): Coded for 15 nm |
| 138 | all | 11001000b | RO | Supported Flags/Actions: Coded for Tx Fault, Tx LOS, Output Squelch for LOS, Alarm Flags |
| 139 | all | 11000101b | RO | Supported Monitors: Coded for Tx Bias, Tx LOP, Internal Temp, Elapsed Time |
| 140 | all | 01100000b | RO | Supported Monitors: Coded for 3.3V, 2.5V |
| 141 | all | 10100010b | RO | Supported Controls: Coded for Ch Disable, Squelch Disable, Input Equalization |
| 142 | all | 00001011b | RO | Supported Controls: Coded for Margin Mode, Ch Polarity Flip, Module Addressing |
| 143 | all | 00h | RO | Supported Functions: |
| 144-151 | all | 00h | RO | Reserved |
| 152-167 | all | 41h 56h 41h 47h 4Fh 20h 20h x10 | RO | Vendor Name in ASCII: Coded "AVAGO" for Avago Technologies, Spaces (20h) for unused characters |
| 168-170 | all | 00h 17h 6Ah | RO | Vendor OUI (IEEE ID): Coded "00h 17h 6Ah" for Avago Technologies |
| 171-186 | all | 41h 46h 42h 52h 2Dh 37h 37h 36h 42h ... | RO | Vendor Part Number in ASCII: AFBR-810B... where bytes 180 through 186 vary with selected option, Spaces (20h) for unused characters |
| 187-188 | all | 30h 32h | RO | Vendor Revision Number in ASCII: Coded "02" |
| 189-204 | all | | RO | Vendor Serial Number (ASCII): Varies by unit |
| 205-212 | all | | RO | Vendor Date Code YYYYMMDD (ASCII): Spaces (20h) for unused characters |
| 213-222 | all | | RO | CLEI Code in ASCII: All spaces (20h) if unused |
| 223 | all | | RO | Check sum addresses 128 through 222 |
| 224-255 | all | | RO | Vendor Specific: All zeroes if unused |

5. Tx Memory Map 01h Upper Page

Details of transmitter upper page 01h follow.

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 128 | all | RO Internal Temperature High Alarm Threshold MSB: Integer part coded in signed 2's complement |
| 129 | all | RO Internal Temperature High Alarm Threshold LSB: Fractional part in units of 1°/256 coded in binary. |
| 130 | all | RO Internal Temperature Low Alarm Threshold MSB: Integer part coded in signed 2's complement |
| 131 | all | RO Internal Temperature Low Alarm Threshold LSB: Fractional part in units of 1°/256 coded in binary. |
| 132-143 | all | RO Reserved: Coded 00h |
| 144-145 | all | RO Internal 3.3 Vcc High Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB. |
| 146-147 | all | RO Internal 3.3 Vcc Low Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB. |
| 148-151 | all | RO Reserved |
| 152-153 | all | RO Internal 2.5 Vcc High Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB. |
| 154-155 | all | RO Internal 2.5 Vcc Low Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB. |
| 156-159 | all | RO Reserved |
| 160-175 | all | RO Thresholds Reserved: Coded 00h |
| 176-177 | all | RO Tx Bias Current All Channels High Alarm Threshold: Current in 2 μA units coded as 16 bit unsigned integer, low address is MSB. |
| 178-179 | all | RO Tx Bias Current All Channels Low Alarm Threshold: Current in 2 μA units coded as 16 bit unsigned integer, low address is MSB. |
| 180-183 | all | RO Reserved |
| 184-185 | all | RO Tx Optical Power All Channels High Alarm Threshold: Optical power in 0.1 μW units coded as 16 bit unsigned integer, low address is MSB. |
| 186-187 | all | RO Tx Optical Power All Channels Low Alarm Threshold: Optical power in 0.1 μW units coded as 16 bit unsigned integer, low address is MSB. |
| 188-223 | all | RO Thresholds Reserved: Coded 00h |
| 224 | all | RO Check sum: Low order 8 bits of the sum of all bytes from 128 through 223 inclusive |
| 225 | 7-1 | RWn Reserved: Coded 0000000b |
| 225 | 0 | RWn IntL Pulse/Static Option: Writing 1 sets IntL to Static mode, Default is 0 for Pulse mode |
| 226 | 7-4 | RWn Reserved: Coded 0000b |
| 226 | 3 | RWn Input Polarity Flip Channel 11: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 226 | 2 | RWn Input Polarity Flip Channel 10: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 226 | 1 | RWn Input Polarity Flip Channel 9: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 226 | 0 | RWn Input Polarity Flip Channel 8: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 227 | 7 | RWn Input Polarity Flip Channel 7: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 227 | 6 | RWn Input Polarity Flip Channel 6: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 227 | 5 | RWn Input Polarity Flip Channel 5: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 227 | 4 | RWn Input Polarity Flip Channel 4: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 227 | 3 | RWn Input Polarity Flip Channel 3: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 227 | 2 | RWn Input Polarity Flip Channel 2: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 227 | 1 | RWn Input Polarity Flip Channel 1: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 227 | 0 | RWn Input Polarity Flip Channel 0: Writing 1 inverts truth of the differential input pair, Default is 0. |
| 228 | 7-4 | RWn Tx Input Equalization Control Channel 11: See below for code description. Default = 7 |
| 228 | 3-0 | RWn Tx Input Equalization Control Channel 10: See below for code description. Default = 7 |
| 229 | 7-4 | RWn Tx Input Equalization Control Channel 9: See below for code description. Default = 7 |
| 229 | 3-0 | RWn Tx Input Equalization Control Channel 8: See below for code description. Default = 7 |
| 230 | 7-4 | RWn Tx Input Equalization Control Channel 7: See below for code description. Default = 7 |
| 230 | 3-0 | RWn Tx Input Equalization Control Channel 6: See below for code description. Default = 7 |
| 231 | 7-4 | RWn Tx Input Equalization Control Channel 5: See below for code description. Default = 7 |
| 231 | 3-0 | RWn Tx Input Equalization Control Channel 4: See below for code description. Default = 7 |
| 232 | 7-4 | RWn Tx Input Equalization Control Channel 3: See below for code description. Default = 7 |
| 232 | 3-0 | RWn Tx Input Equalization Control Channel 2: See below for code description. Default = 7 |

| Address | Type | Field Name/Description |
|---------|------|---|
| Byte | Bit | |
| 233 | 7-4 | RWn Tx Input Equalization Control Channel 1: See below for code description. Default = 7 |
| 233 | 3-0 | RWn Tx Input Equalization Control Channel 0: See below for code description. Default = 7 |
| 234-243 | all | RWn Reserved: Coded 00h |
| 244 | 7 | RWv Mask High Tx Bias Current Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 244 | 6 | RWv Mask Low Tx Bias Current Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 244 | 5-4 | RWv Reserved |
| 244 | 3 | RWv Mask High Tx Bias Current Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 244 | 2 | RWv Mask Low Tx Bias Current Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 244 | 1-0 | RWv Reserved |
| 245 | 7 | RWv Mask High Tx Bias Current Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0 |
| 245 | 6 | RWv Mask Low Tx Bias Current Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0 |
| 245 | 5-4 | RWv Reserved |
| 245 | 3 | RWv Mask High Tx Bias Current Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 245 | 2 | RWv Mask Low Tx Bias Current Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 245 | 1-0 | RWv Reserved |
| 246 | 7 | RWv Mask High Tx Bias Current Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 246 | 6 | RWv Mask Low Tx Bias Current Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 246 | 5-4 | RWv Reserved |
| 246 | 3 | RWv Mask High Tx Bias Current Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 246 | 2 | RWv Mask Low Tx Bias Current Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 246 | 1-0 | RWv Reserved |
| 247 | 7 | RWv Mask High Tx Bias Current Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 247 | 6 | RWv Mask Low Tx Bias Current Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 247 | 5-4 | RWv Reserved |
| 247 | 3 | RWv Mask High Tx Bias Current Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 247 | 2 | RWv Mask Low Tx Bias Current Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 247 | 1-0 | RWv Reserved |
| 248 | 7 | RWv Mask High Tx Bias Current Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 248 | 6 | RWv Mask Low Tx Bias Current Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 248 | 5-4 | RWv Reserved |
| 248 | 3 | RWv Mask High Tx Bias Current Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 248 | 2 | RWv Mask Low Tx Bias Current Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 248 | 1-0 | RWv Reserved |
| 249 | 7 | RWv Mask High Tx Bias Current Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 249 | 6 | RWv Mask Low Tx Bias Current Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 249 | 5-4 | RWv Reserved |
| 249 | 3 | RWv Mask High Tx Bias Current Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0 |
| 249 | 2 | RWv Mask Low Tx Bias Current Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0 |
| 249 | 1-0 | RWv Reserved |
| 250 | 7 | RWv Mask High Tx Power Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 250 | 6 | RWv Mask Low Tx Power Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 250 | 5-4 | RWv Reserved |
| 250 | 3 | RWv Mask High Tx Power Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 250 | 2 | RWv Mask Low Tx Power Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 250 | 1-0 | RWv Reserved |

| Address | Type | Field Name/Description |
|---------|------|---|
| Byte | Bit | |
| 251 | 5-4 | RWv Reserved |
| 251 | 3 | RWv Mask High Tx Power Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 251 | 2 | RWv Mask Low Tx Power Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 251 | 1-0 | RWv Reserved |
| 252 | 7 | RWv Mask High Tx Power Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 252 | 6 | RWv Mask Low Tx Power Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 252 | 5-4 | RWv Reserved |
| 252 | 3 | RWv Mask High Tx Power Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 252 | 2 | RWv Mask Low Tx Power Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 252 | 1-0 | RWv Reserved |
| 253 | 7 | RWv Mask High Tx Power Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 253 | 6 | RWv Mask Low Tx Power Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 253 | 5-4 | RWv Reserved |
| 253 | 3 | RWv Mask High Tx Power Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 253 | 2 | RWv Mask Low Tx Power Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 253 | 1-0 | RWv Reserved |
| 254 | 7 | RWv Mask High Tx Power Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 254 | 6 | RWv Mask Low Tx Power Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 254 | 5-4 | RWv Reserved |
| 254 | 3 | RWv Mask High Tx Power Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 254 | 2 | RWv Mask Low Tx Power Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 254 | 1-0 | RWv Reserved |
| 255 | 7 | RWv Mask High Tx Power Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 255 | 6 | RWv Mask Low Tx Power Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 255 | 5-4 | RWv Reserved |
| 255 | 3 | RWv Mask High Tx Power Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0 |
| 255 | 2 | RWv Mask Low Tx Power Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0 |
| 255 | 1-0 | RWv Reserved |

Transmitter Input Equalization Control Code Description

Control registers 228 through 233 permit input equalization control. Four bit code blocks (either bits 7 through 4 or 3 through 0 where bit 7 or 3 is the msb) are assigned to each channel.

Codes 1xxx are reserved.

Code 0111 calls for full scale equalization and code 0000 calls for no equalization.

Intermediate code values provide intermediate levels of compensation.

6. Rx Memory Map 5ih Lower Page

Details of the base or lower page of the memory map for a receiver follow.

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 0 | all | RO Type Identifier: Coded 00h for unspecified |
| 1 | all | RO Reserved: Coded 00h |
| 2 | 7-3 | RO Reserved: Coded 000000b |
| 2 | 2 | RO LOS Status: Coded 1 when a LOS flag (bytes 9 and 10 of this page) is asserted for any channel, else 0. Clears when LOS flags are cleared. |
| 2 | 1 | RO IntL Status: Coded 1 for asserted IntL. Clears to 0 when all flags including LOS are cleared. |
| 2 | 0 | RO Data Not Ready: Coded 1 until data is available in monitor registers. Coded 0 in normal operation. |
| 3 - 7 | all | RO Reserved: Coded 00h |
| 8 | 0 | Module Ready Interrupt. Coded 1 when asserted and module is Ready to respond to TWS commands, Latched, Clears on Read. |
| 9 | 7-4 | RO Reserved: Coded 0000b |
| 9 | 3 | RO LOS Latched Rx Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 9 | 2 | RO LOS Latched Rx Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 9 | 1 | RO LOS Latched Rx Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 9 | 0 | RO LOS Latched Rx Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 7 | RO LOS Latched Rx Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 6 | RO LOS Latched Rx Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 5 | RO LOS Latched Rx Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 4 | RO LOS Latched Rx Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 3 | RO LOS Latched Rx Channel 3: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 2 | RO LOS Latched Rx Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 1 | RO LOS Latched Rx Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 10 | 0 | RO LOS Latched Rx Channel 0: Coded 1 when asserted, Latched, Clears on Read. |
| 11-12 | all | RO Reserved: Coded 00h |
| 13 | 7 | RO High Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 13 | 6 | RO Low Internal Temperature Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 13 | 5-0 | RO Reserved |
| 14 | 7 | RO High Internal 3.3 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 14 | 6 | RO Low Internal 3.3 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 14 | 5-4 | RO Reserved |
| 14 | 3 | RO High Internal 2.5 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 14 | 2 | RO Low Internal 2.5 Vcc Alarm Latched: Coded 1 when asserted, Latched, Clears on Read. |
| 14 | 1-0 | RO Reserved |
| 15-21 | all | RO Reserved: Coded 00h |
| 22 | 7 | RO High Rx Power Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 22 | 6 | RO Low Rx Power Alarm Latched Channel 11: Coded 1 when asserted, Latched, Clears on Read. |
| 22 | 5-4 | RO Reserved |
| 22 | 3 | RO High Rx Power Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 22 | 2 | RO Low Rx Power Alarm Latched Channel 10: Coded 1 when asserted, Latched, Clears on Read. |
| 22 | 1-0 | RO Reserved |
| 23 | 7 | RO High Rx Power Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 23 | 6 | RO Low Rx Power Alarm Latched Channel 9: Coded 1 when asserted, Latched, Clears on Read. |
| 23 | 5-4 | RO Reserved |
| 23 | 3 | RO High Rx Power Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 23 | 2 | RO Low Rx Power Alarm Latched Channel 8: Coded 1 when asserted, Latched, Clears on Read. |
| 23 | 1-0 | RO Reserved |

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 24 | 7 | RO High Rx Power Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 24 | 6 | RO Low Rx Power Alarm Latched Channel 7: Coded 1 when asserted, Latched, Clears on Read. |
| 24 | 5-4 | RO Reserved |
| 24 | 3 | RO High Rx Power Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 24 | 2 | RO Low Rx Power Alarm Latched Channel 6: Coded 1 when asserted, Latched, Clears on Read. |
| 24 | 1-0 | RO Reserved |
| 25 | 7 | RO High Rx Power Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 25 | 6 | RO Low Rx Power Alarm Latched Channel 5: Coded 1 when asserted, Latched, Clears on Read. |
| 25 | 5-4 | RO Reserved |
| 25 | 3 | RO High Rx Power Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 25 | 2 | RO Low Rx Power Alarm Latched Channel 4: Coded 1 when asserted, Latched, Clears on Read. |
| 25 | 1-0 | RO Reserved |
| 26 | 7 | RO High Rx Power Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read. |
| 26 | 6 | RO Low Rx Power Alarm Latched Channel 3: Coded 1 when asserted, Latched, Clears on Read. |
| 26 | 5-4 | RO Reserved |
| 26 | 3 | RO High Rx Power Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 26 | 2 | RO Low Rx Power Alarm Latched Channel 2: Coded 1 when asserted, Latched, Clears on Read. |
| 26 | 1-0 | RO Reserved |
| 27 | 7 | RO High Rx Power Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 27 | 6 | RO Low Rx Power Alarm Latched Channel 1: Coded 1 when asserted, Latched, Clears on Read. |
| 27 | 5-4 | RO Reserved |
| 27 | 3 | RO High Rx Power Alarm Latched Channel 0: Coded 1 when asserted, Latched, Clears on Read. |
| 27 | 2 | RO Low Rx Power Alarm Latched Channel 01: Coded 1 when asserted, Latched, Clears on Read. |
| 27 | 1-0 | RO Reserved |
| 28 | all | RO Internal Temperature Monitor MSB: Integer part coded in signed 2's complement. Tolerance is $\pm 3^{\circ}\text{C}$. |
| 29 | all | RO Internal Temperature Monitor LSB: Fractional part in units of $1^{\circ}/256$ coded in binary. |
| 30-31 | all | RO Reserved: Coded 00h |
| 32-33 | all | RO Internal 3.3 Vcc Monitor: Voltage in 100 μV units coded as 16 bit unsigned integer, Byte 32 is MSB. Tolerance is $\pm 0.150\text{V}$. |
| 34-35 | all | RO Internal 2.5 Vcc Monitor: Voltage in 100 μV units coded as 16 bit unsigned integer, Byte 34 is MSB. Tolerance is $\pm 0.150\text{V}$. |
| 36-63 | all | RO Reserved: Coded 00h |
| 64-65 | all | RO Rx Optical Input, Pave, Monitor Channel 11: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 64 is MSB. Tolerance is $\pm 3\text{dB}$ for -10 dBm to -1.0 dBm range. |
| 66-67 | all | RO Rx Optical Input, Pave, Monitor Channel 10: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 66 is MSB. Tolerance is $\pm 3\text{dB}$ for -10 dBm to -1.0 dBm range. |
| 68-69 | all | RO Rx Optical Input, Pave, Monitor Channel 9: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 68 is MSB. Tolerance is $\pm 3\text{dB}$ for -10 dBm to -1.0 dBm range. |
| 70-71 | all | RO Rx Optical Input, Pave, Monitor Channel 8: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 70 is MSB. Tolerance is $\pm 3\text{dB}$ for -10 dBm to -1.0 dBm range. |
| 72-73 | all | RO Rx Optical Input, Pave, Monitor Channel 7: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 72 is MSB. Tolerance is $\pm 3\text{dB}$ for -10 dBm to -1.0 dBm range. |
| 74-75 | all | RO Rx Optical Input, Pave, Monitor Channel 6: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 74 is MSB. Tolerance is $\pm 3\text{dB}$ for -10 dBm to -1.0 dBm range. |
| 76-77 | all | RO Rx Optical Input, Pave, Monitor Channel 5: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 76 is MSB. Tolerance is $\pm 3\text{dB}$ for -10 dBm to -1.0 dBm range. |
| 78-79 | all | RO Rx Optical Input, Pave, Monitor Channel 4: Optical power in 0.1 μW units coded as 16 bit unsigned integer, Byte 78 is MSB. Tolerance is $\pm 3\text{dB}$ for -10 dBm to -1.0 dBm range. |

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 80-81 | all | RO Rx Optical Input, Pave, Monitor Channel 3: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 80 is MSB. Tolerance is \pm 3dB for -10 dBm to -1.0 dBm range. |
| 82-83 | all | RO Rx Optical Input, Pave, Monitor Channel 2: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 82 is MSB. Tolerance is \pm 3dB for -10 dBm to -1.0 dBm range. |
| 84-85 | all | RO Rx Optical Input, Pave, Monitor Channel 1: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 84 is MSB. Tolerance is \pm 3dB for -10 dBm to -1.0 dBm range. |
| 86-87 | all | RO Rx Optical Input, Pave, Monitor Channel 0: Optical power in 0.1 μ W units coded as 16 bit unsigned integer, Byte 86 is MSB. Tolerance is \pm 3dB for -10 dBm to -1.0 dBm range. |
| 88-89 | all | RO Elapsed (Power-on) Operating Time: Elapsed time in 2 hour units coded as 16 bit unsigned integer, Byte 88 is MSB, Tolerance is \pm 10% |
| 90 | all | RWv Reserved: Coded 00h |
| 91 | 7-1 | RWv Reserved: Coded 0000000b |
| 91 | 0 | RWv Receiver Reset: Writing 1 return all registers except non-volatile RW to factory default values. Reads 0 after operation. |
| 92 | 7-4 | RWv Reserved: Coded 0000b |
| 92 | 3 | RWv Rx Channel 11 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 92 | 2 | RWv Rx Channel 10 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 92 | 1 | RWv Rx Channel 9 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 92 | 0 | RWv Rx Channel 8 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 93 | 7 | RWv Rx Channel 7 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 93 | 6 | RWv Rx Channel 6 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 93 | 5 | RWv Rx Channel 5 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 93 | 4 | RWv Rx Channel 4 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 93 | 3 | RWv Rx Channel 3 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 93 | 2 | RWv Rx Channel 2 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 93 | 1 | RWv Rx Channel 1 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 93 | 0 | RWv Rx Channel 0 Disable: Writing 1 deactivates the electrical output, Default is 0. |
| 94 | 7-4 | RWv Reserved: Coded 0000b |
| 94 | 3 | RWv Squelch Disable Channel 11: Writing 1 inhibits squelch for the channel, Default is 0. |
| 94 | 2 | RWv Squelch Disable Channel 10: Writing 1 inhibits squelch for the channel, Default is 0. |
| 94 | 1 | RWv Squelch Disable Channel 9: Writing 1 inhibits squelch for the channel, Default is 0. |
| 94 | 0 | RWv Squelch Disable Channel 8: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 7 | RWv Squelch Disable Channel 7: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 6 | RWv Squelch Disable Channel 6: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 5 | RWv Squelch Disable Channel 5: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 4 | RWv Squelch Disable Channel 4: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 3 | RWv Squelch Disable Channel 3: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 2 | RWv Squelch Disable Channel 2: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 1 | RWv Squelch Disable Channel 1: Writing 1 inhibits squelch for the channel, Default is 0. |
| 95 | 0 | RWv Squelch Disable Channel 0: Writing 1 inhibits squelch for the channel, Default is 0. |
| 96 | 7-6 | RWv Rate Select Channel 11: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 96 | 5-4 | RWv Rate Select Channel 10: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 96 | 3-2 | RWv Rate Select Channel 9: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 96 | 1-0 | RWv Rate Select Channel 8: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 97 | 7-6 | RWv Rate Select Channel 7: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 97 | 5-4 | RWv Rate Select Channel 6: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 97 | 3-2 | RWv Rate Select Channel 5: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 97 | 1-0 | RWv Rate Select Channel 4: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 98 | 7-6 | RWv Rate Select Channel 3: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 98 | 5-4 | RWv Rate Select Channel 2: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 98 | 3-2 | RWv Rate Select Channel 1: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 98 | 1-0 | RWv Rate Select Channel 0: Write 00 for max. BW, 01 for SDR BW, rest reserved. Default is 00 |
| 99-105 | all | RWv Reserved: Coded 00h |
| 106-111 | all | RWv Reserved: Coded 00h |
| 112 | 7-4 | RWv Reserved: Coded 0000b |
| 112 | 3 | RWv Mask LOS Rx Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 112 | 2 | RWv Mask LOS Rx Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 112 | 1 | RWv Mask LOS Rx Channel 9: Writing 1 Prevents IntL generation, Default = 0 |
| 112 | 0 | RWv Mask LOS Rx Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 7 | RWv Mask LOS Rx Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 6 | RWv Mask LOS Rx Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 5 | RWv Mask LOS Rx Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 4 | RWv Mask LOS Rx Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 3 | RWv Mask LOS Rx Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 2 | RWv Mask LOS Rx Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 1 | RWv Mask LOS Rx Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 113 | 0 | RWv Mask LOS Rx Channel 0: Writing 1 Prevents IntL generation, Default = 0 |
| 114-115 | all | RWv Reserved: Coded 00h |
| 116 | 7 | RWv Mask Internal High Temperature Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 116 | 6 | RWv Mask Internal Low Temperature Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 116 | 5-0 | RWv Reserved |
| 117 | 7 | RWv Mask Internal High 3.3 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 117 | 6 | RWv Mask Internal Low 3.3 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 117 | 5-4 | RWv Reserved |
| 117 | 3 | RWv Mask Internal High 2.5 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 117 | 2 | RWv Mask Internal Low 2.5 Vcc Alarm: Writing 1 Prevents IntL generation, Default = 0 |
| 117 | 1-0 | RWv Reserved |
| 118 | all | RW Rx input power alarm level select. Custom=01h, Factory Default=00h |
| 119-120 | all | RW Rx Optical Power All Channels Custom High Alarm Threshold: Optical power in 0.1 uW units coded as 16 bit unsigned integer, low address is MSB |
| 121-122 | all | RW Rx Optical Power All Channels Custom Low Alarm Threshold: Optical power in 0.1 uW units coded as 16 bit unsigned integer, low address is MSB |
| 123-126 | all | RW Reserved: Coded 00h |
| 127 | all | RWv Page Select Byte |

7. Rx Memory Map 00h Upper Page

Receiver serial id page 00h entries follow. Description of the registers can be found in Section 9 below.

| Address | Contents | | Type | Field Name/Description |
|---------|----------|---|------|---|
| | Byte | Bit Code | | |
| 128 | all | 00h | RO | Type Identifier: Coded 00h for unspecified. See SFF-8472 for reference |
| 129 | all | 01000000b | RO | Module Description: Coded for < 2.0 W |
| 130 | all | 11000000b | RO | Required Power Supplies: Coded for 3.3V & 2.5V supplies |
| 131 | all | 01010000b | RO | Max Recommended Operating Case Temperature in Degrees C: Coded for 80°C |
| 132 | all | 00011001b | RO | Min Bit Rate in 100 Mb/s units: Coded for 2500 Mb/s |
| 133 | all | 01100100b | RO | Max Bit Rate in 100 Mb/s units: Coded for 10000 Mb/s |
| 134-135 | all | 00h | RO | Nominal Laser Wavelength (Wavelength in nm = value / 20): Coded 00h for Rx |
| 136-137 | all | 00h | RO | Wavelength deviation from nominal (tolerance in nm = +/- value / 200): Coded 00h for Rx |
| 138 | all | 00101000b | RO | Supported Flags/Actions: Coded for Rx LOS, Output Squelch for LOS, Alarm Flags |
| 139 | all | 00110101b | RO | Supported Monitors: Coded for Rx Input, Pave, Internal Temp, Elapsed Time |
| 140 | all | 01100000b | RO | Supported Monitors: Coded for 3.3V, 2.5V |
| 141 | all | 10101000b | RO | Supported Controls: Coded for Ch Disable, Squelch Disable, Rate Select |
| 142 | all | 10100011b | RO | Supported Controls: Coded for Rx Amplitude, Rx De-emphasis, Ch Polarity Flip, Addressing |
| 143 | all | 00h | RO | Supported Functions |
| 144-151 | all | 00h | RO | Reserved |
| 152-167 | all | 41h 56h 41h 47h 4Fh 20h 20h x10 | RO | Vendor Name in ASCII: Coded "AVAGO" for Avago Technologies, Spaces (20h) for unused characters |
| 168-170 | all | 00h 17h 6Ah | RO | Vendor OUI (IEEE ID): Coded "00h 17h 6Ah" for Avago Technologies |
| 171-186 | all | 41h 46h 42h 52h 2Dh 37h 38h 36h 42h ... | RO | Vendor Part Number in ASCII: AFBR-820B... where bytes 180 through 186 vary with selected option, Spaces (20h) for unused characters |
| 187-188 | all | 30h 32h | RO | Vendor Revision Number in ASCII: Coded "02" |
| 189-204 | all | | RO | Vendor Serial Number (ASCII): Varies by unit |
| 205-212 | all | | RO | Vendor Date Code YYYYMMDD (ASCII): Spaces (20h) for unused characters |
| 213-222 | all | | RO | CLEI Code in ASCII: All spaces (20h) if unused |
| 223 | all | | RO | Check sum addresses 128 through 222 |
| 224-255 | all | | RO | Vendor Specific: All zeroes if unused |

8. Rx Memory Map 01h Upper Page

Details of receiver upper page 01h follow.

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 128 | all | RO Internal Temperature High Alarm Threshold MSB: Integer part coded in signed 2's complement |
| 129 | all | RO Internal Temperature High Alarm Threshold LSB: Fractional part in units of 1°/256 coded in binary. |
| 130 | all | RO Internal Temperature Low Alarm Threshold MSB: Integer part coded in signed 2's complement |
| 131 | all | RO Internal Temperature Low Alarm Threshold LSB: Fractional part in units of 1°/256 coded in binary. |
| 132-143 | all | RO Reserved |
| 144-145 | all | RO Internal 3.3 Vcc High Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB. |
| 146-147 | all | RO Internal 3.3 Vcc Low Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB. |
| 148-151 | all | RO Reserved |
| 152-153 | all | RO Internal 2.5 Vcc High Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB. |
| 154-155 | all | RO Internal 2.5 Vcc Low Alarm Threshold: Voltage in 100 μV units coded as 16 bit unsigned integer, low address is MSB. |
| 156-159 | all | RO Reserved |
| 160-183 | all | RO Thresholds Reserved: Coded 00h |
| 184-185 | all | RO Rx Optical Power All Channels High Alarm Threshold: Optical power in 0.1 μW units coded as 16 bit unsigned integer, low address is MSB. |
| 186-187 | all | RO Rx Optical Power All Channels Low Alarm Threshold: Optical power in 0.1 μW units coded as 16 bit unsigned integer, low address is MSB. |
| 188-223 | all | RO Thresholds Reserved: Coded 00h |
| 224 | all | RO Check sum: Low order 8 bits of the sum of all bytes from 128 through 223 inclusive |
| 225 | 7-1 | RWn Reserved: Coded 0000000b |
| 225 | 0 | RWn IntL Pulse/Static Option: Writing 1 sets IntL to Static mode, Default is 0 for Pulse mode |
| 226 | 7-4 | RWn Reserved: Coded 0000b |
| 226 | 3 | RWn Output Polarity Flip Channel 11: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 226 | 2 | RWn Output Polarity Flip Channel 10: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 226 | 1 | RWn Output Polarity Flip Channel 9: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 226 | 0 | RWn Output Polarity Flip Channel 8: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 227 | 7 | RWn Output Polarity Flip Channel 4: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 227 | 6 | RWn Output Polarity Flip Channel 6: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 227 | 5 | RWn Output Polarity Flip Channel 5: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 227 | 4 | RWn Output Polarity Flip Channel 4: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 227 | 3 | RWn Output Polarity Flip Channel 3: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 227 | 2 | RWn Output Polarity Flip Channel 2: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 227 | 1 | RWn Output Polarity Flip Channel 1: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 227 | 0 | RWn Output Polarity Flip Channel 0: Writing 1 inverts truth of the differential output pair, Default is 0. |
| 228 | 7-4 | RWn Rx Output Amplitude Control: Channel 11. See below for code description. Default = 5 |
| 228 | 3-0 | RWn Rx Output Amplitude Control: Channel 10. See below for code description. Default = 5 |
| 229 | 7-4 | RWn Rx Output Amplitude Control: Channel 9. See below for code description. Default = 5 |
| 229 | 3-0 | RWn Rx Output Amplitude Control: Channel 8. See below for code description. Default = 5 |
| 230 | 7-4 | RWn Rx Output Amplitude Control: Channel 7. See below for code description. Default = 5 |
| 230 | 3-0 | RWn Rx Output Amplitude Control: Channel 6. See below for code description. Default = 5 |
| 231 | 7-4 | RWn Rx Output Amplitude Control: Channel 5. See below for code description. Default = 5 |
| 231 | 3-0 | RWn Rx Output Amplitude Control: Channel 4. See below for code description. Default = 5 |
| 232 | 7-4 | RWn Rx Output Amplitude Control: Channel 3. See below for code description. Default = 5 |
| 232 | 3-0 | RWn Rx Output Amplitude Control: Channel 2. See below for code description. Default = 5 |
| 233 | 7-4 | RWn Rx Output Amplitude Control: Channel 1. See below for code description. Default = 5 |
| 233 | 3-0 | RWn Rx Output Amplitude Control: Channel 0. See below for code description. Default = 5 |

| Address | Type | Field Name/Description |
|---------|------|--|
| Byte | Bit | |
| 234 | 7-4 | RWn Rx Output De-emphasis Control: Channel 11. See below for code description. Default = 4 |
| 234 | 3-0 | RWn Rx Output De-emphasis Control: Channel 10. See below for code description. Default = 4 |
| 235 | 7-4 | RWn Rx Output De-emphasis Control: Channel 9. See below for code description. Default = 4 |
| 235 | 3-0 | RWn Rx Output De-emphasis Control: Channel 8. See below for code description. Default = 4 |
| 236 | 7-4 | RWn Rx Output De-emphasis Control: Channel 7. See below for code description. Default = 4 |
| 236 | 3-0 | RWn Rx Output De-emphasis Control: Channel 6. See below for code description. Default = 4 |
| 237 | 7-4 | RWn Rx Output De-emphasis Control: Channel 5. See below for code description. Default = 4 |
| 237 | 3-0 | RWn Rx Output De-emphasis Control: Channel 4. See below for code description. Default = 4 |
| 238 | 7-4 | RWn Rx Output De-emphasis Control: Channel 3. See below for code description. Default = 4 |
| 238 | 3-0 | RWn Rx Output De-emphasis Control: Channel 2. See below for code description. Default = 4 |
| 239 | 7-4 | RWn Rx Output De-emphasis Control: Channel 1. See below for code description. Default = 4 |
| 239 | 3-0 | RWn Rx Output De-emphasis Control: Channel 0. See below for code description. Default = 4 |
| 240-243 | all | RWn Reserved: Coded 00h |
| 244-249 | all | RWv Reserved: Coded 00h |
| 250 | 7 | RWv Mask High Rx Power Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 250 | 6 | RWv Mask Low Rx Power Alarm Channel 11: Writing 1 Prevents IntL generation, Default = 0 |
| 250 | 5-4 | RWv Reserved |
| 250 | 3 | RWv Mask High Rx Power Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 250 | 2 | RWv Mask Low Rx Power Alarm Channel 10: Writing 1 Prevents IntL generation, Default = 0 |
| 250 | 1-0 | RWv Reserved |
| 251 | 7 | RWv Mask Bt High Rx Power Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0 |
| 251 | 6 | RWv Mask Low Rx Power Alarm Channel 9: Writing 1 Prevents IntL generation, Default = 0 |
| 251 | 5-4 | RWv Reserved |
| 251 | 3 | RWv Mask High Rx Power Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 251 | 2 | RWv Mask Low Rx Power Alarm Channel 8: Writing 1 Prevents IntL generation, Default = 0 |
| 251 | 1-0 | RWv Reserved |
| 252 | 7 | RWv Mask High Rx Power Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 252 | 6 | RWv Mask Low Rx Power Alarm Channel 7: Writing 1 Prevents IntL generation, Default = 0 |
| 252 | 5-4 | RWv Reserved |
| 252 | 3 | RWv Mask High Rx Power Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 252 | 2 | RWv Mask Low Rx Power Alarm Channel 6: Writing 1 Prevents IntL generation, Default = 0 |
| 252 | 1-0 | RWv Reserved |
| 253 | 7 | RWv Mask High Rx Power Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 253 | 6 | RWv Mask Low Rx Power Alarm Channel 5: Writing 1 Prevents IntL generation, Default = 0 |
| 253 | 5-4 | RWv Reserved |
| 253 | 3 | RWv Mask High Rx Power Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 253 | 2 | RWv Mask Low Rx Power Alarm Channel 4: Writing 1 Prevents IntL generation, Default = 0 |
| 253 | 1-0 | RWv Reserved |
| 254 | 7 | RWv Mask High Rx Power Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 254 | 6 | RWv Mask Low Rx Power Alarm Channel 3: Writing 1 Prevents IntL generation, Default = 0 |
| 254 | 5-4 | RWv Reserved |
| 254 | 3 | RWv Mask High Rx Power Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 254 | 2 | RWv Mask Low Rx Power Alarm Channel 2: Writing 1 Prevents IntL generation, Default = 0 |
| 254 | 1-0 | RWv Reserved |
| 255 | 7 | RWv Mask High Rx Power Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 255 | 6 | RWv Mask Low Rx Power Alarm Channel 1: Writing 1 Prevents IntL generation, Default = 0 |
| 255 | 5-4 | RWv Reserved |
| 255 | 3 | RWv Mask High Rx Power Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0 |
| 255 | 2 | RWv Mask Low Rx Power Alarm Channel 0: Writing 1 Prevents IntL generation, Default = 0 |
| 255 | 1-0 | RWv Reserved |

Receiver Output Amplitude Control Code Description

Control registers 228 through 233 permit output signal amplitude selection. Four bit code blocks (either bits 7 through 4 or 3 through 0 where bit 7 or 3 is the msb) are assigned to each channel. Codes 1xxx are reserved. Code 0111 calls for full scale signal amplitude and code 0000 calls for minimum signal amplitude. See table below.

| Code | Receiver Output Amplitude – No De-emphasis | | | Reference | |
|-------|--|---------|-----|-----------|------------|
| | Min | Nominal | Max | | Units |
| 1xxx | | | | Reserved | |
| 0111b | | 850 | | mVpp | Full Scale |
| 0110b | | 760 | | mVpp | |
| 0101b | | 670 | | mVpp | |
| 0100b | | 580 | | mVpp | |
| 0011b | | 490 | | mVpp | |
| 0010b | | 400 | | mVpp | |
| 0001b | | 310 | | mVpp | |
| 0000b | | 220 | | mVpp | |

Receiver Output De-emphasis Control Code Description

Control registers 234 through 239 permit output de-emphasis selection. Four bit code blocks (either bits 7 through 4 or 3 through 0 where bit 7 or 3 is the msb) are assigned to each channel.

Codes 1xxx are reserved.

Code 0111 calls for full scale, 6 dB, de-emphasis and code 0000 calls for no de-emphasis.

Intermediate code values yield intermediate de-emphasis levels.

9. Serial ID 00h Upper Page Description

Description of Serial id page 00h codes follows.

Byte 128 Module Type

| Address | Field Name/Description | |
|---------|------------------------|--|
| Byte | Code | Module Type |
| 128 | | Type Identifier: See SFF-8472 for reference, also SFP & XFP MSA, Coded 00h if unspecified. |

Byte 129 Module Description

| Address | Field Name/Description | |
|---------|------------------------|---|
| Byte | Bit | Code |
| 129 | 7-6 | 00b Power Class 1: Module Power Consumption < 1.5 W |
| | 7-6 | 01b Power Class 2: Module Power Consumption < 2.0 W |
| | 7-6 | 10b Power Class 3: Module Power Consumption < 2.5 W |
| | 7-6 | 11b Power Class 4: Module Power Consumption < 3.5 W |
| | 5 | Coded 1 for Tx CDR provided; else coded 0 |
| | 4 | Coded 1 for Rx CDR provided; else coded 0 |
| | 3 | Coded 1 for Required Reference Clock; else coded 0 |
| | 2 | Coded 1 for Page 02 provided; else coded 0 |
| | 1 | Coded 1 for Controlled Launch Transmitter (TIA 492AAAC); else coded 0 |
| | 0 | Reserved |

Byte 130 Module Description: Required Power Supplies

| Address | Field Name/Description | |
|---------|------------------------|---|
| Byte | Bit | Code |
| 130 | 7 | 3.3 V, Coded 1 if required, else coded 0. |
| | 6 | 2.5 V, Coded 1 if required, else coded 0. |
| | 5 | 1.8 V, Coded 1 if required, else coded 0. |
| | 4 | Vo Supply, Coded 1 if required, else coded 0. |
| | 3 | Variable Supply, Coded 1 if required, else coded 0. |
| | 2-0 | Reserved |

Byte 131 Module Description: Max Recommended Operating Case Temperature

| Address | Field Name/Description | |
|---------|------------------------|-------------------------------|
| Byte | Bit | Code |
| 131 | | Max Tc = binary value x 1.0°C |

Byte 132 Module Description Min Signal Rate per channel

| Address | Field Name/Description | |
|---------|------------------------|---|
| Byte | Code | |
| 132 | 00h | Unknown/unspecified |
| | rest | Min Signal Rate = binary value x 100 Mb/s |

Byte 133 Module Description Max Signal Rate per channel

| Address | Field Name/Description | |
|---|------------------------|---------------------|
| Byte | Code | |
| 133 | 00h | Unknown/unspecified |
| Max Signal Rate = binary value x 100 Mb/s | | |

Byte 134 - 137 Module Description Wavelength & Tolerance

| Address | Field Name/Description | |
|---------|--|--|
| Byte | Code | |
| 134-135 | Nominal Center Wavelength: Wavelength in nm = binary value / 20, Coded 00b if unspecified/unused. | |
| 136-137 | Wavelength Tolerance: Tolerance in nm = \pm binary value / 200, Coded 00b if unspecified/unused. | |

Byte 138 Supported Functions – Flags/Actions

| Address | Field Name/Description | |
|---------|------------------------|--|
| Byte | Bit | Code |
| 138 | 7 | Coded 1 for Tx Fault Flag provided, else coded 0 |
| | 6 | Coded 1 for Tx LOS Flag provided, else coded 0 |
| | 5 | Coded 1 for Rx LOS Flag provided, else coded 0 |
| | 4 | Coded 1 for CDR LOL Flag provided, else coded 0 |
| | 3 | Coded 1 for Output Squelch for LOS provided, else coded 0 |
| | 2 | Coded 1 for Monitor Alarm & Warning Flags provided, coded 0 for Monitor Alarm Flags provided |
| | 1-0 | Reserved |

Byte 139 - 140 Supported Functions - Monitors

| Address | Field Name/Description | |
|---------|------------------------|---|
| Byte | Bit | Code |
| 139 | 7 | Coded 1 for Tx Bias Monitor, else coded 0 |
| 139 | 6 | Coded 1 for Tx LOP Monitor, else coded 0 |
| 139 | 5 | Coded 1 for individual Rx Input Power Monitors, coded 0 for single-channel or group monitor |
| 139 | 4 | Coded 1 for Rx Input Power reported as Pave, coded 0 for reported as OMA |
| 139 | 3 | Coded 1 for Case Temperature Monitor, else coded 0 |
| 139 | 2 | Coded 1 for Internal Temperature Monitor, else coded 0 |
| 139 | 1 | Coded 1 for Peak Temperature Monitor, else coded 0 |
| 139 | 0 | Coded 1 for Elapsed Time Monitor, else coded 0 |
| 140 | 7 | Coded 1 for BER Monitor, else coded 0 |
| 140 | 6 | Coded 1 for Internal 3.3 V Vcc Monitor, else coded 0 |
| 140 | 5 | Coded 1 for Internal 2.5 V Vcc Monitor, else coded 0 |
| 140 | 4 | Coded 1 for Internal 1.8 V Vcc Monitor, else coded 0 |
| 140 | 3 | Coded 1 for Internal Vo Vcc Monitor, else coded 0 |
| 140 | 2 | Coded 1 for TEC current Monitor, else coded 0 |
| 140 | 1-0 | Reserved |

Byte 141 Supported Functions – Controls

| Address | | | Field Name/Description |
|---------|-----|------|--|
| Byte | Bit | Code | |
| 141 | 7-6 | 00 | Channel Disable Control not provided/unspecified |
| | 7-6 | 01 | Global Channel Disable Control implemented |
| | 7-6 | 10 | Individual and independent Channel Disable Control implemented |
| | 7-6 | 11 | Reserved |
| 5-4 | 00 | | Squelch Disable Control not provided/unspecified |
| | 01 | | Global Squelch Disable Control implemented |
| | 10 | | Individual and independent Channel Squelch Control implemented |
| | 11 | | Reserved |
| 3-2 | 00 | | Rate Select Control not provided/unspecified |
| | 01 | | Global Rate Select Control implemented |
| | 10 | | Individual and independent Rate Select Control implemented |
| | 11 | | Reserved |
| 1-0 | 00 | | Tx Input Equalization Control not provided/unspecified |
| | 01 | | Global Tx Input Equalization Control implemented |
| | 10 | | Individual and independent Tx Input Equalization Control implemented |
| | 11 | | Reserved |

Byte 142 Supported Functions – Controls

| Address | | | Field Name/Description |
|---------|-----|------|--|
| Byte | Bit | Code | |
| 142 | 7-6 | 00 | Rx Output Amplitude Control not provided/unspecified |
| | 7-6 | 01 | Global Rx Output Amplitude Control implemented |
| | 7-6 | 10 | Individual and independent Rx Output Amplitude Control implemented |
| | 7-6 | 11 | Reserved |
| 5-4 | 00 | | Rx Output De-emphasis Control not provided/unspecified |
| | 01 | | Global Rx Output De-emphasis Control implemented |
| | 10 | | Individual and independent Rx Output De-emphasis Control implemented |
| | 11 | | Reserved |
| | 3 | | Coded 1 for Tx Margin Mode provided, else coded 0 |
| | 2 | | Coded 1 for Channel Reset Control provided, else coded 0 |
| | 1 | | Coded 1 for Channel Polarity Flip Control provided, else coded 0 |
| | 0 | | Coded 1 for Module Addressing Control provided, else coded 0 |

Byte 143 Supported Functions

| Address | | | Field Name/Description |
|---------|-----|------|---|
| Byte | Bit | Code | |
| 143 | 7 | | Coded 1 for FEC Control, else coded 0 |
| | 6 | | Coded 1 for PEC Control, else coded 0 |
| | 5 | | Coded 1 for JTAG Control, else coded 0 |
| | 4 | | Coded 1 for AC-JTAG Control, else coded 0 |
| | 3 | | Coded 1 for BIST, else coded 0 |
| | 2 | | Coded 1 for TEC Temperature Control, else coded 0 |
| | 1 | | Coded 1 for Sleep Mode Set Control provided, else coded 0 |
| | 0 | | Coded 1 for CDR Bypass Control provided, else coded 0 |

Byte144 - 151 Reserved

| Address | | | Field Name/Description |
|---------|-----|------|------------------------|
| Byte | Bit | Code | |
| 144-151 | | | Reserved: Coded 00h |

Byte 152 - 221 Vendor Information

| Address | | | Field Name/Description |
|---------|-----|------|--|
| Byte | Bit | Code | |
| 152-167 | | | Vendor Name ASCII – 16 bytes |
| 168-170 | | | Vendor OUI – 3 bytes; Unspecified where coded all zeroes |
| 171-186 | | | Vendor Part Number ASCII – 16 bytes |
| 187-188 | | | Vendor Revision Number ASCII – 2 bytes |
| 189-204 | | | Vendor Serial Number ASCII – 16 bytes |
| 205-212 | | | Vendor Date Code ASCII – 8 bytes; coded YYYYMMDD with spaces (20h) for unused characters |
| 213-222 | | | CLEI Code – 10 bytes; Unspecified where coded all zeroes |

Byte 223 Check Sum for bytes 128 through 222

| Address | | | Field Name/Description |
|---------|-----|------|---|
| Byte | Bit | Code | |
| 223 | | | Check Code – 1 byte: Low order 8 bits of the sum of all bytes from 128 through 222 inclusive. |

Byte 224 - 255 Vendor Specific

| Address | | | Field Name/Description |
|---------|-----|------|----------------------------|
| Byte | Bit | Code | |
| 224-255 | | | Vendor Specific – 32 bytes |

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