Freescale Semiconductor
Data Sheet: Technical Data

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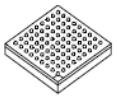
BSC9132

BSC9132 QorIQ Qonverge Multicore Baseband Processor



FC-PBGA–780
23 mm x 23 mm

The following list provides an overview of the feature set:

- Two high-performance 32-bit e500 cores built on Power Architecture® technology:
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache
  - Enhanced hardware and software debug support
  - 800 Mhz/1 GHz/1.2 GHz clock frequency
  - 512-Kbyte L2 cache with ECC; also configurable as SRAM and stashing memory
- Two SC3850 core subsystems; each core connects to the following:
  - 32 Kbyte 8-way level 1 data/instruction cache (L1 Dcache/ICache)
  - 512 Kbyte 8-way level 2 unified instruction/data cache (L2 cache/M2 memory)
  - Memory management unit (MMU)
  - Enhanced programmable interrupt controller (EPIC)
  - Debug and profiling unit (DPU)
  - Two 32-bit quad timers
- 32 Kbytes of shared M3 memory
- Multi Accelerator Platform Engine for Pico Base Station Baseband Processing (MAPLE-B2P)
  - Supports variable sizes in Fourier Transforms, Convolution, Filtering, Turbo, Viterbi, Chiprate, MIMO
  - Consists of accelerators for UMTS chip rate processing, LTE UP/DL channel processing, Matrix Inversion operations, and CRC algorithms
- Two DDR3/DDR3L SDRAM memory controllers support 32-bit with ECC
- Integrated security engine (ULE CAAM)
  - Protocol support includes DES, AES, RNG, CRC, MDE, PKE, SHA, and MD5
- Secure boot capability
- Two enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration, quality of service, and classification capabilities
  - IEEE Std 1588™ support
  - Supports SGMII interfaces
- High-speed interfaces supporting the following multiplexing options:
  - One PCI Express interface with 5G support
  - Four lanes of high-speed serial interfaces (SerDes) to be shared between PCI Express, SGMII, and CPRI
- High-speed USB controller (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface
- Enhanced secure digital (SD/MMC) host controller (eSDHC)
- Integrated Flash controller (IFC), supporting NAND, NOR, and general ASIC
- Two TDM interfaces
- Antenna interface controller (AIC), supporting four industry standard JESD/four custom parallel RF interfaces (three dual and one single port) and a 2-lane CPRI interface
- Universal Subscriber Identity Module (USIM) interface
  - Facilitates communication to SIM cards or Eurochip pre-paid phone cards
- Two enhanced serial peripheral interfaces (eSPI)
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Two DMA controllers
  - 4-channel DMA on Power Architecture side
  - 32 unidirectional channels, providing up to 16 memory-to-memory channels on DSP side
- Two I^2C interfaces
- Two dual UART (DUART) interfaces
- 96 general-purpose I/O signals
- Eight 32-bit timers
- Operating temperature (Ta - T_j) range: 0–105° C

Table of Contents

This figure shows the major functional units.

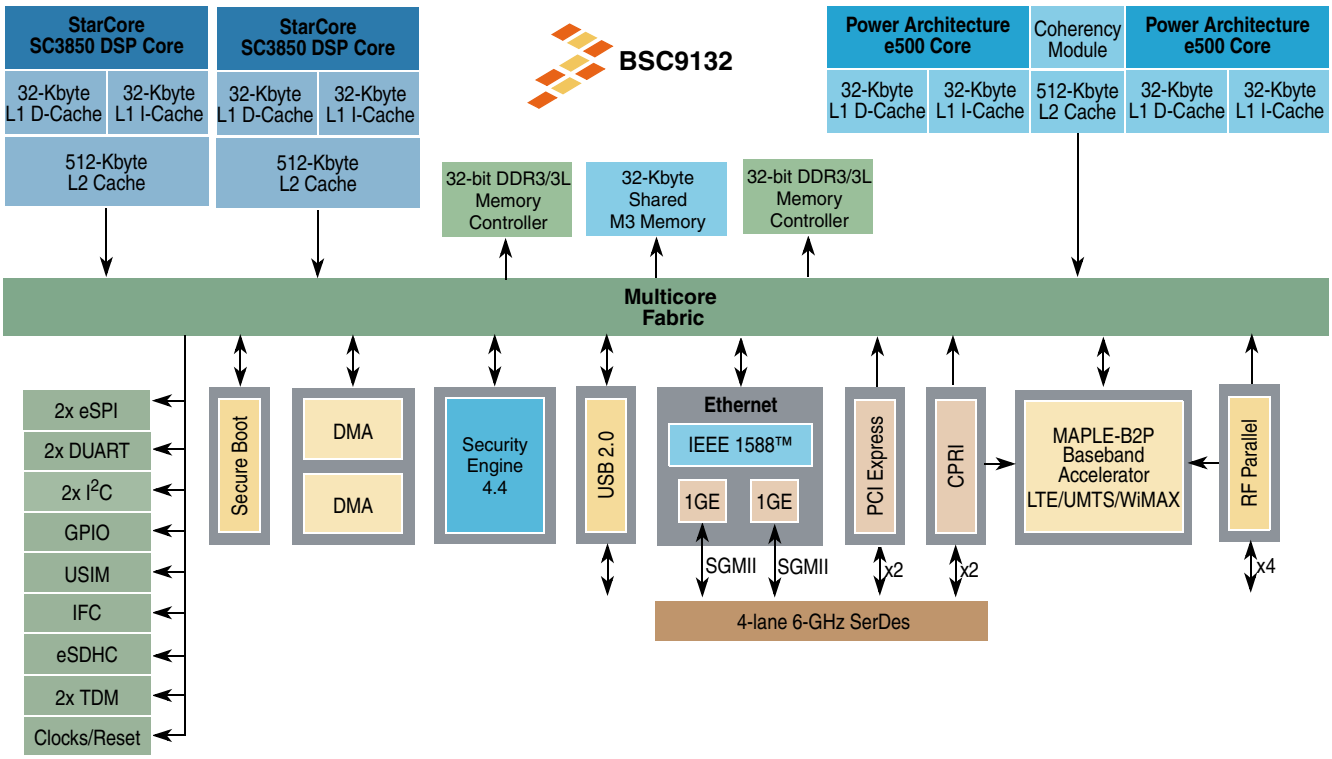


Figure 1. BSC9132 Block Diagram

1 Pin Assignments

This section contains a top-level ball layout diagram followed by four detailed quadrant views and a pinout listing table.

1.1 Ball Layout Diagrams

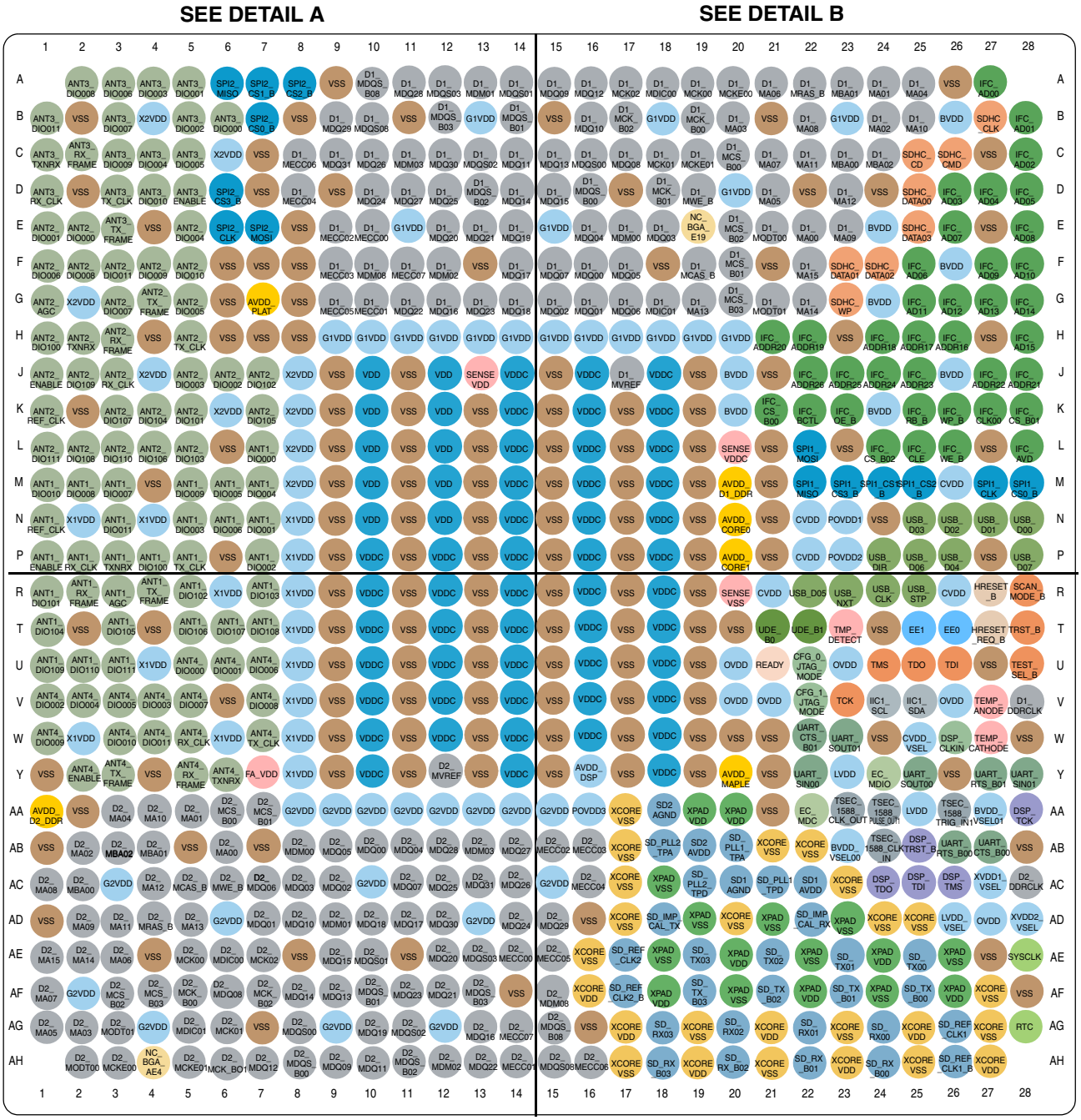


Figure 2. Ball Layout Diagram—Top-Level View

Figure 3 shows detailed view A.

DETAIL A

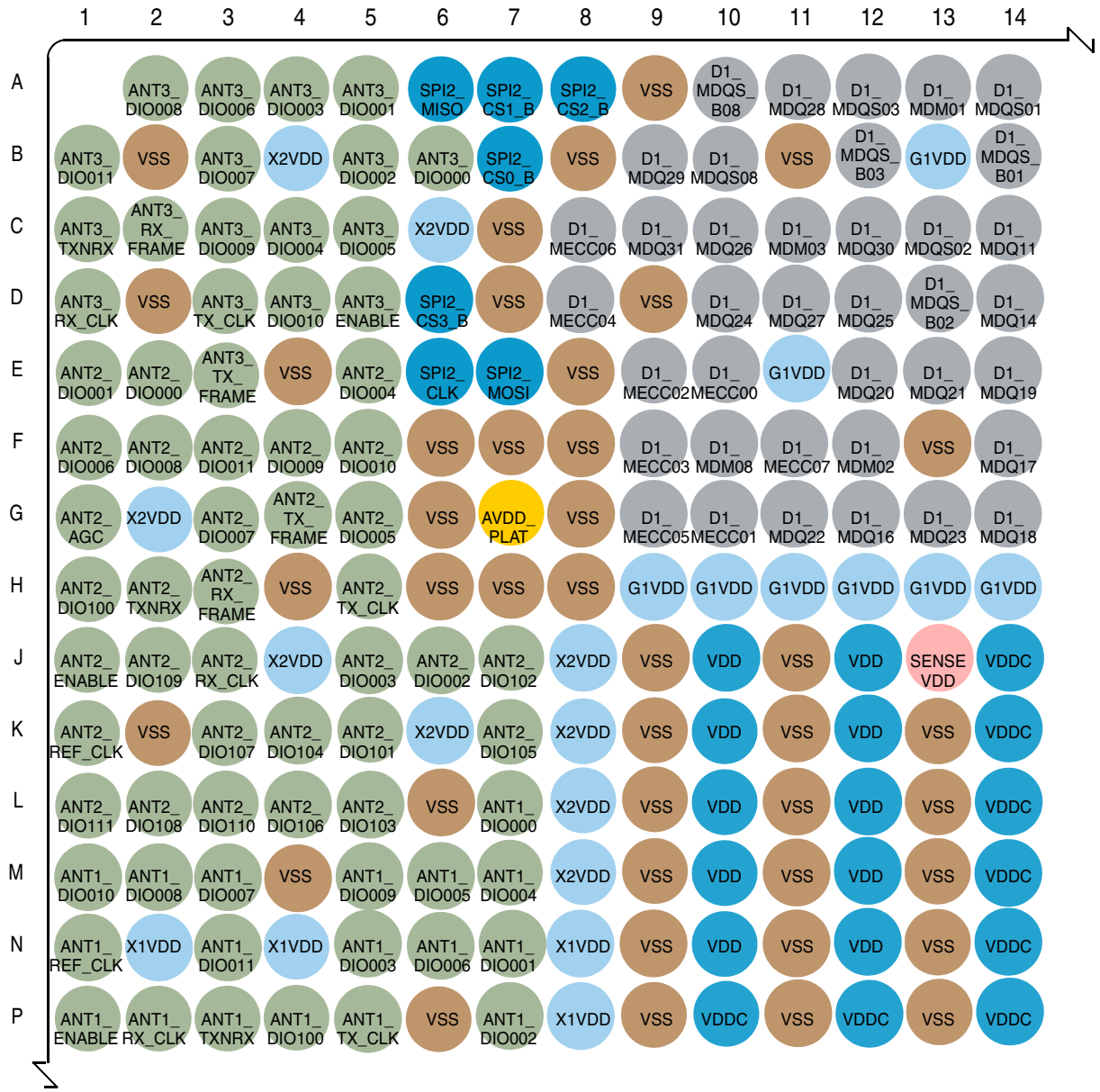


Figure 3. Ball Layout Diagram—Detail A

Figure 4 shows detailed view B.

DETAIL B

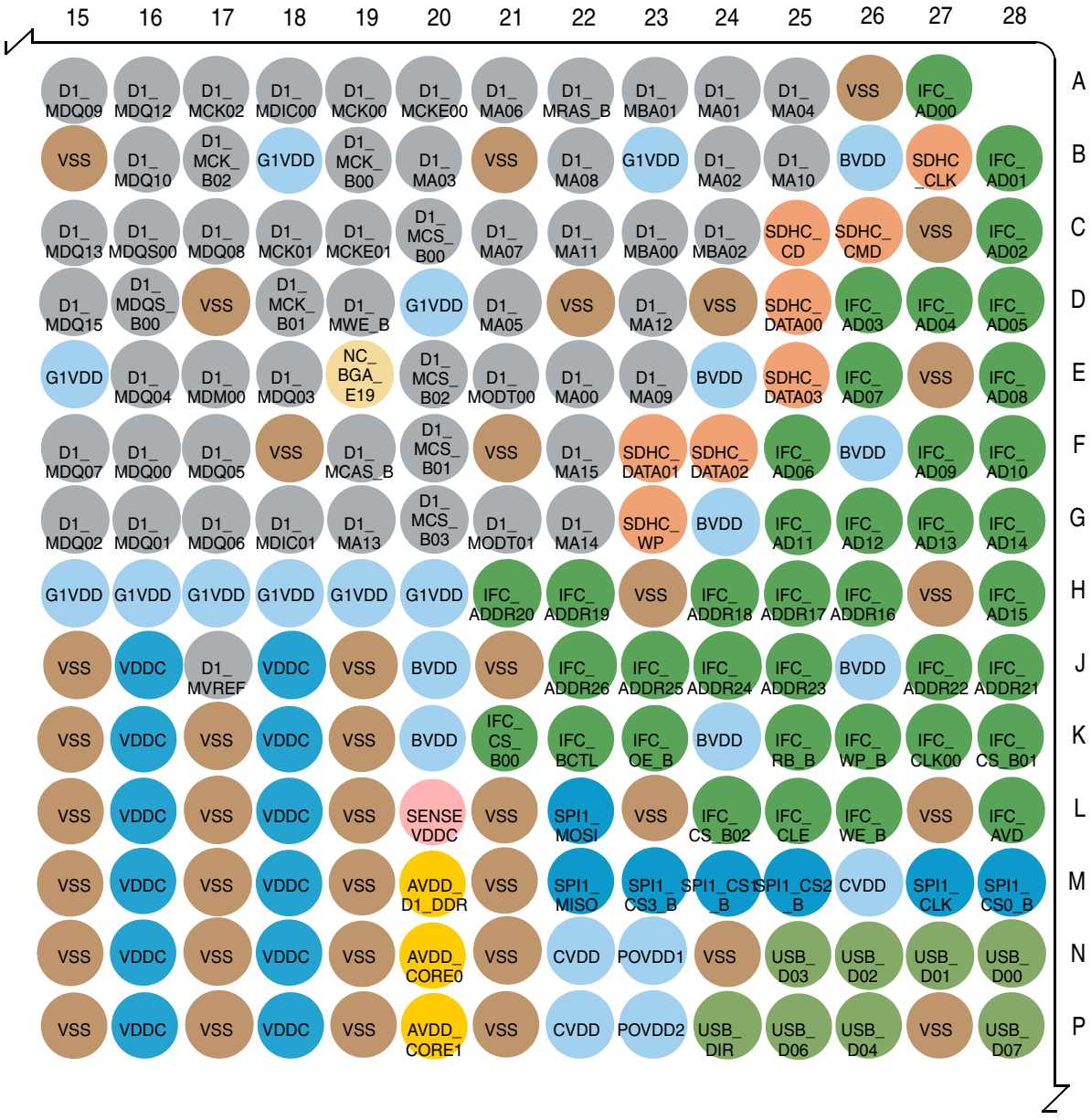


Figure 4. Ball Layout Diagram—Detail B

Figure 5 shows detailed view C.

DETAIL C

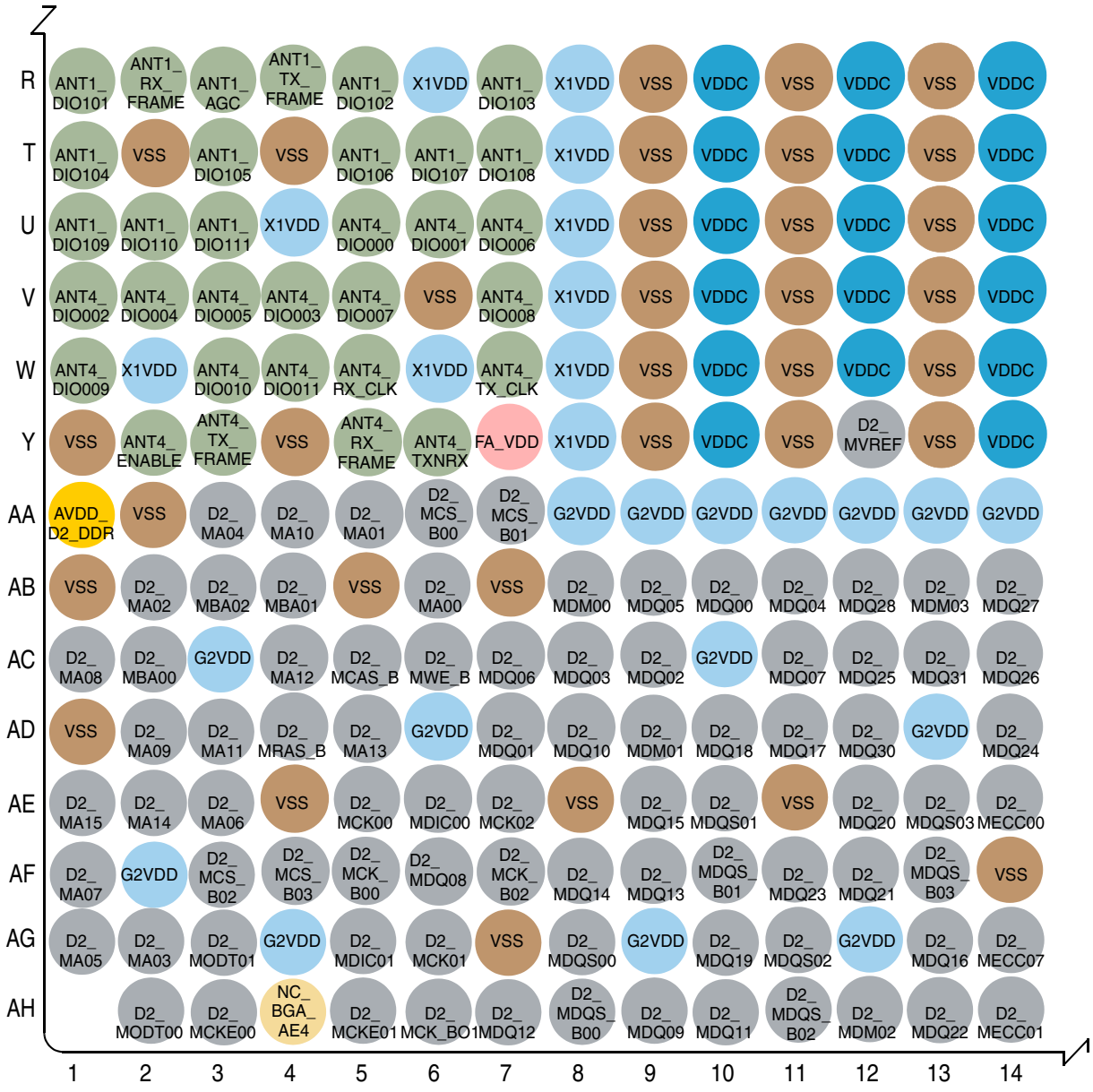


Figure 5. Ball Layout Diagram—Detail C

Figure 6 shows detailed view D.

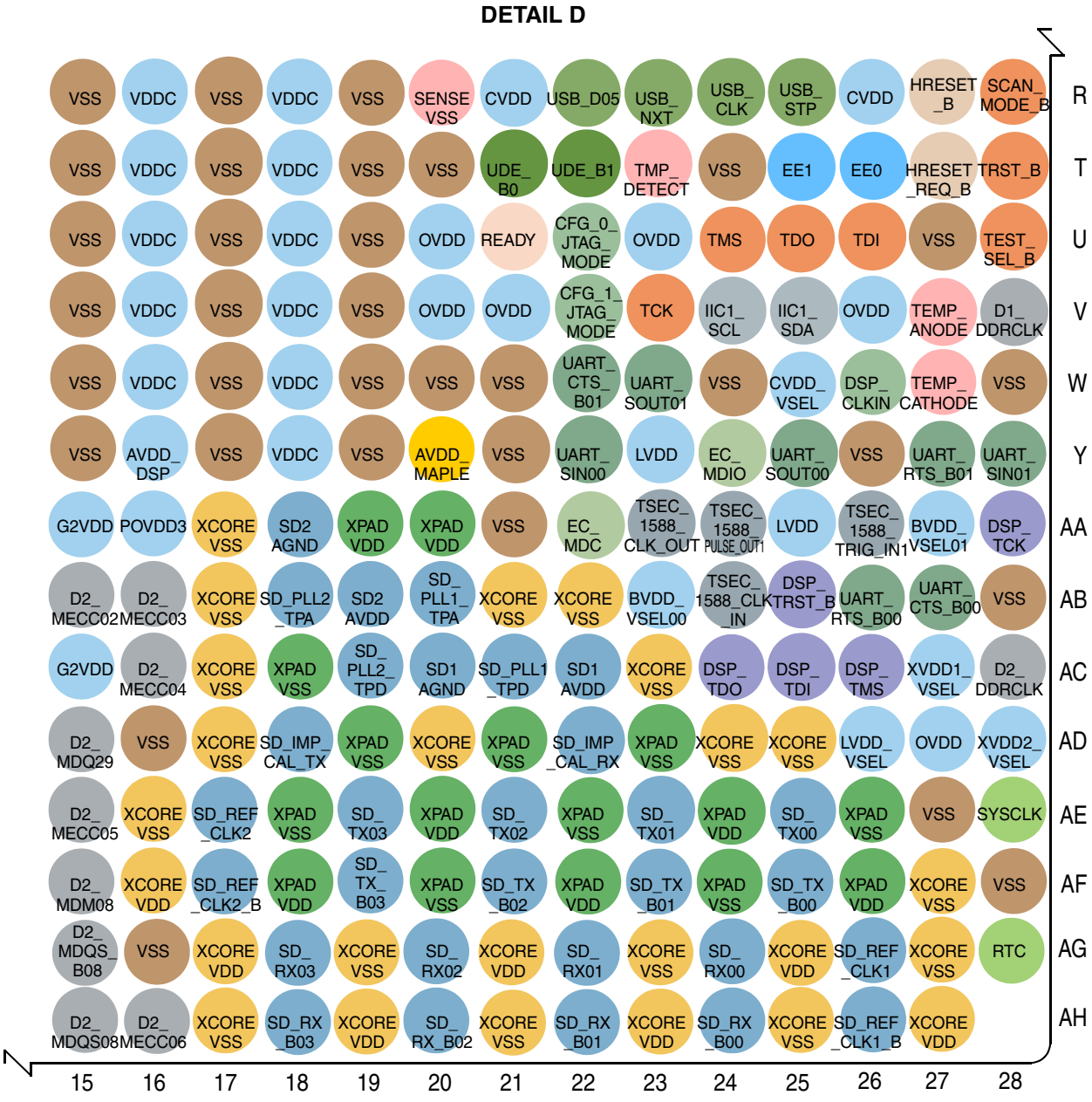


Figure 6. Ball Layout Diagram—Detail D

1.2 Pinout Assignments

This table provides the pinout listing.

Table 1. BSC9132 Pinout Listing

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
DDR 1 (Power Architecture)					
D1_MDQ00	Data	F16	I/O	G1VDD	—
D1_MDQ01	Data	G16	I/O	G1VDD	—
D1_MDQ02	Data	G15	I/O	G1VDD	—
D1_MDQ03	Data	E18	I/O	G1VDD	—
D1_MDQ04	Data	E16	I/O	G1VDD	—
D1_MDQ05	Data	F17	I/O	G1VDD	—
D1_MDQ06	Data	G17	I/O	G1VDD	—
D1_MDQ07	Data	F15	I/O	G1VDD	—
D1_MDQ08	Data	C17	I/O	G1VDD	—
D1_MDQ09	Data	A15	I/O	G1VDD	—
D1_MDQ10	Data	B16	I/O	G1VDD	—
D1_MDQ11	Data	C14	I/O	G1VDD	—
D1_MDQ12	Data	A16	I/O	G1VDD	—
D1_MDQ13	Data	C15	I/O	G1VDD	—
D1_MDQ14	Data	D14	I/O	G1VDD	—
D1_MDQ15	Data	D15	I/O	G1VDD	—
D1_MDQ16	Data	G12	I/O	G1VDD	—
D1_MDQ17	Data	F14	I/O	G1VDD	—
D1_MDQ18	Data	G14	I/O	G1VDD	—
D1_MDQ19	Data	E14	I/O	G1VDD	—
D1_MDQ20	Data	E12	I/O	G1VDD	—
D1_MDQ21	Data	E13	I/O	G1VDD	—
D1_MDQ22	Data	G11	I/O	G1VDD	—
D1_MDQ23	Data	G13	I/O	G1VDD	—
D1_MDQ24	Data	D10	I/O	G1VDD	—
D1_MDQ25	Data	D12	I/O	G1VDD	—
D1_MDQ26	Data	C10	I/O	G1VDD	—
D1_MDQ27	Data	D11	I/O	G1VDD	—
D1_MDQ28	Data	A11	I/O	G1VDD	—
D1_MDQ29	Data	B9	I/O	G1VDD	—
D1_MDQ30	Data	C12	I/O	G1VDD	—
D1_MDQ31	Data	C9	I/O	G1VDD	—
D1_MDM00	Data Mask	E17	O	G1VDD	—
D1_MDM01	Data Mask	A13	O	G1VDD	—
D1_MDM02	Data Mask	F12	O	G1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D1_MDM03	Data Mask	C11	O	G1VDD	—
D1_MDQS00	Data Strobe	C16	I/O	G1VDD	—
D1_MDQS01	Data Strobe	A14	I/O	G1VDD	—
D1_MDQS02	Data Strobe	C13	I/O	G1VDD	—
D1_MDQS03	Data Strobe	A12	I/O	G1VDD	—
D1_MDQS_B00	Data Strobe	D16	I/O	G1VDD	—
D1_MDQS_B01	Data Strobe	B14	I/O	G1VDD	—
D1_MDQS_B02	Data Strobe	D13	I/O	G1VDD	—
D1_MDQS_B03	Data Strobe	B12	I/O	G1VDD	—
D1_MBA00	Bank Select	C23	O	G1VDD	—
D1_MBA01	Bank Select	A23	O	G1VDD	—
D1_MBA02	Bank Select	C24	O	G1VDD	—
D1_MA00	Address	E22	O	G1VDD	—
D1_MA01	Address	A24	O	G1VDD	—
D1_MA02	Address	B24	O	G1VDD	—
D1_MA03	Address	B20	O	G1VDD	—
D1_MA04	Address	A25	O	G1VDD	—
D1_MA05	Address	D21	O	G1VDD	—
D1_MA06	Address	A21	O	G1VDD	—
D1_MA07	Address	C21	O	G1VDD	—
D1_MA08	Address	B22	O	G1VDD	—
D1_MA09	Address	E23	O	G1VDD	—
D1_MA10	Address	B25	O	G1VDD	—
D1_MA11	Address	C22	O	G1VDD	—
D1_MA12	Address	D23	O	G1VDD	—
D1_MA13	Address	G19	O	G1VDD	—
D1_MA14	Address	G22	O	G1VDD	—
D1_MA15	Address	F22	O	G1VDD	—
D1_MWE_B	Write Enable	D19	O	G1VDD	—
D1_MRAS_B	Row Address Strobe	A22	O	G1VDD	—
D1_MCAS_B	Column Address Strobe	F19	O	G1VDD	—
D1_MCS_B00	Chip Select	C20	O	G1VDD	—
D1_MCS_B01	Chip Select	F20	O	G1VDD	—
D1_MCS_B02	Chip Select	E20	O	G1VDD	—
D1_MCS_B03	Chip Select	G20	O	G1VDD	—
D1_MCKE00	Clock Enable	A20	O	G1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D1_MCKE01	Clock Enable	C19	O	G1VDD	—
D1_MCK00	Clock	A19	O	G1VDD	—
D1_MCK01	Clock	C18	O	G1VDD	—
D1_MCK02	Clock	A17	O	G1VDD	—
D1_MCK_B00	Clock Complements	B19	O	G1VDD	—
D1_MCK_B01	Clock Complements	D18	O	G1VDD	—
D1_MCK_B02	Clock Complements	B17	O	G1VDD	—
D1_MODT00	On Die Termination	E21	O	G1VDD	—
D1_MODT01	On Die Termination	G21	O	G1VDD	—
D1_MDIC00	Driver Impedence Calibration	A18	I/O	VSS	—
D1_MDIC01	Driver Impedence Calibration	G18	I/O	G1VDD	—
D1_MECC00	ECC data	E10	I/O	G1VDD	—
D1_MECC01	ECC data	G10	I/O	G1VDD	—
D1_MECC02	ECC data	E9	I/O	G1VDD	—
D1_MECC03	ECC data	F9	I/O	G1VDD	—
D1_MECC04	ECC data	D8	I/O	G1VDD	—
D1_MECC05	ECC data	G9	I/O	G1VDD	—
D1_MECC06	ECC data	C8	I/O	G1VDD	—
D1_MECC07	ECC data	F11	I/O	G1VDD	—
D1_MDQS08	ECC Strobe	B10	I/O	G1VDD	—
D1_MDQS_B08	ECC Strobe	A10	I/O	G1VDD	—
D1_MDM08	ECC Data Mask	F10	O	G1VDD	—
DDR 2 (DSP)					
D2_MDQ00	Data	AB10	I/O	G2VDD	—
D2_MDQ01	Data	AD7	I/O	G2VDD	—
D2_MDQ02	Data	AC9	I/O	G2VDD	—
D2_MDQ03	Data	AC8	I/O	G2VDD	—
D2_MDQ04	Data	AB11	I/O	G2VDD	—
D2_MDQ05	Data	AB9	I/O	G2VDD	—
D2_MDQ06	Data	AC7	I/O	G2VDD	—
D2_MDQ07	Data	AC11	I/O	G2VDD	—
D2_MDQ08	Data	AF6	I/O	G2VDD	—
D2_MDQ09	Data	AH9	I/O	G2VDD	—
D2_MDQ10	Data	AD8	I/O	G2VDD	—
D2_MDQ11	Data	AH10	I/O	G2VDD	—
D2_MDQ12	Data	AH7	I/O	G2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D2_MDQ13	Data	AF9	I/O	G2VDD	—
D2_MDQ14	Data	AF8	I/O	G2VDD	—
D2_MDQ15	Data	AE9	I/O	G2VDD	—
D2_MDQ16	Data	AG13	I/O	G2VDD	—
D2_MDQ17	Data	AD11	I/O	G2VDD	—
D2_MDQ18	Data	AD10	I/O	G2VDD	—
D2_MDQ19	Data	AG10	I/O	G2VDD	—
D2_MDQ20	Data	AE12	I/O	G2VDD	—
D2_MDQ21	Data	AF12	I/O	G2VDD	—
D2_MDQ22	Data	AH13	I/O	G2VDD	—
D2_MDQ23	Data	AF11	I/O	G2VDD	—
D2_MDQ24	Data	AD14	I/O	G2VDD	—
D2_MDQ25	Data	AC12	I/O	G2VDD	—
D2_MDQ26	Data	AC14	I/O	G2VDD	—
D2_MDQ27	Data	AB14	I/O	G2VDD	—
D2_MDQ28	Data	AB12	I/O	G2VDD	—
D2_MDQ29	Data	AD15	I/O	G2VDD	—
D2_MDQ30	Data	AD12	I/O	G2VDD	—
D2_MDQ31	Data	AC13	I/O	G2VDD	—
D2_MDM00	Data Mask	AB8	O	G2VDD	—
D2_MDM01	Data Mask	AD9	O	G2VDD	—
D2_MDM02	Data Mask	AH12	O	G2VDD	—
D2_MDM03	Data Mask	AB13	O	G2VDD	—
D2_MDQS00	Data Strobe	AG8	I/O	G2VDD	—
D2_MDQS01	Data Strobe	AE10	I/O	G2VDD	—
D2_MDQS02	Data Strobe	AG11	I/O	G2VDD	—
D2_MDQS03	Data Strobe	AE13	I/O	G2VDD	—
D2_MDQS_B00	Data Strobe	AH8	I/O	G2VDD	—
D2_MDQS_B01	Data Strobe	AF10	I/O	G2VDD	—
D2_MDQS_B02	Data Strobe	AH11	I/O	G2VDD	—
D2_MDQS_B03	Data Strobe	AF13	I/O	G2VDD	—
D2_MBA00	Bank Select	AC2	O	G2VDD	—
D2_MBA01	Bank Select	AB4	O	G2VDD	—
D2_MBA02	Bank Select	AB3	O	G2VDD	—
D2_MA00	Address	AB6	O	G2VDD	—
D2_MA01	Address	AA5	O	G2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D2_MA02	Address	AB2	O	G2VDD	—
D2_MA03	Address	AG2	O	G2VDD	—
D2_MA04	Address	AA3	O	G2VDD	—
D2_MA05	Address	AG1	O	G2VDD	—
D2_MA06	Address	AE3	O	G2VDD	—
D2_MA07	Address	AF1	O	G2VDD	—
D2_MA08	Address	AC1	O	G2VDD	—
D2_MA09	Address	AD2	O	G2VDD	—
D2_MA10	Address	AA4	O	G2VDD	—
D2_MA11	Address	AD3	O	G2VDD	—
D2_MA12	Address	AC4	O	G2VDD	—
D2_MA13	Address	AD5	O	G2VDD	—
D2_MA14	Address	AE2	O	G2VDD	—
D2_MA15	Address	AE1	O	G2VDD	—
D2_MWE_B	Write Enable	AC6	O	G2VDD	—
D2_MRAS_B	Row Address Strobe	AD4	O	G2VDD	—
D2_MCAS_B	Column Address Strobe	AC5	O	G2VDD	—
D2_MCS_B00	Chip Select	AA6	O	G2VDD	—
D2_MCS_B01	Chip Select	AA7	O	G2VDD	—
D2_MCS_B02	Chip Select	AF3	O	G2VDD	—
D2_MCS_B03	Chip Select	AF4	O	G2VDD	—
D2_MCKE00	Clock Enable	AH3	O	G2VDD	—
D2_MCKE01	Clock Enable	AH5	O	G2VDD	—
D2_MCK00	Clock	AE5	O	G2VDD	—
D2_MCK01	Clock	AG6	O	G2VDD	—
D2_MCK02	Clock	AE7	O	G2VDD	—
D2_MCK_B00	Clock Complements	AF5	O	G2VDD	—
D2_MCK_B01	Clock Complements	AH6	O	G2VDD	—
D2_MCK_B02	Clock Complements	AF7	O	G2VDD	—
D2_MODT00	On Die Termination	AH2	O	G2VDD	—
D2_MODT01	On Die Termination	AG3	O	G2VDD	—
D2_MDIC00	Driver Impedence Calibration	AE6	I/O	VSS	—
D2_MDIC01	Driver Impedence Calibration	AG5	I/O	G2VDD	—
D2_MECC00	ECC data	AE14	I/O	G2VDD	—
D2_MECC01	ECC data	AH14	I/O	G2VDD	—
D2_MECC02	ECC data	AB15	I/O	G2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D2_MECC03	ECC data	AB16	I/O	G2VDD	—
D2_MECC04	ECC data	AC16	I/O	G2VDD	—
D2_MECC05	ECC data	AE15	I/O	G2VDD	—
D2_MECC06	ECC data	AH16	I/O	G2VDD	—
D2_MECC07	ECC data	AG14	I/O	G2VDD	—
D2_MDQS08	ECC Strobe	AH15	I/O	G2VDD	—
D2_MDQS_B08	ECC Strobe	AG15	I/O	G2VDD	—
D2_MDM08	ECC Data Mask	AF15	O	G2VDD	—
Ethernet Management					
EC_MDC	Management Data Clock	AA22	O	LVDD	2
EC_MDIO	Management Data In/Out	Y24	I/O	LVDD	2
eTSEC 1588					
TSEC_1588_CLK_IN	1588 Clock In	AB24	I	LVDD	—
TSEC_1588_CLK_OUT/ CLK_OUT	1588 Clock Out	AA23	O	LVDD	2
TSEC_1588_TRIG_IN1	1588 Trigger In	AA26	I	LVDD	—
TSEC_1588_PULSE_OUT1/ PPS_OUT	1588 Pulse Out	AA24	O	LVDD	2
IFC/GPIO/Interrupts					
IFC_AD00	IFC Muxed Address,Data	A27	I/O	BVDD	—
IFC_AD01	IFC Muxed Address,Data	B28	I/O	BVDD	—
IFC_AD02	IFC Muxed Address,Data	C28	I/O	BVDD	—
IFC_AD03	IFC Muxed Address,Data	D26	I/O	BVDD	—
IFC_AD04	IFC Muxed Address,Data	D27	I/O	BVDD	—
IFC_AD05	IFC Muxed Address,Data	D28	I/O	BVDD	—
IFC_AD06	IFC Muxed Address,Data	F25	I/O	BVDD	2
IFC_AD07	IFC Muxed Address,Data	E26	I/O	BVDD	—
IFC_AD08/ GPIO34	IFC Muxed Address,Data	E28	I/O	BVDD	—
IFC_AD09/ GPIO35	IFC Muxed Address,Data	F27	I/O	BVDD	—
IFC_AD10/ GPIO36	IFC Muxed Address,Data	F28	I/O	BVDD	—
IFC_AD11/ GPIO37/ IRQ08	IFC Muxed Address,Data	G25	I/O	BVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_AD12/ GPIO38/ IRQ09	IFC Muxed Address,Data	G26	I/O	BVDD	—
IFC_AD13/ GPIO39/ IRQ07	IFC Muxed Address,Data	G27	I/O	BVDD	—
IFC_AD14/ GPIO40/ IRQ06	IFC Muxed Address,Data	G28	I/O	BVDD	—
IFC_AD15/ GPIO41/ TIMER02	IFC Muxed Address,Data	H28	I/O	BVDD	—
IFC_ADDR16/ GPO08	IFC Address/GPO	H26	O	BVDD	2
IFC_ADDR17/ GPO09	IFC Address/GPO	H25	O	BVDD	2
IFC_ADDR18/ GPO10	IFC Address/GPO	H24	O	BVDD	2
IFC_ADDR19/ GPO11	IFC Address/GPO	H22	O	BVDD	2
IFC_ADDR20/ GPO12	IFC Address/GPO	H21	O	BVDD	2
IFC_ADDR21/ GPO13	IFC Address/GPO	J28	O	BVDD	2
IFC_ADDR22/ GPO14	IFC Address/GPO	J27	O	BVDD	—
IFC_ADDR23/ GPO15	IFC Address/GPO	J25	O	BVDD	2
IFC_ADDR24/ GPO16	IFC Address/GPO	J24	O	BVDD	2
IFC_ADDR25/ GPO17	IFC Address/GPO	J23	O	BVDD	2
IFC_ADDR26/ GPO18	IFC Address/GPO	J22	O	BVDD	2
IFC_AVD/ GPO54	IFC Address Valid	L28	O	BVDD	2
IFC_CS_B00/ GPO55	IFC Chip Select	K21	O	BVDD	—
IFC_CS_B01/ GPO64	IFC Chip Select/GPO	K28	O	BVDD	—
IFC_CS_B02/ GPO65	IFC Chip Select/GPO	L24	O	BVDD	—
IFC_WE_B/ GPO52	IFC Write Enable/GPCM Write Byte Select0/ Generic ASIC i/f Start of Frame	L26	O	BVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_CLE/ GPO48	NAND Command Latch Enable/GPCM Write Byte Select1	L25	O	BVDD	—
IFC_OE_B/ GPO49	NOR Output Enable/NAND Read Enable/ GPCM Output Enable/Generic ASIC Interface Read-Write Indicator	K23	I/O	BVDD	2
IFC_WP_B/ GPO66	IFC Write Protect	K26	O	BVDD	—
IFC_RB_B/ GPO50	IFC Read Busy/GPCM External Transreciver/ Generic ASIC i/f Ready Indicator	K25	I/O	BVDD	—
IFC_BCTL/ GPO67	Data Buffer Control/GPO	K22	O	BVDD	—
IFC_CLK00/ GPO68	IFC Clock/GPO	K27	O	BVDD	—
eSDHC/USIM					
SDHC_CLK/ SIM_CLK/ GPO52	SDHC Clock/SIM Clock	B27	O	BVDD	—
SDHC_CMD/ SIM_RST_B/ GPIO48	SDHC Command/SIM Reset	C26	I/O	BVDD	—
SDHC_DATA00/ SIM_TRXD/ GPIO49	SDHC Data/SIM TX RX Data	D25	I/O	BVDD	—
SDHC_DATA01/ SIM_SVEN/ GPIO50	SDHC Data/SIM Enable	F23	I/O	BVDD	—
SDHC_DATA02/ SIM_PD/ GPIO51	SDHC Data	F24	I/O	BVDD	—
SDHC_DATA03/ DMA_DDONE_B00/ CKSTP1_IN_B/ GPIO77	SDHC Data	E25	I/O	BVDD	—
SDHC_WP/ DMA_DREQ_B00/ CKSTP0_IN_B/ GPIO78	SDHC Write Protect	G23	I/O	BVDD	—
SDHC_CD/ DMA_DACK_B00/ MCP1_B/ GPIO79/ IRQ10	SDHC Card Detect	C25	I/O	BVDD	—
USB/DUART/Interrupts					

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
USB_CLK/ UART_SIN02/ GPIO69/ IRQ11/ TIMER03	ULPI Clock	R24	I/O	CVDD	—
USB_D07/ UART_SOUT02/ GPIO70	ULPI Data	P28	I/O	CVDD	—
USB_D06/ UART_CTS_B02/ GPIO62	ULPI Data	P25	I/O	CVDD	—
USB_D05/ UART_RTS_B02/ GPIO63	ULPI Data	R22	I/O	CVDD	—
USB_D04/ GPIO00/ IRQ00	ULPI Data	P26	I/O	CVDD	—
USB_D03/ GPIO01/ IRQ01	ULPI Data	N25	I/O	CVDD	—
USB_D02/ IIC2_SDA/ GPIO71	ULPI Data	N26	I/O	CVDD	12
USB_D01/ IIC2_SCL/ GPIO72	ULPI Data	N27	I/O	CVDD	—
USB_D00/ IRQ02/ GPIO53	ULPI Data	N28	I/O	CVDD	—
USB_STP/ IRQ_OUT_B/ GPO73	ULPI Stop	R25	O	CVDD	—
USB_DIR/ GPIO02/ TIMER01/ MCP0_B	ULPI Data Direction	P24	I/O	CVDD	—
USB_NXT/ GPIO03/ IRQ03/ TRIG_IN	ULPI Next Data Throttle Control	R23	I/O	CVDD	—
SPI1/DUART/USIM/GPO					
SPI1_MOSI/ UART_SIN03/ SIM_SVEN/ GPIO54	SPI Master Out Slave In Data	L22	I/O	CVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SPI1_MISO/ UART_CTS_B03/ SIM_RST_B/ GPIO55	SPI Master In Slave Out Data	M22	I/O	CVDD	—
SPI1_CLK/ SIM_CLK	SPI Serial Clock	M27	O	CVDD	—
SPI1_CS0_B/ UART_RTS_B03/ SIM_TRXD	SPI Slave Select	M28	I/O	CVDD	—
SPI1_CS1_B/ UART_SOUT03/ GPO74	SPI Slave Select	M24	O	CVDD	—
SPI1_CS2_B/ CKSTP0_OUT_B/ GPO75	SPI Slave Select	M25	O	CVDD	—
SPI1_CS3_B/ CKSTP1_OUT_B/ GPO76	SPI Slave Select	M23	O	CVDD	—
DUART/Interrupts					
UART_SOUT00	UART0 Transmit Data	Y25	O	OVDD	2
UART_SIN00	UART0 Receive Data	Y22	I	OVDD	—
UART_CTS_B00/ SIM_PD/ TIMER04/ GPIO42/ IRQ04	UART0 Clear to Send	AB27	I/O	OVDD	—
UART_RTS_B00/ PPS_LED/ GPO43	UART0 Ready to Send	AB26	O	OVDD	2
UART_SOUT01/ GPO56	UART1 Transmit Data	W23	O	OVDD	2
UART_SIN01/ GPIO57	UART1 Receive Data	Y28	I/O	OVDD	—
UART_CTS_B01/ SYS_DMA_REQ/ SRESET_B/ GPIO44/ IRQ05	UART1 Clear to Send	W22	I/O	OVDD	—
UART_RTS_B01/ SYS_DMA_DONE/ GPO45/ ANT4_AGC	UART1 Ready to Send	Y27	O	OVDD	2
I^2C1					
IIC1_SDA/ GPIO46	Serial Data	V25	I/O	OVDD	5

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IIC1_SCL/ GPIO47	Serial Clock	V24	I/O	OVDD	5
System Control/Power Management					
HRESET_B	Hard Reset	R27	I	OVDD	—
HRESET_REQ_B	Hard Reset Request Out	T27	O	OVDD	2, 4
READY/ ASLEEP/ READY_P1	Ready/Trigger Out/Asleep	U21	O	OVDD	2
UDE_B0	Unconditional Debug Event	T21	I	OVDD	—
UDE_B1	Unconditional Debug Event	T22	I	OVDD	—
EE0	DSP Debug Request	T26	I	OVDD	—
EE1	DSP Debug Acknowledge	T25	O	OVDD	2
TMP_DETECT	Tamper Detect	T23	I	OVDD	—
Clocking					
SYSCLK	System Clock	AE28	I	OVDD	—
D1_DDRCLK	DDR PLL Reference Clock	V28	I	OVDD	—
D2_DDRCLK	DDR PLL Reference Clock	AC28	I	OVDD	—
RTC	Real Time Clock	AG28	I	OVDD	—
DSP_CLKIN	DSP PLL Reference Clock	W26	I	OVDD	—
I/O Voltage Select					
BVDD_VSEL00	BVDD Voltage Selection	AB23	I	OVDD	—
BVDD_VSEL01	BVDD Voltage Selection	AA27	I	OVDD	—
CVDD_VSEL	CVDD Voltage Selection	W25	I	OVDD	—
LVDD_VSEL	LVDD Voltage Selection	AD26	I	OVDD	—
XVDD1_VSEL	XVDD 1 Voltage Selection	AC27	I	OVDD	—
XVDD2_VSEL	XVDD 2 Voltage Selection	AD28	I	OVDD	—
Test					
SCAN_MODE_B	Scan Mode	R28	I	OVDD	1
CFG_0_JTAG_MODE	JTAG mode selection 0	U22	I	OVDD	10
CFG_1_JTAG_MODE	JTAG mode selection 1	V22	I	OVDD	10
TEST_SEL_B	Test Select	U28	I	OVDD	11
JTAG (Power Architecture)					
TCK	Test Clock	V23	I	OVDD	
TDI	Test Data In	U26	I	OVDD	3
TDO	Test Data Out	U25	O	OVDD	—
TMS	Test Mode Select	U24	I	OVDD	3

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
TRST_B	Test Reset	T28	I	OVDD	3
JTAG (DSP)					
DSP_TCK	Test Clock	AA28	I	OVDD	—
DSP_TDI	Test Data In	AC25	I	OVDD	3
DSP_TDO	Test Data Out	AC24	O	OVDD	—
DSP_TMS	Test Mode Select	AC26	I	OVDD	3
DSP_TRST_B	Test Reset	AB25	I	OVDD	3
SerDes					
SD_TX03	Tx Data out	AE19	O	XPADVDD	—
SD_TX02	Tx Data out	AE21	O	XPADVDD	—
SD_TX01	Tx Data out	AE23	O	XPADVDD	—
SD_TX00	Tx Data out	AE25	O	XPADVDD	—
SD_TX_B03	Tx Data out, inverted	AF19	O	XPADVDD	—
SD_TX_B02	Tx Data out, inverted	AF21	O	XPADVDD	—
SD_TX_B01	Tx Data out, inverted	AF23	O	XPADVDD	—
SD_TX_B00	Tx Data out, inverted	AF25	O	XPADVDD	—
SD_RX03	Rx Data in	AG18	I	XCOREVDD	—
SD_RX02	Rx Data in	AG20	I	XCOREVDD	—
SD_RX01	Rx Data in	AG22	I	XCOREVDD	—
SD_RX00	Rx Data in	AG24	I	XCOREVDD	—
SD_RX_B03	Rx Data in, Inverted	AH18	I	XCOREVDD	—
SD_RX_B02	Rx Data in, Inverted	AH20	I	XCOREVDD	—
SD_RX_B01	Rx Data in, Inverted	AH22	I	XCOREVDD	—
SD_RX_B00	Rx Data in, Inverted	AH24	I	XCOREVDD	—
SD_REF_CLK1	Reference clock	AG26	I	XCOREVDD	—
SD_REF_CLK1_B	Reference clock	AH26	I	XCOREVDD	—
SD_REF_CLK2	Reference clock	AE17	I	XCOREVDD	—
SD_REF_CLK2_B	Reference clock	AF17	I	XCOREVDD	—
SD_IMP_CAL_TX	Transmitter impedance calibration	AD18	I	XPADVDD	6
SD_IMP_CAL_RX	Receiver impedance calibration	AD22	I	XCOREVDD	6
SD_PLL1_TPA	PLL test point analog	AB20	O	SD1AVDD	—
SD_PLL1_TPD	PLL test point digital	AC21	O	XPADVDD	—
SD_PLL2_TPA	PLL test point analog	AB18	O	SD2AVDD	—
SD_PLL2_TPD	PLL test point digital	AC19	O	XPADVDD	—
RF Interface 1/GPIO					
ANT1_REF_CLK	Parallel Interface Reference Clock	N1	I	X1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_AGC/ GPO58	AGC Control	R3	O	X1VDD	2
ANT1_TX_CLK/ TSEC_1588_ALARM_OUT2	Transmit Clock	P5	O	X1VDD	—
ANT1_RX_CLK/ TSEC_1588_TRIG_IN2/ GPIO95	Receive Clock	P2	I/O	X1VDD	—
ANT1_TXNRX/ TSEC_1588_PULSE_OUT2/ GPO19	TX_RX Control	P3	O	X1VDD	—
ANT1_ENABLE/ TSEC_1588_ALARM_OUT1	Antenna Enable	P1	O	X1VDD	—
ANT1_TX_FRAME/ GPO20	Transmit Frame	R4	O	X1VDD	4,13
ANT1_RX_FRAME/ GPIO80	Receive Frame	R2	I/O	X1VDD	—
ANT1_DIO000	Data	L7	I/O	X1VDD	2
ANT1_DIO001	Data	N7	I/O	X1VDD	2, 4
ANT1_DIO002	Data	P7	I/O	X1VDD	2
ANT1_DIO003	Data	N5	I/O	X1VDD	2
ANT1_DIO004	Data	M7	I/O	X1VDD	4,13
ANT1_DIO005	Data	M6	I/O	X1VDD	4,13
ANT1_DIO006	Data	N6	I/O	X1VDD	2
ANT1_DIO007	Data	M3	I/O	X1VDD	2
ANT1_DIO008	Data	M2	I/O	X1VDD	2
ANT1_DIO009	Data	M5	I/O	X1VDD	2
ANT1_DIO010	Data	M1	I/O	X1VDD	2
ANT1_DIO011	Data	N3	I/O	X1VDD	2
ANT1_DIO100/ GPIO81	Data	P4	I/O	X1VDD	—
ANT1_DIO101/ GPIO82	Data	R1	I/O	X1VDD	—
ANT1_DIO102/ GPIO83	Data	R5	I/O	X1VDD	—
ANT1_DIO103/ GPIO84	Data	R7	I/O	X1VDD	—
ANT1_DIO104/ GPIO85	Data	T1	I/O	X1VDD	—
ANT1_DIO105/ GPIO86	Data	T3	I/O	X1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_DIO106/ GPIO87/ IRQ10	Data	T5	I/O	X1VDD	—
ANT1_DIO107/ GPIO88/ IRQ11	Data	T6	I/O	X1VDD	—
ANT1_DIO108/ GPIO21/ IRQ08	Data	T7	I/O	X1VDD	—
ANT1_DIO109/ GPIO22/ IRQ09	Data	U1	I/O	X1VDD	—
ANT1_DIO110/ TIMER06/ GPIO23	Data	U2	I/O	X1VDD	—
ANT1_DIO111/ TIMER07/ GPIO24	Data	U3	I/O	X1VDD	—
RF Interface 2/USB/DMA/TDM1/Interrupts/GPIO					
ANT2_REF_CLK/ ANT3_AGC	Parallel Interface Reference Clock	K1	I/O	X2VDD	—
ANT2_AGC/ GPO89	AGC Control	G1	O	X2VDD	2
ANT2_TX_CLK/ GPO90	Transmit Clock	H5	O	X2VDD	—
ANT2_RX_CLK/ GPIO91	Receive Clock	J3	I/O	X2VDD	—
ANT2_TXNRX/ DMA_DACK_B00	TX_RX Control	H2	O	X2VDD	—
ANT2_ENABLE/ USB_STP	Antenna Enable	J1	O	X2VDD	—
ANT2_TX_FRAME/ DMA_DDONE_B00	Transmit Frame	G4	O	X2VDD	4,13
ANT2_RX_FRAME/ DMA_DREQ_B00	Receive Frame	H3	I	X2VDD	—
ANT2_DIO000/ USB_D00/ GPIO25	Data	E2	I/O	X2VDD	—
ANT2_DIO001/ USB_D01/ GPIO26	Data	E1	I/O	X2VDD	—
ANT2_DIO002/ USB_D02/ GPIO27	Data	J6	I/O	X2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO003/ USB_D03/ GPIO28	Data	J5	I/O	X2VDD	—
ANT2_DIO004/ USB_D04/ GPIO29	Data	E5	I/O	X2VDD	—
ANT2_DIO005/ USB_D05/ GPIO30	Data	G5	I/O	X2VDD	—
ANT2_DIO006/ USB_D06/ GPIO31	Data	F1	I/O	X2VDD	—
ANT2_DIO007/ USB_D07/ GPIO32	Data	G3	I/O	X2VDD	—
ANT2_DIO008/ USB_DIR/ GPIO33	Data	F2	I/O	X2VDD	—
ANT2_DIO009/ USB_CLK/ GPIO59	Data	F4	I/O	X2VDD	—
ANT2_DIO010/ USB_NXT/ GPIO60	Data	F5	I/O	X2VDD	—
ANT2_DIO011/ GPIO61	Data	F3	I/O	X2VDD	—
ANT2_DIO100/ TDM1_TCK	Data	H1	I/O	X2VDD	—
ANT2_DIO101/ TDM1_TFS	Data	K5	I/O	X2VDD	—
ANT2_DIO102/ TDM1_RXD	Data	J7	I/O	X2VDD	—
ANT2_DIO103/ TDM1_TXD	Data	L5	I/O	X2VDD	—
ANT2_DIO104/ TDM1_RCK/ GPIO92	Data	K4	I/O	X2VDD	—
ANT2_DIO105/ TDM1_RFS/ TIMER08	Data	K7	I/O	X2VDD	—
ANT2_DIO106/ IRQ04	Data	L4	I/O	X2VDD	—
ANT2_DIO107/ IRQ05	Data	K3	I/O	X2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO108/ IRQ06	Data	L2	I/O	X2VDD	—
ANT2_DIO109/ IRQ07	Data	J2	I/O	X2VDD	—
ANT2_DIO110	Data	L3	I/O	X2VDD	—
ANT2_DIO111	Data	L1	I/O	X2VDD	—
RF Interface 3/CPRI/TDM2/Clocking					
ANT3_TX_CLK	Transmit Clock	D3	O	X2VDD	—
ANT3_RX_CLK/ TDM2_TCK/ GPIO04	Receive Clock	D1	I/O	X2VDD	—
ANT3_TXNRX	TX_RX Control	C1	I/O	X2VDD	—
ANT3_ENABLE	Antenna Enable	D5	I/O	X2VDD	—
ANT3_TX_FRAME	Transmit Frame	E3	I/O	X2VDD	2
ANT3_RX_FRAME/ GPIO05	Receive Frame	C2	I/O	X2VDD	—
ANT3_DIO000/ CP_SYNC1	Data	B6	I/O	X2VDD	2, 4
ANT3_DIO001/ CP_SYNC2	Data	A5	I/O	X2VDD	4,13
ANT3_DIO002/ CP_LOS1	Data	B5	I/O	X2VDD	4,13
ANT3_DIO003/ CP_LOS2	Data	A4	I/O	X2VDD	4,13
ANT3_DIO004/ CP_TX_INT_B	Data	C4	I/O	X2VDD	4,13
ANT3_DIO005/ CP_RCLK	Data	C5	I/O	X2VDD	4,13
ANT3_DIO006/ CP_RX_INT_B	Data	A3	I/O	X2VDD	4,13
ANT3_DIO007/ TDM2_TFS	Data	B3	I/O	X2VDD	2
ANT3_DIO008/ TDM2_RCK/ CKSTP0_OUT_B	Data	A2	I/O	X2VDD	2
ANT3_DIO009/ TDM2_RFS/ CKSTP1_OUT_B	Data	C3	I/O	X2VDD	4,13
ANT3_DIO010/ TDM2_RXD	Data	D4	I/O	X2VDD	4,13
ANT3_DIO011/ TDM2_TXD	Data	B1	I/O	X2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
RF Interface 4/GPIO/Timers/DMA/Interrupts/Clocking					
ANT4_TX_CLK	Transmit Clock	W7	O	X1VDD	—
ANT4_RX_CLK/ GPIO04/ TRIG_IN	Receive Clock	W5	I/O	X1VDD	—
ANT4_TXNRX	TX_RX Control	Y6	O	X1VDD	—
ANT4_ENABLE/ SYS_DMA_DONE	Antenna Enable	Y2	O	X1VDD	—
ANT4_TX_FRAME/ GPO06	Transmit Frame	Y3	O	X1VDD	2
ANT4_RX_FRAME/ GPIO05	Receive Frame	Y5	I/O	X1VDD	—
ANT4_DIO000/ TIMER05	Data	U5	I/O	X1VDD	—
ANT4_DIO001/ SYS_DMA_REQ	Data	U6	I/O	X1VDD	—
ANT4_DIO002/ IRQ00	Data	V1	I/O	X1VDD	—
ANT4_DIO003/ IRQ01	Data	V4	I/O	X1VDD	—
ANT4_DIO004/ IRQ02	Data	V2	I/O	X1VDD	—
ANT4_DIO005/ IRQ03	Data	V3	I/O	X1VDD	—
ANT4_DIO006/ IRQ_OUT_B	Data	U7	I/O	X1VDD	—
ANT4_DIO007/ MCP1_B	Data	V5	I/O	X1VDD	—
ANT4_DIO008/ MCP0_B	Data	V7	I/O	X1VDD	—
ANT4_DIO009/ CKSTP0_IN_B	Data	W1	I/O	X1VDD	—
ANT4_DIO010/ CKSTP1_IN_B	Data	W3	I/O	X1VDD	—
ANT4_DIO011/ SRESET_B	Data	W4	I/O	X1VDD	—
RF Interface SPI & Control					
SPI2_CLK	SPI Serial Clock	E6	O	X2VDD	—
SPI2_MOSI	SPI Master Out Slave In Data	E7	O	X2VDD	2
SPI2_MISO	SPI Master In Slave Out Data	A6	I	X2VDD	—
SPI2_CS0_B	SPI Slave Select	B7	O	X2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SPI2_CS1_B	SPI Slave Select	A7	O	X2VDD	—
SPI2_CS2_B/ GPO93	SPI Slave Select	A8	O	X2VDD	—
SPI2_CS3_B/ GPO94	SPI Slave Select	D6	O	X2VDD	—
Analog					
D1_MVREF	DDR Reference Voltage	J17	I	G1VDD	—
D2_MVREF	DDR Reference Voltage	Y12	I	G2VDD	—
TEMP_ANODE	Temperature Diode Anode	V27	I	—	9
TEMP_CATHODE	Temperature Diode Cathode	W27	I	—	9
SENSEVDD	VDD Sensing Pin—MAPLE	J13	I	—	—
SENSEVDDC	VDD Sensing Pin	L20	I	—	—
SENSEVSS	GND Sensing Pin	R20	I	—	—
Power Supply					
AVDD_PLAT	Platform PLL Supply	G7	—	AVDD_PLAT	—
AVDD_CORE0	Core PLL Supply	N20	—	AVDD_CORE0	—
AVDD_CORE1	Core PLL Supply	P20	—	AVDD_CORE1	—
AVDD_D1_DDR	DDR PLL Supply	M20	—	AVDD_D1_DDR	—
AVDD_D2_DDR	DDR PLL Supply	AA1	—	AVDD_D2_DDR	—
AVDD_DSP	DSP PLL Supply	Y16	—	AVDD_DSP	—
AVDD_MAPLE	MAPLE PLL Supply	Y20	—	AVDD_MAPLE	—
SD1AVDD	SerDes PLL Supply	AC22	—	SD1AVDD	—
SD2AVDD	SerDes PLL Supply	AB19	—	SD2AVDD	—
POVDD1	Secure Fuse Programming Overdrive	N23	—	POVDD1	8
POVDD2	Central Fuse Programming Overdrive—DSP	P23	—	—	8
POVDD3	Central Fuse Programming Overdrive—DSP	AA16	—	—	8
FA_VDD	POSt VDD	Y7	—	—	7
VDDC	Core/Platform Supply	J14	—	VDDC	—
VDDC	Core/Platform Supply	K14	—	VDDC	—
VDDC	Core/Platform Supply	L14	—	VDDC	—
VDDC	Core/Platform Supply	M14	—	VDDC	—
VDDC	Core/Platform Supply	N14	—	VDDC	—
VDDC	Core/Platform Supply	P10	—	VDDC	—
VDDC	Core/Platform Supply	P12	—	VDDC	—
VDDC	Core/Platform Supply	P14	—	VDDC	—
VDDC	Core/Platform Supply	R10	—	VDDC	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VDDC	Core/Platform Supply	R12	—	VDDC	—
VDDC	Core/Platform Supply	R14	—	VDDC	—
VDDC	Core/Platform Supply	T10	—	VDDC	—
VDDC	Core/Platform Supply	T12	—	VDDC	—
VDDC	Core/Platform Supply	T14	—	VDDC	—
VDDC	Core/Platform Supply	U10	—	VDDC	—
VDDC	Core/Platform Supply	U12	—	VDDC	—
VDDC	Core/Platform Supply	U14	—	VDDC	—
VDDC	Core/Platform Supply	V10	—	VDDC	—
VDDC	Core/Platform Supply	V12	—	VDDC	—
VDDC	Core/Platform Supply	V14	—	VDDC	—
VDDC	Core/Platform Supply	W10	—	VDDC	—
VDDC	Core/Platform Supply	W12	—	VDDC	—
VDDC	Core/Platform Supply	W14	—	VDDC	—
VDDC	Core/Platform Supply	Y10	—	VDDC	—
VDDC	Core/Platform Supply	Y14	—	VDDC	—
VDDC	Core/Platform Supply	J16	—	VDDC	—
VDDC	Core/Platform Supply	J18	—	VDDC	—
VDDC	Core/Platform Supply	K16	—	VDDC	—
VDDC	Core/Platform Supply	K18	—	VDDC	—
VDDC	Core/Platform Supply	L16	—	VDDC	—
VDDC	Core/Platform Supply	L18	—	VDDC	—
VDDC	Core/Platform Supply	M16	—	VDDC	—
VDDC	Core/Platform Supply	M18	—	VDDC	—
VDDC	Core/Platform Supply	N16	—	VDDC	—
VDDC	Core/Platform Supply	N18	—	VDDC	—
VDDC	Core/Platform Supply	P16	—	VDDC	—
VDDC	Core/Platform Supply	P18	—	VDDC	—
VDDC	Core/Platform Supply	R16	—	VDDC	—
VDDC	Core/Platform Supply	R18	—	VDDC	—
VDDC	Core/Platform Supply	T16	—	VDDC	—
VDDC	Core/Platform Supply	T18	—	VDDC	—
VDDC	Core/Platform Supply	U16	—	VDDC	—
VDDC	Core/Platform Supply	U18	—	VDDC	—
VDDC	Core/Platform Supply	V16	—	VDDC	—
VDDC	Core/Platform Supply	V18	—	VDDC	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VDDC	Core/Platform Supply	W16	—	VDDC	—
VDDC	Core/Platform Supply	W18	—	VDDC	—
VDDC	Core/Platform Supply	Y18	—	VDDC	—
VDD	MAPLE Supply	J10	—	VDD	—
VDD	MAPLE Supply	J12	—	VDD	—
VDD	MAPLE Supply	K10	—	VDD	—
VDD	MAPLE Supply	K12	—	VDD	—
VDD	MAPLE Supply	L10	—	VDD	—
VDD	MAPLE Supply	L12	—	VDD	—
VDD	MAPLE Supply	M10	—	VDD	—
VDD	MAPLE Supply	M12	—	VDD	—
VDD	MAPLE Supply	N10	—	VDD	—
VDD	MAPLE Supply	N12	—	VDD	—
G1VDD	DDR Supply	B13	—	G1VDD	—
G1VDD	DDR Supply	E11	—	G1VDD	—
G1VDD	DDR Supply	H9	—	G1VDD	—
G1VDD	DDR Supply	H10	—	G1VDD	—
G1VDD	DDR Supply	H11	—	G1VDD	—
G1VDD	DDR Supply	H12	—	G1VDD	—
G1VDD	DDR Supply	H13	—	G1VDD	—
G1VDD	DDR Supply	H14	—	G1VDD	—
G1VDD	DDR Supply	H15	—	G1VDD	—
G1VDD	DDR Supply	H16	—	G1VDD	—
G1VDD	DDR Supply	H17	—	G1VDD	—
G1VDD	DDR Supply	H18	—	G1VDD	—
G1VDD	DDR Supply	H19	—	G1VDD	—
G1VDD	DDR Supply	H20	—	G1VDD	—
G1VDD	DDR Supply	B18	—	G1VDD	—
G1VDD	DDR Supply	B23	—	G1VDD	—
G1VDD	DDR Supply	D20	—	G1VDD	—
G1VDD	DDR Supply	E15	—	G1VDD	—
G2VDD	DDR Supply	AC3	—	G2VDD	—
G2VDD	DDR Supply	AC10	—	G2VDD	—
G2VDD	DDR Supply	AA8	—	G2VDD	—
G2VDD	DDR Supply	AA9	—	G2VDD	—
G2VDD	DDR Supply	AA10	—	G2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
G2VDD	DDR Supply	AA11	—	G2VDD	—
G2VDD	DDR Supply	AA12	—	G2VDD	—
G2VDD	DDR Supply	AA13	—	G2VDD	—
G2VDD	DDR Supply	AA14	—	G2VDD	—
G2VDD	DDR Supply	AA15	—	G2VDD	—
G2VDD	DDR Supply	AD6	—	G2VDD	—
G2VDD	DDR Supply	AD13	—	G2VDD	—
G2VDD	DDR Supply	AF2	—	G2VDD	—
G2VDD	DDR Supply	AG4	—	G2VDD	—
G2VDD	DDR Supply	AG9	—	G2VDD	—
G2VDD	DDR Supply	AG12	—	G2VDD	—
G2VDD	DDR Supply	AC15	—	G2VDD	—
LVDD	Ethernet Supply	Y23	—	LVDD	—
LVDD	Ethernet Supply	AA25	—	LVDD	—
BVDD	IFC, eSDHC, USIM Supply	B26	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	E24	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	F26	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	G24	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	J20	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	J26	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	K20	—	BVDD	—
BVDD	IFC, eSDHC, USIM Supply	K24	—	BVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	N22	—	CVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	P22	—	CVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	M26	—	CVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	R21	—	CVDD	—
CVDD	USB, eSPI, DUART, I2C, USIM Supply	R26	—	CVDD	—
OVDD	DUART, System, I2C, JTAG Supply	U20	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	V20	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	V21	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	V26	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	U23	—	OVDD	—
OVDD	DUART, System, I2C, JTAG Supply	AD27	—	OVDD	—
X1VDD	RF Supply	N2	—	X1VDD	—
X1VDD	RF Supply	N4	—	X1VDD	—
X1VDD	RF Supply	N8	—	X1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
X1VDD	RF Supply	U4	—	X1VDD	—
X1VDD	RF Supply	W2	—	X1VDD	—
X1VDD	RF Supply	W6	—	X1VDD	—
X1VDD	RF Supply	P8	—	X1VDD	—
X1VDD	RF Supply	R6	—	X1VDD	—
X1VDD	RF Supply	R8	—	X1VDD	—
X1VDD	RF Supply	T8	—	X1VDD	—
X1VDD	RF Supply	U8	—	X1VDD	—
X1VDD	RF Supply	V8	—	X1VDD	—
X1VDD	RF Supply	W8	—	X1VDD	—
X1VDD	RF Supply	Y8	—	X1VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	B4	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	C6	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	G2	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	J4	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	J8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	K6	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	K8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	L8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	M8	—	X2VDD	—
XCOREVDD	SerDes Core Logic Supply	AH19	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AH23	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AH27	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG25	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AF16	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG17	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG21	—	XCOREVDD	—
XPADVDD	SerDes Transceiver Supply	AA19	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AA20	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF18	—	XPADVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
XPADVDD	SerDes Transceiver Supply	AE20	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF22	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF26	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AE24	—	XPADVDD	—
Ground					
VSS	Platform and Core Ground	A9	—	—	—
VSS	Platform and Core Ground	A26	—	—	—
VSS	Platform and Core Ground	B2	—	—	—
VSS	Platform and Core Ground	B8	—	—	—
VSS	Platform and Core Ground	B11	—	—	—
VSS	Platform and Core Ground	B15	—	—	—
VSS	Platform and Core Ground	B21	—	—	—
VSS	Platform and Core Ground	C27	—	—	—
VSS	Platform and Core Ground	D17	—	—	—
VSS	Platform and Core Ground	D22	—	—	—
VSS	Platform and Core Ground	D24	—	—	—
VSS	Platform and Core Ground	E27	—	—	—
VSS	Platform and Core Ground	F18	—	—	—
VSS	Platform and Core Ground	F21	—	—	—
VSS	Platform and Core Ground	H23	—	—	—
VSS	Platform and Core Ground	H27	—	—	—
VSS	Platform and Core Ground	J15	—	—	—
VSS	Platform and Core Ground	J19	—	—	—
VSS	Platform and Core Ground	J21	—	—	—
VSS	Platform and Core Ground	K15	—	—	—
VSS	Platform and Core Ground	K17	—	—	—
VSS	Platform and Core Ground	K19	—	—	—
VSS	Platform and Core Ground	L15	—	—	—
VSS	Platform and Core Ground	L17	—	—	—
VSS	Platform and Core Ground	L19	—	—	—
VSS	Platform and Core Ground	L27	—	—	—
VSS	Platform and Core Ground	L21	—	—	—
VSS	Platform and Core Ground	L23	—	—	—
VSS	Platform and Core Ground	M15	—	—	—
VSS	Platform and Core Ground	M17	—	—	—
VSS	Platform and Core Ground	M19	—	—	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	M21	—	—	—
VSS	Platform and Core Ground	N15	—	—	—
VSS	Platform and Core Ground	N17	—	—	—
VSS	Platform and Core Ground	N19	—	—	—
VSS	Platform and Core Ground	N21	—	—	—
VSS	Platform and Core Ground	N24	—	—	—
VSS	Platform and Core Ground	P27	—	—	—
VSS	Platform and Core Ground	P15	—	—	—
VSS	Platform and Core Ground	P17	—	—	—
VSS	Platform and Core Ground	P19	—	—	—
VSS	Platform and Core Ground	P21	—	—	—
VSS	Platform and Core Ground	R15	—	—	—
VSS	Platform and Core Ground	R17	—	—	—
VSS	Platform and Core Ground	R19	—	—	—
VSS	Platform and Core Ground	T15	—	—	—
VSS	Platform and Core Ground	T17	—	—	—
VSS	Platform and Core Ground	T19	—	—	—
VSS	Platform and Core Ground	T20	—	—	—
VSS	Platform and Core Ground	T24	—	—	—
VSS	Platform and Core Ground	U27	—	—	—
VSS	Platform and Core Ground	U15	—	—	—
VSS	Platform and Core Ground	U17	—	—	—
VSS	Platform and Core Ground	U19	—	—	—
VSS	Platform and Core Ground	V15	—	—	—
VSS	Platform and Core Ground	V17	—	—	—
VSS	Platform and Core Ground	V19	—	—	—
VSS	Platform and Core Ground	W15	—	—	—
VSS	Platform and Core Ground	W17	—	—	—
VSS	Platform and Core Ground	W19	—	—	—
VSS	Platform and Core Ground	W20	—	—	—
VSS	Platform and Core Ground	W21	—	—	—
VSS	Platform and Core Ground	W24	—	—	—
VSS	Platform and Core Ground	W28	—	—	—
VSS	Platform and Core Ground	Y21	—	—	—
VSS	Platform and Core Ground	Y15	—	—	—
VSS	Platform and Core Ground	Y17	—	—	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	Y19	—	—	—
VSS	Platform and Core Ground	Y26	—	—	—
VSS	Platform and Core Ground	AB28	—	—	—
VSS	Platform and Core Ground	AA21	—	—	—
VSS	Platform and Core Ground	AD16	—	—	—
VSS	Platform and Core Ground	AE27	—	—	—
VSS	Platform and Core Ground	AF28	—	—	—
VSS	Platform and Core Ground	AG16	—	—	—
VSS	Platform and Core Ground	AD1	—	—	—
VSS	Platform and Core Ground	AE4	—	—	—
VSS	Platform and Core Ground	AE8	—	—	—
VSS	Platform and Core Ground	AE11	—	—	—
VSS	Platform and Core Ground	AF14	—	—	—
VSS	Platform and Core Ground	AG7	—	—	—
VSS	Platform and Core Ground	C7	—	—	—
VSS	Platform and Core Ground	D2	—	—	—
VSS	Platform and Core Ground	D7	—	—	—
VSS	Platform and Core Ground	D9	—	—	—
VSS	Platform and Core Ground	E4	—	—	—
VSS	Platform and Core Ground	E8	—	—	—
VSS	Platform and Core Ground	F6	—	—	—
VSS	Platform and Core Ground	F7	—	—	—
VSS	Platform and Core Ground	F8	—	—	—
VSS	Platform and Core Ground	F13	—	—	—
VSS	Platform and Core Ground	G6	—	—	—
VSS	Platform and Core Ground	G8	—	—	—
VSS	Platform and Core Ground	H4	—	—	—
VSS	Platform and Core Ground	H6	—	—	—
VSS	Platform and Core Ground	H7	—	—	—
VSS	Platform and Core Ground	H8	—	—	—
VSS	Platform and Core Ground	J9	—	—	—
VSS	Platform and Core Ground	J11	—	—	—
VSS	Platform and Core Ground	K2	—	—	—
VSS	Platform and Core Ground	K9	—	—	—
VSS	Platform and Core Ground	K11	—	—	—
VSS	Platform and Core Ground	K13	—	—	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	L6	—	—	—
VSS	Platform and Core Ground	L9	—	—	—
VSS	Platform and Core Ground	L11	—	—	—
VSS	Platform and Core Ground	L13	—	—	—
VSS	Platform and Core Ground	M11	—	—	—
VSS	Platform and Core Ground	M13	—	—	—
VSS	Platform and Core Ground	M4	—	—	—
VSS	Platform and Core Ground	M9	—	—	—
VSS	Platform and Core Ground	N9	—	—	—
VSS	Platform and Core Ground	N11	—	—	—
VSS	Platform and Core Ground	N13	—	—	—
VSS	Platform and Core Ground	P9	—	—	—
VSS	Platform and Core Ground	P11	—	—	—
VSS	Platform and Core Ground	P13	—	—	—
VSS	Platform and Core Ground	R9	—	—	—
VSS	Platform and Core Ground	R11	—	—	—
VSS	Platform and Core Ground	R13	—	—	—
VSS	Platform and Core Ground	P6	—	—	—
VSS	Platform and Core Ground	T2	—	—	—
VSS	Platform and Core Ground	T4	—	—	—
VSS	Platform and Core Ground	T9	—	—	—
VSS	Platform and Core Ground	T11	—	—	—
VSS	Platform and Core Ground	T13	—	—	—
VSS	Platform and Core Ground	AB1	—	—	—
VSS	Platform and Core Ground	AB5	—	—	—
VSS	Platform and Core Ground	AB7	—	—	—
VSS	Platform and Core Ground	AA2	—	—	—
VSS	Platform and Core Ground	Y1	—	—	—
VSS	Platform and Core Ground	Y4	—	—	—
VSS	Platform and Core Ground	Y9	—	—	—
VSS	Platform and Core Ground	Y11	—	—	—
VSS	Platform and Core Ground	Y13	—	—	—
VSS	Platform and Core Ground	W9	—	—	—
VSS	Platform and Core Ground	W11	—	—	—
VSS	Platform and Core Ground	W13	—	—	—
VSS	Platform and Core Ground	V9	—	—	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	V11	—	—	—
VSS	Platform and Core Ground	V13	—	—	—
VSS	Platform and Core Ground	V6	—	—	—
VSS	Platform and Core Ground	U9	—	—	—
VSS	Platform and Core Ground	U11	—	—	—
VSS	Platform and Core Ground	U13	—	—	—
XCOREVSS	SerDes Core Logic Ground	AH17	—	—	—
XCOREVSS	SerDes Core Logic Ground	AH21	—	—	—
XCOREVSS	SerDes Core Logic Ground	AH25	—	—	—
XCOREVSS	SerDes Core Logic Ground	AG19	—	—	—
XCOREVSS	SerDes Core Logic Ground	AG23	—	—	—
XCOREVSS	SerDes Core Logic Ground	AG27	—	—	—
XCOREVSS	SerDes Core Logic Ground	AF27	—	—	—
XCOREVSS	SerDes Core Logic Ground	AD17	—	—	—
XCOREVSS	SerDes Core Logic Ground	AD20	—	—	—
XCOREVSS	SerDes Core Logic Ground	AD24	—	—	—
XCOREVSS	SerDes Core Logic Ground	AD25	—	—	—
XCOREVSS	SerDes Core Logic Ground	AE16	—	—	—
XCOREVSS	SerDes Core Logic Ground	AA17	—	—	—
XCOREVSS	SerDes Core Logic Ground	AB17	—	—	—
XCOREVSS	SerDes Core Logic Ground	AC17	—	—	—
XCOREVSS	SerDes Core Logic Ground	AB21	—	—	—
XCOREVSS	SerDes Core Logic Ground	AB22	—	—	—
XCOREVSS	SerDes Core Logic Ground	AC23	—	—	—
XPADVSS	SerDes Transceiver Ground	AF20	—	—	—
XPADVSS	SerDes Transceiver Ground	AC18	—	—	—
XPADVSS	SerDes Transceiver Ground	AE18	—	—	—
XPADVSS	SerDes Transceiver Ground	AE22	—	—	—
XPADVSS	SerDes Transceiver Ground	AE26	—	—	—
XPADVSS	SerDes Transceiver Ground	AF24	—	—	—
XPADVSS	SerDes Transceiver Ground	AD19	—	—	—
XPADVSS	SerDes Transceiver Ground	AD21	—	—	—
XPADVSS	SerDes Transceiver Ground	AD23	—	—	—
SD2AGND	SerDes PLL Ground	AA18	—	—	—
SD1AGND	SerDes PLL Ground	AC20	—	—	—
No Connect					

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
NC	Address Parity Error	E19	—	—	—
NC	Address Parity Error	AH4	—	—	—

1 These are test signals for factory use only and must be pulled up (with 100 Ω–1 kΩ) to OVDD for normal operation.

2 This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull up or active driver is needed.

3 These pins have weak internal pull-up P-FETs that are always enabled.

4 This pin must NOT be pulled down during power-on reset.

5 This pin is an open drain signal.

6 This pin should be pulled down with 200Ω ± 1% resistor when used in autocalibration mode.

7 This pin should be pulled down to VSS with 10 kΩ.

8 This pin is used for fuse programming. Should be tied to VSS for normal operation (fuse read). See section Section 2.2, "Power Sequencing," for more details.

9 This pin may be connected to a temperature diode monitoring device such as the Analog Devices, ADT7461A™. If a temperature diode monitoring device will not be connected, these pins may be connected to test point or left as a no connect.

10 Pin should be pulled high or low depending on the JTAG topology selected. Refer to Section 3.11, "JTAG Configuration Signals."

11 This pin should be tied to GND/VSS when MAPLE is powered down; otherwise it should be tied to OVDD.

12 This pin is an open-drain signal if the IIC2 pin is selected.

13 It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull up or active driver is needed.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Platform supply voltage	V_{DDC}	–0.3 to 1.05	V	—
MAPLE-B2P supply voltage	V_{DD}	–0.3 to 1.05	V	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
PLL supply voltage		$AV_{DD\_CORE[0–1]}$ $AV_{DD\_D[1–2]\_DDR}$ AV_{DD_PLAT} AV_{DD_DSP} AV_{DD_MAPLE} $SD[1–2]AV_{DD}$	–0.3 to 1.05	V	2
Fuse programming supply		POV_{DD1} POV_{DD2} POV_{DD3}	–0.3 to 1.65	V	—
DDR3/DDR3L DRAM I/O voltage		$GV_{DD[1–2]}$	–0.3 to 1.65 –0.3 to 1.45	V	—
Three-speed Ethernet, Ethernet management (eTSEC) and 1588		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
IFC, eSDHC, USIM		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	3
DUART1, SYSCLK, system control and power management, I^2C1, clocking, I/O voltage select, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
USB, eSPI1, DUART2, I^2C2, USIM		CV_{DD}	–0.3 to 3.63 –0.3 to 1.98	V	3, 4
RF parallel interface		$X1V_{DD}$	–0.3 to 3.63 –0.3 to 1.98	V	—
eSPI2, USB, TDM1, TDM2, RF parallel interface		$X2V_{DD}$	–0.3 to 3.63 –0.3 to 1.98	V	—
SerDes pad voltage		$XPADV_{DD}$	–0.3 to 1.65	V	—
SerDes core voltage		$XCOREV_{DD}$	–0.3 to 1.05	V	—
Input voltage	DDR3/DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	5, 10
	DDR3/DDR3L DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2 + 0.3)	V	10
	Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	6, 10
	IFC, eSDHC, USIM signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	7, 10
	DUART1, SYSCLK, system control and power management, I^2C1, clocking, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	8, 10
	USB, eSPI1, DUART2, I^2C2, USIM	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 10
	RF parallel interface	$X1V_{IN}$	–0.3 to ($X1V_{DD}$ + 0.3)	V	9, 10
	eSPI2, USB, TDM1, TDM2, RF parallel interface	$X2V_{IN}$	–0.3 to ($X2V_{DD}$ + 0.3)	V	9, 10
Storage temperature range		T_{STG}	–55 to 150	°C	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic	Symbol	Max Value	Unit	Note

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. AV_{DD} is measured at the input to the filter and not at the pin of the device.
3. USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.
4. Caution: CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Caution: LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. Caution: BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. Caution: X[1-2]V_{IN} must not exceed X[1-2]V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. (C,X,B,G,L,O,R)V_{DD} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Platform supply voltage	V_{DDC}	1 + 50 mV / – 30mV	V	1
MAPLE-B2P supply voltage	V_{DD}	1 + 50 mV / – 30mV	V	—
PLL supply voltage	$AV_{DD\_CORE[0–1]}$ $AV_{DD\_D[1–2]\_DDR}$ AV_{DD_PLAT} AV_{DD_DSP} AV_{DD_MAPLE} SD[1–2]AV_{DD}	1 + 50 mV / – 30mV	V	1
Fuse supply voltage	POV_{DD1}	1.5 V ± 75 mV	V	1
DDR3 DRAM I/O voltage	G[1–2]V_{DD}	1.5 V ± 75 mV	—	—
DDR3L DRAM I/O voltage	G[1–2]V_{DD}	1.35 V +100mV/ –67mV	—	—
Three-speed Ethernet, Ethernet management (eTSEC) and 1588	LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
DUART1, SYSCLK, system control and power management, I^2C1, clocking, I/O voltage select, and JTAG I/O voltage	OV_{DD}	3.3 V ± 165 mV	V	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
IFC, eSDHC, USIM		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	2
USB, eSPI1, DUART2, I^2C2, USIM		CV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	2
RF parallel interface		$X1V_{DD}$	3.3 V ± 165 mV 1.8 V ± 90 mV	V	—
eSPI2, USB, TDM1, TDM2, RF parallel interface		$X2V_{DD}$	3.3 V ± 165 mV 1.8 V ± 90 mV	V	—
SerDes pad voltage		$XPADV_{DD}$	1.5 V ± 75 mV	V	—
SerDes core voltage		$XCOREV_{DD}$	1.0 V ± 50 mV	V	—
Input voltage	DDR3/DDR3L DRAM	MV_{IN}	GND to GV_{DD}	V	—
	DDR3/DDR3L DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Ethernet, USB	LV_{IN}	GND to LV_{DD}	V	—
	IFC, eSDHC signals	BV_{IN}	GND to BV_{DD}	V	—
	DUART1, SYSCLK, system control and power management, eSPI, I^2C1, USIM, clocking, I/O voltage select, and JTAG I/O voltage	OV_{IN}	GND to OV_{DD}	V	—
	USB, eSPI, eSDHC, DUART2, I^2C2, USIM	CV_{IN}	GND to CV_{DD}	V	—
	RF parallel interface	$X1V_{IN}$	GND to $X1V_{DD}$	V	—
	eSPI2, USB, TDM1, TDM2, RF parallel interface	$X2V_{IN}$	GND to $X2V_{DD}$	V	—
Maximum input capacitance		C_{INMAX}	10	pF	3
Operating Temperature range	Standard	T_A/T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—
	Extended	T_A/T_J	T_A = –40 (min) to T_J = 105 (max)	°C	—
	Secure boot fuse programming	T_A/T_J	T_A = 0 (min) to T_J = 70 (max)	°C	1

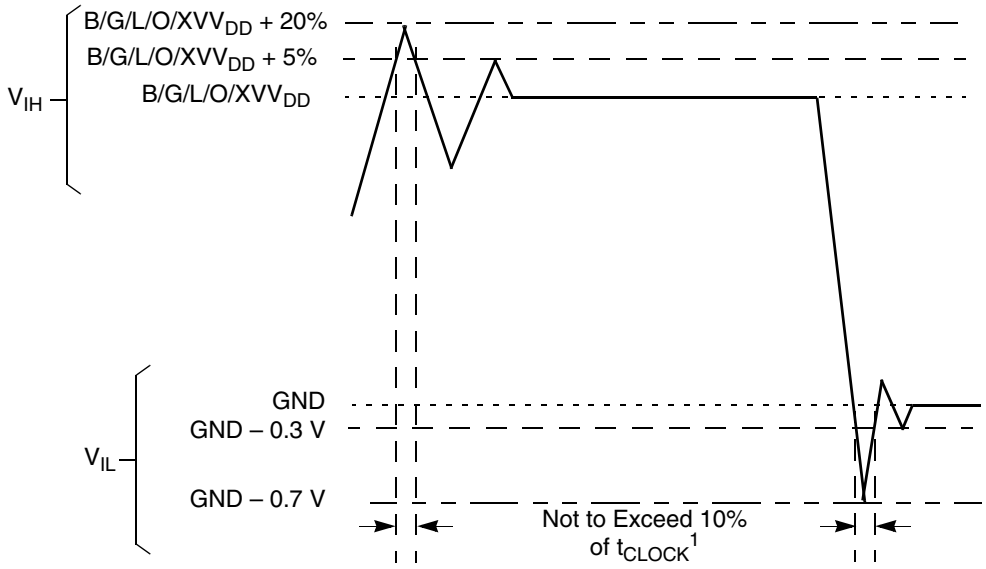
Note:

1 **Caution:** POV_{DD1} must be supplied 1.5 V and the device must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD1} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power Sequencing."

2 USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.

3 Unless otherwise stated in an interface's DC specifications, the maximum allowed input capacitance in this table is a general recommendation for signals.

This figure shows the undershoot and overshoot voltages at the interfaces.



Note:
1. t_{CLOCK} refers to the clock period associated with the respective interface:
For I^2C and JTAG, t_{CLOCK} references SYSCLK.
For DDR, t_{CLOCK} references MCLK.
For eTSEC, t_{CLOCK} references TSEC*n*_GTX_CLK125.
For IFC, t_{CLOCK} references IFC_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/X1V_{DD}/X2V_{DD}$

The core voltage must always be provided at nominal 1 V (see Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR3 SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Note
IFC, GPIO[0:7], eSDHC	47 ± 7	BV_{DD} = 3.3/2.5/1.8 V	—
DDR3 (programmable)	16 32 (half strength mode)	GV_{DD} = 1.5 V DDR3 GV_{DD} = 1.35 V DDR3L	1
eTSEC, USB	47 ± 7	LV_{DD} = 3.3/2.5 V	—
DUART1, system control, I^2C1, USIM, JTAG	47 ± 7	OV_{DD} = 3.3 V	2
USB, eSPI1, DUART2, I^2C2, USIM	47 ± 7	CV_{DD} = 3.3/1.8 V	2
RF parallel interface	LVCMOS	$X1V_{DD}$ = 3.3/1.8 V	—
eSPI2, USB, TDM1, TDM2, RF parallel interface	—	$X2V_{DD}$ = 3.3/1.8 V	—

Table 4. Output Drive Capability (continued)

Driver Type	Output Impedance (Ω)	Supply Voltage	Note

Note:

1 The drive strength of the DDR3 interface in half-strength mode is at T_j = 125°C and at GV_{DD} (min).

2 USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. VDD, VDDC, AVDD (all PLL supplies), XCOREVDD
2. LVDD, BVDD, CVDD, OVDD, X1VDD, X2VDD, G1VDD, G2VDD, XPADVDD
3. For secure boot fuse programming: After deassertion of HRESET_B, drive POV_{DD1} = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return POV_{DD1} = GND before the system is power cycled (HRESET_B assertion) or powered down (V_{DDC} ramp down) per the required timing specified in Table 5. See Section 3.14, "Security Fuse Processor," for additional details.

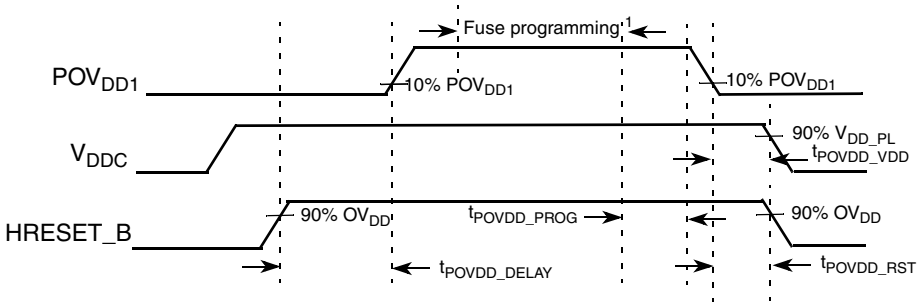
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device. Only one secure boot fuse programming event is permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD1} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD1} = GND.

POV_{DD2} and POV_{DD3} are always tied to GND.

This figure provides the POV_{DD1} timing diagram.



NOTE: POVDD must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD1} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD1}.

Table 5. POV_{DD1} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	1500	—	t_{SYSCLK}	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3

Table 5. POV_{DD1} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_RST}	0	—	μs	4

Note:

1. Delay required from the deassertion of HRESET_B to driving POV_{DD1} ramp up. Delay measured from HRESET_B deassertion at 90% OV_{DD} to 10% POV_{DD1} ramp up.
2. Delay required from fuse programming finished to POV_{DD1} ramp down start. Fuse programming must complete while POV_{DD1} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD1} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD1} = GND. After fuse programming is completed, it is required to return POV_{DD1} = GND.
3. Delay required from POV_{DD1} ramp down complete to V_{DDC} ramp down start. POV_{DD1} must be grounded to minimum 10% POV_{DD1} before V_{DDC} is at 90% V_{DDC}.
4. Delay required from POV_{DD1} ramp down complete to HRESET_B assertion. POV_{DD1} must be grounded to minimum 10% POV_{DD1} before HRESET_B assertion reaches 90% OV_{DD}.
5. Only one secure boot fuse programming event is permitted per lifetime of a device.

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, the sequencing for GV_{DD} is not required.

2.3 Power-Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

2.4 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. Table 6 provides the RESET initialization AC timing specifications.

Table 6. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Note
Required assertion time of HRESET_B	600	—	μs	1, 2, 5
Minimum assertion time of TRESET_B simultaneous to HRESET_B assertion	25	—	ns	3
Minimum assertion time for SRESET_B	3	—	t_{SYSCLK}	4
PLL input setup time with stable SYSCLK before HRESET_B negation	25	—	μs	—
Input setup time for POR configurations (other than PLL configuration) with respect to negation of HRESET_B	4	—	t_{SYSCLK}	4
Input hold time for all POR configurations (including PLL configuration) with respect to negation of HRESET_B	2	—	t_{SYSCLK}	4
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of HRESET_B	—	8	t_{SYSCLK}	4

Table 6. RESET Initialization Timing Specifications (continued)

Parameter	Min	Max	Unit	Note

Note:
1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. TRST is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in Section 3.11.1, "Termination of Unused Signals."
4. SYSCLK is the primary clock input.
5. Reset initialization should start only after all power supplies are stable.

This table provides the PLL lock times.

Table 7. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

2.5 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. Table 8 provides the power supply ramp rate specifications.

Table 8. Power Supply Ramp Rate

Parameter	Min	Max	Unit
Required ramp rate	—	36000	V/s
Required ramp time	—	50	ms

Note:
1. Ramp rate is specified as a linear ramp from 10 to 90% of the nominal voltage of the specific voltage supply.
2. All MCKE signals must remain low during the power up sequence.

2.6 Power Characteristics

This table shows the power dissipations of the V_{DDC} and V_{DD} supplies for various operating DSP and core complex bus clock (CCB_clk) frequencies versus the core and DDR clock frequencies.

Table 9. Core Power Dissipation

Power Mode	PA Core Frequency (MHz)	DSP Core Frequency (MHz)	CCB Frequency (MHz)	PA/DSP DDR Frequency (MHz)	MAPLE eTVPE Frequency (MHz)	V_{DDC} (V)	V_{DD} (V)	Junction Temp (°C)	$V_{DDC} + V_{DD}$ Power (W)	Note
Typical	1200	1200	600	1333	800	1	1	65	8.9	1, 2
Thermal								105	11.9	1, 3, 5
Maximum									14.8	1, 4, 5
Typical	1000	1000	500	1333	800	1	1	65	8.7	1, 2
Thermal								105	11.3	1, 3, 5
Maximum									13.9	1, 4, 5

Table 9. Core Power Dissipation (continued)

Power Mode	PA Core Frequency (MHz)	DSP Core Frequency (MHz)	CCB Frequency (MHz)	PA/DSP DDR Frequency (MHz)	MAPLE eTVPE Frequency (MHz)	V_{DDC} (V)	V_{DD} (V)	Junction Temp (°C)	V_{DDC} + V_{DD} Power (W)	Note

Note:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is a measured value while running a typical use case using the *nominal* process and *recommended* core, platform voltages (V_{DDC}), and MAPLE (V_{DD}) at 65 °C junction temperature (see Table 3).
3. Thermal power is the power measured while running a 50% (Cores) and 40% (Platform) utilization case, using the *worst case* process and *recommended* core, platform voltages (V_{DDC}), and MAPLE (V_{DD}) at maximum operating junction temperature (see Table 3).
4. Maximum power is measured while running a maximum power pattern using the worst case process, and recommended core, platform voltages (VDDC), and MAPLE (VDD) at maximum operating junction temperature (see Table 3).
5. An estimated IO power while running a USE case using the nominal process and recommended voltages is 1.5 W (see Table 3).

Table 10. I/O Power

PS#	Primary pin name	Pin width	Voltage domain	Recommended value	Current max	Typical current (A)	Max (A)	Note
I/O	OVDD	37	General I/O supply	3.3V	—	0.178	0.266	
	BVDD	46	Local Bus and GPIO I/O supply	1.8V/ 2.5V/ 3.3V	—	0.097	0.148	3
	LVDD	32	TSEC I/O supply	3.3V/ 2.5V	—	0.051	0.076	3
	CVDD	19	ULPI/SPI/UART/SIM I/O supply	3.3V/ 1.8V	—	0.030	0.045	3
	GVDD1	—	DDR1 (PPC Side) I/O supply	1.5V/ 1.35V	—	0.710	0.950	1, 2, 3
	GVDD2	—	DDR2 (DSP Side) I/O supply	1.5V/ 1.35V	—	0.710	0.950	1, 2, 3
	X1VDD	—	ANT1I/O supply	3.3V/ 1.8V	—	0.098	0.140	3
	X2VDD	—	ANT2, ANT3 I/O supply	3.3V/ 1.8V	—	0.098	0.140	3
SD	SVDD	—	SerDes Core logic supply	1.0V	—	0.144	0.144	—
	XVDD	—	SerDes I/O supply	1.5V	—	0.058	0.058	—
Analog	AVDD_CORE0	—	Core 0 PLL supply	1.0V	—	0.005	0.015	—
	AVDD_CORE1	—	Core 1 PLL supply		—			—
	AVDD_DSP	—	DSP PLL supply		—			—
	AVDD_PLAT	—	Platform PLL supply		—			—
	AVDD_D1_DDR	—	DDR PLL supply		—			—
	AVDD_D2_DDR	—	DDR PLL supply		—			—
	SDAVDD1	—	SerDes PLL supply		—			—
	SDAVDD2	—	SerDes PLL supply		—			—

Note:

1 For DDR typical, it is 40% DIMM utilization.

2 For DDR max, it is 75% DIMM utilization.

3 For I/O with different possible voltages, the currents listed above are for the higher voltage.

2.7 Input Clocks

This section provides information about the system clock specifications, spread spectrum sources, real time clock specifications, TDM clock specifications, and other input sources.

2.7.1 System Clock and DDR Clock Specifications

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) 3.3 V DC specifications.

Table 11. SYSCLK/DDRCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) AC timing specifications.

Table 12. SYSCLK/DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	66	—	100	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	10	ns	1, 2
DDRCLK frequency	f_{DDRCLK}	66	—	166	MHz	1
DDRCLK cycle time	t_{DDRCLK}	6.0	—	15.15	ns	—
SYSCLK/DDRCLK duty cycle	t_{KHK}/ $t_{SYSCLK/DDRCLK}$	40	—	60	%	2
SYSCLK/DDRCLK slew rate	—	1	—	4	V/ns	3
SYSCLK/DDRCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK/DDRCLK jitter phase noise at –56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.7.2 DSP Clock (DSPCLKIN) Specifications

This table provides the DSP clock (DSPCLKIN) 3.3 V DC specifications.

Table 13. DSPCLKIN DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the DSP clock (DSPCLKIN) AC timing specifications.

Table 14. DSPCLKIN AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
DSPCLKIN frequency	f_{SYSCLK}	66	—	133	MHz	1, 2
DSPCLKIN cycle time	t_{SYSCLK}	7.5	—	10	ns	1, 2
DSPCLKIN duty cycle	t_{KHK}/ t_{SYSCLK}	40	—	60	%	2
DSPCLKIN slew rate	—	1	—	4	V/ns	3
DSPCLKIN peak period jitter	—	—	—	±150	ps	—
DSPCLKIN jitter phase noise at –56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. **Caution:** The relevant clock **r**atio settings must be chosen such that the resulting DSPCLKIN frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.7.3 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the input cycle-to-cycle jitter requirement. Frequency modulation and spread are

separate concerns, and the device is compatible with spread spectrum sources if the recommendations listed in this table are observed.

Table 15. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Note
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:
1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 99.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device

CAUTION

The processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.7.4 Real Time Clock Specifications

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.7.5 RF Parallel Interface Clock Specifications

The following table lists the RF parallel interface clock DC electrical characteristics.

Table 16. RF Parallel Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	C	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

The following table lists the RF parallel interface clock AC electrical characteristics.

Table 17. RF Parallel Reference Clock AC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
ANT*n*_REF_CLK frequency	$f_{ANT\_REF\_CLK}$	—	19.2	—	MHz	—
ANT*n*_REF_CLK cycle time	$t_{ANT\_REF\_CLK}$	—	52	—	ns	—

Table 17. RF Parallel Reference Clock AC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
ANT*n*_REF_CLK duty cycle	$t_{KHK}/t_{ANT\_REF\_CLK}$	48	50	52	%	—
ANT*n*_REF_CLK slew rate	—	1	—	4	V/ns	1
ANT*n*_REF_CLK peak period jitter	—	—	—	±100	ps	—
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.

2.7.6 Other Input Clocks

A description of the overall clocking of this device is available in the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such as SerDes, Ethernet Management, eSDHC, and IFC, see the specific interface section.

2.8 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V and 1.35 V when interfacing to DDR3 or DDR3L SDRAM, respectively.

2.8.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed ±1% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must be able to supply up to125 μA current.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 19. DDR3L SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.35 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.090	V	5
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.3	mA	6, 7
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.3	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver.Peak-to-peak noise on MVREFn may not exceed the MVREFn DC level by more than ±1% of GV_{DD} (i.e. ±13.5 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must be able to supply up to125 μA current.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. IOH and IOL are measured at GV_{DD} = 1.282 V
7. See the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR controller interface capacitance for DDR3.

Table 20. DDR3 SDRAM Capacitance

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, DQS_B	C_{IO}	6	8	pF	—
Delta input/output capacitance: DQ, DQS, DQS_B	C_{DIO}	—	0.5	pF	—

This table provides the current draw characteristics for MVREF*n*.

Table 21. Current Draw Characteristics for MVREF*n*

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Current draw for DDR3 SDRAM for MVREF*n*	I_{MVREFn}	—	700	μA	—
Current draw for DDR3L SDRAM for MVREF*n*	I_{MVREFn}	—	700	μA	—

2.8.2 DDR3 and DDR3L SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM, and the required GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.8.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 22. DDR3 SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage > 1200 MHz data rate ≤ 1200 MHz data rate	V_{ILAC}	—	 MVREFn – 0.150 MVREFn – 0.175	V	—
AC input high voltage > 1200 MHz data rate ≤ 1200 MHz data rate	V_{IHAC}	 MVREF*n* + 0.150 MVREF*n* + 0.175	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 23. DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage > 1067 MHz data rate ≤ 1067 MHz data rate	V_{ILAC}	—	 MVREF*n* – 0.135 MVREF*n* – 0.160	V	—
AC input high voltage > 1067 MHz data rate ≤ 1067 MHz data rate	V_{IHAC}	 MVREF*n* + 0.135 MVREF*n* + 0.160	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3/3L SDRAM.

Table 24. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
1333 MHz data rate		–125	125		
1200 MHz data rate		–147.5	147.5		
1066 MHz data rate		–170	170		
800 MHz data rate		–200	200		
667 MHz data rate		–240	240		

Table 24. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	2
1333 MHz data rate		–250	250		
1200 MHz data rate		–275	275		
1066 MHz data rate		–300	300		
800 MHz data rate		–425	425		
667 MHz data rate		–510	510		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

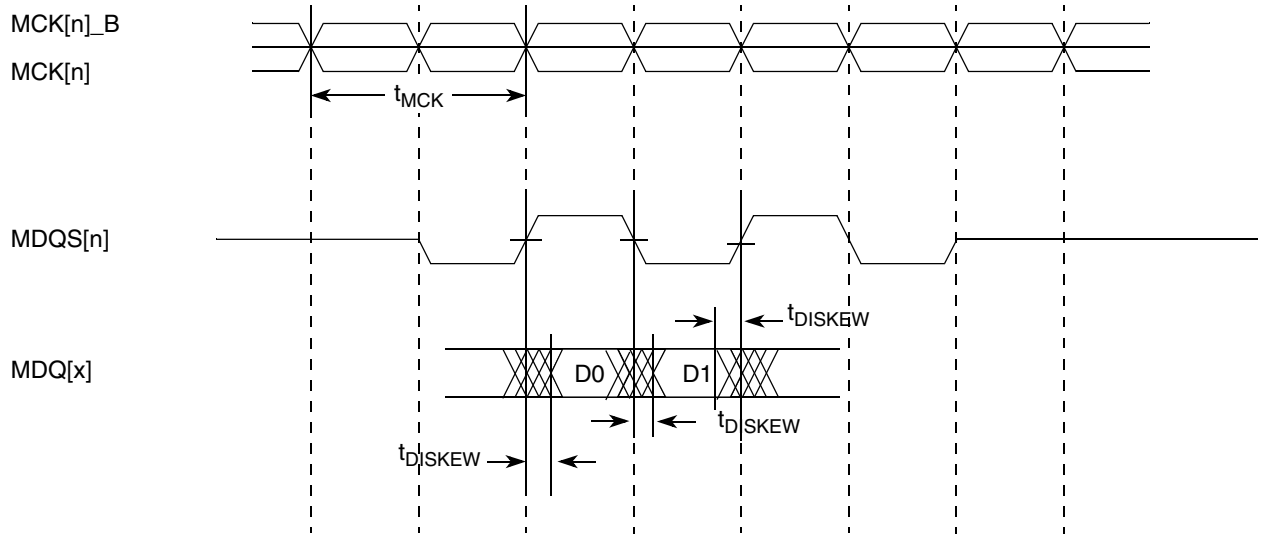


Figure 9. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

2.8.2.2 DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR3 and DDR3L SDRAM interface.

Table 25. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[n] cycle time	t_{MCK}	1.5	3	ns	2

Table 25. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
1333 MHz data rate		0.606	—		
1200 MHz data rate		0.675	—		
1066 MHz data rate		0.744	—		
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
1333 MHz data rate		0.606	—		
1200 MHz data rate		0.675	—		
1066 MHz data rate		0.744	—		
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCS[n]_B output setup with respect to MCK	t_{DDKHCS}			ns	3
1333 MHz data rate		0.606	—		
1200 MHz data rate		0.675	—		
1066 MHz data rate		0.744	—		
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCS[n]_B output hold with respect to MCK	t_{DDKHCX}			ns	3
1333 MHz data rate		0.606	—		
1200 MHz data rate		0.675	—		
1066 MHz data rate		0.744	—		
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
≥ 1066 MHz data rate		–0.245	0.245		
800 MHz data rate		–0.375	0.375		
667 MHz data rate		–0.6	0.6		

Table 25. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
1333 MHz data rate		250	—		
1200 MHz data rate		275	—		
1066 MHz data rate		300	—		
800 MHz data rate		375	—		
667 MHz data rate		450	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
1333 MHz data rate		250	—		
1200 MHz data rate		275	—		
1066 MHz data rate		300	—		
800 MHz data rate		375	—		
667 MHz data rate		450	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 25, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

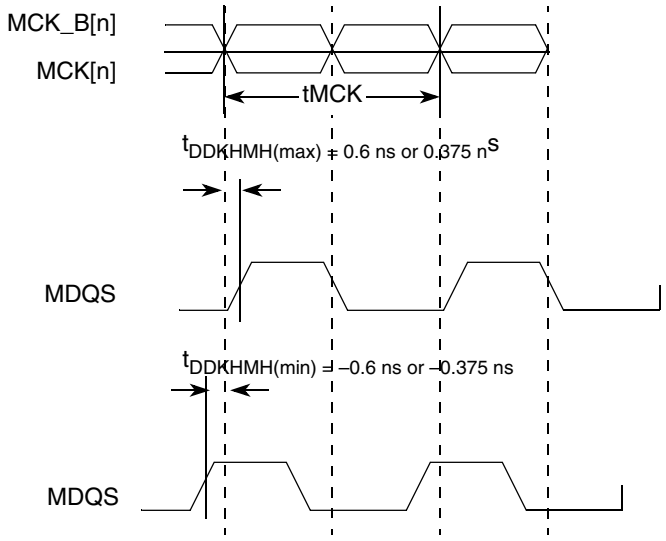


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

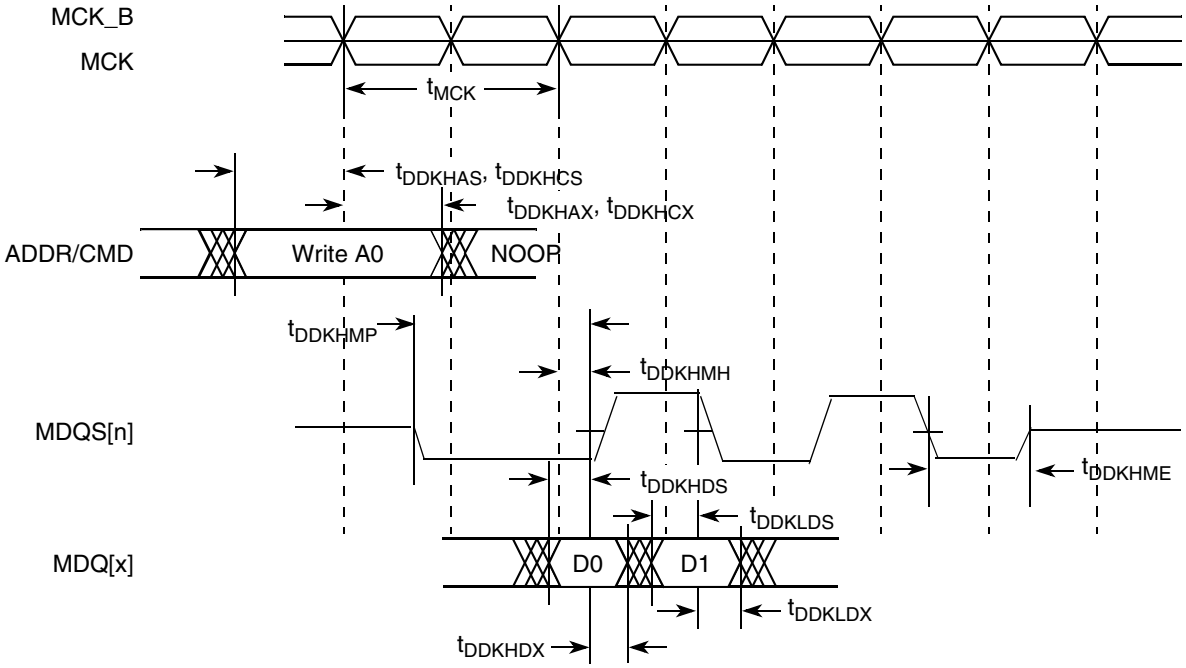


Figure 11. DDR3 and DDR3L Output Timing Diagram

This figure provides the AC test load for the DDR3 and DDR3Lcontroller bus.

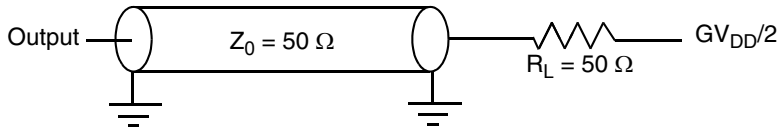


Figure 12. DDR3 and DDR3L Controller Bus AC Test Load

2.8.2.3 DDR3 and DDR3L SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 SDRAM controller interface. Figure 13 shows the differential timing specification.

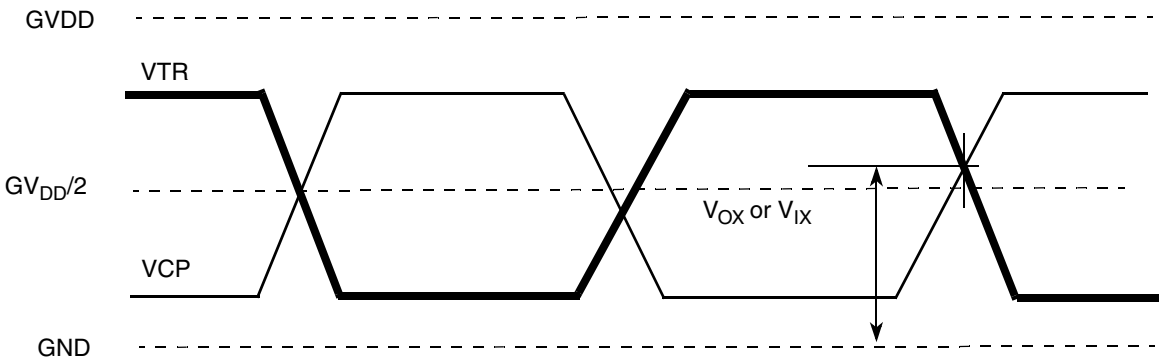


Figure 13. DDR3, and DDR3L SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as MCK_B or MDQS_B).

This table provides the DDR3 differential specifications for the differential signals MDQS/MDQS_B and MCK/MCK_B.

Table 26. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.150$	$0.5 \times GV_{DD} + 0.150$	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.115$	$0.5 \times GV_{DD} + 0.115$	V	1

Note:
1. I/O drivers are calibrated before making measurements.

This table provides the DDR3 differential specifications for the differential signals MDQS/MDQS_B and MCK/MCK_B.

Table 27. DDR3L SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.135$	$0.5 \times GV_{DD} + 0.135$	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.105$	$0.5 \times GV_{DD} + 0.105$	V	1

Note:
1. I/O drivers are calibrated before making measurements.

2.9 eSPI

This section describes the DC and AC electrical specifications for the SPI.

2.9.1 eSPI1 DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI1 on the device operating on a 3.3 V power supply.

Table 28. eSPI1 DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (0 V ≤ V_{IN} ≤ CV_{DD})	I_{IN}	—	±10	μA	2
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (I_{OL} = 6.0 mA)	V_{OL}	—	0.5	V	—
Output low voltage (IOL = 3.2 mA)	V_{OL}	—	0.4	V	—

Note:

1 The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2 The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the eSPI1 and eSPI2 on the device operating on a 1.8 V power supply.

Table 29. eSPI DC Electrical Characteristics (CV_{DD}, $X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (0 V ≤ V_{IN} ≤ CV_{DD}/$X2V_{DD}$)	I_{IN}	—	±40	μA	2, 3
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	1.35	—	V	—
Output low voltage (I_{OL} = 6.0 mA)	V_{OL}	—	0.4	V	—

Note:

1 The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2 The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

3 eSPI1 is powered on CV_{DD}, SPI2 is on $X2V_{DD}$ (see Table 3).

2.9.2 eSPI1 AC Timing Specifications

This table provides the eSPI1 input and output AC timing specifications.

Table 30. eSPI1 AC Timing Specifications

For recommended operating conditions, see Table 3.

Characteristic	Symbol[1]	Min	Max	Unit	Note
eSPI outputs—Master data (internal clock) hold time	t_{NIKHOX}	0.5 + ($t_{PLATFORM\_CLK}$/2)	—	ns	2

Table 30. eSPI1 AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol[1]	Min	Max	Unit	Note
eSPI outputs—Master data (internal clock) delay	t_{NIKHOV}	—	6.0 + ($t_{PLATFORM\_CLK}$/2)	ns	2
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
eSPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
eSPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This figure provides the AC test load for eSPI1.

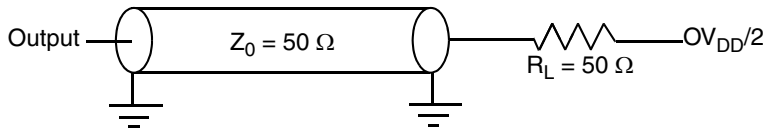


Figure 14. eSPI1 AC Test Load

This figure represents the AC timing from Table 30 in master mode (internal clock). Note that although the specifications are generally refer to the rising edge of the clock, Figure 14 also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI1.

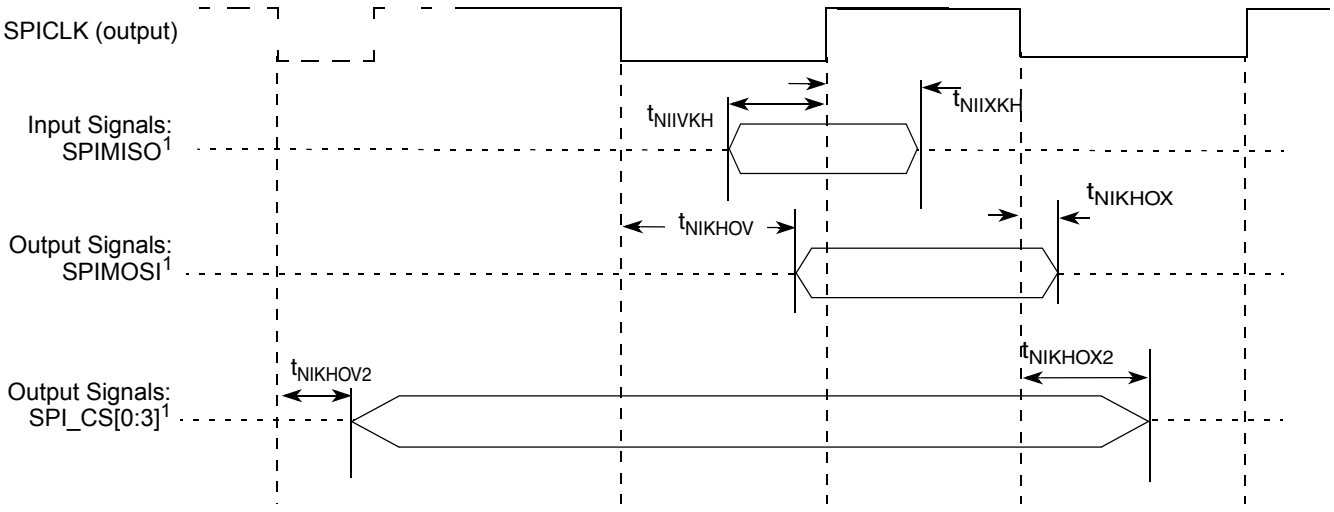


Figure 15. eSPI1 AC Timing in Master Mode (Internal Clock) Diagram

2.10 DUART

This section describes the DC and AC electrical specifications for the DUART interfaces.

2.10.1 DUART DC Electrical Characteristics

Table 31 and Table 33 provide the DC electrical characteristics for the two DUARTs on the device, which correspond to four UART interfaces. DUART1 is powered by OV_{DD}, while DUART2 is powered by the CV_{DD}.

This table provides the DC timing parameters for the DUART interface operating from a 3.3 V power supply.

Table 31. DUART DC Electrical Characteristics (OV_{DD}, CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN}/CV_{IN} = 0 V or OV_{IN}/CV_{IN} = OV_{DD}/CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD}/CV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD}/CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN}/CV_{IN} values found in Figure 3.
2. Note that the symbol OV_{IN}/CV_{IN} represents the input voltage of the supply. It is referenced in Figure 3.

This table provides the DC timing parameters for the DUART interface operating from a 1.8 V power supply.

Table 32. DUART DC Electrical Characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (CV_{IN} = 0 V or CV_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Figure 3.
2. Note that the symbol CV_{IN} represents the input voltage of the supply. It is referenced in Figure 3.

2.10.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 33. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Note:

1. CCB clock refers to the platform clock.
2. Actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.11 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for enhanced three-speed Ethernet10/100/1000 controller and MII management.

2.11.1 SGMII Interface Electrical Characteristics

For SGMII interface electrical characteristics, see Section 2.20, "High-Speed Serial Interface (HSSI) DC Electrical Characteristics."

2.11.2 MII Management

2.11.2.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V and 2.5 V. The DC electrical characteristics for MDIO and MDC are provided in Table 34 and Table 35.

Table 34. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.4	V	—

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

Table 35. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD},)	I_{IH}	—	10	μA	1, 2
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	—
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 3.

2.11.2.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 36. MII Management AC Timing Specifications

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16*t_{plb\_clk}) - 3$	—	$(16*t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the platform (CCB) clock.

This figure shows the MII management interface timing diagram.

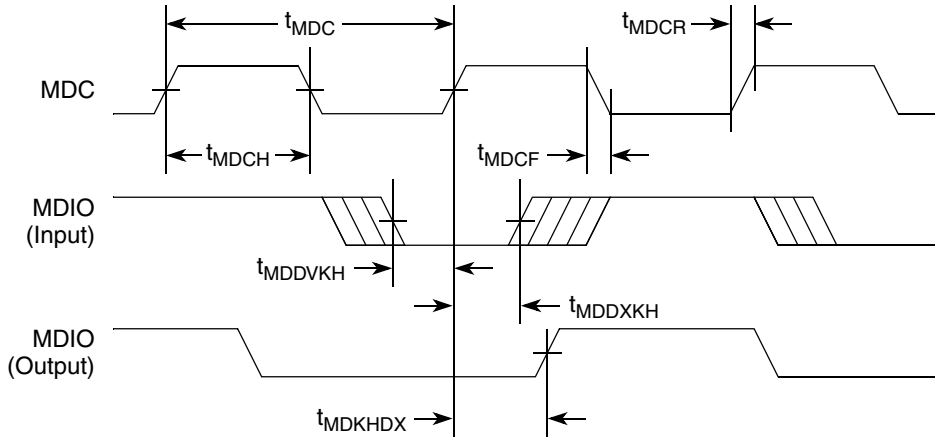


Figure 16. MII Management Interface Timing Diagram

2.11.3 eTSEC IEEE Std 1588 Electrical Specifications

2.11.3.1 eTSEC IEEE Std 1588 DC Specifications

This table shows IEEE Std 1588 DC electrical characteristics when operating at LV_{DD} = 3.3 V supply.

Table 37. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions with LV_{DD} = 3.3 V.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

This table shows the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 38. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—

Table 38. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V) (continued)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.11.3.2 eTSEC IEEE Std 1588 AC Specifications

This table provides the IEEE Std 1588 AC timing specifications.

Table 39. eTSEC IEEE 1588 AC Timing Specifications

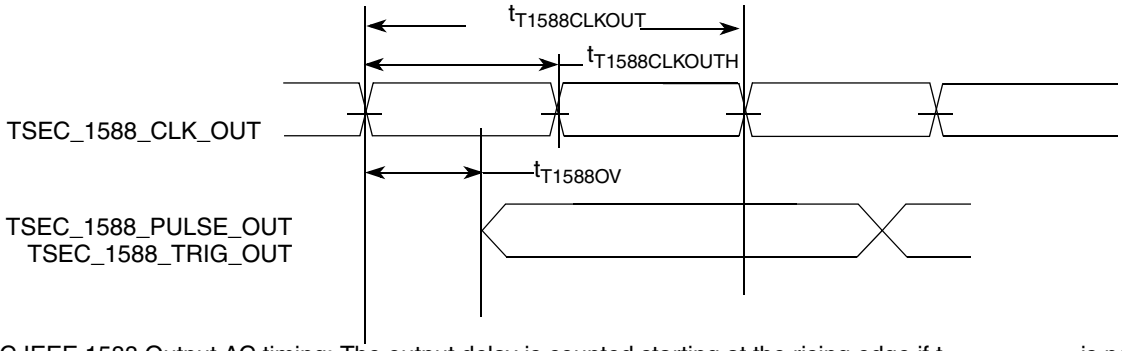
For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	5	—	T_{RX_CLK}*7	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns respectively.

Figure 17 shows the data and command output AC timing diagram.



1 eTSEC IEEE 1588 Output AC timing: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 17. eTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

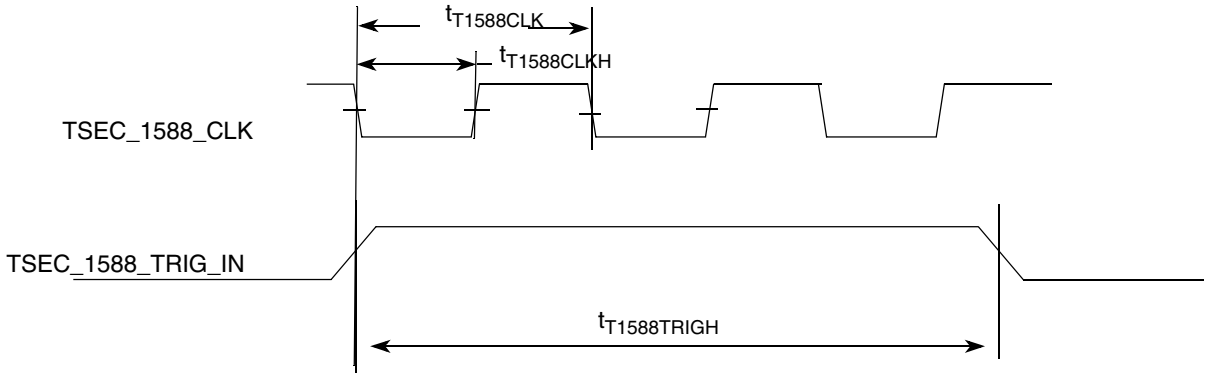


Figure 18. eTSEC IEEE 1588 Input AC Timing

2.12 USB

This section provides the AC and DC electrical specifications for the USB interface.

2.12.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the ULPI interface when operating at 3.3 V.

Table 40. USB DC Electrical Characteristics ($CV_{DD}/X2V_{DD}$ = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($CV_{IN}/X2V_{IN}$ = 0 V or $CV_{IN}/X2V_{IN}$ = $CV_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—

Table 40. USB DC Electrical Characteristics ($CV_{DD}/X2V_{DD}$ = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage ($CV_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol CV_{IN} and $X2V_{IN}$ represent the input voltage of the power supplies. See Table 3.

This table provides the DC electrical characteristics for the ULPI interface when operating at 1.8 V.

Table 41. USB DC Electrical Characteristics ($CV_{DD}/X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($CV_{IN}/X2V_{IN}$ = 0 V or $CV_{IN}/X2V_{IN}$ = $CV_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($CV_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

2.12.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 42. USB General Timing Parameters (ULPI Mode)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Table 42. USB General Timing Parameters (ULPI Mode) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 19 and Figure 20 provide the USB AC test load and signals, respectively.

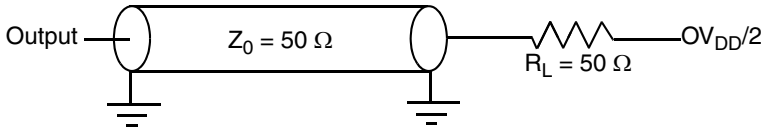


Figure 19. USB AC Test Load

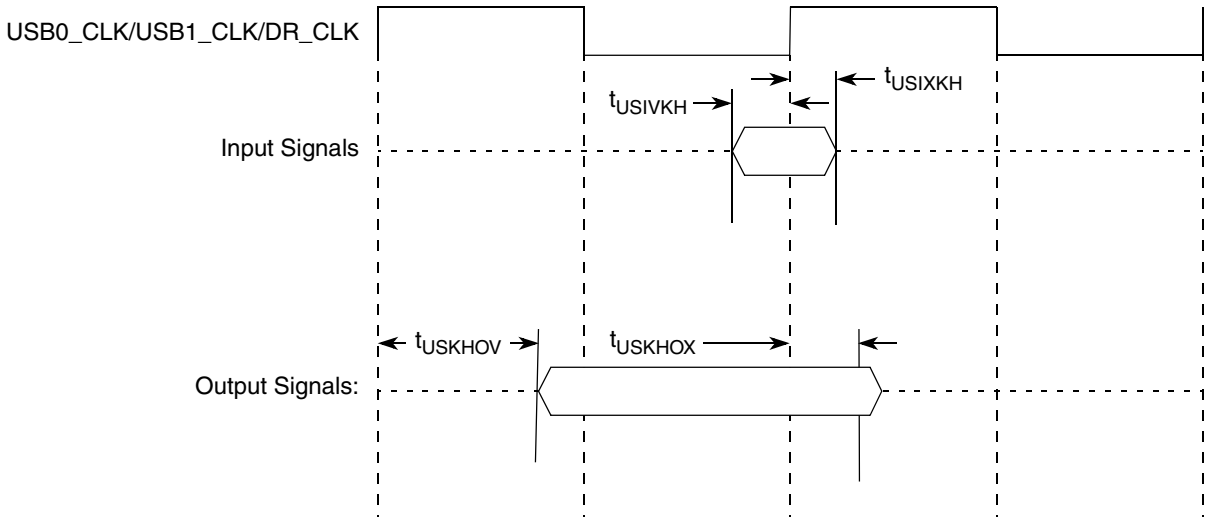


Figure 20. USB Signals

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 43. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	Steady state	$f_{USB\_CLK\_IN}$	59.97	60	60.03	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.05	0	0.05	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

2.13 Integrated Flash Controller (IFC)

This section describes the DC and AC electrical specifications for the integrated flash controller.

2.13.1 IFC DC Electrical Characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 3.3 V.

Table 44. Integrated Flash Controller DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 2.5 V.

Table 45. Integrated Flash Controller DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—

Table 45. Integrated Flash Controller DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 1.8 V.

Table 46. Integrated Flash Controller DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.13.2 IFC AC Timing Specifications

This section describes the AC timing specifications for the integrated flash controller.

2.13.2.1 Test Condition

This figure provides the AC test load for the integrated flash controller.

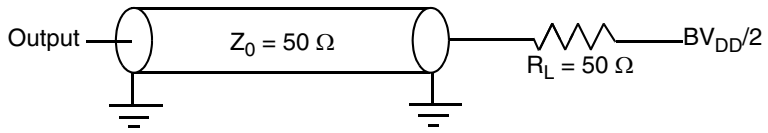


Figure 21. Integrated Flash Controller AC Test Load

2.13.2.2 IFC AC Timing Specifications

All output signal timings are relative to the falling edge of any IFC_CLK. The external circuit must use the rising edge of the IFC_CLKs to latch the data.

All input timings are relative to the rising edge of IFC_CLKs.

This table describes the timing specifications of the integrated flash controller interface.

Table 47. IFC Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
IFC_CLK cycle time	t_{IBK}	10	—	ns	—
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	—
Input setup	t_{IBIVKH}	4	—	ns	—
Input hold	t_{IBIXKH}	1	—	ns	—
Output delay	t_{IBKLOV}	—	1.5	ns	—
Output hold	t_{IBKLOX}	–2	—	ns	5, 6

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of IFC_CLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different IFC_CLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{IBONOT} is a measurement of the maximum time between the negation of ALE and any change in AD when FTIM0_CSn[TEAHC] = 0.
5. Here the negative sign means output transit happens earlier than the falling edge of IFC_CLK.
6. Here a convention has been followed in which the more negative/less-positive the number, the smaller the number would be. For example –2 is smaller then –1 and –1 is smaller then 0. So if the min value of this parameter is shown as –2 ns than the for any part parameter's measure will never go to –3ns though it can go to –1 ns.

This figure shows the AC timing diagram.

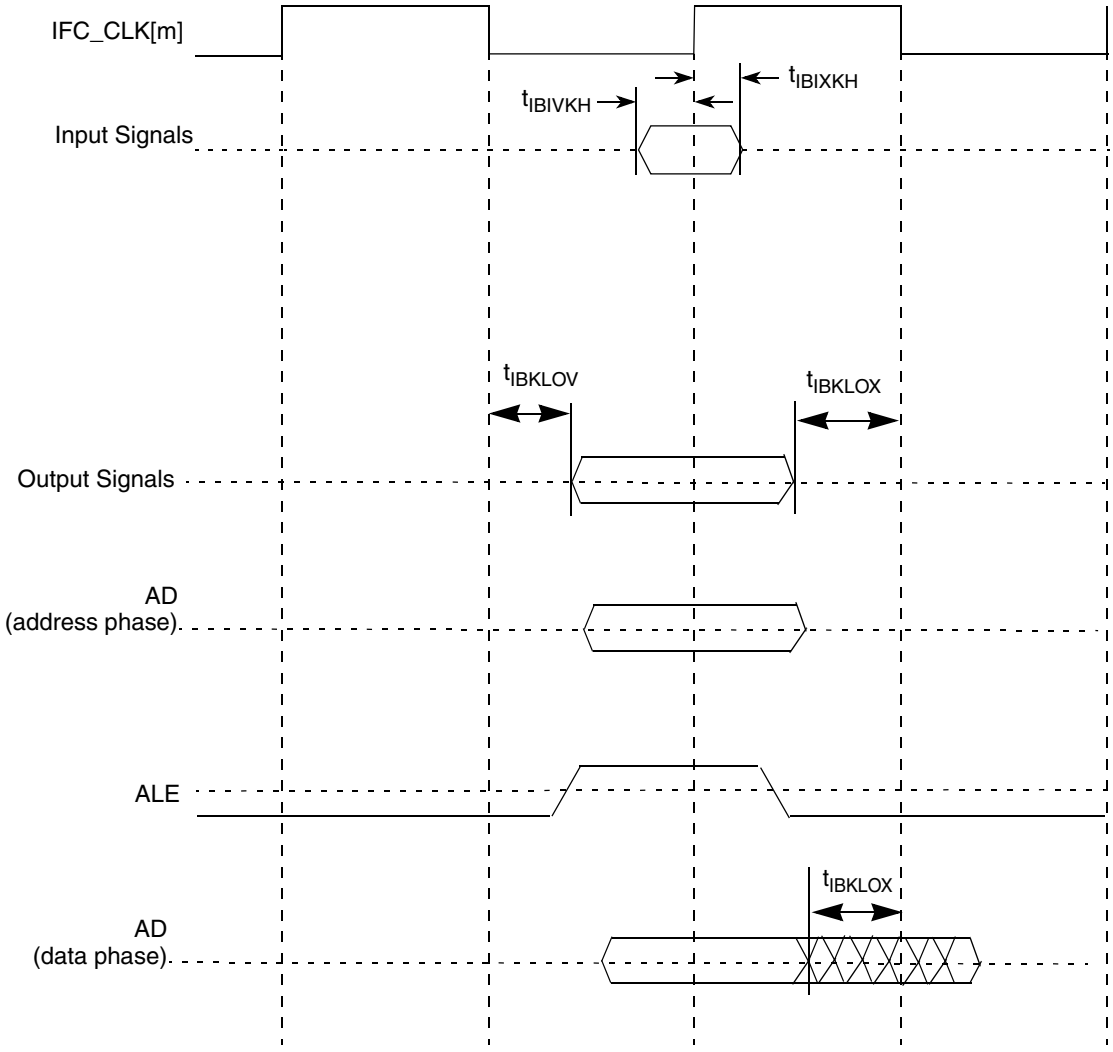
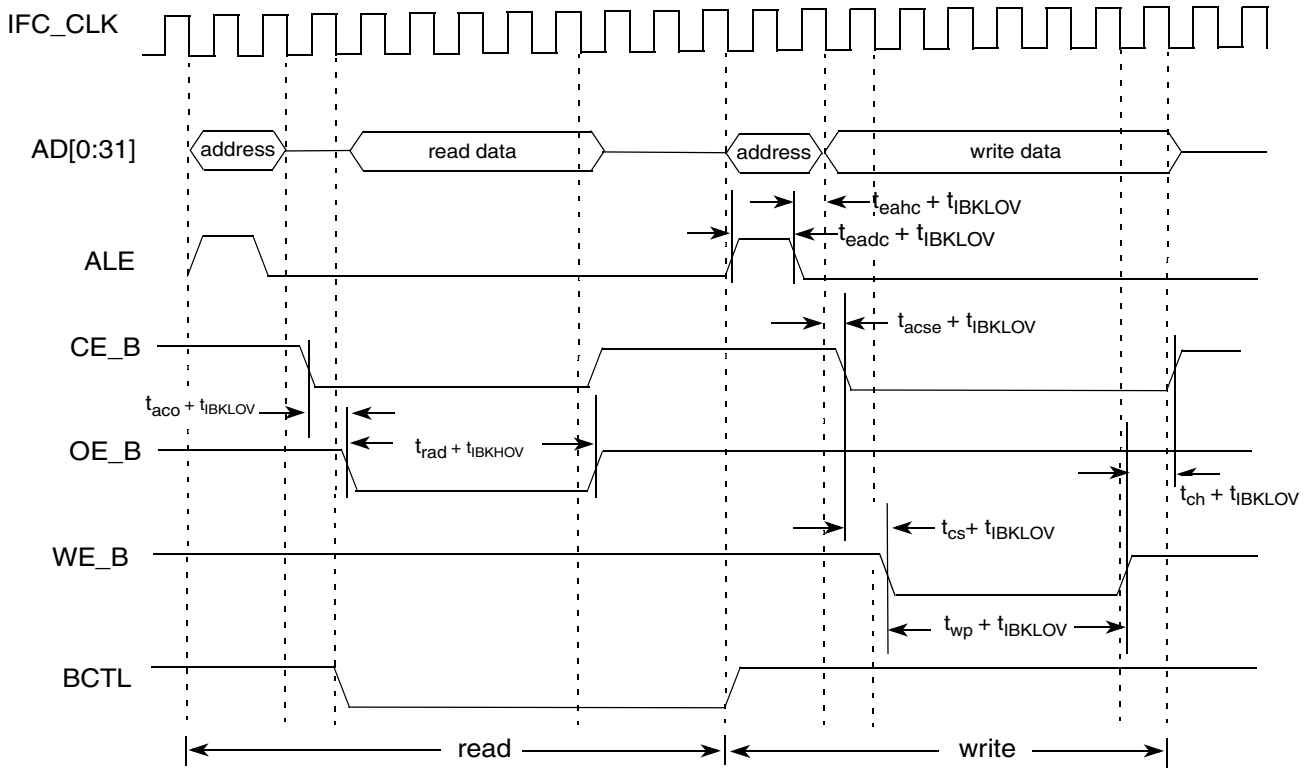


Figure 22. Integrated Flash Controller Signals

Figure 22 applies to all the controllers that IFC supports.

For input signals, the AC timing data is used directly for all controllers. For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

This figure shows how the AC timing diagram applies to GPCM. The same principle also applies to other controllers of IFC.



1 t_{aco}, t_{rad}, t_{eahc}, t_{eadc}, t_{acse}, t_{cs}, t_{ch}, t_{wp} are programmable. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual*.

2 For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

Figure 23. GPCM Output Timing Diagram

2.14 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.14.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 48. eSDHC Interface DC Electrical Characteristics

At recommended operating conditions with BV_{DD} = 3.3 V or 1.8 V.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × BV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × BV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 uA at BV_{DD} min	0.75 × BV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100uA at BV_{DD} min	—	0.125 × BV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 uA	BV_{DD} - 0.2	—	V	2

Table 48. eSDHC Interface DC Electrical Characteristics (continued)

At recommended operating conditions with BV_{DD} = 3.3 V or 1.8 V.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Figure 3.
2. Open drain mode for MMC cards only.

2.14.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in Figure 25.

Table 49. eSDHC AC Timing Specifications

At recommended operating conditions with BV_{DD} = 3.3 or 1.8 V

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SFSCK}	 0 0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SFSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SFSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx	$t_{SFSIVKH}$	2.5	—	ns	3, 4
Input hold times: SD_CMD, SD_DATx	$t_{SFSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SFSKHOV}$	—	3	ns	4
Output delay time: SD_CLK to SD_CMD, SD_DATx hold time	$t_{SFSKHOX}$	–3	—	ns	4

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
3. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1.5 ns.
4. CCARD ≤10 pF, (1 card), and CL = CBUS + CHOST + CCARD ≤ 40 pF

This figure provides the eSDHC clock input timing diagram.

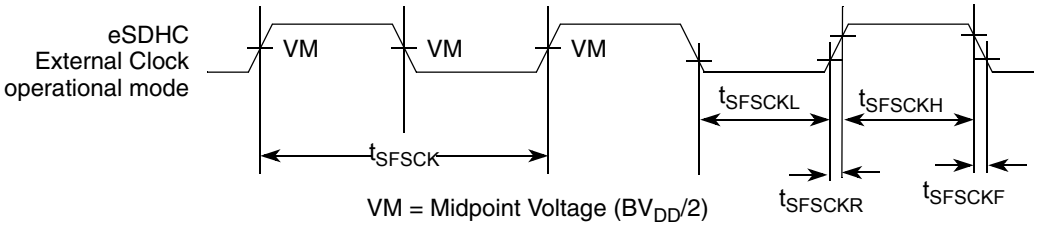


Figure 24. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

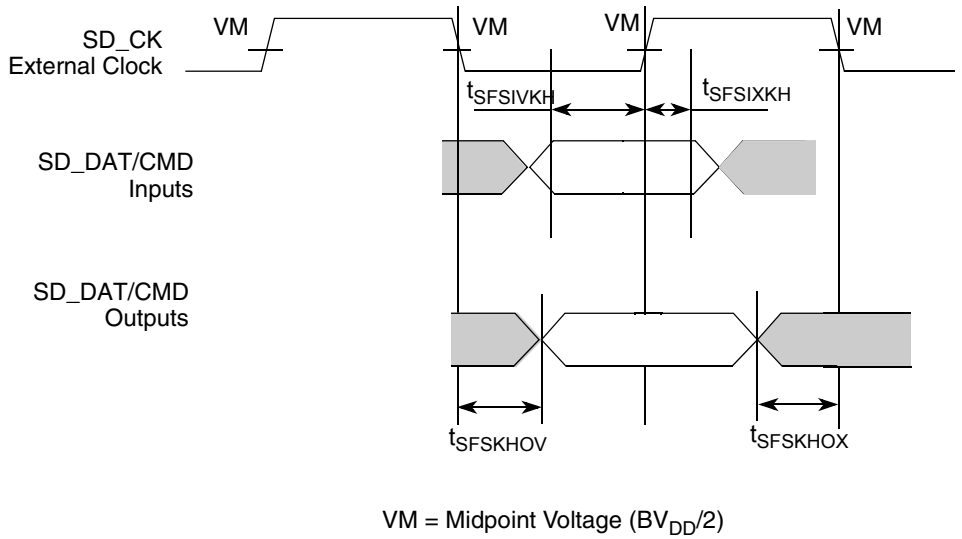


Figure 25. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.15 Programmable Interrupt Controller (PIC) Specifications

This section describes the DC and AC electrical specifications for the PIC.

2.15.1 PIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the PIC interface when operating at $CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = 3.3 V.

Table 50. PIC DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = 0V or $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN} = CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 50. PIC DC Electrical Characteristics (3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

This table provides the DC electrical characteristics for the PIC interface when operating at $LV_{DD}/OV_{DD}/BV_{DD}/CV_{DD}$ = 2.5 V.

Table 51. PIC DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current ($CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = 0V or $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = $CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

This table provides the DC electrical characteristics for the PIC interface when operating at $LV_{DD}/OV_{DD}/BV_{DD}/CV_{DD}$ = 1.8 V.

Table 52. PIC DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = 0V or $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = $CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—

Table 52. PIC DC Electrical Characteristics (1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

2.15.2 PIC AC Timing Specifications

This table provides the PIC input and output AC timing specifications.

Table 53. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs should be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.16 JTAG

This section describes the AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface. This section applies to both the Power Architecture and DSP JTAG ports. The BSC9132 has multiple JTAG topology; see Section 3.11, "JTAG Configuration Signals," for details.

2.16.1 JTAG DC Electrical Characteristics

This table provides the JTAG DC electrical characteristics.

Table 54. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.1	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.16.2 JTAG AC Timing Specifications

This table provides the JTAG AC timing specifications as defined in Figure 26 through Figure 29.

Table 55. JTAG AC Timing Specifications

For recommended operating conditions see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	2	ns	—
TRST_B assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times	t_{JTKLDV}	4	10	ns	3
Output hold times	t_{JTKLDX}	30	—	ns	3

Table 55. JTAG AC Timing Specifications (continued)

For recommended operating conditions see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
JTAG external clock to output high impedance	t_{JTKLDZ}	4	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs.

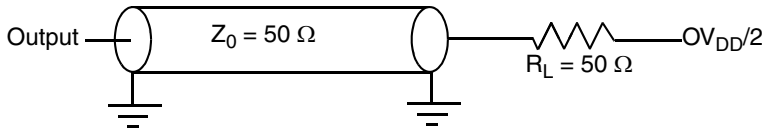


Figure 26. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

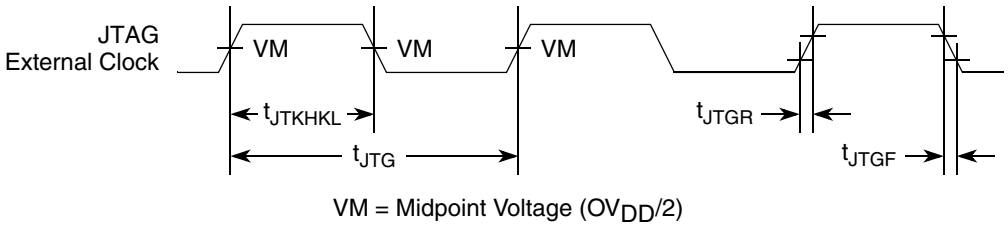


Figure 27. JTAG Clock Input Timing Diagram

This figure provides the TRST_B timing diagram.

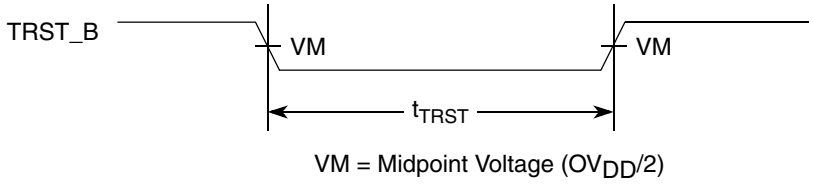


Figure 28. TRST_B Timing Diagram

This figure provides the boundary-scan timing diagram.

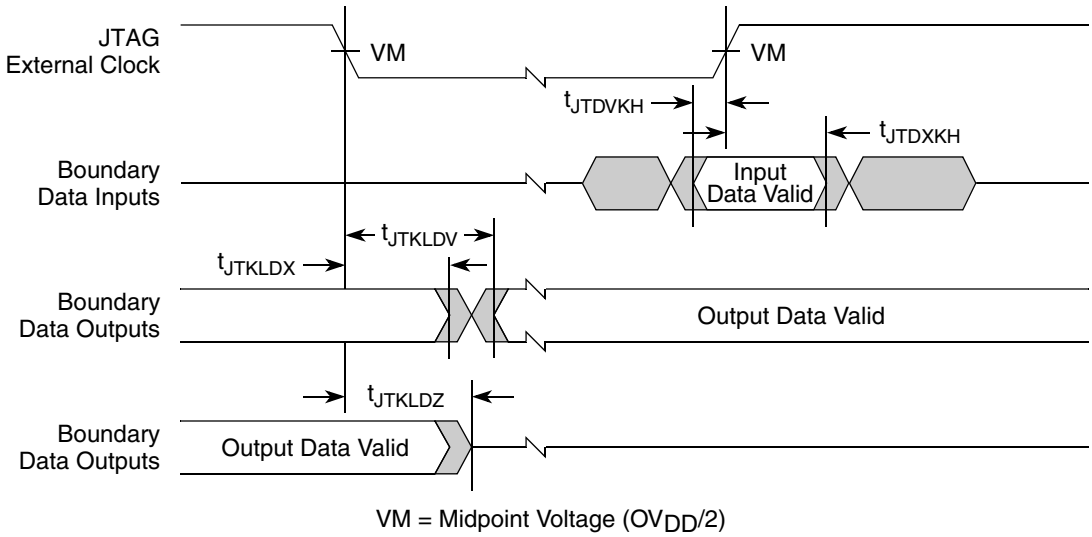


Figure 29. Boundary-Scan Timing Diagram

2.17 I²C

This section describes the DC and AC electrical characteristics for the two I²C interfaces. The input voltage for I²C1 is provided by a OV_{DD} (3.3 V) power supply, while the input voltage for I²C2 is provided by a CV_{DD} (3.3 V/1.8 V) power supply.

2.17.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interfaces operating from a 3.3 power supply.

Table 56. I²C DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

This table provides the DC timing parameters for the I^2C interface operating from a 1.8 V power supply.

Table 57. I^2C DC Electrical Characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (CV_{IN} = 0 V or CV_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Figure 3.
2. Note that the symbol CV_{IN} represents the input voltage of the supply. It is referenced in Figure 3.

2.17.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interfaces.

Table 58. I^2C AC Electrical Specifications

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 56)

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Table 58. I²C AC Electrical Specifications (continued)

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 56)

Parameter	Symbol[1]	Min	Max	Unit	Note

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the device acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919 referred to in note 4 below is recommended.
4. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

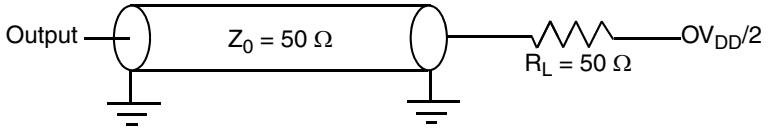


Figure 30. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

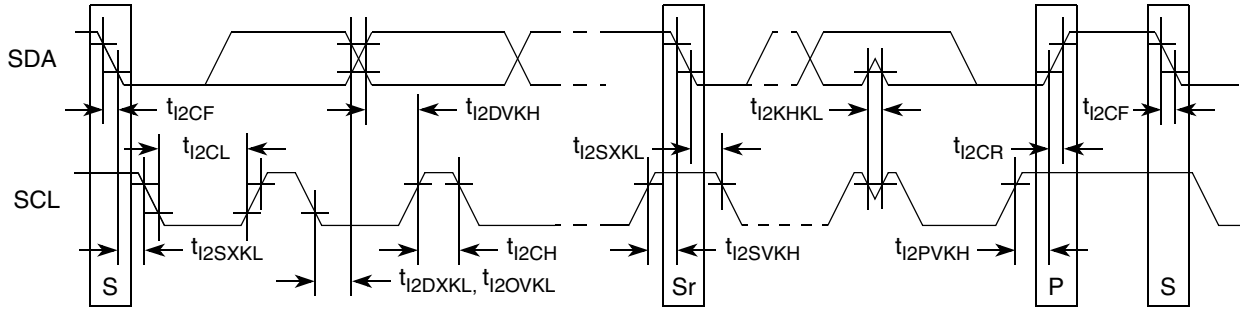


Figure 31. I²C Bus AC Timing Diagram

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface when operating from 3.3-V supply.

Table 59. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 2.5-V supply.

Table 60. GPIO DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OH}	1.7	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.7	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 1.8-V supply.

Table 61. GPIO DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Table 61. GPIO DC Electrical Characteristics (1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 62. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

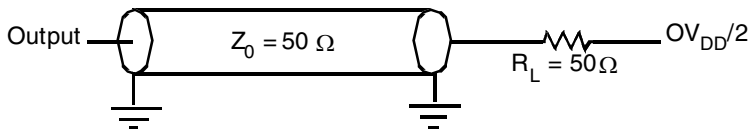


Figure 32. GPIO AC Test Load

2.19 TDM

This section describes the DC and AC electrical specifications for the TDM.

2.19.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics for the TDM interface when operating at 3.3 V.

Table 63. TDM DC Electrical Characteristics ($X2V_{DD}$ = 3.3 V)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	–0.3	0.8	V	1
Input current ($X2V_{IN}$ = 0 V or $X2V_{IN}$ = $X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage ($X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Table 63. TDM DC Electrical Characteristics ($X2V_{DD}$ = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max $X2V_{IN}$ respective values found in Table 3
2. Note that the symbol $X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3

This table provides the DC electrical characteristics for the TDM interface when operating at 1.8 V.

Table 64. TDM DC Electrical Characteristics ($X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($X2V_{IN}$ = 0 V or $X2V_{IN}$ = $X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max $X2V_{IN}$ respective values found in Table 3
2. Note that the symbol $X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3

2.19.2 TDM AC Electrical Characteristics

This table provides the input and output AC timing specifications for the TDM interface.

Table 65. TDM AC Timing Specifications for 62.5 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit	Note
TDMxRCK/TDMxTCK	t_{DM}	16.0	—	ns	3
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	7.0	—	ns	3
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	7.0	—	ns	3
TDM all input setup time	t_{DMIVKH}	3.6	—	ns	4, 5
TDMxRD input hold time	$t_{DMRDIXKH}$	1.9	—	ns	4, 8
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	1.9	—	ns	5
TDMxTCK high to TDMxTD output active	t_{DM_OUTAC}	2.5	—	ns	7
TDMxTCK high to TDMxTD output valid	$t_{DMTKHOV}$	—	9.8	ns	7, 9
TDMxTD hold time	$t_{DMTKHOX}$	2.5	—	ns	7
TDMxTCK high to TDMxTD output high impedance	t_{DM_OUTHI}	—	9.8	ns	7
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	9.25	ns	6
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.0	—	ns	6

Table 65. TDM AC Timing Specifications for 62.5 MHz[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Note

Note: Output values are based on 30 pF capacitive load.

Note: Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. t_{DMxTCK} and t_{DMxRCK} are shown using the rising edge.

1. All values are based on a maximum TDM interface frequency of 62.5 MHz.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the output internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. Relevant for all pins that function as TDM RX/TX clock—pins may be TDM_RCK and TDM_TCK, pending TDM port configuration.
4. Relevant for all pins that function as TDM receive data—pins may be TDM_RCK, TDM_RSN, TDM_RDT, TDM_TDT, pending TDM port configuration.
5. Relevant for all pins that function as TDM input frame sync (TX/RX)—pins may be TDM_TSN, TDM_RSN, pending TDM port configuration.
6. Relevant for all pins that function as TDM output frame sync (TX/RX)—pins may be TDM_TSN, TDM_RSN, pending TDM port configuration.
7. Relevant for all pins that function as TDM transmit data—pins may be TDM_RCK, TDM_RSN, TDM_RDT, TDM_TDT, pending TDM port configuration.
8. Applies to any TDM pin that functions as Rx data (including TDMxTD and others).
9. Represents the time from the positive clock edge to the valid data on the Tx data like; it applies to any TDM pin that functions as Tx data (including TDMxRD and others).

This figure shows the TDM receive signal timing.

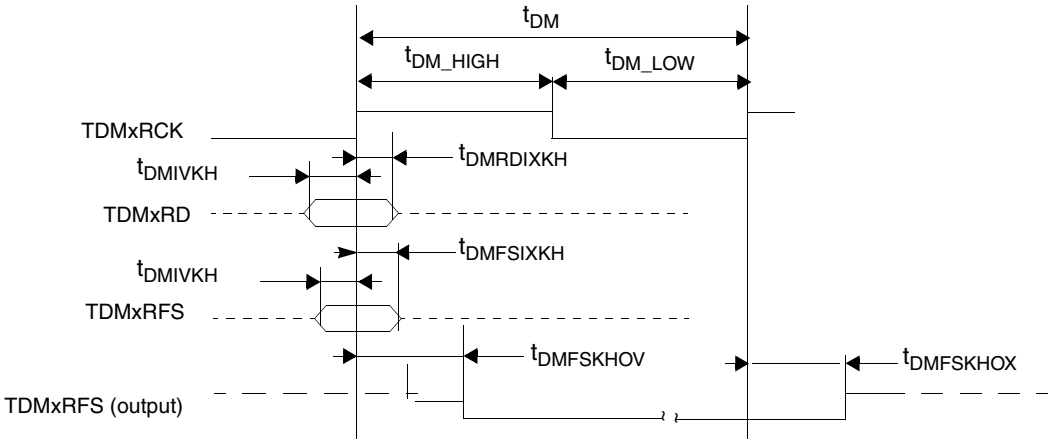


Figure 33. TDM Receive Signals

This figure shows the TDM transmit signal timing.

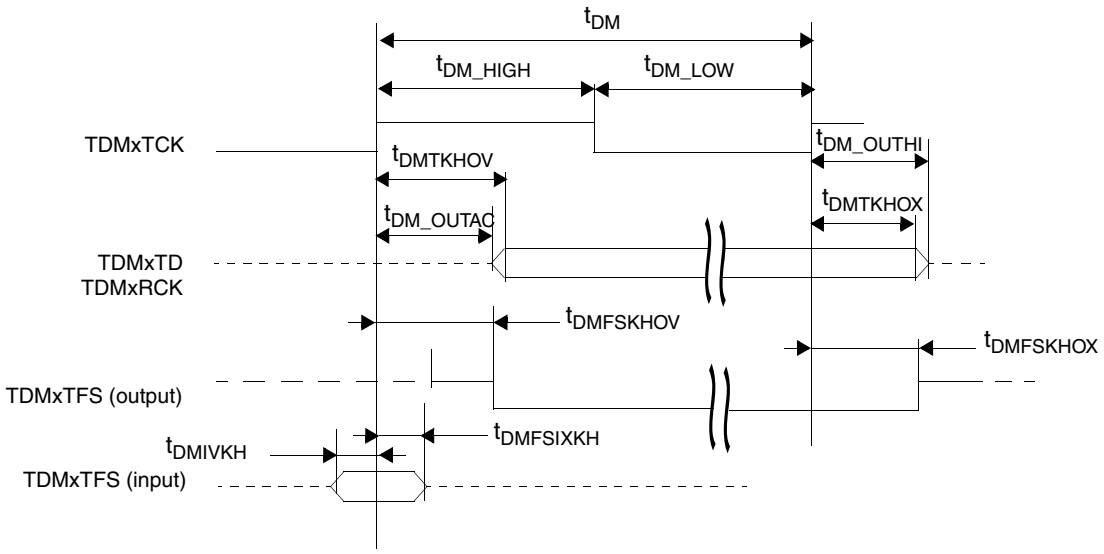


Figure 34. TDM Transmit Signals

This figure provides the AC test load for the TDM.

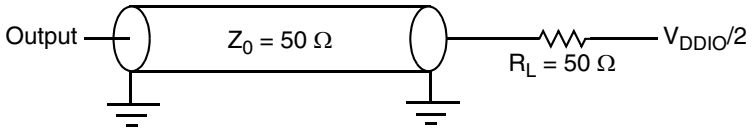


Figure 35. TDM AC Test Load

2.20 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The device features an HSSI that includes one 4-channel SerDes port (lanes 0 through 3) used for high-speed serial interface applications (PCI Express, CPRI, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the reset configuration word. Specific AC electrical characteristics are defined in Section 2.20.3, "HSSI AC Timing Specifications."

2.20.1 SerDes

2.20.1.1 SerDes Signal Term Definitions

The SerDes interface uses differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 36 shows how the signals are defined. Figure 36 shows the waveform for either a transmitter output (SD_TX[0:3] and SD_TX_B[0:3]) or a receiver input (SD_RX[0:3] and SD_RX_B[0:3]). Each signal swings between X volts and Y volts where X > Y.

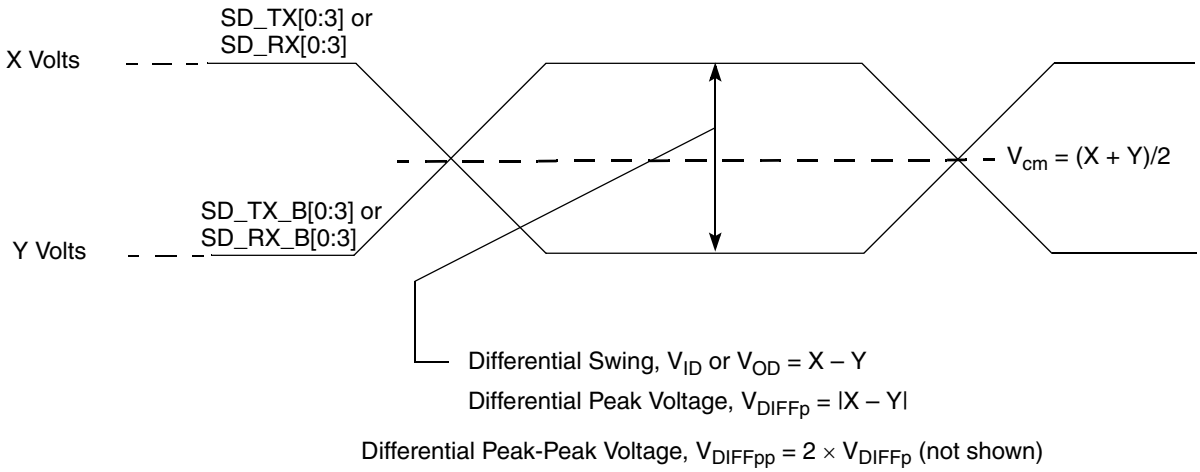


Figure 36. Differential Voltage Definitions for Transmitter/Receiver

This table lists the definitions based on this waveform. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

Table 66. Differential Signal Definitions

Term	Definition
Single-Ended Swing	The transmitter output signals and the receiver input signals SD_TX[0:3], SD_TX_B[0:3], SD_RX[0:3] and SD_RX_B[0:3] each have a peak-to-peak swing of X – Y volts. This is also referred to as each signal wire's single-ended swing.
Differential Output Voltage, VOD (or Differential Output Swing):	The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX[0:3]} - V_{SD\_TX\_B[0:3]}$. The V_{OD} value can be either positive or negative.
Differential Input Voltage, VID (or Differential Input Swing)	The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX[0:3]} - V_{SD\_RX\_B[0:3]}$. The V_{ID} value can be either positive or negative.
Differential Peak Voltage, V_{DIFFp}	The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |X– Y| volts.
Differential Peak-to-Peak, $V_{DIFFp-p}$	Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 × V_{DIFFp} = 2 × |(A – B)| volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 × |V_{OD}|.

Table 66. Differential Signal Definitions (continued)

Term	Definition
Differential Waveform	The differential waveform is constructed by subtracting the inverting signal (SD_TX_B[0:3], for example) from the non-inverting signal (SD_TX_B[0:3], for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 36 as an example for differential waveform.
Common Mode Voltage, V_{cm}	The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TX[0:3]} + V_{SD\_TX\_B[0:3]}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output differential swing (V_{OD}) has the same amplitude as each signal single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.1.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SD_REF_CLK1/SD_REF_CLK1_B or SD_REF_CLK2/SD_REF_CLK2_B. Figure 37 shows a receiver reference diagram of the SerDes reference clocks.

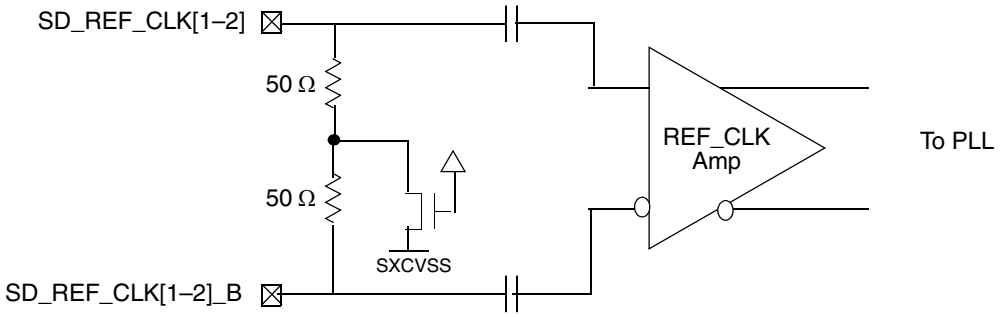


Figure 37. Receiver of SerDes Reference Clocks

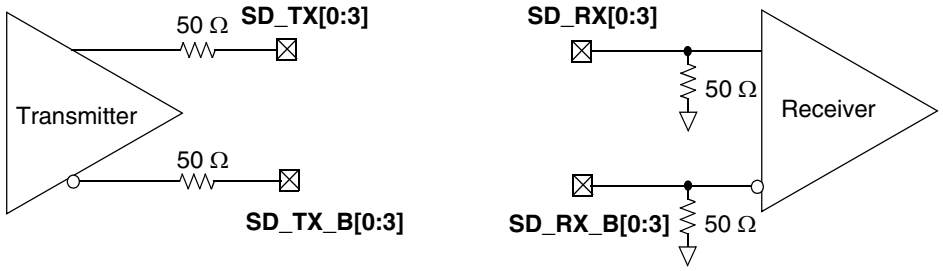
The characteristics of the clock signals are:

- The supply voltage requirements for $XCOREV_{DD}$ are as specified in Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK[1–2] and SD_REF_CLK[1–2]_B are internally AC-coupled differential inputs as shown in Figure 37. Each differential clock input (SD_REF_CLK[1–2] or SD_REF_CLK[1–2]_B has on-chip 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.

- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V / 50 = 8 mA) while the minimum common mode input level is 0.1 V above GND_{SXC}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK[1–2] and SD_REF_CLK[1–2]_B inputs cannot drive 50 Ω to GND_{SXC} DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in Section 2.20.2.1, "DC-Level Requirements for SerDes Reference Clocks."

2.20.1.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [0:3] indicates the specific SerDes lane. Actual signals are assigned by the RCW assignments at reset.

Figure 38. SerDes Transmitter and Receiver Reference Circuits

2.20.1.4 SerDes Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond that allowed by the specification. To offset a portion of these effects, equalization can be used. The following is a list of the most commonly used equalization techniques:

- Pre-emphasis on the transmitter.
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

2.20.2 HSSI DC Timing Specifications

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the CPRI data lines, and the SGMII data lines.

2.20.2.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 39 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

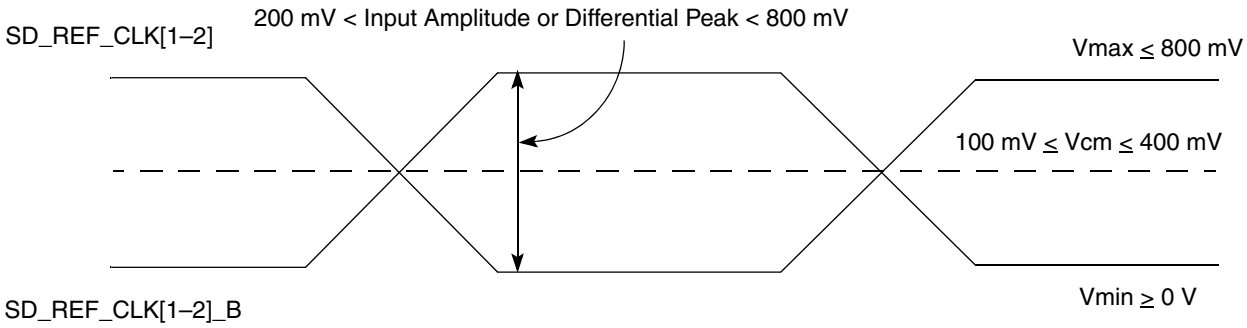


Figure 39. Differential Reference Clock Input DC Requirements (External DC-Coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC}. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC}. Figure 40 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

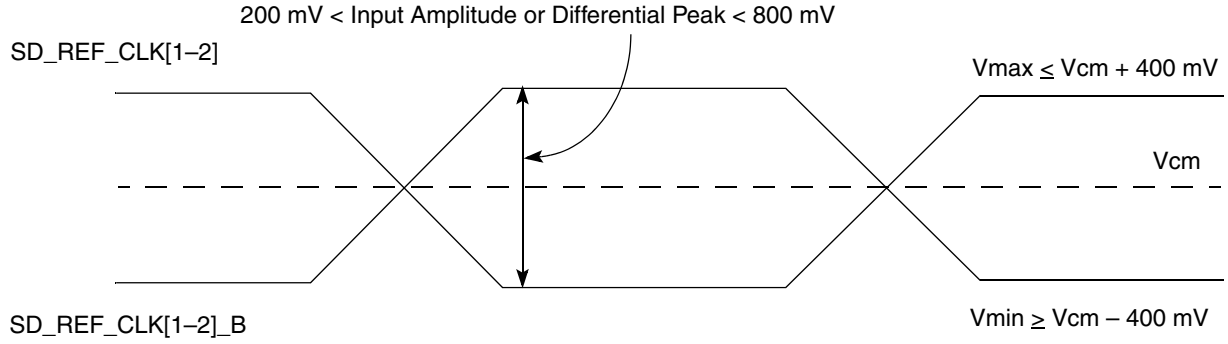


Figure 40. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The SD_REF_CLK[1–2] input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with SD_REF_CLK[1–2]_B either left unconnected or tied to ground.
  - The SD_REF_CLK[1–2] input average voltage must be between 200 and 400 mV. Figure 41 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD_REF_CLK[1–2]_B) through the same source impedance as the clock input (SD_REF_CLK[1–2]) in use.

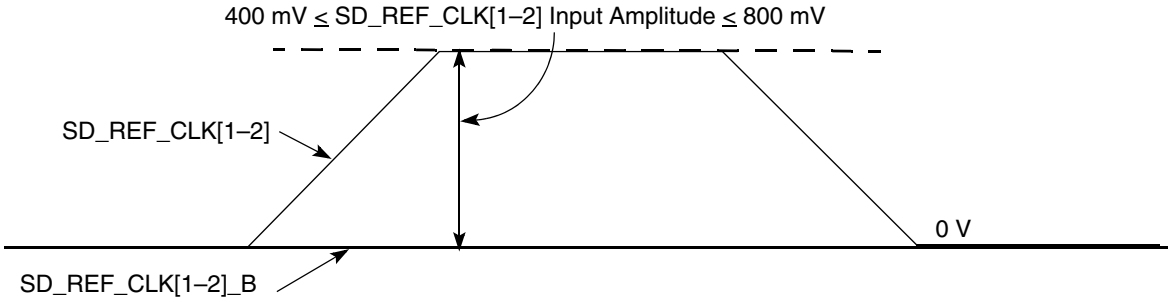


Figure 41. Single-Ended Reference Clock Input DC Requirements

2.20.2.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The BSC9132 supports a 2.5 Gbps and a 5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 2.0*. The transmitter specifications for 2.5 Gbps are defined in Table 67 and the receiver specifications are defined in Table 68. For 5 Gbps, the transmitter specifications are defined in Table 69 and the receiver specifications are defined in Table 1.

Note that specifications are valid at the recommended operating conditions listed in Table 3.

Table 67. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Differential peak-to-peak output voltage swing	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$, Measured at the package pins with a test load of 50 Ω to GND on each pin.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low Impedance
DC single-ended TX impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Table 68. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Note
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	5

Table 68. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Note

Note:

1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{–}}|$. Measured at the package pins of the receiver.

Table 69. PCI Express (5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Differential peak-to-peak output voltage swing	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \|V_{TX\text{-}D+} - V_{TX\text{-}D\text{–}}\|$, Measured at the package pins with a test load of 50 Ω to GND on each pin.
Low power differential peak-to-peak output voltage swing	$V_{TX\text{-}DIFFp\text{-}p\_low}$	400	500	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \|V_{TX\text{-}D+} - V_{TX\text{-}D\text{–}}\|$, Measured at the package pins with a test load of 50 Ω to GND on each pin.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
DC differential Tx impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Tx DC differential mode low impedance
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Table 1. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Note
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	—	175	mV	5

Table 1. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Note

Note:

1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D-}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D-}|$. Measured at the package pins of the receiver.

2.20.2.3 DC-Level Requirements for CPRI Configurations

This section provide various DC-level requirements for CPRI Configurations. Specifications are valid at the recommended operating conditions listed in Table 3.

Table 70. CPRI Transmitter DC Specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Output voltage	V_O	–0.40	—	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair.
Differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	L[0:3]TECR0[AMP_RED] = 0b000000.
Differential resistance	T_Rd	80	100	120	Ω	—

Note: LV is XAUI-based.

Table 71. CPRI Transmitter DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	800	—	1200	mV	L[0:3]TECR0[AMP_RED] = 0x000000
Differential resistance	T_Rd	80	100	120	Ω	—

Note: LV-II is CEI-6G-LR-based.

Table 72. CPRI Receiver DC Specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Differential input voltage	V_{IN}	200	—	1600	mVp-p	Measured at receiver.
Difference resistance	R_Rdin	80	—	120	Ω	—

Note: LV is XAUI-based.

Table 73. CPRI Receiver DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Input differential voltage	R_Vdiff	N/A	—	1200	mV	It is assumed that for the R_Vdiff min specification, that the eye can be closed at the receiver after passing the signal through a CEI/CPRI Level II LR compliant channel.
Differential resistance	R_Rdin	80	—	120	Ω	—

Note: LV-II is CEI-6G-LR-based.

2.20.2.4 DC-Level Requirements for SGMII Configurations

Table 74 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Specifications are valid at the recommended operating conditions listed in Table 3.

Table 74. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	500	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000000
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	459	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000010
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	417	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b000101
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	376	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001000

Table 74. SGMII DC Transmitter Electrical Characteristics (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	333	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001100
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	292	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001111
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	250	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b010011
Output impedance (single-ended)	R_O	40	50	60	Ω	—
Output high voltage	V_{OH}	—	—	1.5 × $\|V_{OD}$, max|	mV	—
Output low voltage	V_{OL}	$\|V_{OD}\|$, min/2	—	—	mV	—

Table 75 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 75. SGMII DC Receiver Electrical Characteristics[1,2]

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Input differential voltage[3]	$V_{RX\_DIFFp\text{-}p}$	100	—	1200	mV	L[0:3]GCR1[RECTL_SIGD] = 0b001
		175	—	1200	mV	L[0:3]GCR1[RECTL_SIGD] = 0b100
Loss of signal threshold[4]	VLOS	30	—	100	mV	L[0:3]GCR1[RECTL_SIGD] = 0b001
		65	—	175	mV	L[0:3]GCR1[RECTL_SIGD] = 0b100
Receiver differential input impedance	Z_{RX_DIFF}	80	—	120	Ω	—

Note:

1. The supply voltage is 1.0 V.
2. Input must be externally AC-coupled.
3. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
4. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the *PCI Express Specification* document. for details.

2.20.3 HSSI AC Timing Specifications

The following subsections define the AC timing requirements for the SerDes reference clocks, the PCI Express data lines, and the SGMII data lines.

2.20.3.1 AC-Level Requirements for SerDes Reference Clock

Table 76 lists AC requirements for the SerDes reference clocks.

Table 76. SD_REF_CLK[1–2] and SD_REF_CLK[1–2]_B Input Clock Requirements

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Note
SD_REF_CLK[1–2]/SD_REF_CLK[1–2]_B frequency range	t_{CLK_REF}	—	100/125 CPRI: 122.88	—	MHz	1
SD_REF_CLK[1–2]/SD_REF_CLK[1–2]_B clock frequency tolerance CPRI, SGMII PCI Express interface	t_{CLK_TOL}	 –100 –300	 — —	 100 300	 ppm ppm	—
SD_REF_CLK[1–2]/SD_REF_CLK[1–2]_B reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK[1–2]/SD_REF_CLK[1–2]_B max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK[1–2]/SD_REF_CLK[1–2]_B total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at ref_clk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/SD_REF_CLK_B rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD_REF_CLKn to falling edge rate)	Rise-Fall	—	—	20	%	5, 6

Note:

1. Only 100, 122.88, and 125 MHz have been tested. CPRI uses 122.88 MHz. The other interfaces use 100 or 125 MHz. Other values will not work correctly with the rest of the system.
2. Limits are from PCI Express CEM Rev 2.0.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLKn minus SD_REF_CLKn_B). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 42.
4. Measurement taken from differential waveform.
5. Measurement taken from single-ended waveform.
6. Matching applies to rising edge for SD_REF_CLKn and falling edge rate for SD_REF_CLKn_B. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLKn rising meets SD_REF_CLKn_B falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rising edge rate of SD_RF_CLKn should be compared to the falling edge rate of SD_REF_CLKn_B; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 43.
7. REF_CLK jitter must be less than 0.05 UI when measured against a Golden PLL reference. The Golden PLL must have a maximum baud rate bandwidth greater than 1667, with a maximum 20 dB/dec rolloff down to a baud rate of 16.67 with no peaking around the corner frequency.

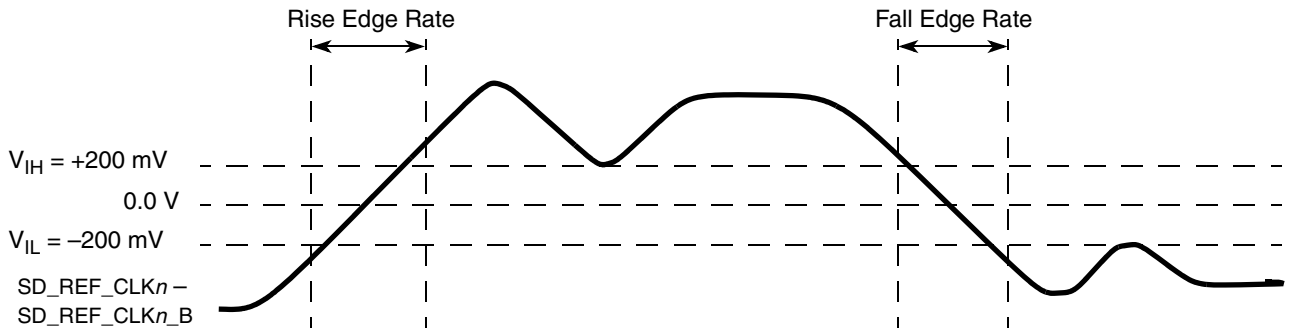


Figure 42. Differential Measurement Points for Rise and Fall Time

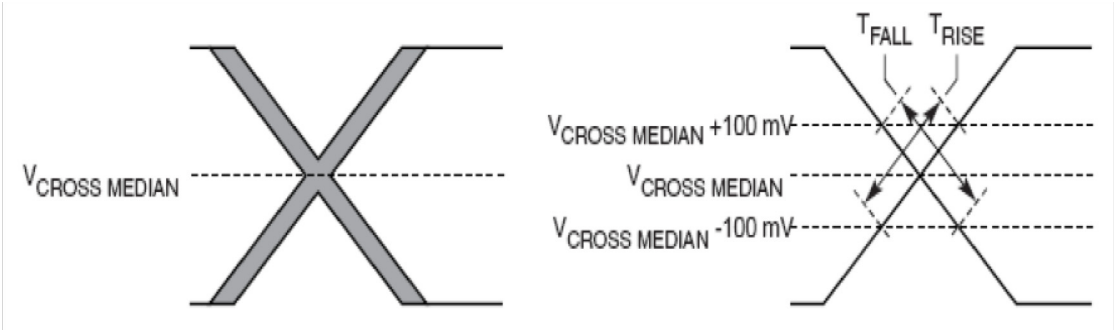


Figure 43. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.3.2 Spread Spectrum Clock

SD_REF_CLK[1–2] and SD_REF_CLK[1–2]_B were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have the same reference clock and the industry protocol supports it. For better results, use a source without significant unintended modulation.

2.20.3.3 PCI Express AC Physical Layer Specifications

The AC requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The BSC9132 supports a 2.5 Gbps or a 5.0 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 2.0*. The 2.5 Gbps transmitter specifications are defined in Table 77 and the receiver specifications are defined in Table 78. The 5.0 Gbps transmitter specifications are defined in Table 79 and the receiver specifications are defined in Table 80. The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

Table 77. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.

Table 77. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. This does not include spread spectrum or REF_CLK jitter. It includes device random jitter at 10^{-12}. See notes 2 and 3.
Time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage test load as shown in Figure 47 and measured over any 250 consecutive Tx UIs.

3 A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-NAX-JITTER} = 0.25$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4 The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 78. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2, 3, and 4.

Table 78. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Comments

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 47 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3 A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4 It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 79. PCI Express 2.0 (5.0 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage test load as shown in Figure 47 and measured over any 250 consecutive Tx UIs.

3 A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER}$ = 0.25 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4 The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 80. PCI Express 2.0 (5.0 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 400 ps ±300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Max Rx inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common REF_CLK Rx architecture
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-TJ-DC}$	—	—	0.34	UI	Max Rx inherent total timing error
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common REF_CLK Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common REF_CLK Rx architecture

Note: No test load is necessarily accosted with this value.

2.20.3.4 CPRI AC Timing Specifications

Table 81 defines the transmitter AC specifications for the CPRI LV lanes. The AC timing specifications do not include REF_CLK jitter.

Table 81. CPRI Transmitter AC Timing Specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Nom	Max	Unit
Deterministic Jitter	JD	—	—	0.17	UI p-p
Total Jitter	JT	—	—	0.35	UI p-p
Unit Interval: 1.2288 GBaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	µs
Unit Interval: 2.4576 GBaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	µs
Unit Interval: 3.072 GBaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	µs

Table 82 defines the transmitter AC specifications for the CPRI LV-II lanes. The AC timing specifications do not include REF_CLK jitter.

Table 82. CPRI Transmitter AC Timing Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Nom	Max	Unit
Uncorrelated High Probability Jitter	T_UHPJ	—	—	0.15	UI p-p
Total Jitter	T_TJ	—	—	0.30	UI p-p
Unit Interval: 1.2288 GBaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	µs
Unit Interval: 2.4576 GBaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	µs
Unit Interval: 3.072 GBaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	µs

Table 82. CPRI Transmitter AC Timing Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Nom	Max	Unit
Unit Interval: 4.9152 GBaud	UI	1/4915.2 – 100ppm	1/4915.2.8	1/4915.2 + 100ppm	µs
Unit Interval: 6.144 GBaud	UI	1/6144.0 – 100ppm	1/6144.0	1/6144.0 + 100ppm	µs

Table 83 defines the Receiver AC specifications for CPRI LV. The AC timing specifications do not include REF_CLK jitter.

Table 83. CPRI Receiver AC Timing Specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Nom	Max	Unit
Deterministic jitter tolerance	JD	—	—	0.37	UI p-p
Combined deterministic and random jitter tolerance	JDR	—	—	0.55	UI p-p
Total Jitter tolerance	JT	—	—	0.65	UI p-p
Unit Interval: 1.2288 GBaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	ps
Unit Interval: 2.4576 GBaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	ps
Unit Interval: 3.072 GBaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	ps
Bit error ratio	BER	—	—	10^{-12}	—

Table 84 defines the Receiver AC specifications for CPRI LV-II. The AC timing specifications do not include REF_CLK jitter.

Table 84. CPRI Receiver AC Timing Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Nom	Max	Unit
Gaussian	R_GJ	—	—	0.275	UI p-p
Uncorrelated bounded high probability jitter	R_UBHPJ	—	—	0.150	UI p-p
Correlated bounded high probability jitter	R_CBHPJ	—	—	0.525	UI p-p
Bounded high probability jitter	R_BHPJ	—	—	0.675	UI p-p
Sinusoidal jitter, maximum	R_SJ-max	—	—	5.000	UI p-p
Sinusoidal jitter, high frequency	R_SJ-hf	—	—	0.050	UI p-p
Total Jitter (does not include sinusoidal jitter).	R_TJ	—	—	0.950	UI p-p
Unit Interval: 1.2288 GBaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	µs
Unit Interval: 2.4576 GBaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	µs
Unit Interval: 3.072 GBaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	µs
Unit Interval: 4.9152 GBaud	UI	1/4915.2 – 100ppm	1/4915.2.8	1/4915.2 + 100ppm	µs
Unit Interval: 6.144 GBaud	UI	1/6144.0 – 100ppm	1/6144.0	1/6144.0 + 100ppm	µs

Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 46. The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PC trace.

NOTE

The intended application is a point-to-point interface up to two connectors. The maximum allowed total loss (channel + interconnects + other loss) is 20.4 dB @ 6.144 Gbps.

2.20.3.5 SGMII AC Timing Specifications

Table 85 provides the SGMII transmit AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 85. SGMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Unit interval	UI	800 – 100ppm	800	800 + 100ppm	pS	± 100ppm
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	—
AC coupling capacitor	CTX	75	—	200	nF	All transmitters must be AC-coupled
Note: The AC specifications do not include REF_CLK jitter.						

Table 86 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 86. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Unit interval	UI	800 – 100ppm	800	800 + 100ppm	pS	± 100ppm
Deterministic jitter tolerance	JD	—	—	0.37	UI p-p	Measured at receiver.
Combined deterministic and random jitter tolerance	JDR	—	—	0.55	UI p-p	Measured at receiver
Total jitter tolerance	JT	—	—	0.65	UI p-p	Measured at receiver
Bit error ratio	BER	—	—	10^{-12}	—	—

Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region shown in Figure 44 or Figure 45.

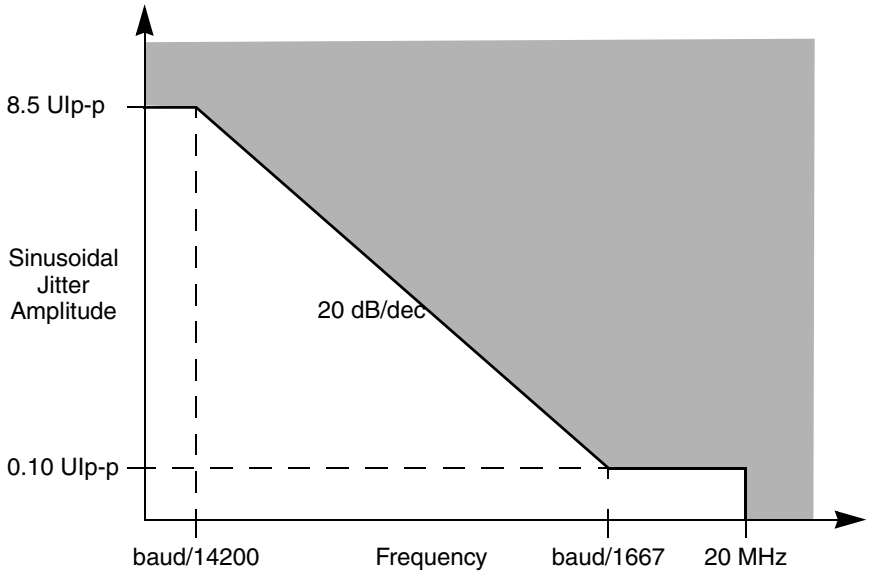


Figure 44. Single Frequency Sinusoidal Jitter Limits for Baud Rate <3.125 Gbps

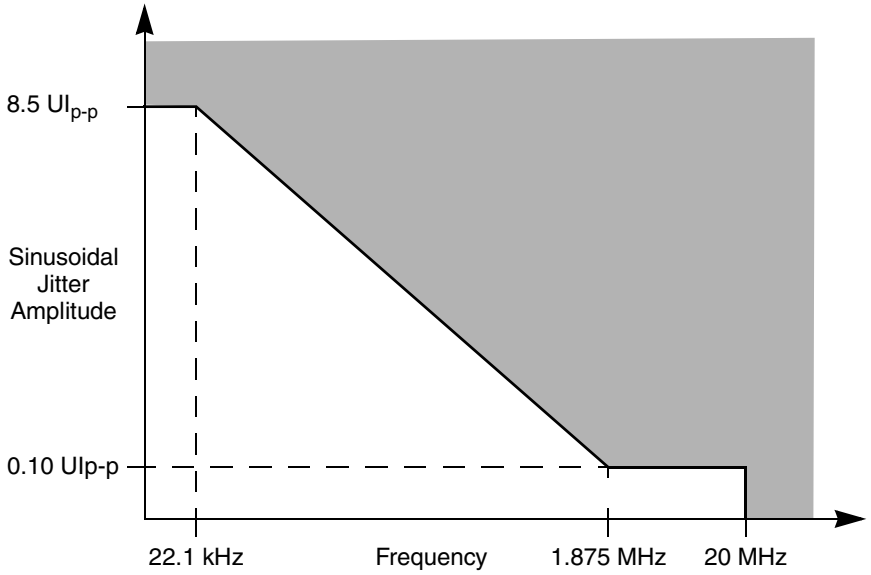


Figure 45. Single Frequency Sinusoidal Jitter Limits for Baud Rate 3.125 Gbps

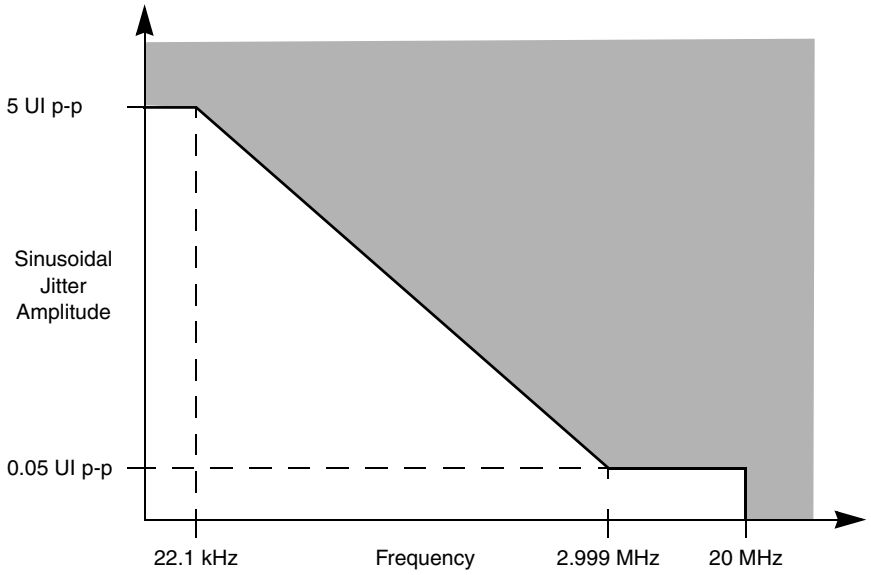


Figure 46. Single Frequency Sinusoidal Jitter Limits for Baud Rate 5.0 Gbps

2.20.3.6 Compliance Test and Measurement Load

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and SD_TX_B*n*) or at the receiver inputs (SD_RX*n* and SD_RX*n*_B). The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 47.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

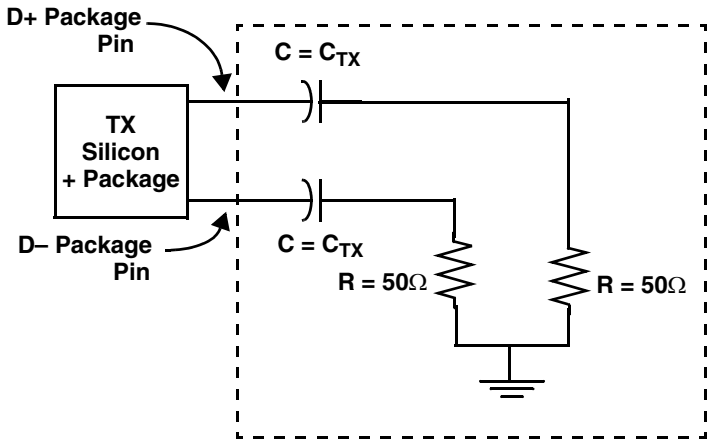


Figure 47. Compliance Test/Measurement Load

2.21 Radio Frequency (RF) Interface

2.21.1 RF Parallel Interface

The BSC9132 has an RF parallel interface.

2.21.1.1 RF Parallel Interface DC Electrical Characteristics (eSPI2)

2.21.1.1.1 RF Parallel Interface DC Data Path

Table 87 provides the DC electrical characteristics for the RF parallel interface when operating at 3.3 V.

Table 87. RF Parallel Interface DC Electrical Characteristics ($X1V_{DD}$, $X2V_{DD}$ = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($X1V_{IN}/X2V_{IN}$ = 0 V or $X1V_{IN}/X2V_{IN}$ = $X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage ($X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $X1V_{IN}/X2V_{IN}$ represent the input voltage of the power supplies. It is referenced in Table 3.

Table 88 provides the DC electrical characteristics for the RF interface when operating at 1.8 V.

Table 88. RF Parallel Interface DC Electrical Characteristics ($X1V_{DD}$, $X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($X1V_{IN}/X2V_{IN}$ = 0 V or $X1V_{IN}/X2V_{IN}$ = $X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

2.21.1.1.2 RF Parallel Interface DC Control Plane

See Table 29 in Section 2.9.1, "eSPI1 DC Electrical Characteristics," for the DC specs for eSPI2, powered by $X2V_{DD}$ = 1.8 V.

2.21.1.2 RF Parallel Interface AC Electrical Characteristics (eSPI2)

2.21.1.2.1 RF Parallel AC Data Interface

Table 89 provides the timing specifications for the RF parallel interface.

Table 89. RF Parallel Interface Timing Specification (3.3 V, 1.8 V)[1,2]

Parameter	Symbol	Min	Max	Unit	Note
Data_clk (MCLK) clock period	t_{PDCP}	16.276 (61.44)	—	ns (MHz)	—
Data_clk (MCLK) and fb_clk (FCLK) pulse width	t_{PDMP}	45% of t_{PDCP}	—	—	—
Delay between MCLK and FCLK at the external RFIC including trace delay	t_{PDCD}	—	7.32	ns	—
MCLK input to FCLK output delay at the BSC9132 BBIC	t_{PDMFD}	—	6.32	ns	—
Control/Data output valid time wrt FCLK during Tx from the BSC9132 BBIC	t_{PDOV}	—	6.0	ns	—
Control/Data hold from FCLK during Tx from the BSC9132 BBIC	t_{PDOX}	1.37	—	ns	3
Control/Data setup wrt MCLK	t_{PDIV}	2.5	—	ns	—
Control/Data hold wrt MCLK	t_{PDIX}	0.4	—	ns	—

Note:

1 The max trace delay of MCLK from the external RFIC to the BSC9132 BBIC and FCK/TXNRX/ENABLE from BBIC to RFIC = 1 ns each.

2 The max allowable trace skew between MCLK/FCLK and the respective data/control is 70 ps.

3 1.37 ns includes 70 ps trace skew.

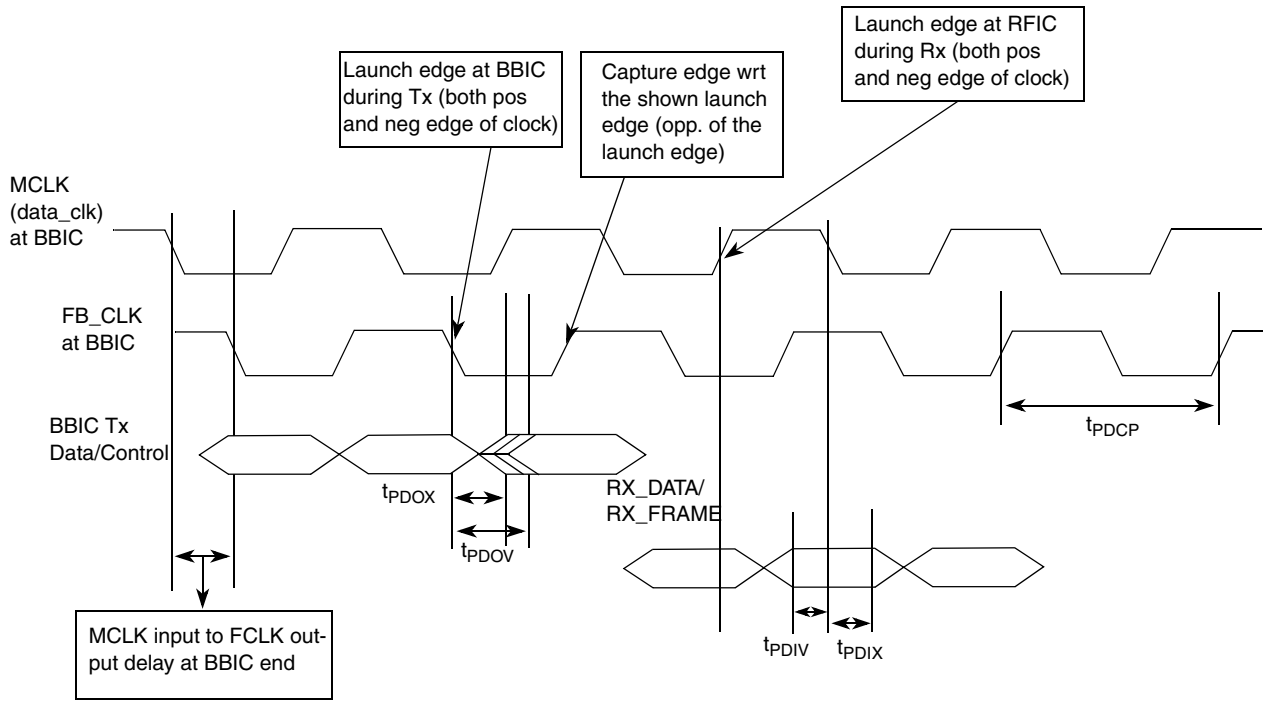


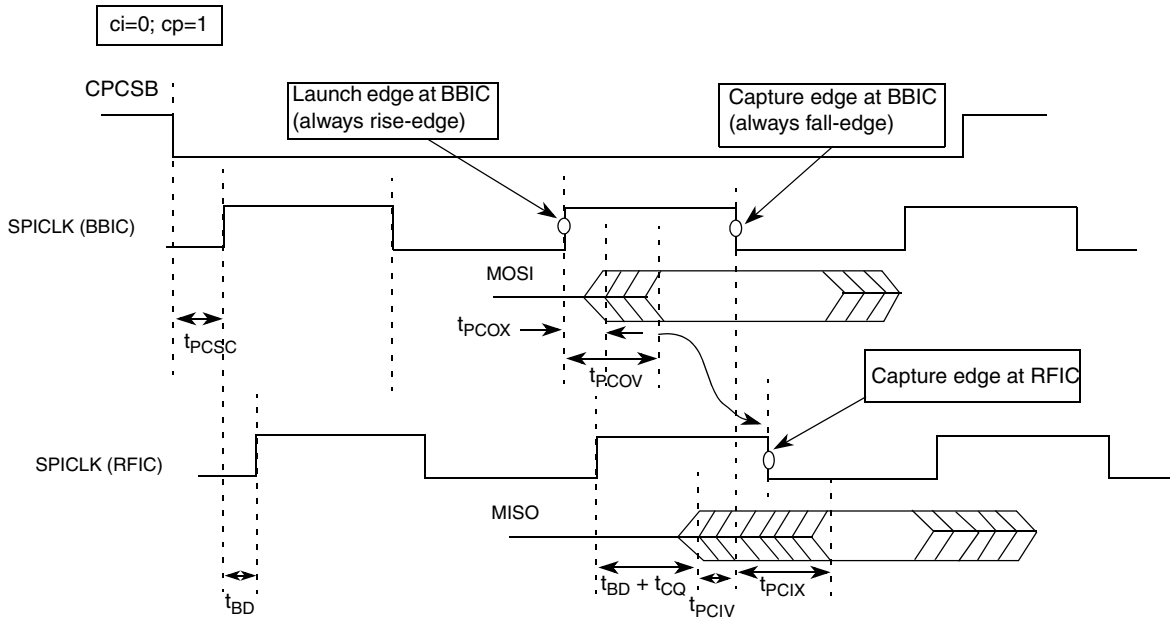
Figure 48. RF Parallel Interface AC Timing Diagram

2.21.1.2.2 RF Parallel Interface AC Control Plane

Table 90. RF Parallel Control Plane Interface AC Timing Specification

Parameter	Symbol	Min	Max	Unit
Control plane clock period	t_{PCCP}	33.3 (30)	—	ns (MHz)
Clock min pulse width	t_{PCMP}	16.6	—	ns
PCB trace delay between the BSC9132 BBIC master and the external RFIC slave	t_{PCBD}	—	1	ns
Setup time from CPCSB assertion to first rising edge of SPICLK	t_{PCSC}	6.1	—	ns
Hold time from last SPICLK falling edge to CPCSB deassertion	t_{PCHC}	9.9	—	ns
MOSI data output setup time against SPICLK	t_{PCOV}	—	15.4	ns
MOSI data ouptut hold time against SPICLK	t_{PCOX}	–16.4	—	ns
MISO data input setup time against SPICLK	t_{PCIV}	7.9	—	ns
MISO data input hold time against SPICLK	t_{PCIX}	21.9	—	ns

Note: RF parallel control plane is SPI2.



t_{BD}: Board delay from the BSC9132 BBIC to the external RFIC or back
t_{CQ}: Delay in RFIC from input of SPICLK to output valid data
Max permissible board skew: 100 ps
Proposed frequency of SPICLK: 30 MHz

Data timing at RF parallel interface:
Input data setup requirement: 1 ns
Input data hold requirement: 0 ns
t_{CQ}: 4.5 ns–6.5 ns (6.5 ns is critical, which defines the max frequency)

Figure 49. RF Parallel Control Plane Interface AC Timing Diagram

2.22 Universal Subscriber Identity Module (USIM)

The USIM module interface consist of a total of five pins. Only “Internal One Wire” interface mode is supported. In this mode, the Rx input of the USIM IP is connected to the TX output of the USIM, which is internal to the device. Only one bidirectional signal (Rx/Tx) is routed to the device pin, which is connected to the external SIM card.

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the Rx/Tx pins; however, the SIM module can work with CLK equal to 16 times the data rate on Rx/Tx pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card will be used by the SIM card to recover the clock from the data much like a standard UART. All five pins of SIM module are asynchronous to each other.

There are no required timing relationships between the pads in normal mode, The SIM card is initiated by the interface device, whereupon the SIM card will send a response with an Answer to Reset. Although the SIM interface has no specific requirement, the ISO-7816 specifies reset and power down sequences. For detailed information, see ISO-7816.

The USIM interface pins are available at two locations. At one location, it is multiplexed with eSDHC and TDM functionality and is powered by the BVDD power supply (3.3V/2.5V/1.8V). At the other location, it is multiplexed with eSPI and UART functionality and is powered by CVDD power supply (3.3V/1.8V).

2.22.1 USIM DC Electrical Characteristics

This table provides the DC electrical characteristics for the USIM interface.

Table 91. USIM Interface DC Electrical Characteristics

At recommended operating conditions with BV_{DD} = 3.3 V/2.5 V/1.8 V.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × BV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × BV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 uA at BV_{DD}min	0.75 × BV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100uA at CV_{DD}min	—	0.125 × BV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 uA	BV_{DD} - 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Figure 3.
2. Open drain mode for SIM cards only.

2.22.2 USIM General Timing Requirements

The timing requirements for the USIM are found in Table 92.

Table 92. USIM Timing Specification, High Drive Strength

Parameter	Symbol	Min	Max	Unit	Note
USIM clock frequency (SIM_CLK)	S_{freq}	0.01	25	MHz	1
USIM clock rise time (SIM_CLK)	S_{rise}	—	0.09 × (1/S_{freq})	ns	2
USIM clock fall time (SIM_CLK)	S_{fall}	—	0.09* × 1/S_{freq})	ns	2
USIM input transition time (SIM_TRXD, SIM_PD)	S_{trans}	10	25	ns	—
USIM I/O rise time / fall time (SIM_TRXD)	Tr/Tf	—	1	µs	3
USIM RST rise time / fall time (SIM_RST)	Tr/Tf	—	1	µs	4

Note:

1 50% duty cycle clock
2 With C = 50 pF
3 With CIN = 30 pF, COUT = 30 pF
4 With C_{IN} = 30 pF

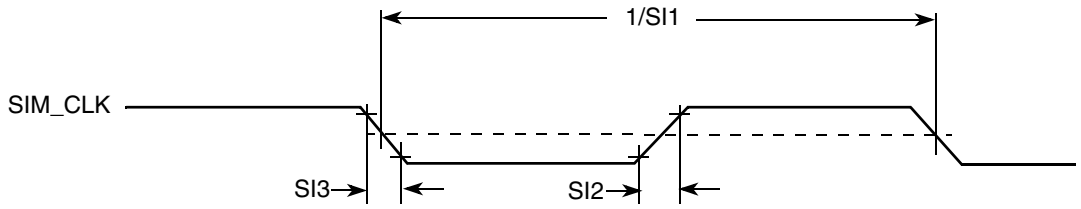


Figure 50. USIM Clock Timing Diagram

2.22.3 USIM External Pull Up/Pull Down Resistor Requirements

External off-chip pull up resistor of 20 KΩ is required on the SIM_TRXD pin.

External off-chip pull down resistors are required on the SIM_PD, SIM_SVEN, SIM_RST pins.

2.22.4 USIM Reset Sequence

2.22.4.1 SIM Cards With Internal Reset

The sequence of reset for this kind of SIM cards is as follows (see Figure 51):

- After power up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, Rx must be high.
- The card must send a response on Rx acknowledging the reset between 400 and 40000 clock cycles after T0.

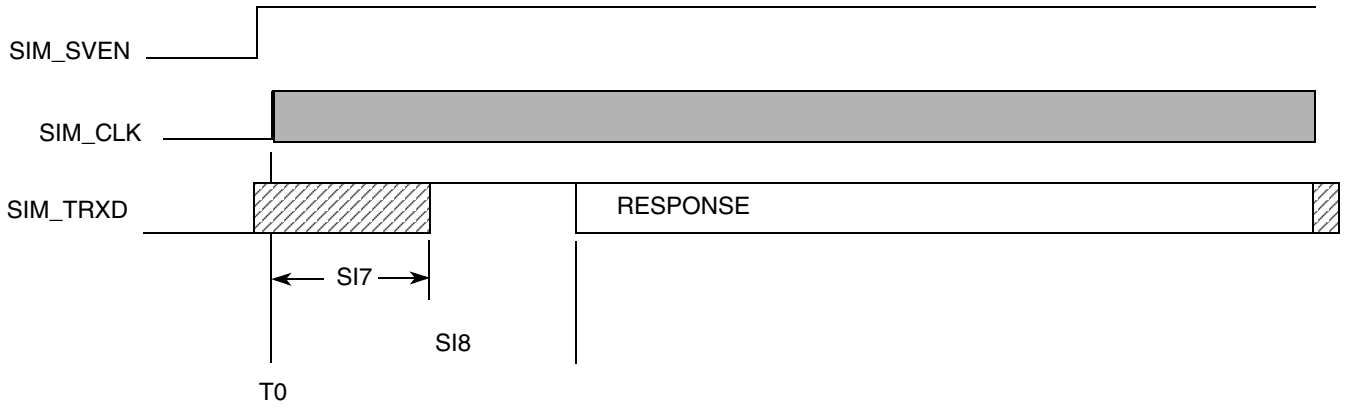


Figure 51. Internal-Reset Card Reset Sequence

Table 93. Parameters of Reset Sequence For Card With Internal Reset

ID	Parameter	Symbol	Min	Max	Unit
SI7	SIM clock to SIM TX data H	$S_{clk2dat}$	—	200	SIM_CLK clock cycle
SI8	SIM clock to SIM get ATR data	$S_{clk2atr}$	400	40000	SIM_CLK clock cycle

2.22.4.2 SIM Cards With Active-Low Reset

The sequence of reset for this kind of card is as follows (see Figure 52):

- After powering up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, SIM_TRXD must be high.
- SIM_RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on Rx during those 40000 clock cycles).
- SIM_RST is set High (time T1).
- SIM_RST must remain High for at least 40000 clock cycles after T1 and a response must be received on SIM_TRXD between 400 and 40000 clock cycles after T1.

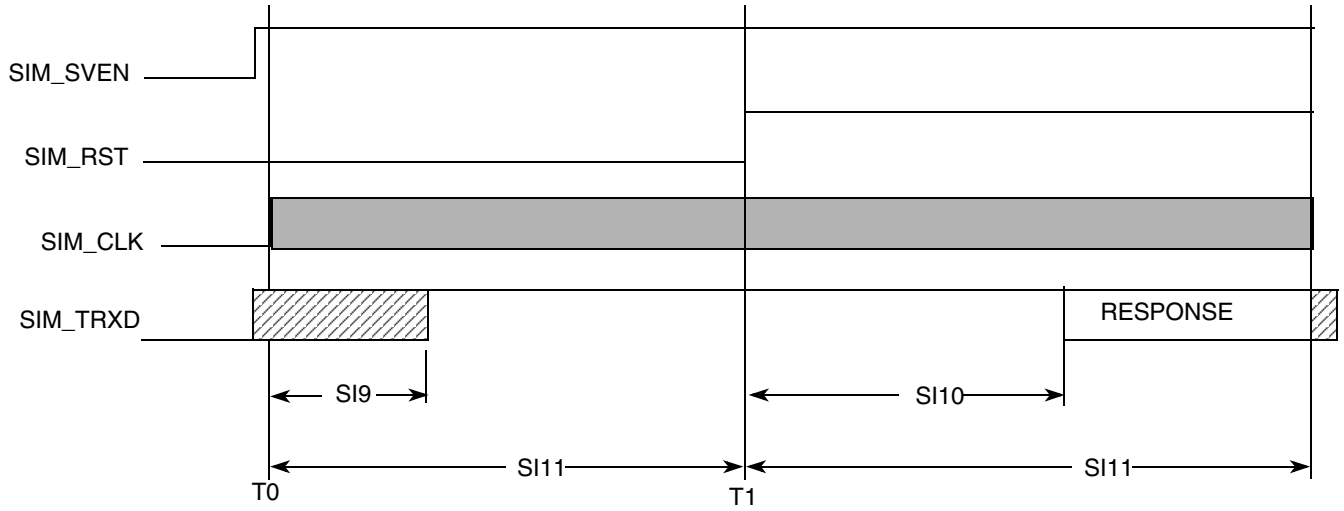


Figure 52. Active-Low Reset Card Reset Sequence

Table 94. Parameters of Reset Sequence For Active-Low Reset Card

ID	Parameter	Symbol	Min	Max	Unit
SI9	SIM clock to SIM TX data H	$S_{clk2dat}$	—	200	SIM_CLK clock cycle
SI10	SIM reset rising to SIM TX data low	$S_{clk2atr}$	400	40000	SIM_CLK clock cycle
SI11	SIM clock to SIM reset signals	$S_{clk2rst}$	40000	—	SIM_CLK clock cycle

2.22.4.3 USIM Power Down Sequence

Power down sequence for SIM interface is as follows:

- SIM_PD port detects the removal of the SIM card
- SIM_RST goes low
- SIM_CLK goes low
- SIM_TRXD goes low
- SIM_SVEN goes low

Each of these steps is done in one CKIL period (typically 32 KHz). Power down is initiated by detection of a SIM card removal or is launched by the processor. See Figure 53 and Table 95 for the timing requirements for this sequence, with F_{CKIL} = CKIL frequency value.

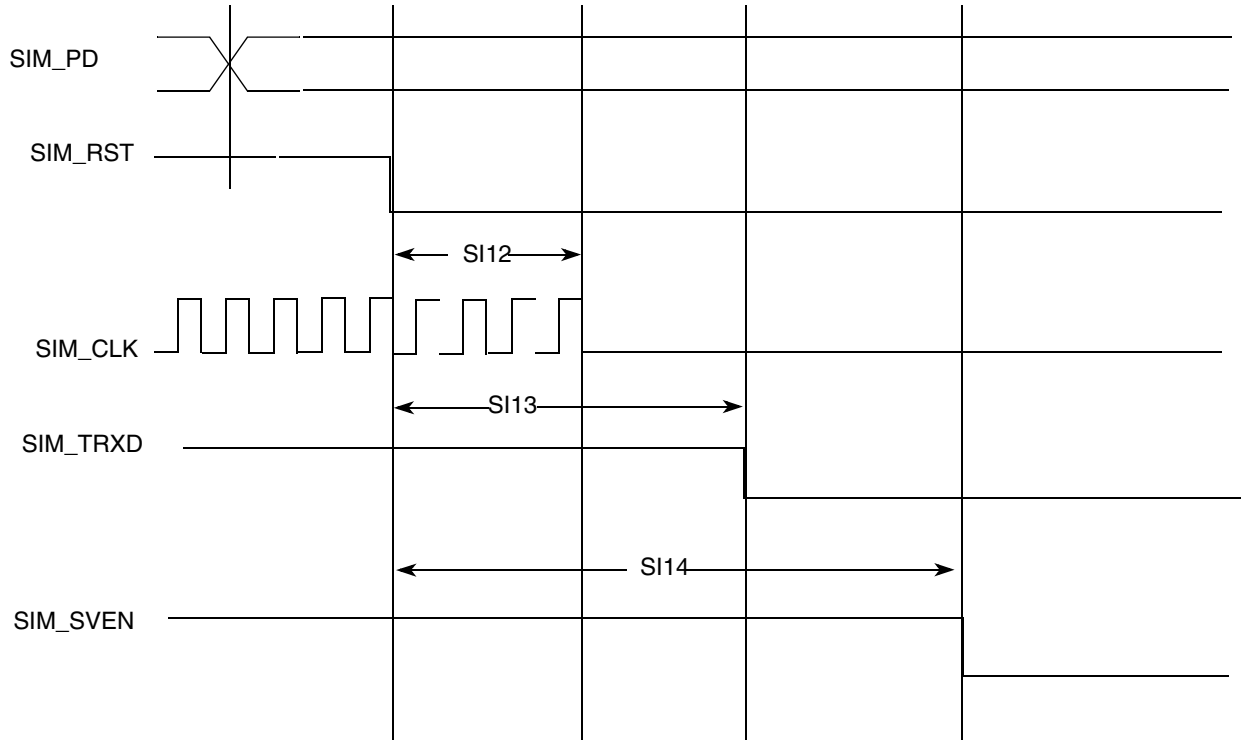


Figure 53. SmartCard Interface Power Down AC Timing

Table 95. Timing Requirements for Power Down Sequence

ID	Parameter	Symbol	Min	Max	Unit
SI12	USIM reset to USIM clock stop	$S_{rst2clk}$	0.9 × 1/Fckil	1.1 × $1/F_{CKIL}$	ns
SI13	USIM reset to USIM Tx data low	$S_{rst2dat}$	1.8 × 1/Fckil	2.2 × $1/F_{CKIL}$	ns
SI14	USIM reset to USIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Fckil	3.3 × $1/F_{CKIL}$	ns
SI15	USIM presence detect to USIM reset low	S_{pd2rst}	0.9 × 1/Fckil	1.1 × $1/F_{CKIL}$	ns

2.23 Timers and Timers_32b AC Timing Specifications

This table lists the timer input AC timing specifications.

Table 96. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Minimum	Unit	Note
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Note:

1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure shows the AC test load for the timers.

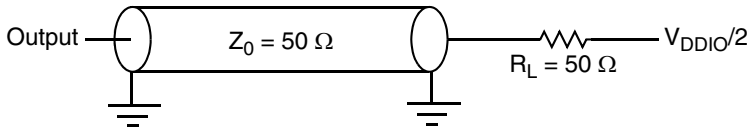


Figure 54. Timer AC Test Load

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 Power Architecture System Clocking

This section describes the PLL configuration for the Power Architecture side of the device. Note that the platform clock is identical to the internal core complex bus (CCB) clock.

This device includes 6 PLLs, as follows:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Power Architecture Platform to SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock from the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 3.1.3, "e500 Core to Platform Clock PLL Ratios." This device has two e500 core PLLs.
- The DDR PLL generates the clocking for the DDR SDRAM controller. The frequency ratio between DDR clock and platform clock is selected using the DDR PLL ratio configuration bits as described in section Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio."
- The SerDes block has two PLLs.

3.1.1 Power Architecture Clock Ranges

Table 97 provides the clocking specifications for the processor core and platform.

Table 97. Power Architecture Processor Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Note
	Min	Max		
e500 core processor frequency	400	1200	MHz	1, 2, 3
Platform CCB bus clock frequency	267	600	MHz	1, 4, 5

Table 97. Power Architecture Processor Clocking Specifications (continued)

Characteristic	Maximum Processor Core Frequency		Unit	Note
	Min	Max		

Note:

1. **Caution:** The Power Architecture platform clock to SYSCLK ratio and e500 core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 3.1.2, "Power Architecture Platform to SYSCLK PLL Ratio," and Section 3.1.3, "e500 Core to Platform Clock PLL Ratios" and Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio," for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform clock frequency of 267 MHz.
3. The reset config signal cfg_core_speed must be pulled low if the core frequency is 1001 MHz or below.
4. These values are preliminary and subject to change.
5. The reset config signal cfg_plat_speed must be pulled low if the CCB bus frequency is lower than 320 MHz.

The DDR memory controller can run in asynchronous mode.

Table 98 provides the clocking specifications for the memory bus.

Table 98. Power Architecture Memory Bus Clocking Specifications

Characteristic	Min	Max	Unit	Note
Memory bus clock frequency	266	400	MHz	1, 2, 3

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e500 core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Section 3.1.2, "Power Architecture Platform to SYSCLK PLL Ratio," and Section 3.1.3, "e500 Core to Platform Clock PLL Ratios," and Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio," for ratio settings.
2. The memory bus clock refers to the memory controllers' Dn_MCK[0:5] and Dn_MCK[0:5]_B output clocks, running at half of the DDR data rate.
3. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. See Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the platform clock rate, which in turn must be less than the DDR data rate.

As a general guideline, the following procedures can be used for selecting the DDR data rate or platform frequency:

1. Start with the processor core frequency selection.
2. Once the processor core frequency is determined, select the platform frequency from the options listed in Table 100 and Table 105.
3. Check the platform to SYSCLK ratio to verify a valid ratio can be chosen from Table 103.
4. Please note that the DDR data rate must be greater than the platform frequency. In other words, running DDR data rate lower than the platform frequency is not supported.
5. Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

3.1.2 Power Architecture Platform to SYSCLK PLL Ratio

The clock that drives the internal CCB bus is called the platform clock. The frequency of the platform clock is set using the following reset signals, as shown in Table 99:

- SYSCLK input signal

- Binary value on IFC_AD[0:2] at power up

These signals must be pulled to the desired values.

In asynchronous mode, the memory bus clock frequency is decoupled from the platform bus frequency.

Table 99. Power Architecture Platform/SYSCLK Clock Ratios

Binary Value of IFC_AD[0:2] Signals	Platform: SYSCLK Ratio
000	4:1
001	5:1
010	6:1
All Others	Reserved

3.1.3 e500 Core to Platform Clock PLL Ratios

The clock ratio between the e500 core0 and the platform clock is determined by the binary value of IFC_AD[3:5] signals at power up. Table 100 describes the supported ratios. There are no default values for these PLL ratios; these signals must be pulled to the desired values. Note that IFC_AD[6] must be pulled low if the core frequency is 1001 MHz or below.

Table 100. e500 Core0 to Platform Clock Ratios

Binary Value of IFC_AD[3:5]Signals	e500 Core0: Platform Ratio
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
All Others	Reserved

The clock ratio between the e500 core1 and the platform clock is determined by the binary value of the IFC_CLE, IFC_OE_B, IFC_WP_B signals at power up. Table 101 describes the supported ratios. There are no default values for these PLL ratios; these signals must be pulled to the desired values. Note that IFC_AD[12] must be pulled low if the core frequency is 1001 MHz or below.

Table 101. e500 Core1 to Platform Clock Ratios

Binary Value of IFC_CLE, IFC_OE_B, IFC_WP_B Signals	e500 Core1: Platform Ratio
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
All Others	Reserved

3.1.4 Power Architecture DDR/DDRCLK PLL Ratio

Table 102 describes the clock ratio between the dual DDR memory controller complexes and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complexes clock frequency is equal to the DDR data rate.

The DDR PLL rate to DDRCLK ratios listed in Table 102 reflects the DDR data rate to DDRCLK ratio, since the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output. This ratio is determined by the binary value of the IFC_AD[7].

Table 102. Power Architecture DDR Clock Ratio

Binary Value of {IFC_AD[7], IFC_ADDR[22]} Signal	DDR:DDRCLK Ratio
00	8:1
01	10:1
10	12:1
11	Reserved

3.1.5 Power Architecture SYSCLK and Platform Frequency Options

Table 103 shows the expected frequency options for SYSCLK and platform frequencies.

Table 103. Power Architecture SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)			
	66.66	80	100	133
	Platform Frequency (MHz)[1]			
4:1	267	320	400	533
5:1	333	400	500	—
6:1	400	480	600	—
8:1	533	—	—	—

1) Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed).

3.2 DSP System Clocking

This section describes the PLL configuration for the DSP side of the device. Note that the platform clock is identical to the internal core complex bus (CCB) clock.

This device has the following PLLs:

- One SC3850 core PLL
- One MAPLE-eTVPE PLL
- One DSP DDR PLL

3.2.1 DSP Clock Ranges

Table 104 provides the clocking specifications for the SC3850 processor core, MAPLE, and DSP memory.

Table 104. DSP Processor Clocking Specifications

DSP Core	Minimum Frequency	Maximum Frequency	Unit
SC3850 cores	800	1200	MHz
MAPLE eVTPE	800	800	MHz
DSP DDR Controller	800	1333	MHz

3.2.2 DSPCLKIN and SC3850 Core Frequency Options

Table 105 shows the expected frequency options for DSPCLKIN and SC3850 core frequencies.

Table 105. Options for SC3850 Core0 and Core1 Clocking

PLL_T2 MF	DSPCLKIN Frequency (MHz)			
	66.66	80	100	133
	SC3850 Core Frequency (MHz)			
1	66.66	80	100	133
6	400	480	600	800
7.5	500	600	750	1000
8	533	640	800	1066
9	600	720	900	1200
10	667	800	1000	—
12	800	960	1200	—
15	1000	1200	—	—

3.3 Supply Power Default Setting

This device is capable of supporting multiple power supply levels on its I/O supply. Table 106 through Table 110 shows the encoding used to select the voltage level for each I/O supply. When setting the VSEL signals, "1" is selected through a pull-up resistor to OVDD (as seen in Table 1).

Table 106. Default Voltage Level for BV_{DD}

BVDD_VSEL[0:1]	I/O Voltage Level
00	3.3 V
01	2.5 V
10	1.8 V
11	Reserved

Table 107. Default Voltage Level for CV_{DD}

CVDD_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 108. Default Voltage Level for $X1V_{DD}$

X1VDD_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 109. Default Voltage Level for $X2V_{DD}$

XVDD2_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 110. Default Voltage Level for LV_{DD}

LVDD_VSEL	I/O Voltage Level
0	3.3 V
1	2.5 V

3.4 PLL Power Supply Design

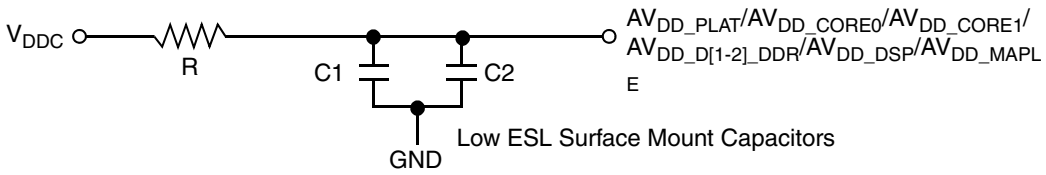
Each of the PLLs listed above is provided with power through independent power supply pins (AVDD_PLAT, AVDD_CORE0, AVDD_CORE1, AVDD_D1_DDR, AVDD_D2_DDR, AVDD_DSP, and AVDD_MAPLE respectively). The AV_{DD} level should always be equivalent to V_{DDC}, and these voltages must be derived directly from V_{DDC} through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 55, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 780 ball FCPBGA the footprint, without the inductance of vias.

Figure 55 shows the core PLL (AV_{DD_CORE}) power supply filter circuit.



Notes:

R = 5Ω ± 5%

C1 = 10μF ± 10%, 603, X5R with ESL ≤ 0.5 nH

C2 = 1.0μF ± 10%, 402 X5R with ESL ≤ 0.5 nH

This circuit applies for system PLL, core PLL, DDR PPLL, and DSP PLL.

Figure 55. PLL Power Supply Filter Circuit

The AVDD_SRDSn signals provides power for the analog portions of the SerDes PLL. Use separate islands (that is, very wide traces) for each PLL bank's SD*n*AGND and SD*n*AVDD connections. The ground islands/wide traces of different PLL banks are to be joined to a single ground plane either with an inductor or through a 0 Ω resistance. While it is possible to connect these islands together to a single supply (possibly via a resistor or ferrite bead), it would be best for this connection to be formed by multiple single-point connections which are as close to the source (and as far away from the chip) as possible. The multiple single-point connections can be optimized as thick multiple wide connections to provide a good return path. The user should simulate the return path impedance and then take appropriate PCB layout tradeoff decisions. Additionally, one should maintain low noise and good stability of the SD*n*AVDD. The user should not place any digital or other bank traces near the PLL power and ground planes.

For maximum effectiveness, the filter circuit should be placed as closely as possible to the SDAVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SDAVDD ball. To provide effective bypass capacitance at high frequencies, these two islands/wide traces should be directly over each other and on the nearest layer (that is, layers 3 and 4 of a 6-layer PC board).

The capacitors are connected from SDAVDD to the ground plane. Only the surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance. The 2.2 nF capacitor is the closest to the package pin, followed by the two 2.2 μF capacitors, and finally the 1 Ω resistor to the board supply plane. The goal is to have a 2.2 nF decoupling capacitor within approximately 0.5 cm of each power pin.

3.5 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, BVDD, CVDD, OVDD, G1VDD, G2VDD, LVDD, RVDD, X1VDD, and X2VDD pin of the device. These decoupling capacitors should receive their power from separate VDD, BVDD, OVDD, G1VDD, G2VDD, LVDD, RVDD, X1VDD, X2VDD, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0201 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

3.6 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power ($XCOREV_{DD}$ and $XPADV_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

- The board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- There should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Between the device and any SerDes voltage regulator there should be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

Figure 56 shows the SerDes PLL power supply filter circuit.

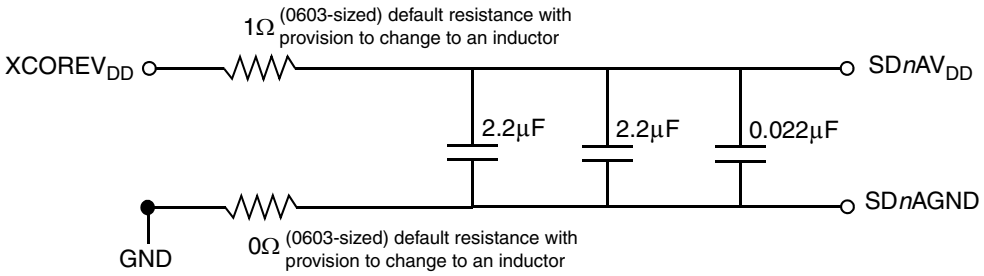


Figure 56. SerDes PLL Power Supply Filter Circuit

The power supplied to the $XCOREV_{DD}$ and $XPADV_{DD}$ are filtered using a circuit similar to Figure 57.

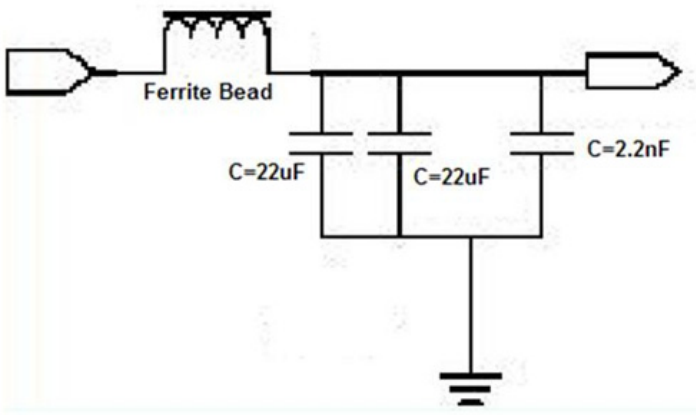


Figure 57. $XCOREV_{DD}$ and $XPADV_{DD}$ Power Supply Filter Circuit

The $XCOREV_{SS}$ and $XPADV_{SS}$ of different banks can be joined to a low noise, solid reference ground plane. Perform the noise coupling simulation on actual PCB design implementation. The user should quantify the noise and then and then take appropriate PCB layout tradeoff decisions, followed by validating the simulated noise against the measured noise for the designed PCB.

In case of a board noise coupling issue, the user may use separate islands/thick wide traces for $XCOREV_{SS}$, $XPADV_{SS}$, $XCOREV_{DD}$ and $XPADV_{DD}$. Connect these “islands" together to a single supply plane; it would be best for this connection to be a single point or multiple single-point connections as close to the source (and as far away from the chip) as possible.

Component values will need to be optimized/finalized based on board level filter measurements to provide best possible attenuation up to 10 GHz, while preserving lowest loss at DC (IR drop).

3.7 Guidelines for High-Speed Interface Termination

This section provides guidelines for when the SerDes interface is entirely unused and when it is partially unused.

3.7.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[3:0], SD_TX_B[3:0]
- SD_RX[3:0], SD_RX_B[3:0]
- SD_IMP_CAL_TX, SD_IMP_CAL_RX

The following pins must be connected to XCOREVSS:

- SD_REF_CLK1, SD_REF_CLK1_B (if entire SerDes bank 1 is unused)
- SD_REF_CLK2, SD_REF_CLK2_B (if entire SerDes bank 2 is unused)

Unused SD_REF_CLK1 and SD_REF_CLK2 must be connected to SGND.

Power should still be applied to the SerDes external pins:

- $XCOREV_{DD}$/VSS(SGND)
- AV_{DD}/VSS
- $XPADV_{DD}$/VSS

3.7.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following unused pins must be left unconnected:

- SD_TX[*n*]
- SD_TX_B[*n*]

The following unused pins must be connected to SGND:

- SD_RX[*n*], SD_RX_B[*n*]
- SD_REF_CLK1, SD_REF_CLK1_B (If entire SerDes bank 1 is unused)
- SD_REF_CLK2, SD_REF_CLK2_B (If entire SerDes bank 2 is unused)

In the RCW configuration field for each bank SRDS_LPD_B*n* with unused lanes, the respective bit for each unused lane must be set to power down the lane.

3.8 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors on open drain type pins including I^2C pins (1 kΩ is recommended) and MPIC interrupt pins (2–10 kΩ is recommended).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 59. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior, and spurious assertion gives unpredictable results.

3.9 Output Buffer DC Impedance

The drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 58). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

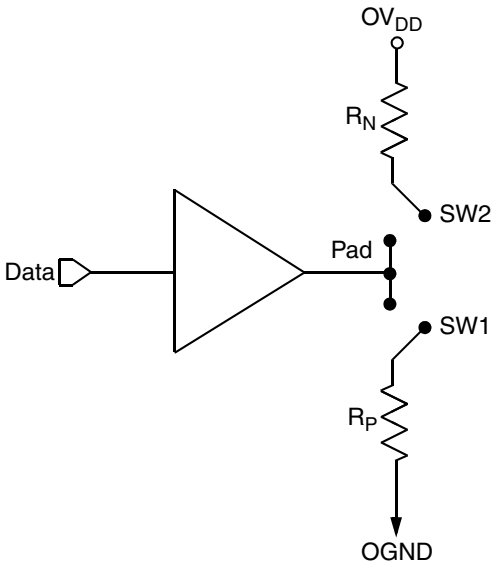


Figure 58. Driver Impedance Measurement

Table 111 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DDC}, nominal OV_{DD}, 90°C.

Table 111. Impedance Characteristics

Impedance	IFC, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	43 Target	20 Target	Z_0	W
R_P	43 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 2.

3.10 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET_B is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET_B is asserted, is latched when HRESET_B deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET_B (and for platform/system clocks after HRESET_B deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with

minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

3.11 JTAG Configuration Signals

There are two JTAG ports:

- Power Architecture JTAG (TDI, TDO, TMS, TCK, and TRST_B)
- DSP JTAG (DSP_TDI, DSP_ TDO, DSP_TMS, DSP_TCK, and DSP_TRST_B)

Note that the DSP JTAG is available as dedicated I/O pins.

The Power Architecture JTAG is the primary JTAG interface of the chip. DSP JTAG is defined as optional debug interface. As seen in Table 112, the JTAG topology is selectable by static value driven on two pins—CFG_0_JTAG_MODE and CFG_1_JTAG_MODE.

Table 112. JTAG Topology

{CFG_0_JTAG_MODE, CFG_1_JTAG_MODE}	Uses Power Architecture Debug Header	Uses DSP Debug Header	JTAG Topology
00	Yes	No	Access Power Architecture domain and DSP domain using Power Architecture JTAG port
01	Yes	No	Access DSP domain using Power Architecture JTAG port
10	Yes	No	Access Power Architecture domain using Power Architecture JTAG port
11	Yes	Yes	Access Power Architecture domain using Power Architecture JTAG and DSP domain using DSP JTAG

Note: For boundary SCAN, set {CFG_0_JTAG_MODE, CFG_1_JTAG_MODE} = 10.

The TRST/DSP_TRST signal is optional in the IEEE 1149.1 specification, but is provided on the device. The device requires TRST/DSP_TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert TRST/DSP_TRST during the power-on reset flow. Simply tying TRST/DSP_TRST to HRESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of the processor allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The arrangement shown in Figure 59 and Figure 60 allows the COP/ONCE port to independently assert HRESET_B or TRST, while ensuring that the target can drive HRESET_B as well.

The COP interface has a standard header for connection to the target system. The 16-pin PA COP connector is shown in Figure 59.

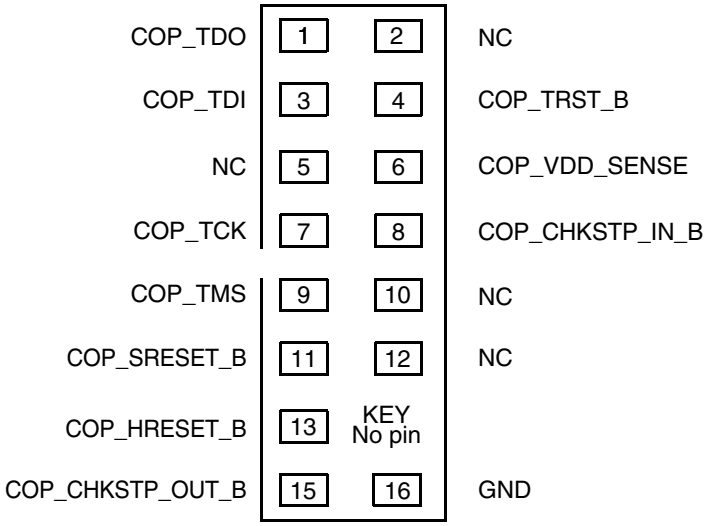


Figure 59. COP Connector Physical Pinout

The ONCE interface also has a standard header for connection to the target system. The 14-pin DSP ONCE connector is shown in Figure 60.

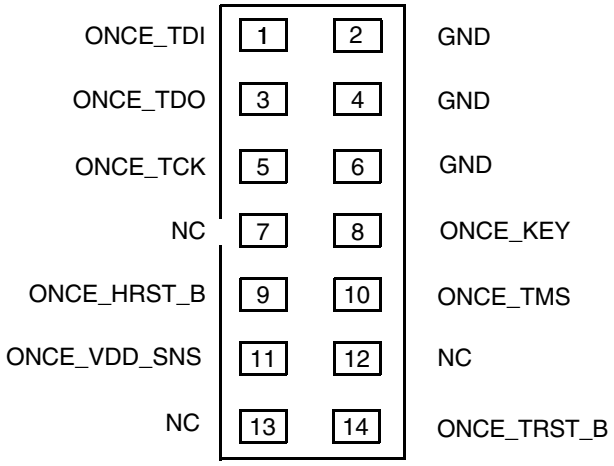


Figure 60. ONCE Connector Physical Pinout

3.11.1 Termination of Unused Signals

If the Power Architecture JTAG or DSP JTAG interface and COP/ONCE header is not used, Freescale recommends the following connections:

- TRST_B should be tied to HRESET_B through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (HRESET_B) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 59. If this is not possible,

the isolation resistor allows future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.

- TCK should be pulled down to GND through a 1 kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TDO, or TMS.

NOTE

In the case where the DSP JTAG is also used (as described in Table 112), DSP_TRST and DSP_TCK need to be handled in the same way as TRST and TCK are, as mentioned above.

3.12 Guidelines for High-Speed Interface Termination

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[3:0]
- SD_TX_B[3:0]

The following pins must be connected to GND:

- SD_RX[3:0], SD_RX_B[3:0]
- SD_REF_CLK, SD_REF_CLK_B

3.13 Thermal

This section describes the thermal specifications.

3.13.1 Thermal Characteristics

Table 113 provides the package thermal characteristics.

Table 113. Package Thermal Resistance Characteristics

Characteristic	JEDEC Board	Symbol	Lid	Unit
Junction-to-Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	21	°C/W
Junction-to-Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	14	°C/W
Junction-to-Ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	15	°C/W
Junction-to-Ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	11	°C/W
Junction-to-Board	—	$R_{\theta JB}$	4.0	°C/W
Junction-to-Case Top	—	$R_{\theta JCtop}$	0.7	°C/W

Note:

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.13.2 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 – 230μA

Ideality factor over 13.5 – 220 μA: n = 1.007 ± 0.008

3.14 Security Fuse Processor

This device implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual*.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD1} pin per Section 2.2, "Power Sequencing." POV_{DD1} should only be powered for the duration of the fuse programming cycle, with a per device limit of one fuse programming cycle. All other times POV_{DD1} should be connected to GND. The sequencing requirements for raising and lowering POV_{DD1} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD1} to GND.

4 Package Information

The following section describes the detailed content and mechanical description of the package.

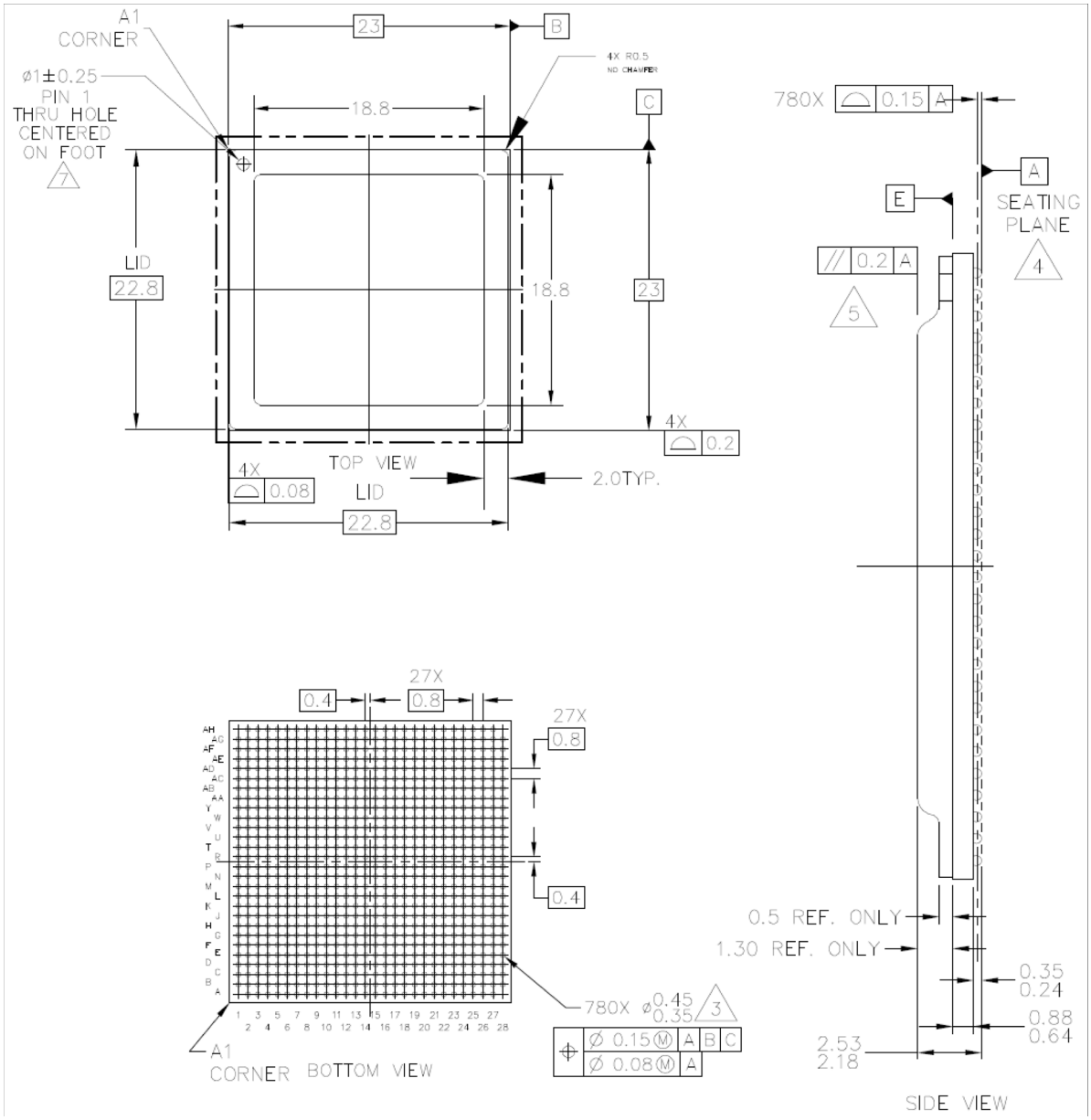
4.1 Package Parameters

The package parameters are provided in the following list. The package type is plastic ball grid array (FC-PBGA).

Package outline	23 mm × 23 mm
Interconnects	780
Pitch	0.8 mm
Ball diameter (typical)	0.4 mm

4.2 Mechanical Dimensions of the FC-PBGA

Figure 61 shows the package and bottom surface nomenclature.



Notes:
1. All dimentions are in milimeters.
2. Dimensions and tolerancing per ASME Y14.5-1994.
3. Maximum ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 through hole should be centered within foot area.

Figure 61. BSC9132 Mechanical Dimensions and Package Diagram

5 Ordering Information

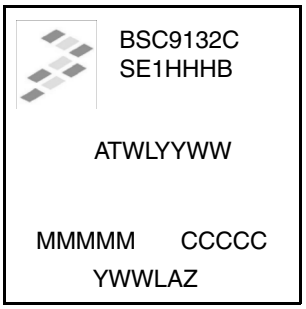
The table below provides the Freescale part numbering nomenclature for the BSC9132. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 114. Part numbering nomenclature

	n	*x*	*t*	*e*	*n*	*c*	*d*	*f*	*r*
Product Code	**Part Identifier**	**Qual Status**	**Temp Range**	**Encryp-tion**	**Package Type**	**CPU Freq**	**DDR Speed**	**DSP Freq**	**Die Revision**
BSC	9132	N = Industrial Tier	S, L = Std temp (0–105°C) X, J = Ext temp (-40–105°C)	E = SEC Present N = No SEC Present	7 = FC-PBGA Pb-free Bumps and Package	K = 1000 MHz M = 1200 MHz P = 1400 MHz	N = 1333 MHz	K = 1000 MHz M = 1200 MHz	B = Rev 1.1

5.1 Part Marking

Parts are marked as the example shown in this figure.



FCPBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.
BSC9132CSE1HHHB is the orderable part number. See Table 114 for details.

Figure 62. Part Marking for FCPBGA Device

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part. Some documents may require a non-disclosure agreement. Contact your local FAE for assistance.

- *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* (BSC9132RM)

- *e500 PowerPC Core Reference Manual* (E500CORERM)

7 Revision History

Table 115. Document Revision History

Rev	Date	Substantive Change(s)
0	03/2014	Initial public release.

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