Freescale Semiconductor
User's Guide

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KIT33912G5DGEVBE Evaluation Kit

Featuring MC33912G5 Evaluation Board with KIT USBSPI Dongle Board

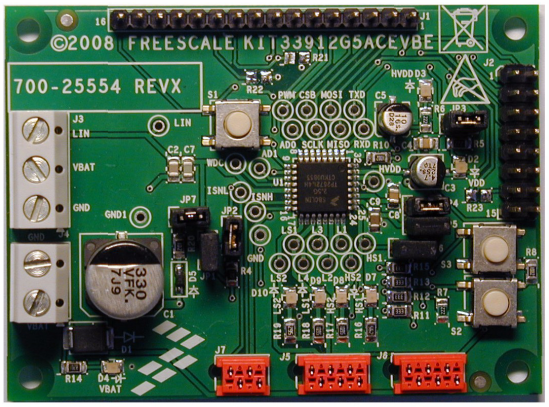

Figure 1. MC33912G5 Evaluation Board

Table of Contents

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1 Kit Contents / Packing List

- 33912G5 Evaluation Board
- USB-SPI Dongle Board
- 16-wire Ribbon Cable
- CD33912G5DG

2 Important Notice

Freescale provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This EVB may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This EVB is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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3 Kit Introduction

This Evaluation Board demonstrates the capability of the MC33912G5 as a System Basis Chip (SBC) with a Local Interconnect Network (LIN) transceiver controlled by a Serial Peripheral Interface (SPI).

It provides two 50mA high-side switches (HSx) and two 150mA low-side switches (LSx) with output protection, through a Micromatch connector as well as four high-voltage inputs and two current sense inputs which are accessible through the Micromatch connectors for an easier out-of-the-box evaluation. The status of the HSx and LSx is provided by LED. The LIN Bus signal is provided through a terminal block connector.

A single terminal block connector for input power supply allows the user to supply the board with an external DC power supply.

The KIT33912G5DGEVBE has the ability of configuration of the watchdog period and allows the disabling of the watchdog. All other features can be programmed via the SPI communication using a standard 100mils 2x8-pin header to communicate with the USB-SPI Dongle. Through the 16-pin header, an external MCU could be connected to control the SBC device.

3.1 EVB Features

- Input voltage nominal operating range of 5.5 to 18V
- Two high-side switches accessible through Micromatch connector
- Two low-side switches accessible through Micromatch connector
- The status of HSx and LSx indicated by LED
- Two current sense Inputs accessible through Micromatch connector
- Four high-voltage analog/logic Inputs accessible through Micromatch connector
- Capable to be controlled via SPI
- RESET and WAKE-UP push buttons
- Configurable watchdog period and allows the watchdog to be disabled
- 100mils 2x8-pin standard header connector for SPI communication
- 100mils 16-pin standard header connector for MCU connection
- Small Board Size (5.2cm x 7.2cm)

3.2 AMPD Device Description/Features

- Full-duplex SPI interface at frequencies up to 4.0 MHz
- LIN transceiver capable of up to 100 kbps with wave shaping
- Two 50 mA high-side and two 150 mA low-side protected switches
- Four high-voltage analog/logic Inputs
- Configurable window watchdog
- 5.0V low drop regulator with fault detection and low-voltage reset (LVR) circuitry
- Current sense module
- Switched/protected 5.0V output (used for Hall sensors)
- Pb-free packaging designated by suffix code AC

4 Required Equipment

Minimum required equipment:

- Power supply: 5.5 to 18V
- USB-SPI Dongle
- USB Cable
- 16-wire ribbon cable with 16 pins ribbon cable connectors on both sides
- USB enabled computer with Windows XP or higher
- SPIGen software (Setup.exe)
- SBC MC33912.exe software

5 EVB Setup Configuration Diagram

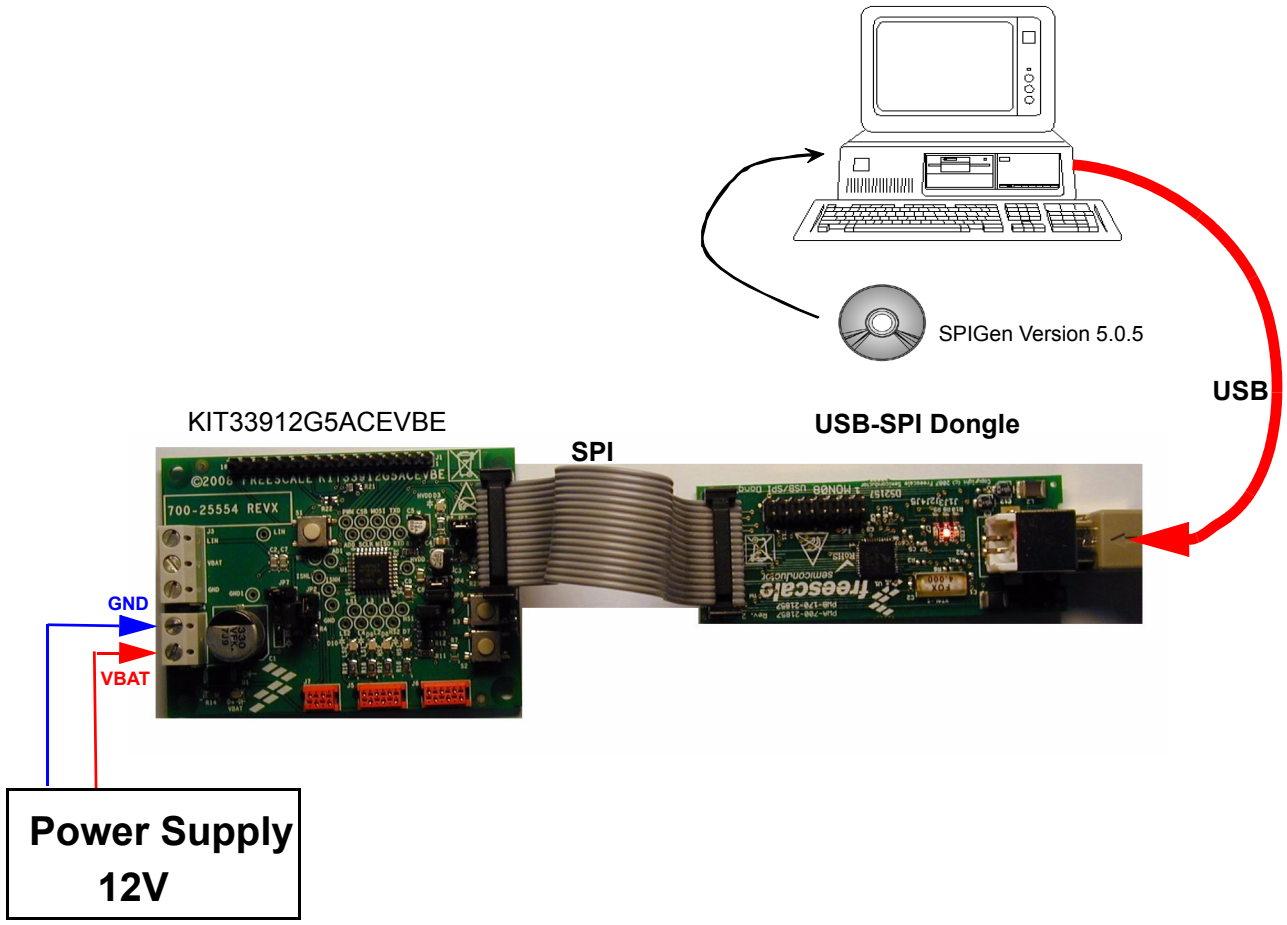


Figure 1. EVB Setup Configuration Diagram

6 Using Hardware

The KIT33912G5DGEVBE operates with a single power supply from 5.5 to 18V and could be controlled via SPI with the help of an USB-SPI Dongle. Applying the Input power supply will start up the device operation. If the Jumper connection is in accord with the Section 6.1, the LEDs, D4 and D2 must be ON (flashing). All features of the device are controlled via SPI, only.

6.1 Jumper Connections

Jumpers

NAME	DESCRIPTION
JP1	1-2 position: Disabled watchdog only if jumper, JP2 is closed Floating: Watchdog enabled only if selected jumper, JP1
JP2	1-2 position: Watchdog time out is 16ms, only if jumper JP1 is open Floating: Watchdog time out is 150ms
JP3	1-2 position: LED diode D2 is connected to (VDD) supply voltage source Floating: LED diode D2 is not indicated presence of voltage on (VDD) pin
JP4	1-2 position: Supply MC33912G5 from Vbat Floating: MC33912G5 is not powered
JP5	1-2 position: Supply MC33912G5 High Side Switches Module from Vbat Floating: High Side Switches Module is not powered
JP6	1-2 position: (HS2) is connected to (L1) input
JP7	1-2 position: Master mode configuration Floating: Slave mode configuration

For the standard EVB operation set up the Jumpers in accordance with the **Figure 2**.

JUMPER	POSITION
JP1	1-2
JP2	1-2
JP3	1-2
JP4	1-2
JP5	1-2
JP6	OPEN
JP7	1-2

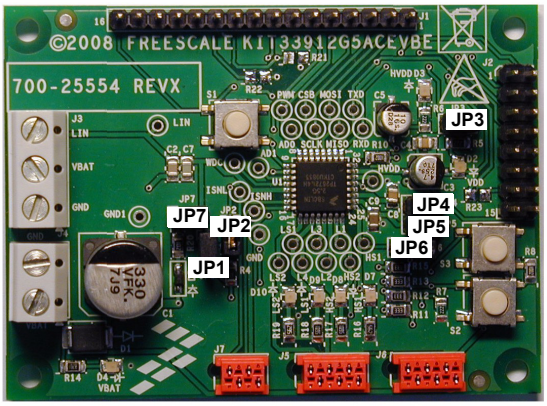


Figure 2. KIT33912G5DGEVBEJumpers settings

6.2 Power supply and Input/Output connectors

The two-pin terminal block (J4) serves as an input terminal for the main power between 5.5 to 18V to operate the KIT33912G5DGEVBE.

The LIN bus signal is accessible through the three-pin terminal block J3 and it can be used as well for the EVB powering.

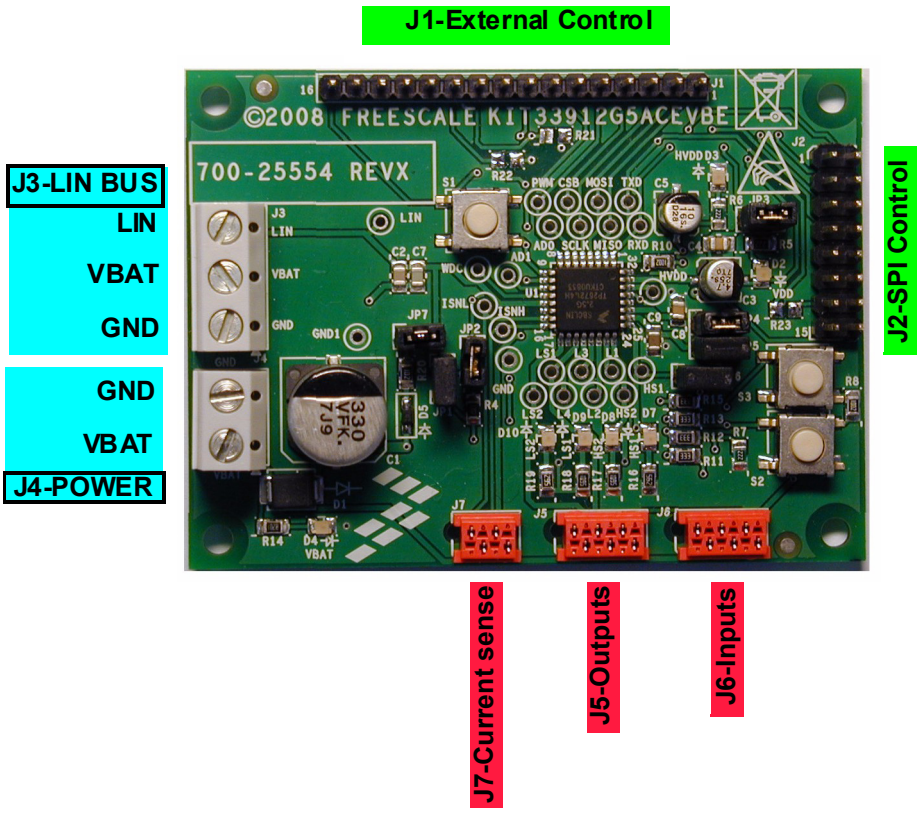


Figure 3. EVB Connectors

6.2.1 Connector J1 - External control

Connector J1

PIN #	PIN NAME	DESCRIPTION
1	MISO	SPI data output. When CS is high, pin is in the high-impedance state
2	MOSI	SPI data input
3	SCLK	SPI clock Input
4	CSB	SPI chip select input pin. CSB is active low
5	PWM	High Side and Low Side Pulse Width Modulation Input
6	NC	NO Connect
7	AD0	Analog Multiplexer Output
8	AD1	Current sense analog output
9	VDD_OUT	+5.0 V main voltage regulator output pin
10	LIRQ	Interrupt output pin, indicating wake-up events from Stop Mode or events from Normal and Normal request modes. IRQ is active low.
11	LRES	Bidirectional Reset I/O pin - driven low when any internal reset source is asserted. RST is active low
12	LINTxD	The transmitter input of the LIN interface which controls the state of the bus output
13	LINRxD	The receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface
14	NC	No Connect
15	NC	No Connect
16	GND	Ground

6.2.2 Connector J2 - SPI Control

Connector J2

PIN #	NAME	DESCRIPTION
1	NC	No Connect
2	CSB	SPI chip select input pin. CSB is active low
3	LIRQ	Interrupt output pin, indicating wake-up events from Stop Mode or events from Normal and Normal request modes. IRQ is active low.
4	MISO	SPI data output. When CS is high, pin is in the high-impedance state
5	LRES	Bidirectional Reset I/O pin - driven low when any internal reset source is asserted. RST is active low
6	MOSI	SPI data input
7	NC	NO Connect

Connector J2 (Continued)

PIN #	NAME	DESCRIPTION
8	SCLK	SPI clock Input
9	NC	NO Connect
10	NC	NO Connect
11	NC	NO Connect
12	NC	NO Connect
13	LINTxD	The transmitter input of the LIN interface which controls the state of the bus output
14	NC	NO Connect
15	NC	NO Connect
16	GND	GROUND

6.2.3 Connector J5 - HSx - LSx Outputs

Connector J5

PIN#	NAME	DESCRIPTION
1	VBAT	Power supply pin output
2	LS2	Relay driver low side output 2
3	LS1	Relay driver low side output 1
4	GND	Ground
5	HS2	High side switch output 2
6	HS1	High side switch output 1

6.2.4 Connector J6 - Lx Inputs

Connector J6

PIN#	NAME	DESCRIPTION
1	GND	Ground
2	L4	The wake-up capable digital input 4. All Lx inputs can be sensed analog via the analog multiplexer
3	L3	The wake-up capable digital input 3.
4	L2	The wake-up capable digital input 2.
5	L1	The wake-up capable digital input 1.
6	HS1	High side switch output 1

6.2.5 Connector J7 - Current sense Inputs

Connector J7

PIN#	NAME	DESCRIPTION
1	ISENSL	Current Sense differential input low
2	GND	Ground
3	ISENSH	Current Sense differential input high
4	GND	Ground

6.2.6 EVB to USB-SPI Dongle Interconnection

Interconnection

KIT33912G5DGEVBE - J2			USB-SPI Dongle - IO PORT	
PIN#	SIGNAL		SIGNAL	PIN#
1	NC		CNTL2	2
2	CSB		CSB	1
3	LIRQ		CNTL1	4
4	MISO		SO	3
5	LRES		CNTL0	6
6	MOSI		SI	5
7	NC		DATA4	8
8	SCLK		SCLK	7
9	NC		DATA3	10
10	NC		CNTL3	9
11	NC		DATA2	12
12	NC		VDD	11
13	LINTxD		DATA1	14
14	NC		REG 3,3V	13
15	NC		DATA0	16
16	GND		GND	15

6.3 Starting up the KIT33912G5DGEVBE

To Start working with the KIT33912G5DGEVBE arrange the connections in accordance **Figure 1** and provide an input voltage 12V connecting the (+) probe to the VBAT terminal and the (-) probe to the GND terminal on the Input power terminal block J4. Turn on the power supply, the LEDs D4 and D2 should turn on.

To operate all the MC33912G5 device functions, it is necessary to connect square wave generator to the connector J1, pin 12 (LINTxD) and use SPI communication.

Section 7 will discuss how to interact with the KIT33912G5DGEVBE using the SPIGen Graphical User Interface developed by Freescale to operate the MC33912G5 device.

7 EVB Software

The 33912G5 uses a standard 8-Bit SPI interface to provide control and status information. Both Low-Side and both High-Side driver outputs can be controlled via the SPI register. The integrated LIN physical layer interface can be configured via the SPI register. SPI control and status data can be accessed by the connector J2

7.1 Installing SPIGen Software

1. Insert CD33912G5DG into the CD drive. Auto-run will start and the initial HTML page will be displayed.

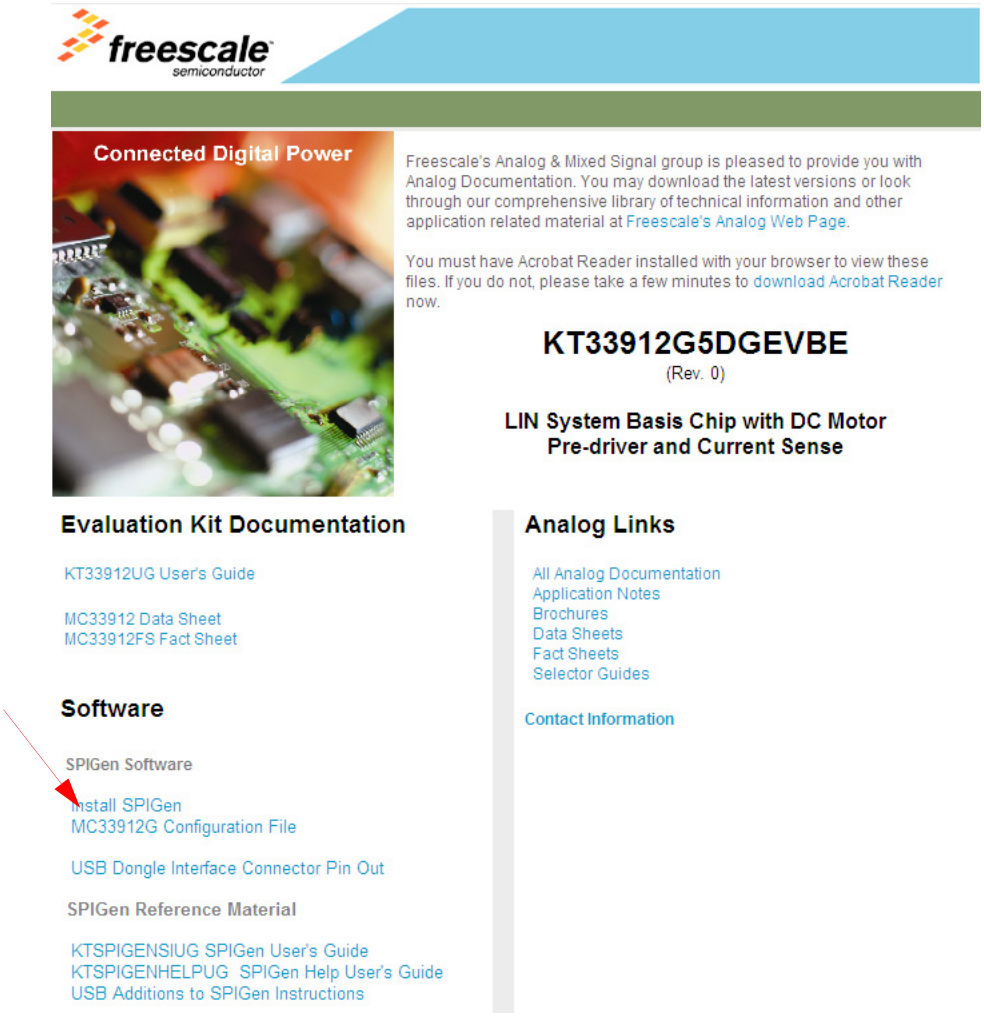


Figure 4. Initial Start Page

2. Click on “Install SPIGen”.
3. Follow the on-screen install options.

7.2 Working with the KIT33912G5DGEVBE with SPIGen GUI

1. Load the “MC33912_EVB_CONFIG_FILE.spi”
2. Be sure that SPIGen software is installed on your PC.
3. Switch ON power supply 12V DC
4. Check if the LED D2 and D4 are lighting
5. Start SPIGen program on PC. Go to *Start -> Program -> SPIGen*:

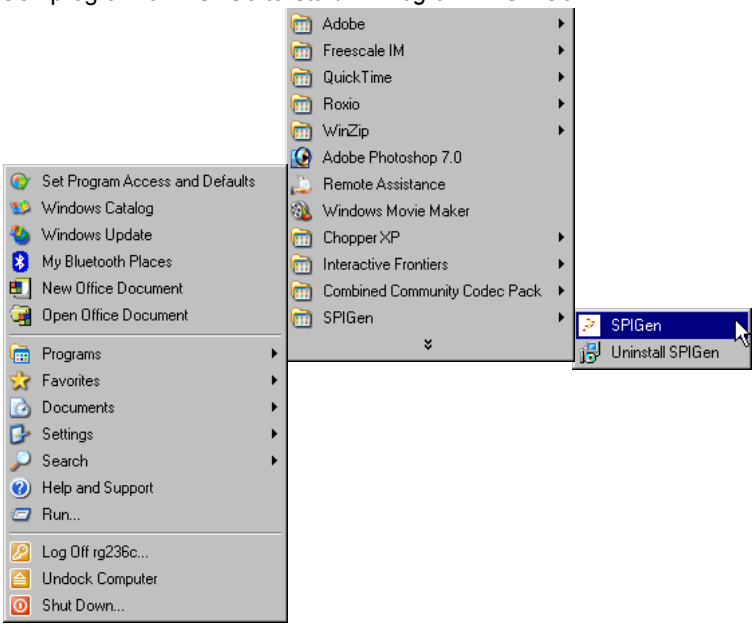
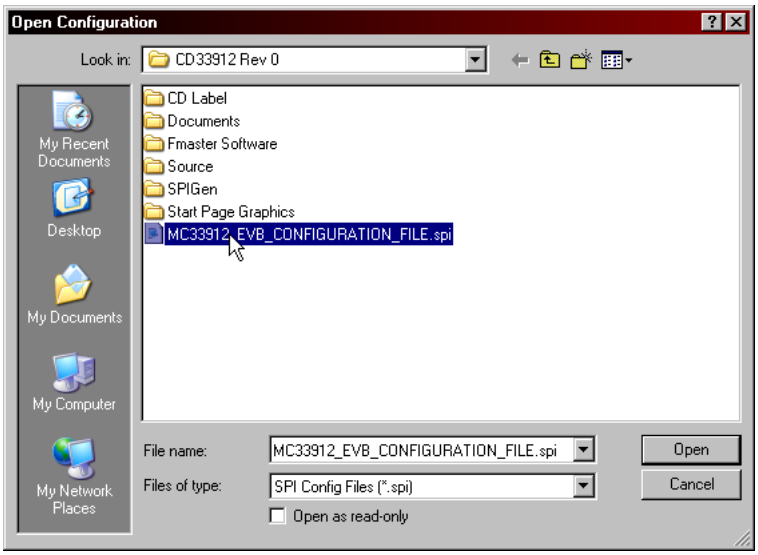


Figure 5. SPIGen Program

6. Select *File -> Open* and select thew file “MC33912_EVB_CONFIGURATION_FILE.spi” from the CD33912G5DG:



7. Select the “MC33912 - SBC LIN 2.5G Tab”

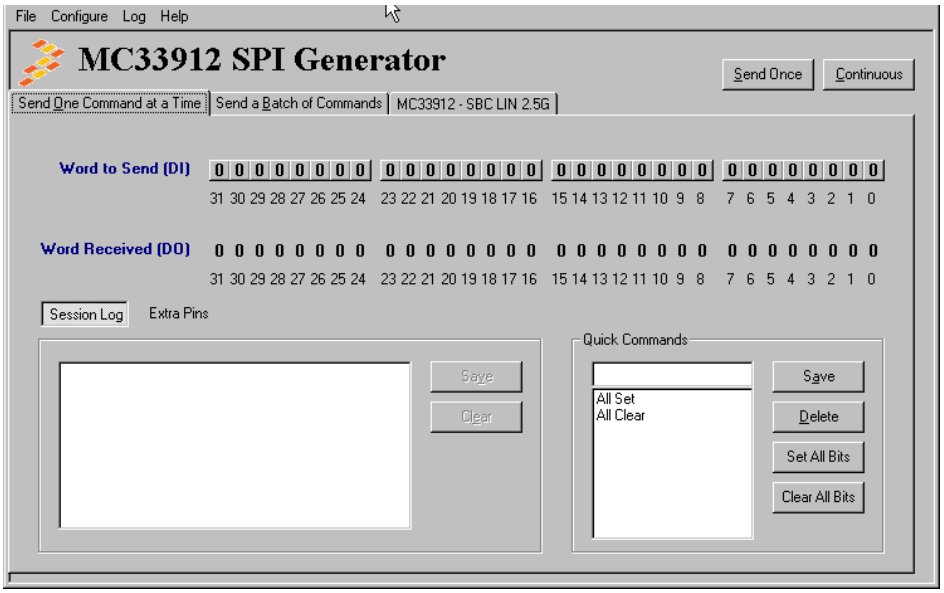
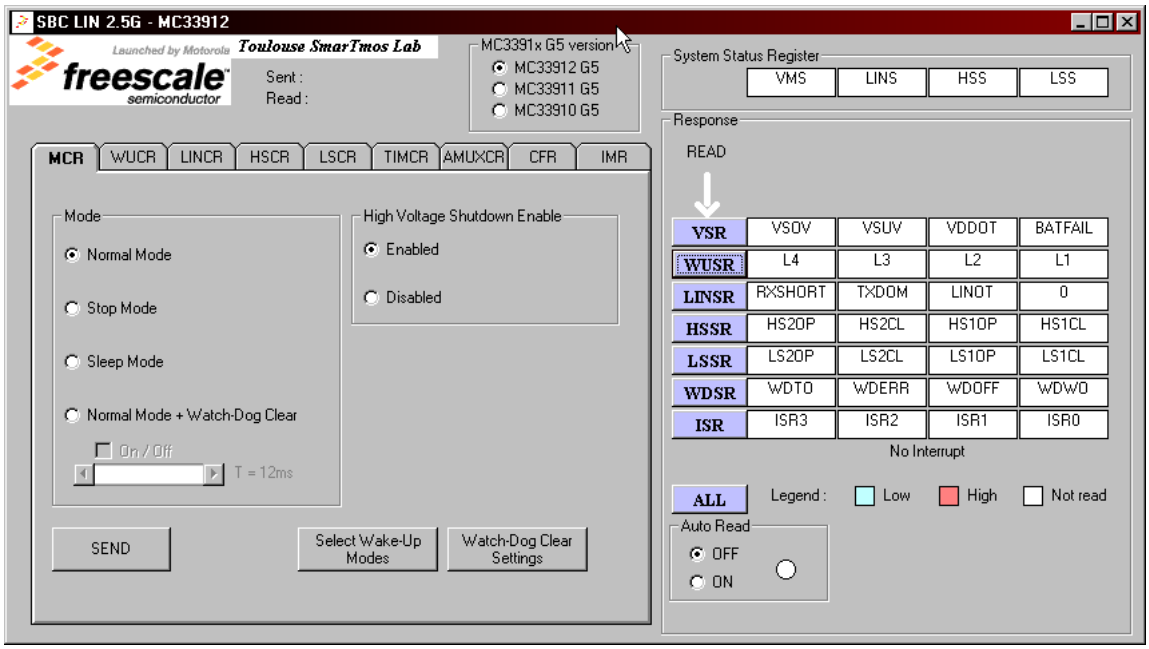


Figure 6. SPIGen Basic Screen with MC33912 Configuration File Loaded

8. SPIGen is now ready for the MC33912:



7.2.1 Using SPIGen with the MC33912G5DG

SPIGen allows you to control the device through a GUI SPI interface.

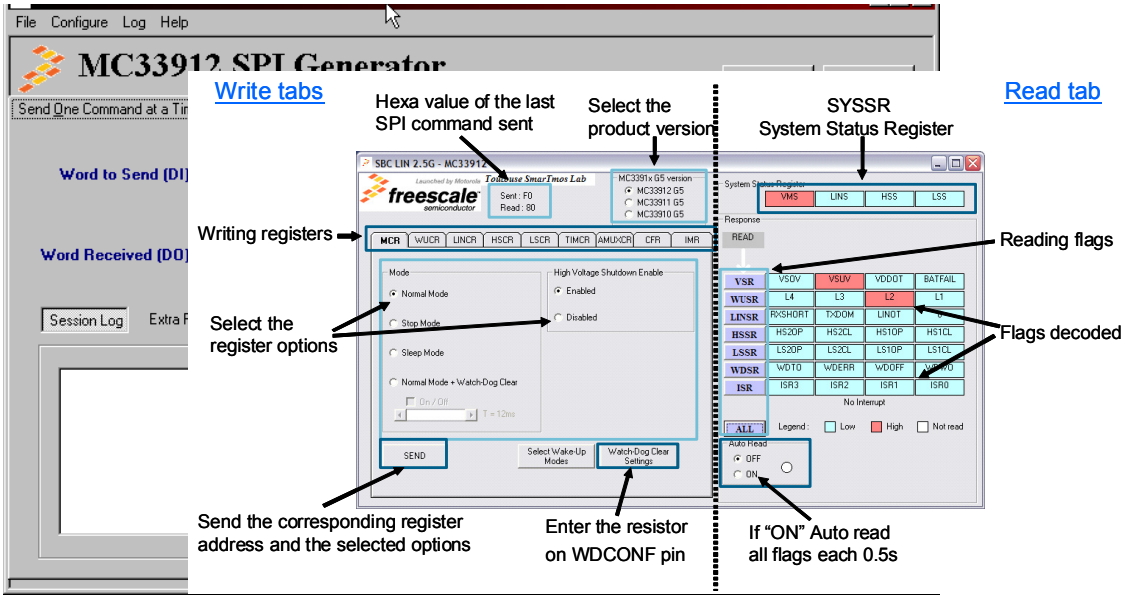


Figure 7. SPIGen GUI Interface

The user can configure any watchdog period by soldering the corresponding external resistor on the watchdog pin and entering the period value in the window as indicated:

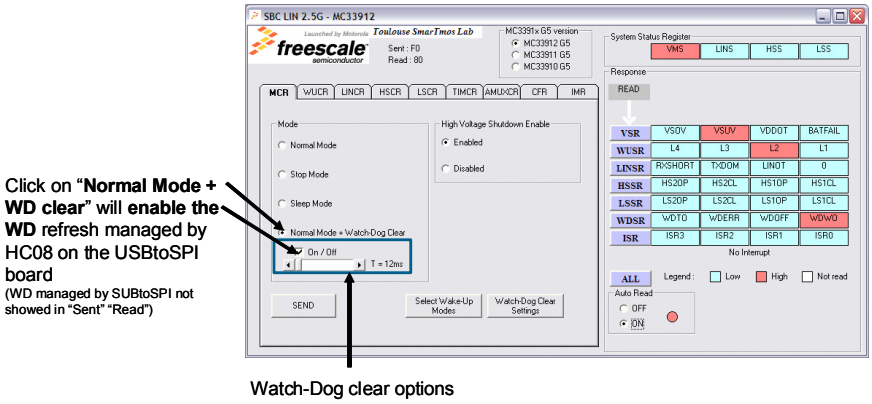


Figure 8. Panel Overview

To enter in Sleep or Stop Mode, the interface will display the different wake-up events allowed before the device enters in the low power mode:

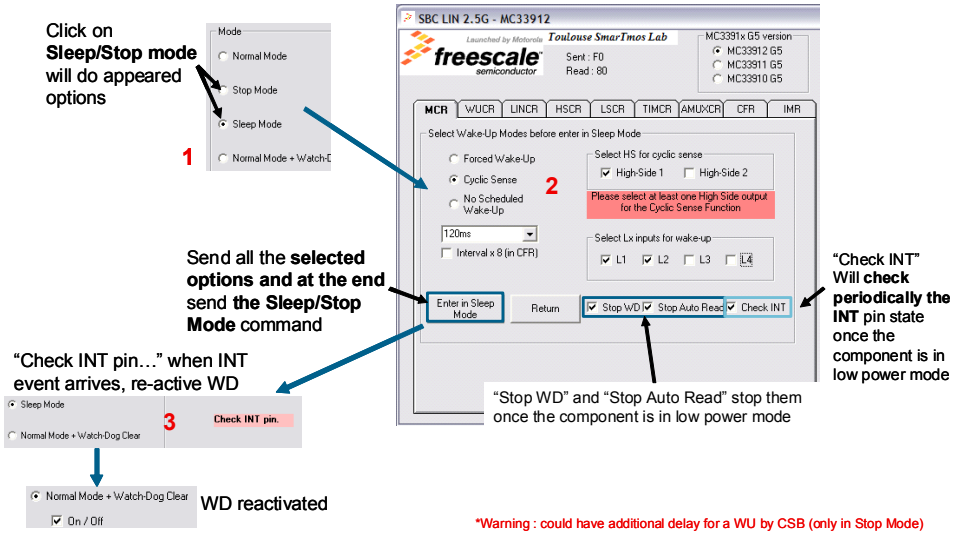


Figure 9. Sleep or Stop Modes

To use the Watchdog pre-scaler option, define the multiple factor of the period in the TIMCR register. The new watchdog period will be automatically managed by the USB-SPI board.

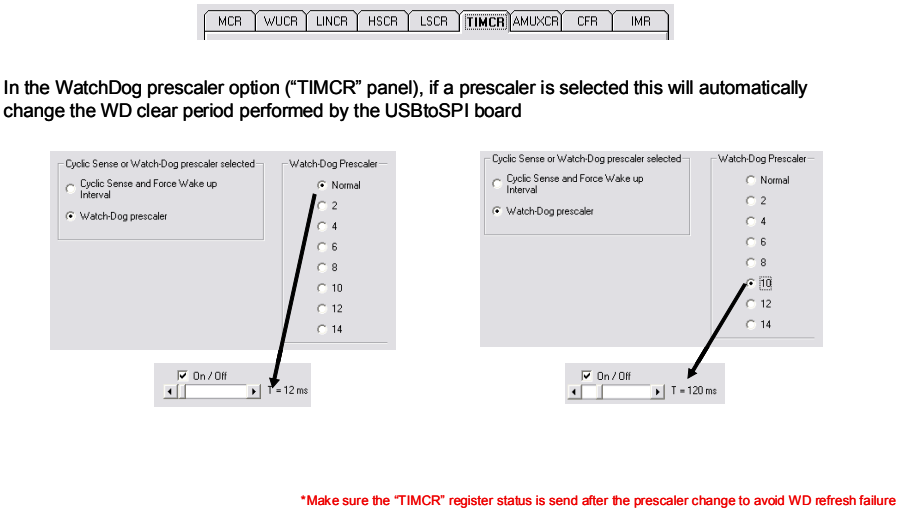


Figure 10. Watchdog Pre-scaler

8 EVB Schematic

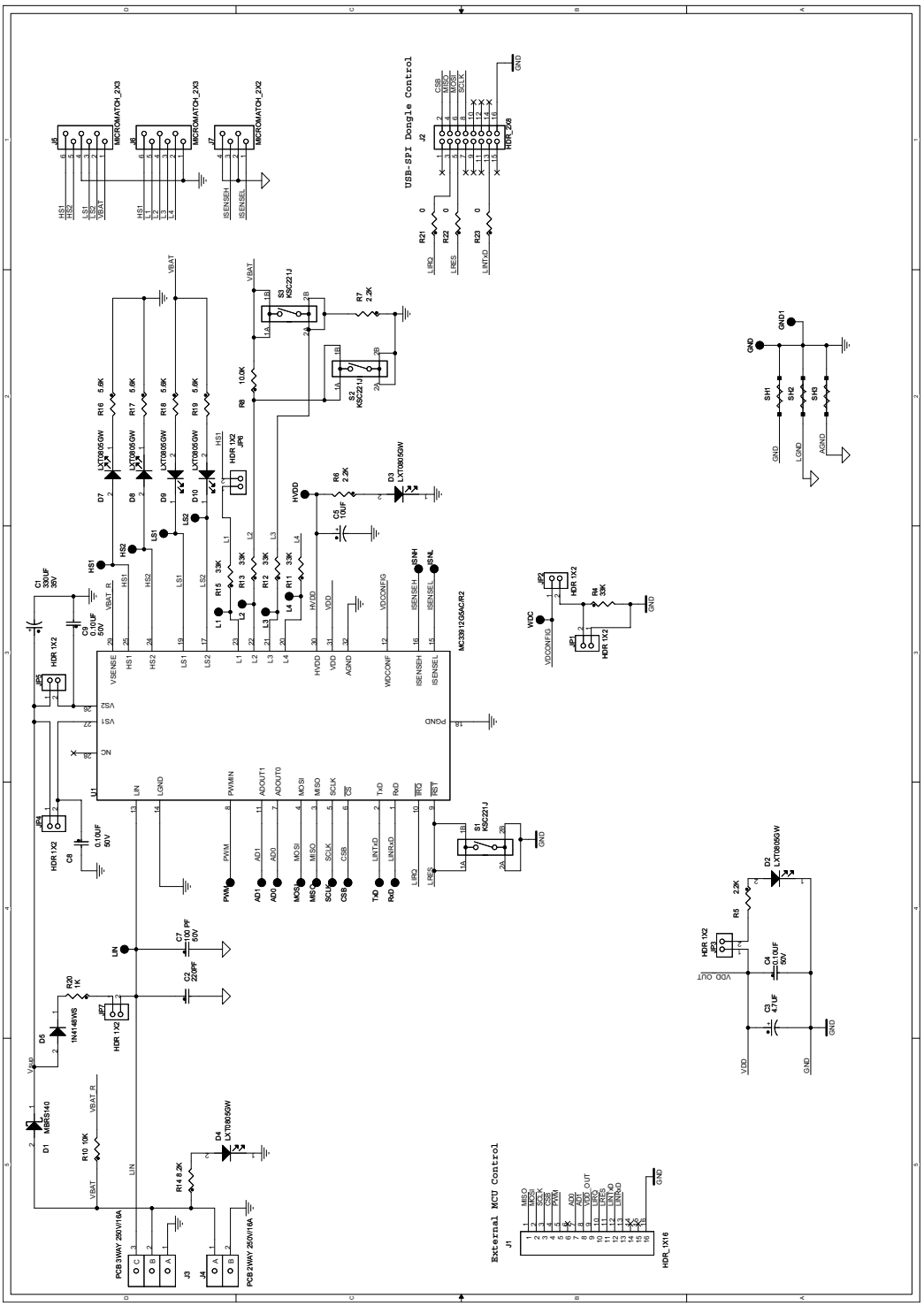


Figure 11. EVB Schematic

9 Board Layout

9.1 Assembly Layer Top

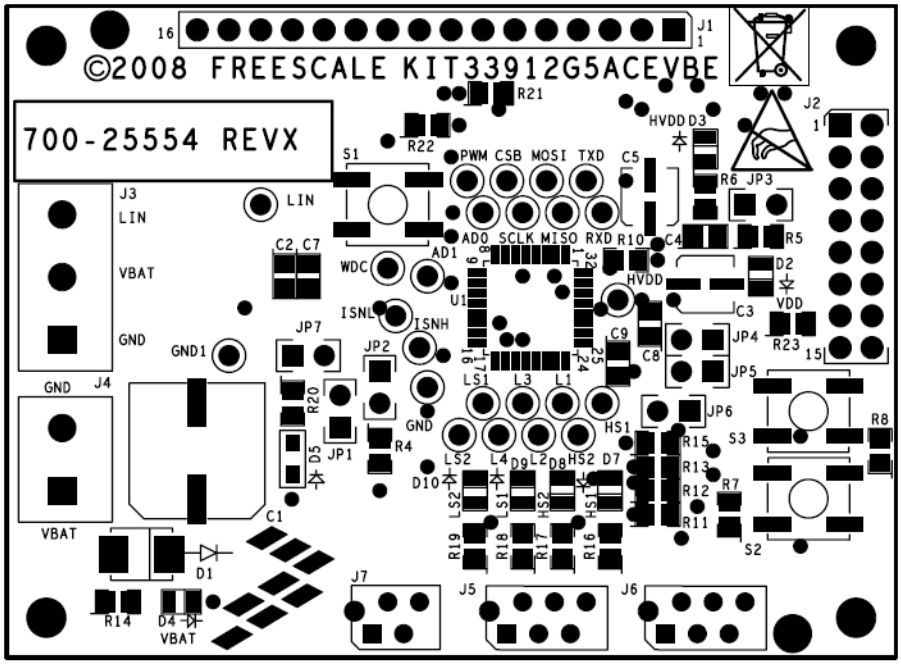


Figure 12. Assembly Layer Top

9.2 Assembly Layer Bottom

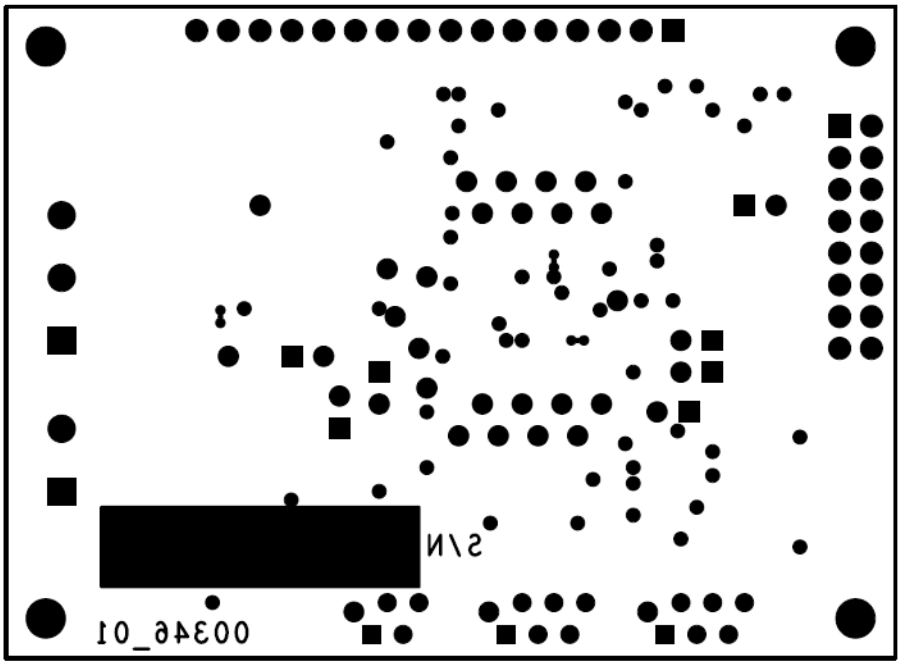


Figure 13. Assembly Layer Bottom

9.3 Top Layer Routing

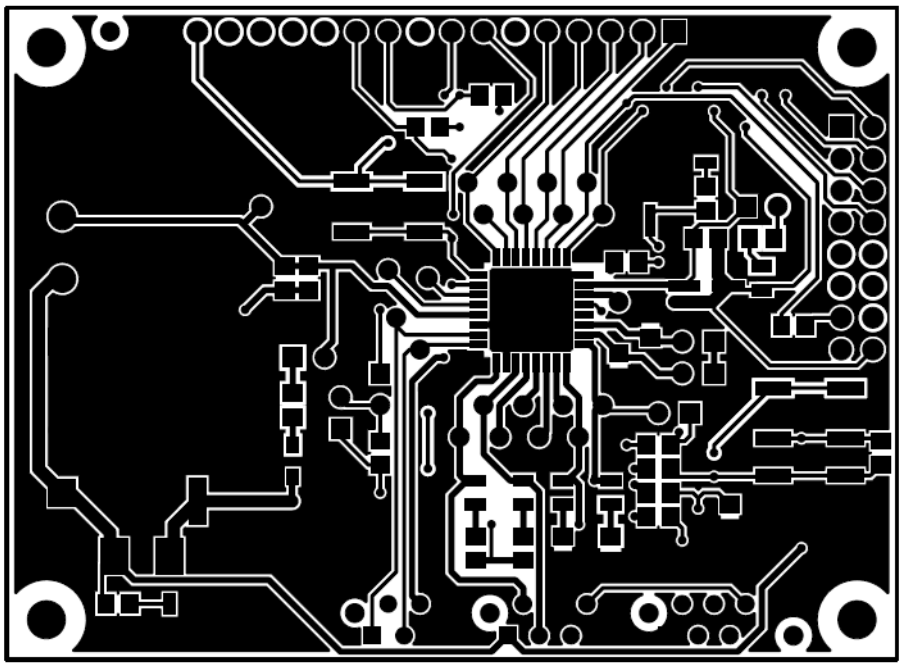


Figure 14. Top Layer Routing

9.4 Bottom Layer Routing

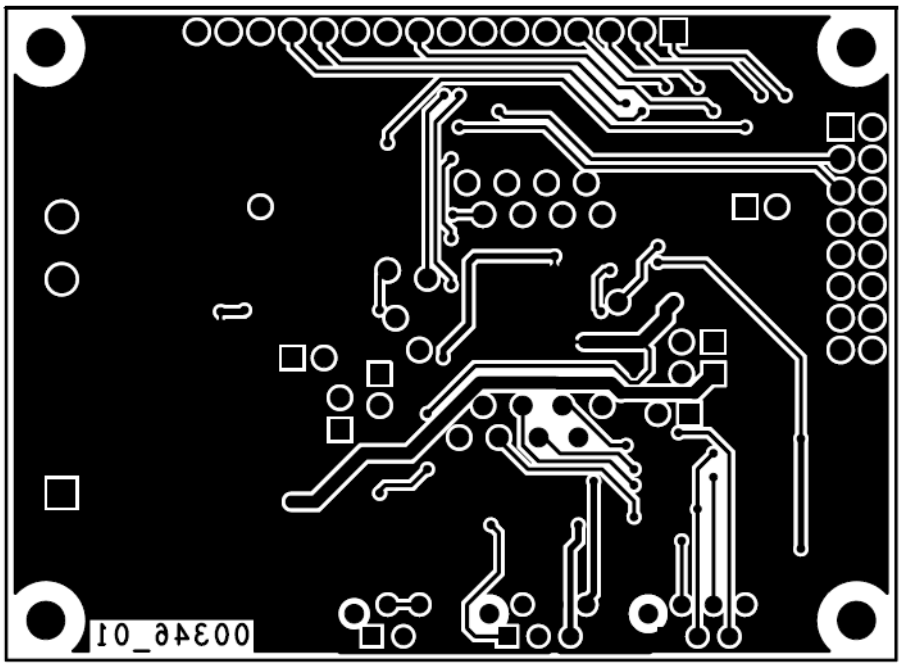


Figure 15. Bottom Layer Routing

10 KIT33912G5DGEVBE Bill of Material

KIT33912G5ACEVBE Evaluation Board				
Item	**Qty**	**Schematic Label**	**Value**	**Description**
1	23	LS1,L1,HS1,AD1,LS2,L2, HS2,L3,L4,WDC,TxD, SCLK,RxD,PWM,MOSI, MISO,LIN,ISNL,ISNH, HVDD,GND,CSB,AD0	TEST POINT BLACK	TEST POINT PIN 0.100 X 0.45 BLACK TH
2	1	C1	330UF	CAP ALEL 330UF 35V 20% -- SMT
3	1	C2	220PF	CAP CER 220PF 50V 10% X7R 0805
4	1	C3	4.7UF	CAP ALEL 4.7UF 25V 20% -- SMT
5	3	C4,C8,C9	0.10UF	CAP CER 0.10UF 50V +80%/-20% Y5V 0805
6	1	C5	10UF	CAP ALEL 10UF 16V 20% CASE B
7	1	C7	100 PF	CAP CER 100PF 50V 5% C0G 0805
8	1	D1	MBRS140	DIODE SCH PWR RECT 1A 40V SMB
9	7	D2,D3,D4,D7,D8,D9 D10	LXT0805GW	LED GRN SGL 20MA SMT 0805
10	1	D5	1N4148WS	DIODE SW 150MA 53V SOD-323
11	7	JP1,JP2,JP3,JP4,JP5,JP6, JP7	HDR 1X2	HDR 1X2 TH 100MIL SP 330H SN
12	1	J1	HDR_16X1	HDR 1X16 TH 100MIL CTR 330H AU
13	1	J2	HDR_2X8	HDR 2X8 TH 100MIL CTR 330H AU
14	1	J3	PCB 3WAY 250V/16A	CON 3 TB TH 5MM SN
15	1	J4	PCB 2WAY 250V/16A	CON 2 TB TH 5MM SN
16	2	J5,J6	CON/6MICROMATCH	CON 6 SKT TH 1.27MM CTR SN
17	1	J7	CON/4MICROMATCH	CON 4 SKT TH 1.27MM CTR SN
18	5	R4,R11,R12,R13,R15	33K	RES MF 33K 1/8W 5% 0805
19	3	R5,R6,R7	2.2K	RES MF 2.2K 1/8W 5% 0805
20	1	R8	10.0K	RES TF 10.0K 1/8W 1% RC0805
21	1	R10	10K	RES TF 10K 1/8W 5% RC0805
22	1	R14	8.2K	RES TF 8.2K 1/8W 5% RC0805
23	4	R16,R17,R18,R19	5.6K	RES MF 5.6K 1/8W 5% 0805
24	1	R20	1K	RES TF 1.0K 1/8W 5% RC0805
25	3	SH1,SH2, SH3	0 OHM	ZERO OHM CUT TRACE 0402 PADS; NO PN TO ORDER
26	3	S1,S2,S3	KSC221J	SW SPST SMT 32V 50MA J-BEND
27	1	U1	MC33912G5AC/R2	IC SBC WITH LIN XCVR LQFP32
28	7	Not Refer	Jumper	Jumper Socket
KITUSBSPIDGLEVME Evaluation Board				
Documentation Available at: http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KITUSBSPIDGLEVME				

Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application

11 References

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Desciption	Links
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12 Revision History

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	12/2009	• Initial Release

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