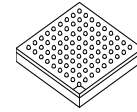




MCIMX53xD

i.MX53xD Applications Processors for Consumer Products



Package Information

Plastic Package

Case TEPBGA-2 19 x 19 mm, 0.8 mm pitch

Case FC-PBGA 12 x 12 mm PoP, 0.4 mm pitch

Ordering Information

See [Table 1 on page 3](#)

1 Introduction

The i.MX53xD multimedia application processor is Freescale Semiconductor's latest addition to a growing family of multimedia-focused products offering high performance processing optimized for lowest power consumption.

The i.MX53xD processor features Freescale's advanced implementation of the ARM™ core, which operates at clock speeds as high as 1.2 GHz and interfaces with DDR2/LVDDR2-800, LPDDR2-800, or DDR3-800 DRAM memories. This device is suitable for applications such as the following:

- Tablets
- Smart devices
- Netbooks (web tablets)
- Nettops (Internet desktop devices)
- Thin clients
- Media phones
- Internet monitors
- High-end mobile Internet devices (MID)

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

Introduction

- High-end portable media players (PMP) with HD video capability
- Portable navigation devices (PND)

The flexibility of the i.MX53xD architecture allows for its use in a wide variety of applications. As the heart of the application chipset, the i.MX53xD processor provides all the interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, camera sensors, and dual displays.

Features of the i.MX53xD processor include the following:

- Applications processor—The i.MX53xD processors boost the capabilities of high-tier portable applications by satisfying the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks such as audio decode.
- Multilevel memory system—The multilevel memory system of the i.MX53xD is based on the L1 instruction and data caches, L2 cache, internal and external memory. The i.MX53xD supports many types of external memory devices, including DDR2, low voltage DDR2, LPDDR2, DDR3, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND including eMMC up to rev 4.4.
- Smart speed technology—The i.MX53xD device has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product requiring levels of power far lower than industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX53xD processor ARM core is boosted by a multilevel cache system, Neon (including advanced SIMD, 32-bit single-precision floating point support) and vector floating point coprocessors. The system is further enhanced by a multi-standard hardware video codec, autonomous image processing unit (IPU), SD and HD720p triple video (TV) encoder with triple video DAC, and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Graphics is the key to mobile game, navigation, web browsing, and other applications. The i.MX53xD processors provide two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator (33 Mtri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance) and an OpenVG™ 1.1 2D graphics accelerator (200 Mpix/s).
- Interface flexibility—The i.MX53xD processor supports connection to a variety of interfaces, including LCD controller for two displays and CMOS sensor interface, high-speed USB on-the-go with PHY, plus three high-speed USB hosts, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I²C, and I²S serial audio, among others).
- Advanced security—The i.MX53xD processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the i.MX53xD security features contact a Freescale representative.

The i.MX53xD application processor is a follow-on to the i.MX51, with improved performance, power efficiency, and multimedia capabilities.

1.1 Ordering Information

Table 1 provides ordering information.

Table 1. Ordering Information

| Part Number | Mask Set | Features | Case Temperature Range (°C) | Package ¹ |
|---------------|----------|---------------------------|-----------------------------|--|
| MCIMX535DVV1C | N78C | 1 GHz, full feature set | -20 to +85 | 19 x 19 mm, 0.8 mm pitch BGA Case TEPBGA-2 |
| MCIMX535DVV2C | N78C | 1.2 GHz, full feature set | -20 to +85 | 19 x 19 mm, 0.8 mm pitch BGA Case TEPBGA-2 |
| SCIMX538DZK1C | N78C | 1 GHz, full feature set | -20 to +85 | 12 x 12 mm PoP, 0.4 mm pitch BGA Case FC-PBGA |

¹ Case TEPBGA-2 and FC-PBGA are RoHS compliant, lead-free MSL (moisture sensitivity level) 3.

1.2 Features

The i.MX53xD multimedia applications processor (AP) is based on the ARM Platform, which has the following features:

- MMU, L1 instruction and L1 data cache
- Unified L2 cache
- Maximum frequency of the core (including Neon, VFPv3 and L1 cache): 1–1.2 GHz
- Neon coprocessor (SIMD media processing architecture) and vector floating point (VFP-Lite) coprocessor supporting VFPv3
- TrustZone

The memory system consists of the following components:

- Level 1 cache:
 - Instruction (32 Kbyte)
 - Data (32 Kbyte)
- Level 2 cache:
 - Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
 - Boot ROM, including HAB (64 Kbyte)
 - Internal multimedia/shared, fast access RAM (128 Kbyte)
 - Secure/non-secure RAM (16 Kbyte)
- External memory interfaces:
 - 16/32-bit DDR2-800, LV-DDR2-800 or DDR3-800 up to 2 Gbyte
 - 32-bit LPDDR2
 - 8/16-bit NAND SLC/MLC Flash, up to 66 MHz, 4/8/14/16-bit ECC
 - 8/16-bit NOR Flash, PSRAM, and cellular RAM.

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- 32-bit multiplexed mode NOR Flash, PSRAM & cellular RAM.
- 8-bit Asynchronous (DTACK mode) EIM interface.
- All EIM pins are muxed on other interfaces (data with NFC pins). I/O muxing logic selects EIM port, as primary muxing at system boot.
- Samsung OneNAND™ and managed NAND including eMMC up to rev 4.4 (in muxed I/O mode)

The i.MX53xD system is built around the following system on chip interfaces:

- 64-bit AMBA AXI v1.0 bus—used by ARM platform, multimedia accelerators (such as VPU, IPU, GPU3D, GPU2D) and the external memory controller (EXTMC) operating at 200 MHz.
- 32-bit AMBA AHB 2.0 bus—used by the rest of the bus master peripherals operating at 133 MHz.
- 32-bit IP bus—peripheral bus used for control (and slow data traffic) of the most system peripheral devices operating at 66 MHz.

The i.MX53xD makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption while freeing up the CPU core for other tasks.

The i.MX53xD incorporates the following hardware accelerators:

- VPU, version 3—video processing unit
- GPU3D—3D graphics processing unit, OpenGL ES 2.0, version 3, 33 Mtri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance, 256 Kbyte RAM memory
- GPU2D—2D graphics accelerator, OpenVG 1.1, version 1, 200 Mpix/s performance,
- IPU, version 3M—image processing unit
- ASRC—asynchronous sample rate converter

The i.MX53xD includes the following interfaces to external devices:

NOTE

Not all interfaces are available simultaneously, depending on I/O multiplexer configuration.

- Hard disk drives:
 - PATA, up to U-DMA mode 5, 100 MByte/s
 - SATA I, 1.5 Gbps
- Displays:
 - Five interfaces available. Total rate of all interfaces is up to 180 Mpixels/s, 24 bpp. Up to two interfaces may be active at once.
 - Two parallel 24-bit display ports. The primary port is up to 165 Mpix/s (for example, UXGA at 60 Hz).
 - LVDS serial ports: one dual channel port up to 165 Mpix/s or two independent single channel ports up to 85 MP/s (for example, WXGA at 60 Hz) each.
 - TV-out/VGA port up to 150 Mpix/s (for example, 1080p60).
- Camera sensors:

- Two parallel 20-bit camera ports. Primary up to 180-MHz peak clock frequency, secondary up to 120-MHz peak clock frequency.
- Expansion cards:
 - Four SD/MMC card ports: three supporting 416 Mbps (8-bit i/f) and one enhanced port supporting 832 Mbps (8-bit, eMMC 4.4).
- USB
 - High-speed (HS) USB 2.0 OTG (up to 480 Mbps), with integrated HS USB PHY
 - Three USB 2.0 (480 Mbps) hosts:
 - High-speed host with integrated on-chip high-speed PHY
 - Two high-speed hosts for external HS/FS transceivers through ULPI/serial, support IC-USB
- Miscellaneous interfaces:
 - One-wire (OWIRE) port
 - Three I2S/SSI/AC97 ports, supporting up to 1.4 Mbps, each connected to audio multiplexer (AUDMUX) providing four external ports.
 - Five UART RS232 ports, up to 4.0 Mbps each. One supports 8-wire, the other four support 4-wire.
 - Two high speed enhanced CSPI (ECSPI) ports plus one CSPI port
 - Three I²C ports, supporting 400 kbps
 - Fast Ethernet controller, IEEE1588 V1 compliant, 10/100 Mbps
 - Two controller area network (FlexCAN) interfaces, 1 Mbps each
 - Sony Phillips Digital Interface (SPDIF), Rx and Tx
 - Enhanced serial audio interface (ESAI), up to 1.4 Mbps each channel
 - Key pad port (KPP)
 - Two pulse-width modulators (PWM)
 - GPIO with interrupt capabilities

The system supports efficient and smart power control and clocking:

- Supporting DVFS (dynamic voltage and frequency scaling) technique for low power modes
- Power gating SRPG (State Retention Power Gating) for ARM core and Neon
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip oscillator amplifier supporting 32.768 kHz external crystal
- On-chip LDO voltage regulators for PLLs

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on)
- Secure JTAG controller (SJC)—Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features

Introduction

- Secure real-time clock (SRTC)—Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches
- Real-time integrity checker, version 3 (RTICv3)—RTIC type1, enhanced with SHA-256 engine
- SAHARAv4 Lite—Cryptographic accelerator that includes true random number generator (TRNG)
- Security controller, version 2 (SCCv2)—Improved SCC with AES engine, secure/non-secure RAM and support for multiple keys as well as TZ/non-TZ separation
- Central security unit (CSU)—Enhancement for the IIM (IC Identification Module). CSU is configured during boot by e-fuses, and determines the security level operation mode as well as the TrustZone (TZ) policy
- Advanced High Assurance Boot (A-HAB)—HAB with the following embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization

NOTE

The actual feature set depends on the part number as described in [Table 1](#). Functions such as video hardware acceleration with 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX53xD processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX53xD processor system.

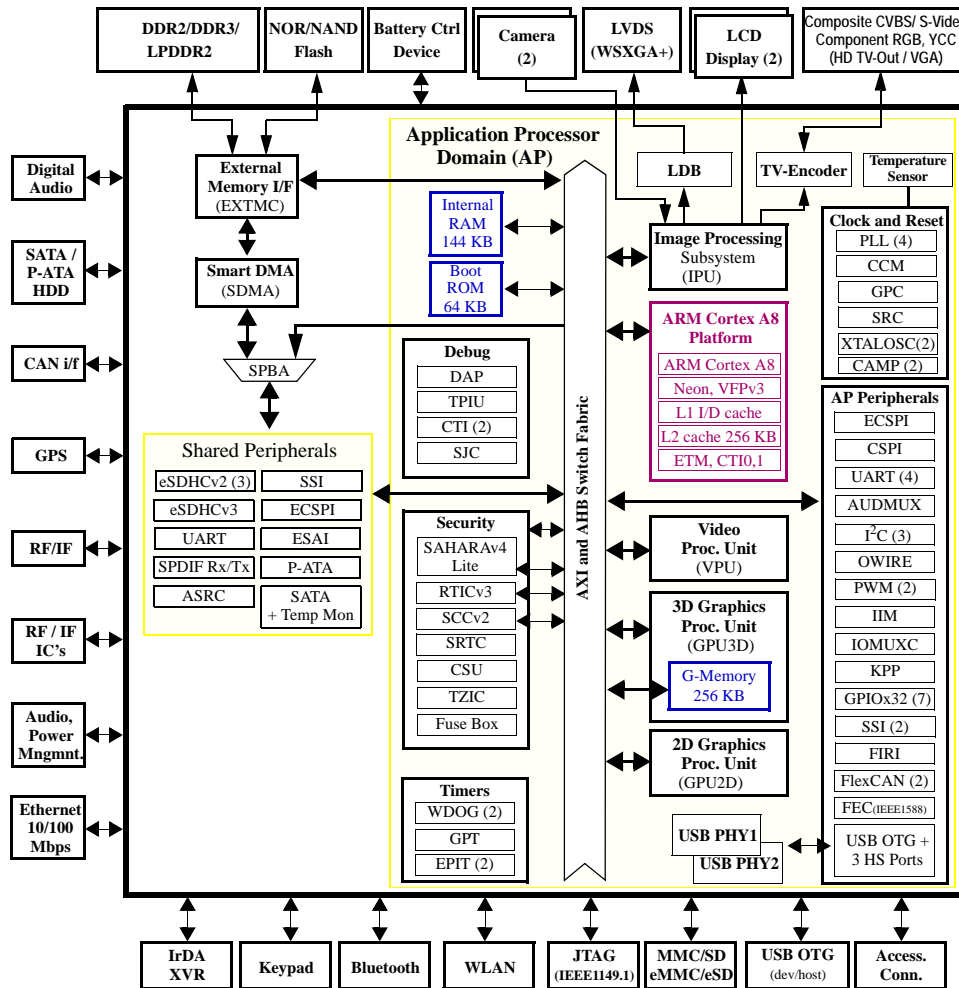


Figure 1. i.MX53xD System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (2) indicates two separate PWM peripherals.

3 Modules List

The i.MX53xD processor contains a variety of digital and analog modules. [Table 2](#) describes these modules in alphabetical order.

Table 2. i.MX53xD Digital and Analog Blocks

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------------------|--|-----------------------------------|---|
| ARM | ARM Platform | ARM | The ARM Cortex™ A8 platform consists of the ARM processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, Level 2 cache controller and a 256 Kbyte L2 cache. The platform also contains an event monitor and debug modules. It also has a NEON coprocessor with SIMD media processing architecture, a register file with 32/64-bit general-purpose registers, an integer execute pipeline (ALU, Shift, MAC), dual single-precision floating point execute pipelines (FADD, FMUL), a load/store and permute pipeline and a non-pipelined vector floating point (VFP Lite) coprocessor supporting VFPv3. |
| ASRC | Asynchronous Sample Rate Converter | Multimedia Peripherals | The asynchronous sample rate converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. |
| AUDMUX | Digital Audio Multiplexer | Multimedia Peripherals | The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports. |
| CAMP-1 CAMP-2 | Clock Amplifier | Clocks, Resets, and Power Control | Clock amplifier |
| CCM GPC SRC | Clock Control Module Global Power Controller System Reset Controller | Clocks, Resets, and Power Control | These modules are responsible for clock and reset distribution in the system, as well as for system power management. The system includes four PLLs. |
| CSPI ECSPI-1 ECSPI-2 | Configurable SPI, Enhanced CSPI | Connectivity Peripherals | Full-duplex enhanced synchronous serial interface, with data rates 16-60 Mbit/s. It is configurable to support master/slave modes. In Master mode it supports four slave selects for multiple peripherals. |
| CSU | Central Security Unit | Security | The central security unit (CSU) is responsible for setting comprehensive security policy within the i.MX53xD platform, and for sharing security information between the various security modules. The security control registers (SCR) of the CSU are set during boot time by the high assurance boot (HAB) code and are locked to prevent further writing. |

Table 2. i.MX53xD Digital and Analog Blocks (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|------------------|-----------------------------------|--------------------------|--|
| DEBUG | Debug System | System Control | <p>The debug system provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView).</p> <p>Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, three cross-system triggers (CTI), counters, and sequencers.</p> <p>debug access port (DAP)— The DAP provides real-time access for the debugger without halting the core to system memory, peripheral register, debug configuration registers and JTAG scan chains.</p> |
| EXTMC | External Memory Controller | Connectivity Peripherals | <p>The EXTMC is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels, fast memories (DDR2/DDR3/LPDDR2) channel, slow memories (NOR-FLASH / PSRAM / NAND-FLASH etc.) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) channel.</p> <p>In order to increase the bandwidth performance, the EXTMC separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses.</p> <p>EXTMC Features:</p> <ul style="list-style-type: none"> • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (read or write) was the last access • Flexible bank interleaving • Support 16/32-bit DDR2-800 or DDR3-800 or LPDDR2. • Support up to 2 GByte DDR memories. • Support NFC, EIM signal muxing scheme. • Support 8/16/32-bit Nor-Flash/PSRAM memories (sync and async operating modes), at slow frequency. (8-bit is not supported on D[23]-D[16]). • Support 4/8/14/16-bit ECC, page sizes of 512-B, 2-KB and 4-KB Nand-Flash (including MLC) • Multiple chip selects (up to 4). • Enhanced DDR memory controller, supporting access latency hiding • Support watermark for security (internal and external memories) |
| EPIT-1 EPIT-2 | Enhanced Periodic Interrupt Timer | Timer Peripherals | <p>Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.</p> |
| ESAI | Enhanced Serial Audio Interface | Connectivity Peripherals | <p>The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors.</p> <p>The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.</p> <p>The ESAI has 12 pins for data and clocking connection to external devices.</p> |

Table 2. i.MX53xD Digital and Analog Blocks (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|-------------------------------------|--|--------------------------|--|
| ESDHCV3-3 | Ultra-High-Speed eMMC / SD Host Controller | Connectivity Peripherals | Ultra high-speed eMMC / SD host controller, enhanced to support eMMC 4.4 standard specification, for 832 MBps. <ul style="list-style-type: none"> Port 3 is specifically enhanced to support eMMC 4.4 specification, for double data rate (832 Mbps, 8-bit port). ESDHCV3 is backward compatible to ESDHCV2 and supports all the features of ESDHCV2 as described below. |
| ESDHCV2-1 ESDHCV2-2 ESDHCv2-4 | Enhanced Multi-Media Card / Secure Digital Host Controller | | Enhanced multimedia card / secure digital host controller <ul style="list-style-type: none"> Ports 1, 2, and 4 are compatible with the “MMC System Specification” version 4.3, full support and supporting 1, 4 or 8-bit data. The generic features of the eSDHCv2 module, when serving as SD / MMC host, include the following: <ul style="list-style-type: none"> Can be configured either as SD / MMC controller Supports eSD and eMMC standard, for SD/MMC embedded type cards Conforms to SD Host Controller Standard Specification, version 2.0, full support. Compatible with the SD Memory Card Specification, version 1.1 Compatible with the SDIO Card Specification, version 1.2 Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards Configurable to work in one of the following modes: <ul style="list-style-type: none"> —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit Full/high speed mode. Host clock frequency variable between 32 kHz to 52 MHz Up to 200 Mbps data transfer for SD/SDIO cards using 4 parallel data lines Up to 416 Mbps data transfer for MMC cards using 8 parallel data lines |
| FEC | Fast Ethernet Controller | Connectivity Peripherals | The Ethernet media access controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX53xD also consists of HW assist for IEEE1588™ standard. See, TSU and CE_RTC (IEEE1588) section for more details. |
| FIRI | Fast Infrared Interface | Connectivity Peripherals | Fast infrared interface |
| FLEXCAN-1 FLEXCAN-2 | Flexible Controller Area Network | Connectivity Peripherals | The controller area network (CAN) protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus. Meets the following specific requirements of this application: real-time processing, reliable operation in the EXTMC environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN is a full implementation of the CAN protocol specification, Version 2.0 B (ISO 11898), which supports both standard and extended message frames at 1 Mbps. |

Table 2. i.MX53xD Digital and Analog Blocks (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--|-----------------------------|----------------------------|---|
| GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7 | General Purpose I/O Modules | System Control Peripherals | These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O. |
| GPT | General Purpose Timer | Timer Peripherals | Each GPT is a 32-bit “free-running” or “set and forget” mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock. |
| GPU3D | Graphics Processing Unit | Multimedia Peripherals | The GPU, version 3, provides hardware acceleration for 2D and 3D graphics algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution. It supports color representation up to 32 bits per pixel. GPU enables high-performance mobile 3D and 2D vector graphics at rates up to 33 Mtriangles/s, 200 Mpix/s, 800 Mpix/s (z). |
| GPU2D | Graphics Processing Unit-2D | Multimedia Peripherals | The GPU2D version 1, provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution. |
| I2C-1 I2C-2 I2C-3 | I ² C Controller | Connectivity Peripherals | I ² C provides serial interface for controlling peripheral devices. Data rates of up to 400 kbps are supported. |
| IIM | IC Identification Module | Security | <p>The IC identification module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module.</p> <p>IIM interfaces to the electrical fuse array (split to banks). Enabled to set up boot modes, security levels, security keys and many other system parameters.</p> <p>i.MX53xDA consists of 4 x 256-bit + 1 x 128-bit fuse-banks (total 1152 bits) through IIM interface.</p> |

Table 2. i.MX53xD Digital and Analog Blocks (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------|------------------------|----------------------------|---|
| IOMUXC | IOMUX Control | System Control Peripherals | This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable. |
| IPU | Image Processing Unit | Multimedia Peripherals | Version 3M IPU enables connectivity to displays, relevant processing and synchronization. It supports two display ports and two camera ports, through the following interfaces: <ul style="list-style-type: none"> • Legacy parallel interfaces • Single/dual channel LVDS display interface • Analog TV or VGA interfaces The processing includes: <ul style="list-style-type: none"> • Image enhancement—color adjustment and gamut mapping, gamma correction and contrast enhancement • Video/graphics combining • Support for display backlight reduction • Image conversion—resizing, rotation, inversion and color space conversion • Hardware de-interlacing support • Synchronization and control capabilities, allowing autonomous operation. |
| KPP | Keypad Port | Connectivity Peripherals | The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: <ul style="list-style-type: none"> • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection |
| LDB | LVDS Display Bridge | Connectivity Peripherals | LVDS display bridge is used to connect the IPU (image processing unit) to external LVDS display interface. LDB supports two channels; each channel has following signals: <ul style="list-style-type: none"> • 1 clock pair • 4 data pairs On-chip differential drivers are provided for each pair. |
| OWIRE | One-Wire Interface | Connectivity Peripherals | One-wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example, Dallas DS2502. |
| PATA | Parallel ATA | Connectivity Peripherals | The PATA block is a AT attachment host interface. Its main use is to interface with hard disk drives and optical disc drives. It interfaces with the ATA-6 compliant device over a number of ATA signals. It is possible to connect a bus buffer between the host side and the device side. |
| PWM-1 PWM-2 | Pulse Width Modulation | Connectivity Peripherals | The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound. |
| INTRAM | Internal RAM | Internal Memory | Internal RAM, shared with VPU. The on-chip memory controller (OCRAM) module, is an interface between the system's AXI bus, to the internal (on-chip) SRAM memory module. It is used for controlling the 128 KB multimedia RAM, through a 64-bit AXI bus. |
| BOOTROM | Boot ROM | Internal Memory | Supports secure and regular boot modes. The ROM controller supports ROM patching. |

Table 2. i.MX53xD Digital and Analog Blocks (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------|-----------------------------|----------------------------|---|
| RTIC | Run-Time Integrity Checker | Security | Protecting read only data from modification is one of the basic elements in trusted platforms. The run-time integrity checker, version 3 (RTIC) block is a data-monitoring device responsible for ensuring that the memory content is not corrupted during program execution. The RTIC mechanism periodically checks the integrity of code or data sections during normal OS run-time execution without interfering with normal operation. The purpose of the RTIC is to ensure the integrity of the peripheral memory contents, protect against unauthorized external memory elements replacement and assist with boot authentication. |
| SAHARA | SAHARA Security Accelerator | Security | SAHARA (symmetric/asymmetric hashing and random accelerator), version 4, is a security coprocessor. It implements symmetric encryption algorithms, (AES, DES, 3DES, RC4 and C2), public key algorithms (RSA and ECC), hashing algorithms (MD5, SHA-1, SHA-224 and SHA-256), and a hardware true random number generator. It has a slave IP Bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory. |
| SATA | Serial ATA | Connectivity Peripherals | SATA HDD interface, includes the SATA controller and the PHY. It is a complete mixed-signal IP solution for SATA HDD connectivity. |
| SCCv2 | Security Controller, ver. 2 | Security | The security controller is a security assurance hardware module designed to safely hold sensitive data, such as encryption keys, digital right management (DRM) keys, passwords and biometrics reference data. The SCCv2 monitors the system's alert signal to determine if the data paths to and from it are secure, that is, it cannot be accessed from outside of the defined security perimeter. If not, it erases all sensitive data on its internal RAM. The SCCv2 also features a key encryption module (KEM) that allows non-volatile (external memory) storage of any sensitive data that is temporarily not in use. The KEM utilizes a device-specific hidden secret key and a symmetric cryptographic algorithm to transform the sensitive data into encrypted data. |
| SDMA | Smart Direct Memory Access | System Control Peripherals | The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off loading various cores in dynamic data routing. The SDMA features list is as follows: <ul style="list-style-type: none"> • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (copy mode) • Up to 8-word buffer for configurable burst transfers to / from the EXTMC • Support of byte swapping and CRC calculations • A library of scripts and API is available |

Table 2. i.MX53xD Digital and Analog Blocks (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|-------------------------|--------------------------------|----------------------------|---|
| SECRAM | Secure / Non-secure RAM | Internal Memory | Secure / non-secure Internal RAM, controlled by SCC. |
| SJC | Secure JTAG Interface | System Control Peripherals | JTAG manipulation is a known hacker's method of executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The JTAG port provides a debug access to several hardware blocks including the ARM processor and the system bus. The JTAG port must be accessible during platform initial laboratory bring-up, manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. However, in order to properly secure the system, unauthorized JTAG usage should be strictly forbidden. In order to prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the i.MX53xD processor incorporates a mechanism for regulating JTAG access. SJC provides four different JTAG security modes that can be selected through an e-fuse configuration. |
| SPBA | Shared Peripheral Bus Arbiter | System Control Peripherals | SPBA (shared peripheral bus arbiter) is a two-to-one IP bus interface (IP bus) arbiter. |
| SPDIF | Sony Philips Digital Interface | Multimedia Peripherals | A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Both transmitter and receiver functionalists are supported. |
| SRTC | Secure Real Time Clock | Security | The SRTC incorporates a special system state retention register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC_POW. The NVCC_SRTC_POW can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR mark the event (security violation indication). |
| SSI-1 SSI-2 SSI-3 | I2S/SSI/AC97 Interface | Connectivity Peripherals | The SSI is a full-duplex synchronous interface used on the i.MX53xDA processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously. |

Table 2. i.MX53xD Digital and Analog Blocks (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|--|--------------------------------------|----------------------------|---|
| IPTP | IEEE1588 Precision Time Protocol | Connectivity Peripherals | <p>The IEEE 1588-2002 (version 1) standard defines a precision time protocol (PTP) - which is a time-transfer protocol that enables synchronization of networks (for example, Ethernet), to a high degree of accuracy and precision.</p> <p>The IEEE1588 hardware assist is composed of the two blocks: time stamp unit and real time clock, which provide the timestamping protocol's functionality, generating and reading the needed timestamps.</p> <p>The hardware-assisted implementation delivers more precise clock synchronization at significantly lower CPU load compared to purely software implementations.</p> |
| Temperature Monitor | (Part of SATA Block) | System Control Peripherals | The temperature sensor is an internal module to the i.MX53xD that monitors the die temperature. The monitor is capable in generating SW interrupt, or trigger the CCM, to reduce the core operating frequency. |
| TVE | TV Encoder | Multimedia | The TV encoder, version 2.1 is implemented in conjunction with the image processing unit (IPU) allowing handheld devices to display captured still images and video directly on a TV or LCD projector. It supports composite PAL/NTSC, VGA, S-video, and component up to HD1080p analog video outputs. |
| TZIC | TrustZone Aware Interrupt Controller | ARM/Control | The TrustZone interrupt controller (TZIC) collects interrupt requests from all i.MX53xD sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported. |
| UART-1 UART-2 UART-3 UART-4 UART-5 | UART Interface | Connectivity Peripherals | <p>Each of the UART blocks supports the following serial data transmit/receive protocols and configurations:</p> <ul style="list-style-type: none"> • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE |
| USB | USB Controller | Connectivity Peripherals | <p>USB supports USB2.0 480 MHz, and contains:</p> <ul style="list-style-type: none"> • One high-speed OTG sub-block with integrated HS USB PHY • One high-speed host sub-block with integrated HS USB PHY • Two identical high-speed Host modules <p>The high-speed OTG module, which is internally connected to the HS USB PHY, is equipped with transceiver-less logic to enable on-board USB connectivity without USB transceivers</p> <p>All the USB ports are equipped with standard digital interfaces (ULPI, HS IC-USB) and transceiver-less logic to enable onboard USB connectivity without USB transceivers.</p> |

Table 2. i.MX53xD Digital and Analog Blocks (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------|-----------------------------------|------------------------|---|
| VPU | Video Processing Unit | Multimedia Peripherals | <p>A high-performing video processing unit (VPU) version 3, which covers many SD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing such as rotation and mirroring.</p> <p>VPU Features:</p> <ul style="list-style-type: none"> • MPEG-2 decode, Mail-High profile, up to 1080i/p resolution, 40 Mbps bit rate • MPEG4/XviD decode, SP/ASP profile, up to 1080 i/p resolution, 40 Mbps bit rate • H.263 decode, P0/P3 profile, up to 16CIF resolution, 20 Mbps bit rate • H.264 decode, BP/MP/HP profile, up to 1080 i/p resolution, 40 Mbps bit rate • VC1 decode, SP/MP/AP profile, up to 1080 i/p resolution, 40 Mbps bit rate • RV10 decode, 8/9/2010 profile, up to 1080 i/p resolution, 40 Mbps bit rate • DivX decode, 3/4/5/6 profile, up to 1080 i/p resolution, 40 Mbps bit rate • MJPEG decode, Baseline profile, up to 8192 x 8192 resolution, 40 Mpixel/s bit rate for 4:4:4 format • MPEG2¹ encode, Main-Main profile, up to D1 resolution, 15 Mbps bit rate • MPEG4 encode, Simple profile, up to 720p resolution, 12 Mbps bit rate² • H.263 encode, P0/P3 profile, up to 4CIF resolution, 8 Mbps bit rate² • H.264 encode, Baseline profile, up to 720p resolution, 14 Mbps bit rate² • MJPEG encode, Baseline profile, up to 8192 x 8192 resolution, 80 Mpixel/s bit rate for 4:2:2 format |
| WDOG-1 | Watch Dog | Timer Peripherals | The watch dog timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line. |
| WDOG-2 (TZ) | Watch Dog (TrustZone) | Timer Peripherals | The TrustZone watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. This situation should be avoided, as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW. |
| XTALOSC | 24 MHz Crystal Oscillator | Clocking | Provides a crystal oscillator amplifier that supports a 24-MHz external crystal |
| XTALOSC_32K | 32.768 kHz Crystal Oscillator I/F | Clocking | Provides a crystal oscillator amplifier that supports a 32.768-kHz external crystal. |

¹ Video partially performed in hardware accelerator (70%) and partially in software.

² VPU can generate higher bit rate than the maximum specified by the corresponding standard.

3.1 Special Signal Considerations

The package contact assignments can be found in [Section 6, “Package Information and Contact Assignments.”](#) Signal descriptions are defined in the i.MX53 Reference Manual. Special signal considerations information is contained in Chapter 1 of *i.MX53 System Development User's Guide* (MX53UG).

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX53xD processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See [Table 3](#) for a quick reference to the individual tables and sections.

Table 3. i.MX53xD Chip-Level Conditions

| For these characteristics, ... | Topic appears ... |
|--|-------------------------------------|
| Absolute Maximum Ratings | Table 4 on page 17 |
| TEPBGA-2 Package Thermal Resistance Data | Table 5 on page 18 |
| i.MX53xD Operating Ranges | Table 7 on page 20 |
| External Clock Sources | Table 8 on page 22 |
| Maximal Supply Currents | Table 9 on page 23 |
| USB Interface Current Consumption | Table 10 on page 25 |

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under [Table 4](#) may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges table is not implied.

Table 4. Absolute Maximum Ratings

| Parameter Description | Symbol | Min | Max | Unit |
|--------------------------------|--------------------------------|------|------|------|
| Peripheral Core Supply Voltage | VCC | -0.3 | 1.35 | V |
| ARM Core Supply Voltage | VDDGP | -0.3 | 1.4 | V |
| Supply Voltage UHVIO | Supplies denoted as I/O Supply | -0.5 | 3.6 | V |
| Supply Voltage for non UHVIO | Supplies denoted as I/O Supply | -0.5 | 3.3 | V |
| USB VBUS | VBUS | — | 5.25 | V |

Table 4. Absolute Maximum Ratings (continued)

| Parameter Description | Symbol | Min | Max | Unit |
|---|------------------|--------|------------------------|------|
| Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins | USB_DP/USB_DN | -0.3 | 3.63 ¹ | V |
| Input/Output Voltage Range | V_{in}/V_{out} | -0.5 | OVDD +0.3 ² | V |
| ESD Damage Immunity: • Human Body Model (HBM) • Charge Device Model (CDM) | V_{esd} | — — | 2000 500 | V |
| Storage Temperature Range | $T_{STORAGE}$ | -40 | 150 | °C |

¹ USB_DN and USB_DP can tolerate 5 V for up to 24 hours.

² The term OVDD in this section refers to the associated supply rail of an input or output. The association is described in Table 112 on page 151. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance

4.1.2.1 TEPBGA-2 Package Thermal Resistance

Table 5 provides the TEPBGA-2 package thermal resistance data.

Table 5. TEPBGA-2 Package Thermal Resistance Data

| Rating | Board | Symbol | Value | Unit |
|---|-------------------------|------------------|-------|------|
| Junction to Ambient (natural convection) ^{1, 2} | Single layer board (1s) | $R_{\theta JA}$ | 28 | °C/W |
| Junction to Ambient (natural convection) ^{1, 2, 3} | Four layer board (2s2p) | $R_{\theta JA}$ | 16 | °C/W |
| Junction to Ambient (at 200 ft/min) ^{1, 3} | Single layer board (1s) | $R_{\theta JMA}$ | 21 | °C/W |
| Junction to Ambient (at 200 ft/min) ^{1, 3} | Four layer board (2s2p) | $R_{\theta JMA}$ | 13 | °C/W |
| Junction to Board ⁴ | — | $R_{\theta JB}$ | 6 | °C/W |
| Junction to Case ⁵ | — | $R_{\theta JC}$ | 4 | °C/W |
| Junction to Package Top (natural convection) ⁶ | — | Ψ_{JT} | 4 | °C/W |

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.1.2.2 PoP Package Thermal Resistance

Table 6 provides the PoP package thermal resistance data.

Table 6. PoP Package Thermal Resistance Data¹

| Rating | Board | Symbol | As designed | Center Array of Pillars used for Ground | Unit |
|---|-------------------------|------------------|-------------|---|------|
| Junction to Ambient (natural convection) ^{2, 3} | Single layer board (1s) | $R_{\theta JA}$ | 45 | 45 | °C/W |
| Junction to Ambient (natural convection) ^{2, 3, 4} | Four layer board (2s2p) | $R_{\theta JA}$ | 23 | 22 | °C/W |
| Junction to Ambient (at 200 ft/min) ^{2, 4} | Single layer board (1s) | $R_{\theta JMA}$ | 36 | 35 | °C/W |
| Junction to Ambient (at 200 ft/min) ^{2, 4} | Four layer board (2s2p) | $R_{\theta JMA}$ | 19 | 18 | °C/W |
| Junction to Board ⁵ | — | $R_{\theta JB}$ | 8.4 | 7.2 | °C/W |
| Junction to Case ⁶ | — | $R_{\theta JC}$ | <0.1 | <0.1 | °C/W |
| Junction to Package Top (natural convection) ⁷ | — | Ψ_{JT} | 2 | 2 | °C/W |

¹ Calculated for just the i.MX53xD package, without the top mounted memory package.

² Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

³ Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

⁴ Per JEDEC JESD51-6 with the board horizontal.

⁵ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁶ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁷ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.1.3 Operating Ranges

Table 7 provides the operating ranges of i.MX53xD processor.

Table 7. i.MX53xD Operating Ranges

| Symbol | Parameter | Minimum ¹ | Nominal ² | Maximum ¹ | Unit |
|--------------------------|--|----------------------|----------------------|----------------------|------|
| VDDGP ³ | ARM core supply voltage $f_{\text{ARM}} \leq 167$ MHz | 0.85 | 0.9 | 0.95 | V |
| | ARM core supply voltage $f_{\text{ARM}} \leq 400$ MHz | 0.9 | 0.95 | 1.05 | V |
| | ARM core supply voltage $f_{\text{ARM}} \leq 800$ MHz | 1.05 | 1.1 | 1.15 | V |
| | ARM core supply voltage $f_{\text{ARM}} \leq 1000$ MHz | 1.2 | 1.25 | 1.3 | V |
| | ARM core supply voltage $f_{\text{ARM}} \leq 1200$ MHz ⁴ | 1.30 | 1.35 | 1.40 | V |
| | ARM core supply voltage Stop mode | 0.8 | 0.85 | 1.3 | V |
| VCC | Peripheral supply voltage ⁵ | 1.25 | 1.3 | 1.35 | V |
| | Peripheral supply voltage—Stop mode | 0.9 | 0.95 | 1.35 | V |
| VDDA ⁶ | Memory arrays voltage | 1.25 | 1.30 | 1.35 | V |
| | Memory arrays voltage—Stop mode | 0.9 | 0.95 | 1.35 | V |
| VDDAL1 ⁶ | L1 Cache Memory arrays voltage | 1.25 | 1.30 | 1.35 | V |
| | L1 Cache Memory arrays voltage—Stop mode | 0.9 | 0.95 | 1.35 | V |
| VDD_DIG_PLL ⁷ | PLL Digital supplies—external regulator option | 1.25 | 1.3 | 1.35 | V |
| VDD_ANA_PLL ⁸ | PLL Analog supplies—external regulator option | 1.75 | 1.8 | 1.95 | V |
| NVCC_CKIH | ESD protection of the CKIH pins, FUSE read Supply and 1.8V bias for the UHVIO pads | 1.65 | 1.8 | 1.95 | V |
| NVCC_LCD NVCC_JTAG | GPIO digital power supplies | 1.65 | 1.8 or 2.775 | 3.1 | V |
| NVCC_LVDS | LVDS interface Supply | 2.25 | 2.5 | 2.75 | V |
| NVCC_LVDS_BG | LVDS Band Gap Supply | 2.25 | 2.5 | 2.75 | V |
| NVCC_EMI_DRAM | DDR Supply DDR2 range | 1.7 | 1.8 | 1.9 | V |
| | DDR Supply LPDDR2 range | 1.14 | 1.2 | 1.3 | |
| | DDR Supply LV-DDR2 range | 1.47 | 1.55 | 1.63 | |
| | | 1.42 | 1.5 | 1.58 | |
| DDR Supply DDR3 range | 1.42 | 1.5 | 1.58 | | |
| VDD_FUSE ⁹ | Fusebox Program Supply (Write Only) | 3.0 | — | 3.3 | V |

Table 7. i.MX53xD Operating Ranges (continued)

| Symbol | Parameter | Minimum ¹ | Nominal ² | Maximum ¹ | Unit |
|--|--|----------------------|----------------------|----------------------|------|
| NVCC_NANDF NVCC_SD1 NVCC_SD2 NVCC_PATA NVCC_KEYPAD NVCC_GPIO NVCC_FEC NVCC_EIM_MAIN NVCC_EIM_SEC NVCC_CSI | Ultra High voltage I/O (UHVIO) supplies: • UHVIO_L • UHVIO_H • UHVIO_UH | 1.65 | 1.8 | 1.95 | V |
| | | 2.5 | 2.775 | 3.1 | |
| | | 3.0 | 3.3 | 3.6 | |
| TVDAC_DHVDD ¹⁰ TVDAC_AHVDDRGB ¹⁰ | TVE digital and analog power supply, TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel For GPIO use only, when TVE is not in use | 2.69 | 2.75 | 2.91 | V |
| NVCC_SRTC_POW | SRTC Core and slow I/O Supply (GPIO) ¹¹ | 1.25 | 1.3 | 1.35 | V |
| NVCC_RESET | LVIO | 1.65 | 1.8 or 2.775 | 3.1 | V |
| USB_H1_VDDA25 USB_OTG_VDDA25 NVCC_XTAL | USB_PHY analog supply, oscillator amplifier analog supply ¹² | 2.25 | 2.5 | 2.75 | V |
| USB_H1_VDDA33 USB_OTG_VDDA33 | USB PHY I/O analog supply | 3.0 | 3.3 | 3.6 | V |
| VBUS | See Table 4 on page 17 and Table 105 on page 143 for details. Note that this is not a power supply. | — | — | — | — |
| VDD_REG ¹³ | Power supply input for the integrated linear regulators | 2.37 | 2.5 | 2.63 | V |
| VP | SATA PHY core power supply | 1.25 | 1.3 | 1.35 | V |
| VPH | SATA PHY I/O supply voltage | 2.25 | 2.5 | 2.75 | V |
| Tj | Junction temperature | -20 | 95 ¹⁴ | 105 | °C |

¹ Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

² The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

³ A voltage transition is allowed for the required supply ramp up to the nominal value prior to achieving a clock speed increase. Similarly, to accommodate a frequency reduction, a voltage transition is allowed for a supply ramp down to the nominal value after the frequency is decreased.

⁴ Only part number MCIMX535DVV2C supports frequency up to 1200 MHz.

⁵ For BSDL mode, the minimum operating temperature is 20 °C and the maximum operating temperature is the maximum temperature specified for the particular part grade.

⁶ VDDA and VDDAL1 can be driven by the VDD_DIG_PLL internal regulator using external connections. When operating in this configuration, the regulator is still operating at the default 1.2 V, as bootup start. During bootup initialization, software should increase this regulator voltage to match VCC (1.3 V nominal) in order to reduce internal leakage current.

Electrical Characteristics

- ⁷ By default, VDD_DIG_PLL is driven from internal on-die 1.2 V linear regulator (LDO). In this case, there is no need driving this supply externally. LDO output to VDD_DIG_PLL should be configured by software after power-up to 1.3 V output. A bypass capacitor of minimal value 22 μ F should be connected to this pad in any case whether it is driven internally or externally. Use of the on-chip LDO is preferred. See i.MX53 System Development User's Guide.
- ⁸ By default, the VDD_ANA_PLL is driven from internal on-die 1.8 V linear regulator (LDO). In this case there is no need driving this supply externally. A bypass capacitor of minimal value 22 μ F should be connected to this pad in any case whether it is driven internally or externally. Use of the on-chip LDO is preferred. See i.MX53 System Development User's Guide.
- ⁹ After fuses are programmed, Freescale strongly recommends the best practice of reading the fuses to verify that they are written correctly. In Read mode, VDD_FUSE should be floated or grounded. Tying VDD_FUSE to a positive supply (3.0 V–3.3 V) increases the possibility of inadvertently blowing fuses and is not recommended in read mode.
- ¹⁰ If not using TVE module or other pads in this power domain for the product, the TVDAC_DHVDD and TVDAC_AHVDDRGB can remain floating.
- ¹¹ GPIO pad operational at low frequency
- ¹² The analog supplies should be isolated in the application design. Use of series inductors is recommended.
- ¹³ VDD_REG is power supply input for the integrated linear regulators of VDD_ANA_PLL and VDD_DIG_PLL when they are configured to the internal supply option. VDDR_REG still has to be tied to 2.5 V supply when VDD_ANA_PLL and VDD_DIG_PLL are configured for external power supply mode although in this case it is not used as supply source.
- ¹⁴ For part number MCIMX535DVV1C, lifetime of 21,900 hours based on 95 °C junction temperature and nominal supply voltages. For part number MCIMX535DVV2C, lifetime of 4,380 hours at 1.2 GHz frequency and lifetime of 17,520 hours at 1 GHz frequency, based on 95 °C junction temperature and nominal supply voltages.

4.1.4 External Clock Sources

The i.MX53xD device has four external input system clocks, a low frequency (CKIL), a high frequency (XTAL), and two general purpose CKIH1 and CKIH2 clocks.

The CKIL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

CKIH1 and CKIH2 provide additional clock source option for peripherals that require specific and accurate frequencies.

Table 8 shows the interface frequency requirements. See Chapter 1 of *i.MX53 System Development User's Guide* (MX53UG) for additional clock and oscillator information.

Table 8. External Input Clock Frequency

| Parameter Description | Symbol | Min | Typ | Max | Unit |
|----------------------------------|------------------------------|---|---------------------------|-----|------|
| CKIL Oscillator ¹ | f_{ckil} | — | 32.768 ² /32.0 | — | kHz |
| CKIH1, CKIH2 Operating Frequency | f_{ckih1} , f_{ckih2} | See Table 33, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 46 | | | MHz |
| XTAL Oscillator | f_{xtal} | 22 | 24 | 27 | MHz |

¹ External oscillator or a crystal with internal oscillator amplifier.

² Recommended nominal frequency 32.768 kHz.

4.1.5 Maximal Supply Currents

Table 9 represents the maximal momentary current transients on power lines, and should be used for power supply selection. Maximal currents higher by far than the average power consumption of typical use cases. For typical power consumption information, refer to i.MX53xD power consumption application note.

Table 9. Maximal Supply Currents

| Power Line | Conditions | Max Current | Unit |
|--------------------------------|-------------------------------------|--|------|
| VDDGP | 1000 MHz ARM clock at 1.27V, 105 °C | 1700 | mA |
| | 1200 MHz ARM clock at 1.37V, 125 °C | 2200 | mA |
| VCC | | 800 | mA |
| VDDA+VDDAL1 | | 100 | mA |
| VDD_DIG_PLL | | 10 | mA |
| VP | | 20 | mA |
| VDD_ANA_PLL | | 10 | mA |
| MVCC_XTAL | | 25 | mA |
| VDD_REG | | 325 | mA |
| VDD_FUSE | Fuse Write Mode operation | 120 | mA |
| NVCC_EMI_DRAM | 1.8V (DDR2) | 800 | mA |
| | 1.5V (DDR3) | 650 | mA |
| | 1.2V (LPDDR2) | 250 | mA |
| TVDAC_DHVDD + TVDAC_AHVDDRGB | | 200 | mA |
| NVCC_SRTC_POW | | <1 | mA |
| USB_H1_VDDA25 + USB_OTG_VDDA25 | | 50 | mA |
| USB_H1_VDDA33 + USB_OTG_VDDA33 | | 20 | mA |
| VPH | | 60 | mA |
| NVCC_CKIH | | Use maximal I/O Eq ¹ , N=4 | |
| NVCC_CSI | | Use maximal I/O Eq ¹ , N=20 | |
| NVCC_EIM_MAIN | | Use maximal I/O Eq ¹ , N=39 | |
| NVCC_EIM_SEC | | Use maximal I/O Eq ¹ , N=16 | |
| NVCC_EMI_DRAM | | Use maximal I/O Eq ¹ , N=78 | |
| NVCC_FEC | | Use maximal I/O Eq ¹ , N=11 | |

Table 9. Maximal Supply Currents (continued)

| Power Line | Conditions | Max Current | Unit |
|--------------|------------|--|------|
| NVCC_GPIO | | Use maximal I/O Eq ¹ , N=13 | |
| NVCC_JTAG | | Use maximal I/O Eq ¹ , N=6 | |
| NVCC_KPAD | | Use maximal I/O Eq ¹ , N=11 | |
| NVCC_LCD | | Use maximal I/O Eq ¹ , N=29 | |
| NVCC_LVDS | | Use maximal I/O Eq ¹ , N=20 | |
| NVCC_LVDS_BG | | Use maximal I/O Eq ¹ , N=1 | |
| NVCC_NANDF | | Use maximal I/O Eq ¹ , N=8 | |
| NVCC_PATA | | Use maximal I/O Eq ¹ , N=29 | |
| NVCC_REST | | Use maximal I/O Eq ¹ , N=5 | |
| NVCC_SD1 | | Use maximal I/O Eq ¹ , N=6 | |
| NVCC_SD2 | | Use maximal I/O Eq ¹ , N=6 | |
| NVCC_XTAL | | Use maximal I/O Eq ¹ , N=2 | |

¹ General Equation for estimated, maximal power consumption of an I/O power supply:

$$I_{max} = N \times C \times V \times (0.5 \times F)$$

Where:

N - Number of I/O pins supplies by the power line

C - Equivalent external capacitive load

V - I/O voltage

(0.5 x F) - Data change rate. Up to 0.5 of the clock rate (F).

4.1.6 USB-OH-3 (OTG + 3 Host ports) Module and the Two USB PHY (OTG and H1) Current Consumption

Table 10 shows the USB interface current consumption.

Table 10. USB Interface Current Consumption

| Parameter | Conditions | | Typical at 25 °C | Max | Unit |
|--|------------|----|------------------|-----|------|
| Analog Supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33 | Full Speed | RX | 5.5 | 6 | mA |
| | | TX | 7 | 8 | |
| | High Speed | RX | 5 | 6 | |
| | | TX | 5 | 6 | |
| Analog Supply 2.5 V USB_H1_VDDA25 USB_OTG_VDDA25 | Full Speed | RX | 6.5 | 7 | mA |
| | | TX | 6.5 | 7 | |
| | High Speed | RX | 12 | 13 | |
| | | TX | 21 | 22 | |
| Digital Supply VCC (1.2 V) | Full Speed | RX | 8 | — | mA |
| | | TX | 8 | — | |
| | High Speed | RX | 8 | — | |
| | | TX | 8 | — | |

4.2 Power Supply Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX53xD processor (worst-case scenario)

4.2.1 Power-Up Sequence

The following observations should be considered:

- The consequent steps in power up sequence should not start before the previous step supplies have been stabilized within 90-110% of their nominal voltage, unless stated otherwise.
- NVCC_SRTC_POW should remain powered ON continuously, to maintain internal real-time clock status. Otherwise, it has to be powered ON together with VCC, or preceding VCC.
- The VCC should be powered ON together, or any time after NVCC_SRTC_POW.
- NVCC_CKIH should be powered ON after VCC is stable and before other I/O supplies (NVCC_XXX) are powered ON.

- I/O Supplies (NVCC_XXX) below or equal to 2.8 V nom./3.1 V max. should not precede NVCC_CKIH. They can start powering ON during NVCC_CKIH ramp-up, before it is stabilized. Within this group, the supplies can be powered-up in any order. Alternatively, the on-chip regulator VDD_ANA_PLL may be used to power NVCC_CKIH and NVCC_RESET. In this case, the sequence defined in the “Interfacing the i.MX53 Processor with LTC3589-1” section of the *i.MX53 System Development User's Guide* (MX53UG) must be followed.
- I/O Supplies (NVCC_XXX) above 2.8 V nom./3.1 V max. should be powered ON only after NVCC_CKIH is stable.
- In case VDD_DIG_PLL and VDD_ANA_PLL are powered ON from internal voltage regulator (default case for i.MX53xD), there are no related restrictions on VDD_REG, as it is used as their internal regulators power source.
If VDD_DIG_PLL and VDD_ANA_PLL are powered on externally, to reduce current leakage during the power-up, it is recommended to activate the VDD_REG before or at the same time with VDD_DIG_PLL and VDD_ANA_PLL. If this sequencing is not possible, make sure that the 2.5 V VDD_REG supply shut-off output impedance is higher than 1 kΩ when it is inactive.
- VDD_REG supply is required to be powered ON to enable DDR operation. It must be powered on after VCC and before NVCC_EMI_DRAM. The sequence should be:
$$VCC \rightarrow VDD_REG \rightarrow NVCC_EMI_DRAM$$
- NVCC_EIM_DRAM_2P5 PoP additional power line timing is the same as DVV_REG
- VDDA and VDDAL1 can be powered ON anytime before POR_B, regardless of any other power signal.
- VDDGP can be powered ON anytime before POR_B, regardless of any other power signal.
- VP and VPH can be powered up together, or anytime after, the VCC. VP and VPH should come before POR.
- TVDAC_DHVDD and TVDAC_AHVDDRGB should be powered from the same regulator. This is due to ESD diode protection circuit, that may cause current leakage if one of the supplies is powered ON before the other.

NOTE

The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage.

Figure 2 shows the power-up sequence diagram.

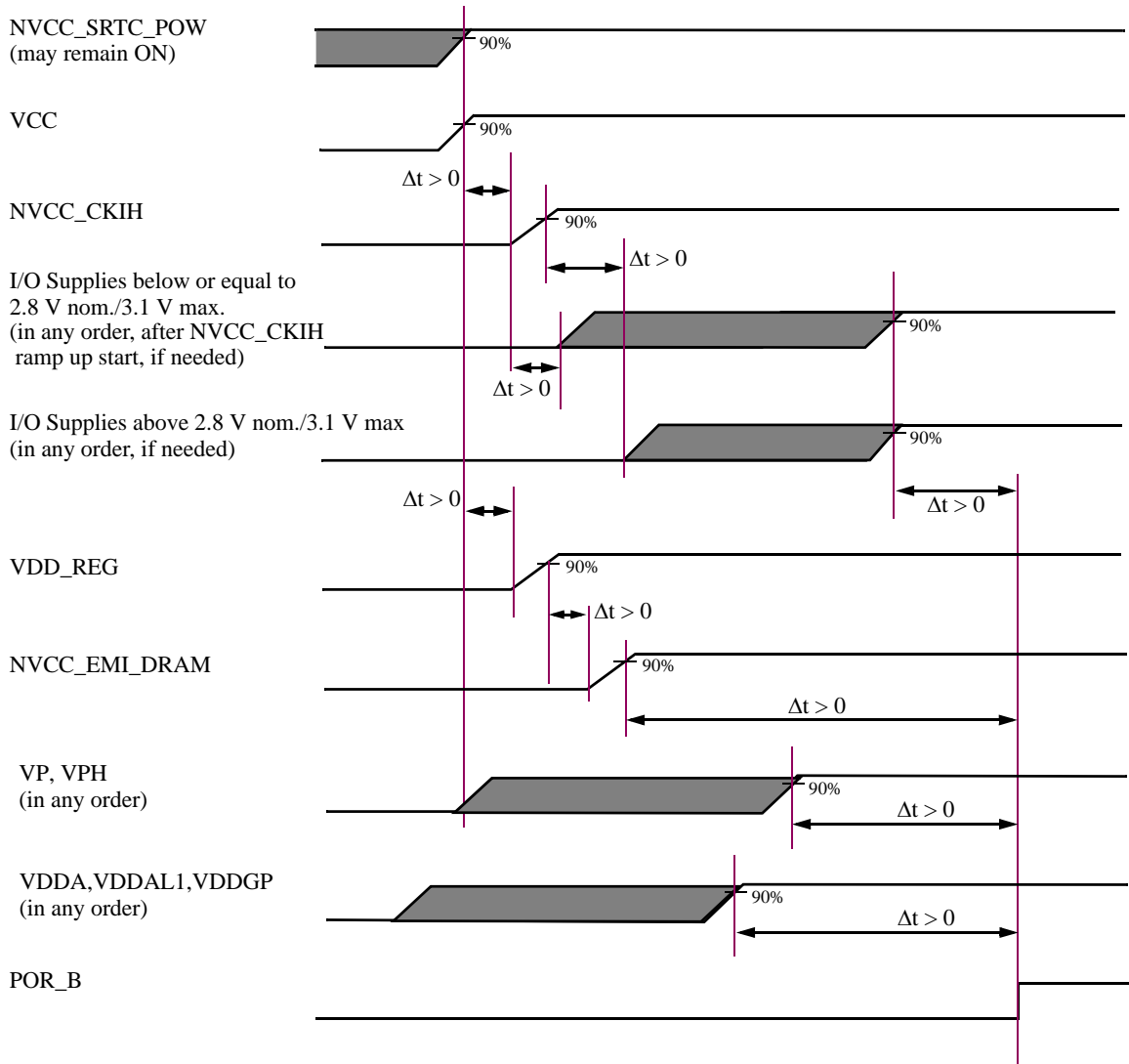


Figure 2. Power-Up Detailed Sequence

¹ If fuse writing is required, VDD_FUSE should be powered ON after NVCC_CKIH is stable.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the parts that use both 1.8 V and the 3.3 V supply).

NOTE

For further details on power-up sequence, see the “Setting up Power Management” chapter of *i.MX53 System Development User’s Guide* (MX53UG).

4.2.2 Power-Down Sequence

Power-down sequence should follow one of the following two options:

- Option 1: Switch all supplies down simultaneously with further free discharge. A deviation of few microseconds of actual power-down of the different power rails is acceptable.
- Option 2: Switch down supplies, in any order, keeping the following rules:
 - NVCC_CKIH must be powered down at the same time or after the UHVIO I/O cell supplies (for full supply list, refer to [Table 7](#), Ultra High voltage I/O (UHVIO) supplies). A deviation of few microseconds of actual power-down of the different power rails is acceptable.
 - VDD_REG must be powered down at the same time or after NVCC_EMI_DRAM supply. A deviation of few microseconds of actual power-down of the different power rails is acceptable.
 - If all of the following conditions are met:
 - VDD_REG is powered down to 0V (Not Hi-Z)
 - VDD_DIG_PLL and VDD_ANA_PLL are provided externally,
 - VDD_REG is powered down before VDD_DIG_PLL and VDD_ANA_PLL
 Then the following rule should be kept: VDD_REG output impedance must be higher than 1 kW, when inactive.

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_XXX) is off. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin refer to “Power Rail” columns in pin list tables of [Section 6, “Package Information and Contact Assignments.”](#)
- If not using SATA interface and the embedded thermal sensor, the VP and VPH should be grounded. In particular, keeping VPH turned OFF while the VP is powered ON is not recommended and might lead to excessive power consumption.
- When internal clock source is used for SATA temperature monitor the USB_PHY supplies and PLL need to be active because they are providing the clock.
- If not using TVE the module, the TVDAC_DHVDD and TVDAC_AHVDDRGB can remain floating. If only the GPIO pads in TVDAC_AHVDDRGB domain are in use, the supplies can be set to GPIO pad voltage range (1.65 V to 3.1 V).

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2 and DDR3 modes
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output. The association is shown in [Table 112](#).

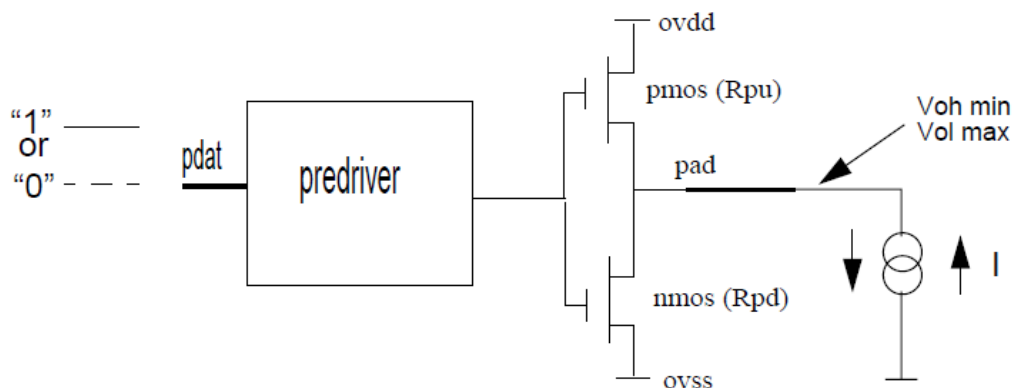


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.3.1 General Purpose I/O (GPIO) DC Parameters

The parameters in [Table 11](#) are guaranteed per the operating ranges in [Table 7](#), unless otherwise noted. [Table 11](#) shows DC parameters for GPIO pads, operating at two supply ranges:

- 1.1 V to 1.3 V
- 1.65 V to 3.1 V

Table 11. GPIO I/O DC Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------|---|-------------|--------------|------------|------|
| High-level output voltage ¹ | Voh | I _{out} = -0.8 mA | OVDD - 0.15 | — | — | V |
| Low-level output voltage ¹ | Vol | I _{out} = 0.8 mA | — | — | 0.15 | V |
| High-Level DC input voltage ^{1, 2} | VIH | — | 0.7 × OVDD | — | OVDD | V |
| Low-Level DC input voltage ^{1, 2} | VIL | — | 0 | — | 0.3 × OVDD | V |
| Input Hysteresis | VHYS | OVDD = 1.875 V OVDD = 2.775 V | 0.25 | 0.34 0.45 | — | V |
| Schmitt trigger VT+ ^{2, 3} | VT+ | — | 0.5 × OVDD | — | — | V |
| Schmitt trigger VT- ^{2, 3} | VT- | — | — | — | 0.5 × OVDD | V |
| Input current (no pull-up/down) | I _{in} | V _{in} = OVDD or 0 | — | — | 10 | μA |
| Input current (22 kΩ Pull-up) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — | — | 161 10 | μA |
| Input current (47 kΩ Pull-up) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — | — | 76 10 | μA |
| Input current (100 kΩ Pull-up) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — | — | 40 10 | μA |

Table 11. GPIO I/O DC Electrical Characteristics (continued)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|-----------------|---|-----|------------------|----------|------------|
| Input current (100 k Ω Pull-down) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — | — | 10 40 | μ A |
| Keeper Circuit Resistance | | | — | 130 ⁴ | — | k Ω |

¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

² To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

³ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

⁴ Use an off-chip pull resistor of less than 60 k Ω to override this keeper.

4.3.2 LPDDR2 I/O DC Parameters

The LPDDR2 I/O pads support DDR2/LVDDR2, LPDDR2, and DDR3 operational modes.

4.3.2.1 DDR2 Mode I/O DC Parameters

The DDR2 interface fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The parameters in [Table 12](#) are guaranteed per the operating ranges in [Table 7](#), unless otherwise noted.

Table 12. DDR2 I/O DC Electrical Parameters¹

| Parameters | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------|---|--------------------------|------------------|---------------------------|------------|
| High-level output voltage ² | V _{oh} | I _{oh} = -0.1 mA | 0.9 x OVDD | — | — | V |
| Low-level output voltage | V _{ol} | I _{ol} = 0.1 mA | — | — | 0.1 x OVDD | V |
| Input Reference Voltage | V _{ref} | | 0.49 x OVDD | 0.5 x OVDD | 0.51 x OVDD | |
| DC input High Voltage (data pins) | V _{ihd} (dc) | — | V _{ref} +0.125V | — | OVDD+0.3 | V |
| DC input Low Voltage (data pins) | V _{ild} (dc) | — | -0.3 | — | V _{ref} - 0.125V | V |
| DC Input voltage range of each differential input ³ | V _{in} (dc) | — | -0.3 | — | OVDD + 0.3 | V |
| DC Differential input voltage required for switching ⁴ | V _{id} (dc) | — | 0.25 | — | OVDD + 0.6 | V |
| Termination Voltage | V _{tt} | V _{tt} | V _{ref} - 0.04 | V _{ref} | V _{ref} + 0.04 | V |
| Input current (no pull-up/down) | I _{in} | V _{in} = 0 V V _{in} = OVDD | — — | — — | 1 1 | μ A |
| Keeper Circuit Resistance | — | — | — | 130 ⁵ | — | k Ω |

¹ Note that the JEDEC SSTL_18 specification (JESD8-15a) for a SSTL interface for class II operation supersedes any specification in this document.

² OVDD is the I/O power supply (1.7 V–1.9 V for DDR2)

³ V_{in}(dc) specifies the allowable DC voltage exertion of each differential input.

- ⁴ Vid(dc) specifies the input differential voltage $|V_{tr}-V_{cp}|$ required for switching, where V_{tr} is the “true” input level and V_{cp} is the “complementary” input level. The minimum value is equal to $V_{ih}(dc) - V_{il}(dc)$.
- ⁵ Use an off-chip pull resistor of less than 60 k Ω to override this keeper.

4.3.2.2 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The parameters in Table 13 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 13. LPDDR2 I/O DC Electrical Parameters¹

| Parameters | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|-----------|-------------------------|-----------------------|------------------|-----------------------|------------|
| High-level output voltage | Voh | Ioh = -0.1 mA | 0.9 x OVDD | — | — | V |
| Low-level output voltage | Vol | Iol = 0.1 mA | — | — | 0.1 x OVDD | V |
| Input Reference Voltage | Vref | | 0.49 x OVDD | 0.5 x OVDD | 0.51 x OVDD | |
| DC input High Voltage | Vih(dc) | — | Vref+0.13V | — | OVDD | V |
| DC input Low Voltage | Vil(dc) | — | OVSS | — | Vref - 0.13V | V |
| Differential Input Logic High | Vih(diff) | | 0.26 | | See Note ² | |
| Differential Input Logic Low | Vil(diff) | | See Note ² | | -0.26 | |
| Input current (no pull-up/down) | Iin | Vin = 0 V Vin = OVDD | — — | — — | 1 1 | μ A |
| Pull-up/Pull-down impedance Mismatch | | | -15 | | +15 | % |
| 240 Ω unit calibration resolution | | | | | 10 | Ω |
| Keeper Circuit Resistance | — | — | — | 140 ³ | — | k Ω |

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

² The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

³ Use an off-chip pull resistor of less than 60 k Ω to override this keeper.

4.3.2.3 DDR3 Mode I/O DC Parameters

The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 14 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 14. DDR3 I/O DC Electrical Parameters

| Parameters | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------|-----------|-----------------|-------------------------|-----|-----------------------|------|
| High-level output voltage | Voh | Ioh = -0.1 mA | 0.8 x OVDD ¹ | — | — | V |
| Low-level output voltage | Vol | Iol = 0.1 mA | — | — | 0.2 x OVDD | V |
| DC input Logic High | VIH(dc) | — | Vref ² +0.1 | — | OVDD | V |
| DC input Logic Low | VIL(dc) | — | OVSS | — | Vref-0.1 | V |
| Differential input Logic High | VIH(diff) | — | 0.2 | — | See Note ³ | V |
| Differential input Logic Low | VIL(diff) | — | See Note ³ | — | -0.2 | V |

Electrical Characteristics

Table 14. DDR3 I/O DC Electrical Parameters (continued)

| | | | | | | |
|---|-------|---------------------------------|-------------|------------------|-------------|------|
| Over/undershoot peak | Vpeak | — | — | — | 0.4 | V |
| Over/undershoot area (above OVDD or below OVSS) | Varea | — | — | — | 0.67 | V-ns |
| Termination Voltage | Vtt | Vtt tracking OVDD/2 | 0.49 x OVDD | Vref | 0.51 x OVDD | V |
| Input current (no pull-up/down) | Iin | VI = 0 V VI=OVDD | — — | — — | 1 1 | μA |
| Pull-up/Pull-down impedance mismatch | — | Minimum impedance configuration | — | — | 3 | Ω |
| 240 Ω unit calibration resolution | — | — | — | — | 10 | Ω |
| Keeper Circuit Resistance | — | — | — | 130 ⁴ | — | kΩ |

¹ OVDD— I/O power supply (1.425 V–1.575 V for DDR3)

² Vref— DDR3 external reference voltage

³ The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

⁴ Use an off-chip pull resistor of less than 60 kΩ to override this keeper.

4.3.3 Low Voltage I/O (LVIO) DC Parameters

The parameters in [Table 15](#) are guaranteed per the operating ranges in [Table 7](#), unless otherwise noted. The LVIO pads operate only as inputs.

Table 15. LVIO DC Electrical Characteristics

| DC Electrical Characteristics | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|--------|----------------------------------|------------|------------------|------------|------|
| High-Level DC input voltage ^{1, 2} | Vih | Ioh = -0.8 mA | 0.7 × OVDD | — | OVDD | V |
| Low-Level DC input voltage ^{1, 2} | Vil | Iol = 0.8 mA | 0 | — | 0.3 × OVDD | V |
| Input Hysteresis | Vhys | OVDD = 1.875 V OVDD = 2.775 V | 0.35 | 0.62 1.27 | — | V |
| Schmitt trigger VT+ ^{2, 3} | VT+ | — | 0.5 × OVDD | — | — | V |
| Schmitt trigger VT- ^{2, 3} | VT- | — | — | — | 0.5 × OVDD | V |
| Input current (no pull-up/down) | Iin | Vin = OVDD or 0 V | — | — | 1 | μA |
| Input current (22 kΩ Pull-up) | Iin | Vin = 0 V Vin = OVDD | — | — | 161 1 | μA |
| Input current (47 kΩ Pull-up) | Iin | Vin = 0 V Vin = OVDD | — | — | 76 1 | μA |
| Input current (100 kΩ Pull-up) | Iin | Vin = 0 V Vin = OVDD | — | — | 36 1 | μA |
| Input current (100 kΩ Pull-down) | Iin | Vin = 0 V Vin = OVDD | — | — | 1 36 | μA |
| Keeper Circuit Resistance | — | — | — | 130 ⁴ | — | kΩ |

- ¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.
- ² To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.
- ³ Hysteresis of 350 mV is guaranteed over all operating conditions when hysteresis is enabled.
- ⁴ Use an off-chip pull resistor of less than 60 kΩ to override this keeper.

4.3.4 Ultra-High Voltage I/O (UHVIO) DC Parameters

The parameters in Table 16 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 16. UHVIO DC Electrical Characteristics

| DC Electrical Characteristics | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------|---|--------------|------------------|--------------|------|
| High-level output voltage ¹ | Voh | I _{out} = -0.8 mA | OVDD-0.15 | — | — | V |
| Low-level output voltage ¹ | Vol | I _{out} = 0.8 mA | — | — | 0.15 | V |
| High-Level DC input voltage ^{1, 2} | VIH | — | 0.7 × OVDD | — | OVDD | V |
| Low-Level DC input voltage ^{1, 2} | VIL | — | 0 | — | 0.3 × OVDD | V |
| Input Hysteresis | VHYS | low voltage mode high voltage mode | 0.38 0.95 | — | 0.43 1.33 | V |
| Schmitt trigger VT+ ^{2, 3} | VT+ | — | 0.5 × OVDD | — | — | V |
| Schmitt trigger VT- ^{2, 3} | VT- | — | — | — | 0.5 × OVDD | V |
| Input current (no pull-up/down) | I _{in} | V _{in} = OVDD or 0 V | — | — | 1 | μA |
| Input current (22 kΩ Pull-up) | I _{in} | V _{in} = 0 V _{in} = OVDD | — | — | 202 1 | μA |
| Input current (75 kΩ Pull-up) | I _{in} | V _{in} = 0 V _{in} = OVDD | — | — | 61 1 | μA |
| Input current (100 kΩ Pull-up) | I _{in} | V _{in} = 0 V _{in} = OVDD | — | — | 47 1 | μA |
| Input current (360 kΩ Pull-down) | I _{in} | V _{in} = 0 V _{in} = OVDD | — | — | 1 5.7 | μA |
| Keeper Circuit Resistance | — | — | — | 130 ⁴ | — | kΩ |

- ¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.
- ² To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.
- ³ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
- ⁴ Use an off-chip pull resistor of less than 60 kΩ to override this keeper.

4.3.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 17 shows the Low Voltage Differential Signaling (LVDS) DC electrical characteristics. The parameters in Table 17 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 17. LVDS DC Electrical Characteristics

| DC Electrical Characteristics | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------|--|-------|-------|-------|------|
| Output Differential Voltage | V_{OD} | Rload = 100 Ω between padP and padN | 250 | 350 | 450 | mV |
| Output High Voltage | V_{OH} | | 1.25 | 1.375 | 1.6 | V |
| Output Low Voltage | V_{OL} | | 0.9 | 1.025 | 1.25 | |
| Offset Voltage | V_{OS} | | 1.125 | 1.2 | 1.375 | |

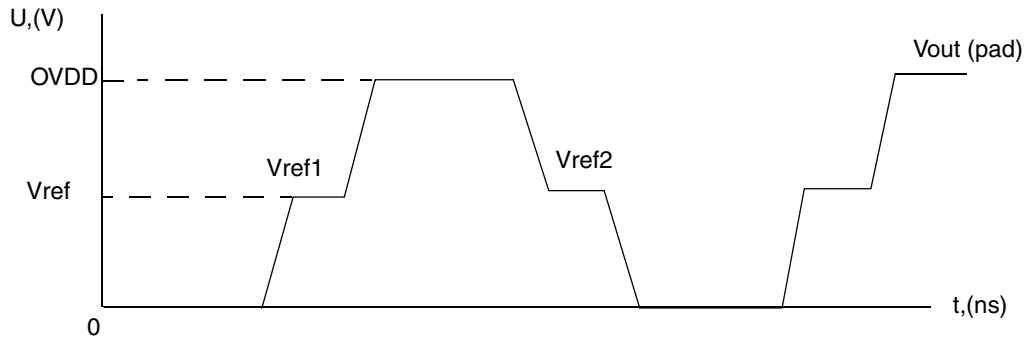
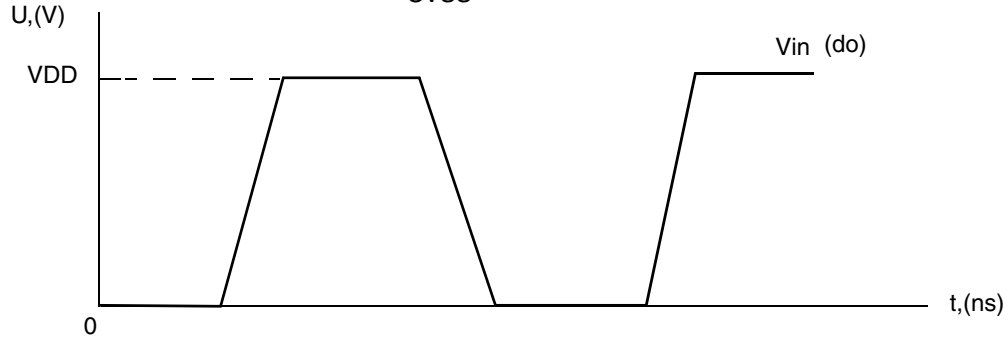
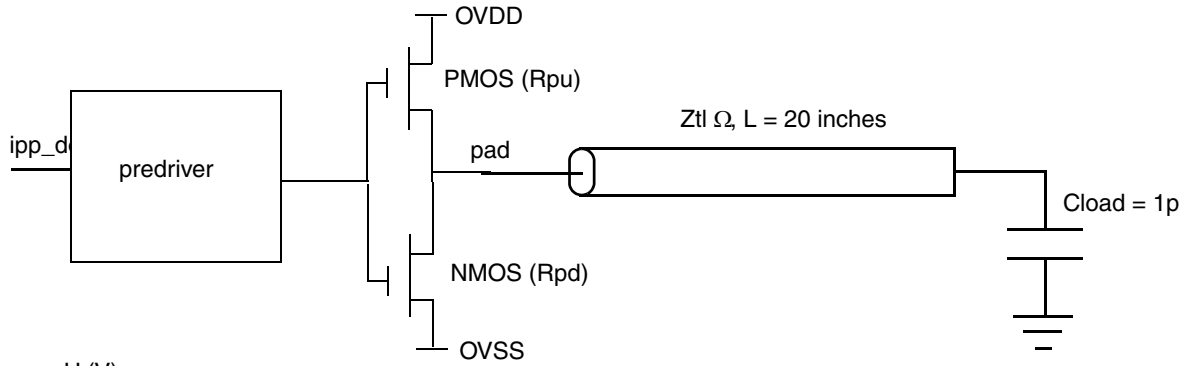
4.4 Output Buffer Impedance Characteristics

This section defines the I/O Impedance parameters of the i.MX53xD processor for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2, and DDR3 modes
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

NOTE

Output driver impedance is measured with “long” transmission line of impedance Z_{tl} attached to I/O pad and incident wave launched into transmission line. R_{pu}/R_{pd} and Z_{tl} form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 4).



$$R_{pu} = \frac{V_{ovdd} - V_{ref1}}{V_{ref1}} \times Z_{tl}$$

$$R_{pd} = \frac{V_{ref2}}{V_{ovdd} - V_{ref2}} \times Z_{tl}$$

Figure 4. Impedance Matching Load for Measurement

4.4.1 GPIO Output Buffer Impedance

Table 18 shows the GPIO output buffer impedance.

Table 18. GPIO Output Buffer Impedance

| Parameter | Symbol | Test Conditions | Min | Typ | | Max | Unit |
|-------------------------|--------|--|-----|--------------|--------------|-----|----------|
| | | | | OVDD 2.775 V | OVDD 1.875 V | | |
| Output Driver Impedance | Rpu | Low Drive Strength, Ztl = 150 Ω | 80 | 104 | 150 | 250 | Ω |
| | | Medium Drive Strength, Ztl = 75 Ω | 40 | 52 | 75 | 125 | |
| | | High Drive Strength, Ztl = 50 Ω | 27 | 35 | 51 | 83 | |
| | | Max Drive Strength, Ztl = 37.5 Ω | 20 | 26 | 38 | 62 | |
| Output Driver Impedance | Rpd | Low Drive Strength, Ztl = 150 Ω | 64 | 88 | 134 | 243 | Ω |
| | | Medium Drive Strength, Ztl = 75 Ω | 32 | 44 | 66 | 122 | |
| | | High Drive Strength, Ztl = 50 Ω | 21 | 30 | 44 | 81 | |
| | | Max Drive Strength, Ztl = 37.5 Ω | 16 | 22 | 34 | 61 | |

4.4.2 DDR Output Driver Average Impedance

The DDR2/LVDDR2 interface fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 19 shows DDR output driver average impedance of the i.MX53 processor.

Table 19. DDR Output Driver Average Impedance¹

| Parameter | Symbol | Test Conditions | Drive strength (DSE) | | | | | | | | Unit |
|-------------------------|-------------------|--|----------------------|-----|-----|-----|-----|-----|-----|-----|------|
| | | | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| Output Driver Impedance | Rdrv ² | LPDDR1/DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 00 Calibration resistance = 300 Ω ³ | Hi-Z | 300 | 150 | 100 | 75 | 60 | 50 | 43 | Ω |
| | | DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 01 Calibration resistance = 180 Ω ³ | Hi-Z | 180 | 90 | 60 | 45 | 36 | 30 | 26 | |
| | | DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 10 Calibration resistance = 200 Ω ³ | Hi-Z | 200 | 100 | 66 | 50 | 40 | 33 | 28 | |
| | | DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 11 Calibration resistance = 140 Ω ³ | Hi-Z | 140 | 70 | 46 | 35 | 28 | 23 | 20 | |
| | | LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 01 ⁴ Calibration resistance = 160 Ω ³ | Hi-Z | 160 | 80 | 53 | 40 | 32 | 27 | 23 | |
| | | LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 10 Calibration resistance = 240 Ω ³ | Hi-Z | 240 | 120 | 80 | 60 | 48 | 40 | 34 | |
| | | LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 11 ⁴ Calibration resistance = 160 Ω ³ | Hi-Z | 160 | 80 | 53 | 40 | 32 | 27 | 23 | |
| | | DDR3 mode NVCC_DRAM = 1.5 V DDR_SEL = 00 Calibration resistance = 200 Ω ³ | Hi-Z | 240 | 120 | 80 | 60 | 48 | 48 | 34 | |

¹ Output driver impedance is controlled across PVTs (process, voltages, and temperatures) using calibration procedure and pu_*cal, pd_*cal input pins.

² Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

³ Calibration is done against external reference resistor. Value of the resistor should be varied depending on DDR mode and DDR_SEL setting.

⁴ If DDR_SEL = '01' or DDR_SEL = '11' are selected with NVCC_DRAM = 1.2 V for LPDDR2 operation, the external reference resistor value must be 160 Ω for a correct ZQ calibration. In any case, reference resistors attached to the DDR memory devices should be kept to 240 Ω per the JEDEC standard.

4.4.3 UHVIO Output Buffer Impedance

Table 20 shows the UHVIO output buffer impedance.

Table 20. UHVIO Output Buffer Impedance

| Parameter | Symbol | Test Conditions | Min | | Typ | | Max | | Unit |
|-------------------------|--------|-----------------------------------|----------------|---------------|-----------------|---------------|----------------|---------------|------|
| | | | OVDD 1.95 V | OVDD 3.0 V | OVDD 1.875 V | OVDD 3.3 V | OVDD 1.65 V | OVDD 3.6 V | |
| Output Driver Impedance | Rpu | Low Drive Strength, Ztl = 150 Ω | 98 | 114 | 124 | 135 | 198 | 206 | Ω |
| | | Medium Drive Strength, Ztl = 75 Ω | 49 | 57 | 62 | 67 | 99 | 103 | |
| | | High Drive Strength, Ztl = 50 Ω | 32 | 38 | 41 | 45 | 66 | 69 | |
| Output Driver Impedance | Rpd | Low Drive Strength, Ztl = 150 Ω | 97 | 118 | 126 | 154 | 179 | 217 | Ω |
| | | Medium Drive Strength, Ztl = 75 Ω | 49 | 59 | 63 | 77 | 89 | 109 | |
| | | High Drive Strength, Ztl = 50 Ω | 32 | 40 | 42 | 51 | 60 | 72 | |

4.4.4 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.5 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2 and DDR3 modes
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

The load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

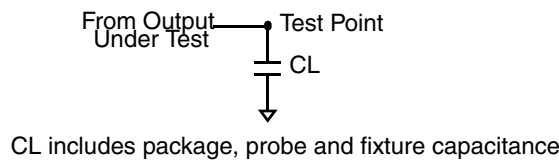


Figure 5. Load Circuit for Output

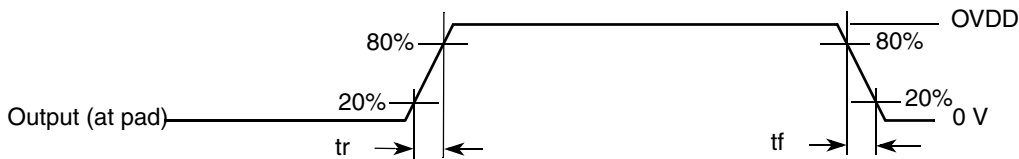


Figure 6. Output Transition Time Waveform

4.5.1 GPIO I/O AC Electrical Characteristics

AC electrical characteristics for GPIO I/O in slow and fast modes are presented in the [Table 21](#) and [Table 22](#), respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 21. GPIO I/O AC Parameters Slow Mode

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|------------------------|-----|-------------------------|-------|
| Output Pad Transition Times (Max Drive) | tr, tf | 15 pF 35 pF | — | — | 1.91/1.52 3.07/2.65 | ns |
| Output Pad Transition Times (High Drive) | tr, tf | 15 pF 35 pF | — | — | 2.22/1.81 3.81/3.42 | ns |
| Output Pad Transition Times (Medium Drive) | tr, tf | 15 pF 35 pF | — | — | 2.88/2.42 5.43/5.02 | ns |
| Output Pad Transition Times (Low Drive) | tr, tf | 15 pF 35 pF | — | — | 4.94/4.50 10.55/9.70 | ns |
| Output Pad Slew Rate (Max Drive) ¹ | tps | 15 pF 35 pF | 0.5/0.65 0.32/0.37 | — | — | V/ns |
| Output Pad Slew Rate (High Drive) ¹ | tps | 15 pF 35 pF | 0.43/0.54 0.26/0.41 | — | — | |
| Output Pad Slew Rate (Medium Drive) ¹ | tps | 15 pF 35 pF | 0.34/0.41 0.18/0.2 | — | — | |
| Output Pad Slew Rate (Low Drive) ¹ | tps | 15 pF 35 pF | 0.20/0.22 0.09/0.1 | — | — | |
| Output Pad di/dt (Max Drive) | tdit | — | — | — | 30 | mA/ns |
| Output Pad di/dt (High Drive) | tdit | — | — | — | 23 | |
| Output Pad di/dt (Medium drive) | tdit | — | — | — | 15 | |
| Output Pad di/dt (Low drive) | tdit | — | — | — | 7 | |
| Input Transition Times ² | trm | — | — | — | 25 | ns |

¹ tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

² Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 22. GPIO I/O AC Parameters Fast Mode

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|------------------------|------|
| Output Pad Transition Times (Max Drive) | tr, tf | 15 pF 35 pF | — | — | 1.45/1.24 2.76/2.54 | ns |
| Output Pad Transition Times (High Drive) | tr, tf | 15 pF 35 pF | — | — | 1.81/1.59 3.57/3.33 | ns |
| Output Pad Transition Times (Medium Drive) | tr, tf | 15 pF 35 pF | — | — | 2.54/2.29 5.25/5.01 | ns |

Electrical Characteristics

Table 22. GPIO I/O AC Parameters Fast Mode (continued)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|------------------------|-----|------------------------|-------|
| Output Pad Transition Times (Low Drive) | tr, tf | 15 pF 35 pF | — | — | 4.82/4.5 10.54/9.95 | ns |
| Output Pad Slew Rate (Max Drive) ¹ | tps | 15 pF 35 pF | 0.69/0.78 0.36/0.39 | — | — | V/ns |
| Output Pad Slew Rate (High Drive) ¹ | tps | 15 pF 35 pF | 0.55/0.62 0.28/0.30 | — | — | V/ns |
| Output Pad Slew Rate (Medium Drive) ¹ | tps | 15 pF 35 pF | 0.39/0.44 0.19/0.20 | — | — | V/ns |
| Output Pad Slew Rate (Low Drive) ¹ | tps | 15 pF 35 pF | 0.21/0.22 0.09/0.1 | — | — | V/ns |
| Output Pad di/dt (Max Drive) | tdit | — | — | — | 70 | mA/ns |
| Output Pad di/dt (High Drive) | tdit | — | — | — | 53 | mA/ns |
| Output Pad di/dt (Medium drive) | tdit | — | — | — | 35 | mA/ns |
| Output Pad di/dt (Low drive) | tdit | — | — | — | 18 | mA/ns |
| Input Transition Times ² | trm | — | — | — | 25 | ns |

¹ tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

² Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.2 LPDDR2 I/O AC Electrical Characteristics

The DDR2/LVDDR2 interface mode fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 23 shows the AC parameters for LPDDR2 I/O operating in DDR2 mode.

Table 23. LPDDR2 I/O DDR2 mode AC Characteristics¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------|--------------------------------|--------------|-----|--------------|------|
| AC input logic high | Vih(ac) | — | Vref+0.25 | — | — | V |
| AC input logic low | Vil(ac) | — | — | — | Vref-0.25 | V |
| AC differential input voltage ² | Vid(ac) | — | 0.5 | — | OVDD | V |
| Input AC differential cross point voltage ³ | Vix(ac) | — | Vref - 0.175 | — | Vref + 0.175 | V |
| Output AC differential cross point voltage ⁴ | Vox(ac) | — | Vref - 0.125 | — | Vref + 0.125 | V |
| Single output slew rate | tsr | At 25 W to Vref | 0.4 | — | 2 | V/ns |
| Skew between pad rise/fall asymmetry + skew caused by SSN | t _{SKD} | clk = 266 MHz clk = 400 MHz | — | — | 0.2 0.1 | ns |

¹ Note that the JEDEC SSTL_18 specification (JESD8-15a) for class II operation supersedes any specification in this document.

- ² Vid(ac) specifies the input differential voltage $|V_{tr} - V_{cp}|$ required for switching, where V_{tr} is the “true” input signal and V_{cp} is the “complementary” input signal. The Minimum value is equal to $V_{ih}(ac) - V_{il}(ac)$.
- ³ The typical value of $V_{ix}(ac)$ is expected to be about $0.5 \times OVDD$. and $V_{ix}(ac)$ is expected to track variation of OVDD. $V_{ix}(ac)$ indicates the voltage at which differential input signal must cross.
- ⁴ The typical value of $V_{ox}(ac)$ is expected to be about $0.5 \times OVDD$ and $V_{ox}(ac)$ is expected to track variation in OVDD. $V_{ox}(ac)$ indicates the voltage at which differential output signal must cross.

Table 24 shows the AC parameters for LPDDR2 I/O operating in LPDDR2 mode.

Table 24. LPDDR2 I/O LPDDR2 mode AC Characteristics¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------|---|------------------|-----|------------------|------|
| AC input logic high | $V_{ih}(ac)$ | — | $V_{ref} + 0.22$ | — | OVDD | V |
| AC input logic low | $V_{il}(ac)$ | — | 0 | — | $V_{ref} - 0.22$ | V |
| AC differential input high voltage ² | $V_{idh}(ac)$ | — | 0.44 | — | — | V |
| AC differential input low voltage | $V_{idl}(ac)$ | — | — | — | 0.44 | V |
| Input AC differential cross point voltage ³ | $V_{ix}(ac)$ | Relative to OVDD/2 | -0.12 | — | 0.12 | V |
| Over/undershoot peak | V_{peak} | — | — | — | 0.35 | V |
| Over/undershoot area (above OVDD or below OVSS) | V_{area} | 266 MHz | — | — | 0.6 | V-ns |
| Single output slew rate | tsr | 50 Ω to V_{ref} . 5pF load. Drive impedance= 40 $\Omega \pm 30\%$ | 1.5 | — | 3.5 | V/ns |
| | | 50 Ω to V_{ref} . 5 pF load. Drive impedance= 60 $\Omega \pm 30\%$ | 1 | — | 2.5 | |
| Skew between pad rise/fall asymmetry + skew caused by SSN | t_{SKD} | clk = 266 MHz clk = 400 MHz | — | — | 0.2 0.1 | ns |

- ¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.
- ² Vid(ac) specifies the input differential voltage $|V_{tr} - V_{cp}|$ required for switching, where V_{tr} is the “true” input signal and V_{cp} is the “complementary” input signal. The Minimum value is equal to $V_{ih}(ac) - V_{il}(ac)$.
- ³ The typical value of $V_{ix}(ac)$ is expected to be about $0.5 \times OVDD$. and $V_{ix}(ac)$ is expected to track variation of OVDD. $V_{ix}(ac)$ indicates the voltage at which differential input signal must cross.

Table 25 shows the AC parameters for LPDDR2 I/O operating in DDR3 mode.

Table 25. LPDDR2 I/O DDR3 mode AC Characteristics¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------|----------------|-------------------|-----|-------------------|------|
| AC input logic high | $V_{ih}(ac)$ | — | $V_{ref} + 0.175$ | — | OVDD | V |
| AC input logic low | $V_{il}(ac)$ | — | 0 | — | $V_{ref} - 0.175$ | V |
| AC differential input voltage ² | $V_{id}(ac)$ | — | 0.35 | — | — | V |
| Input AC differential cross point voltage ³ | $V_{ix}(ac)$ | — | $V_{ref} - 0.15$ | — | $V_{ref} + 0.15$ | V |
| Output AC differential cross point voltage ⁴ | $V_{ox}(ac)$ | — | $V_{ref} - 0.15$ | — | $V_{ref} + 0.15$ | V |

Electrical Characteristics

Table 25. LPDDR2 I/O DDR3 mode AC Characteristics¹ (continued)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------|--------------------------------|-----|-----|------------|------|
| Single output slew rate | tsr | At 25 Ω to Vref | 2.5 | — | 5 | V/ns |
| Skew between pad rise/fall asymmetry + skew caused by SSN | t _{SKD} | clk = 266 MHz clk = 400 MHz | — | — | 0.2 0.1 | ns |

¹ Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

² Vid(ac) specifies the input differential voltage |Vtr-Vcpl| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

³ The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

⁴ The typical value of Vox(ac) is expected to be about 0.5 x OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

4.5.3 LVIO I/O AC Electrical Characteristics

AC electrical characteristics for LVIO I/O in slow and fast modes are presented in the [Table 26](#) and [Table 27](#), respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 26. LVIO I/O AC Parameters in Slow Mode

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|--------|----------------|-----|-----|-----|------|
| Input Transition Times ¹ | trm | — | — | — | 25 | ns |

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.5.4 UHVIO I/O AC Electrical Characteristics

Table 27. LVIO I/O AC Parameters in Fast Mode

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|--------|----------------|-----|-----|-----|------|
| Input Transition Times ¹ | trm | — | — | — | 25 | ns |

¹ Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

[Table 28](#) shows the AC parameters for UHVIO I/O operating in low output voltage mode. [Table 29](#) shows the AC parameters for UHVIO I/O operating in high output voltage mode.

Table 28. AC Electrical Characteristics of UHVIO Pad (Low Output Voltage Mode)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|------------------------|-----|------------------------|-------|
| Output Pad Transition Times (High Drive) | tr, tf | 15 pF 35 pF | — | — | 1.59/1.69 3.05/3.30 | ns |
| Output Pad Transition Times (Medium Drive) | tr, tf | 15 pF 35 pF | — | — | 2.16/2.35 4.45/4.84 | |
| Output Pad Transition Times (Low Drive) | tr, tf | 15 pF 35 pF | — | — | 4.06/4.42 8.79/9.55 | |
| Output Pad Slew Rate (High Drive) ¹ | tps | 15 pF 35 pF | 0.63/0.59 0.33/0.30 | — | — | V/ns |
| Output Pad Slew Rate (Medium Drive) ¹ | tps | 15 pF 35 pF | 0.46/0.42 0.22/0.21 | — | — | |
| Output Pad Slew Rate (Low Drive) ¹ | tps | 15 pF 35 pF | 0.25/0.23 0.11/0.11 | — | — | |
| Output Pad di/dt (High Drive) | tdit | — | — | — | 43.6 | mA/ns |
| Output Pad di/dt (Medium drive) | tdit | — | — | — | 32.3 | |
| Output Pad di/dt (Low drive) | tdit | — | — | — | 18.24 | |
| Input Transition Times ² | trm | — | — | — | 25 | ns |

¹ tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

² Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 29. AC Electrical Characteristics of UHVIO Pad (High Output Voltage Mode)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-------------------------|------|
| Output Pad Transition Times (High Drive) | tr, tf | 15 pF 35 pF | — | — | 1.72/1.92 3.46/3.70 | ns |
| Output Pad Transition Times (Medium Drive) | tr, tf | 15 pF 35 pF | — | — | 2.38/2.56 5.07/5.25 | |
| Output Pad Transition Times (Low Drive) | tr, tf | 15 pF 35 pF | — | — | 4.55/4.58 10.04/9.94 | |

Electrical Characteristics

Table 29. AC Electrical Characteristics of UHVIO Pad (High Output Voltage Mode) (continued)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|------------------------|-----|------|-------|
| Output Pad Slew Rate (High Drive) ¹ | tps | 15 pF 35 pF | 1.05/0.94 0.52/0.49 | — | — | V/ns |
| Output Pad Slew Rate (Medium Drive) ¹ | tps | 15 pF 35 pF | 0.76/0.71 0.36/0.34 | — | — | |
| Output Pad Slew Rate (Low Drive) ¹ | tps | 15 pF 35 pF | 0.40/0.93 0.18/0.18 | — | — | |
| Output Pad di/dt (High Drive) | tdit | — | — | — | 82.8 | mA/ns |
| Output Pad di/dt (Medium drive) | tdit | — | — | — | 65.6 | |
| Output Pad di/dt (Low drive) | tdit | — | — | — | 43.1 | |
| Input Transition Times ² | trm | — | — | — | 25 | ns |

¹ tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

² Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.5.5 LVDS I/O AC Electrical Characteristics

The differential output transition time waveform is shown in [Figure 7](#).

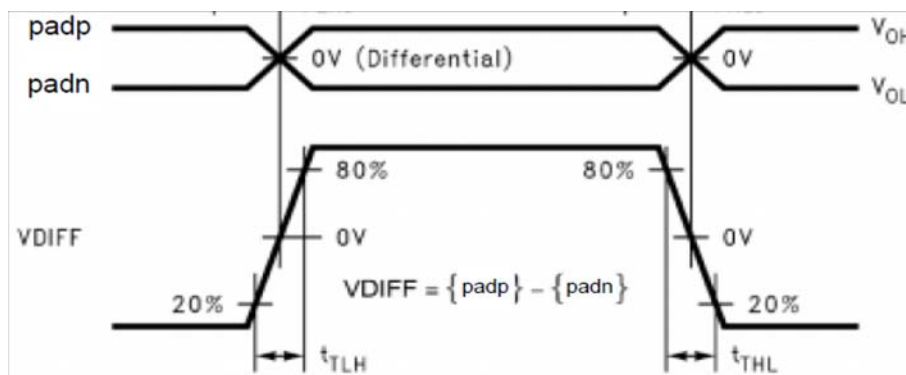


Figure 7. Differential LVDS Driver Transition Time Waveform

[Table 30](#) shows the AC parameters for LVDS I/O.

Table 30. AC Electrical Characteristics of LVDS Pad

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------|---------------------------------|------|-----|-----|------|
| Transition Low to High Time ¹ | t _{TLH} | Rload = 100 Ω, Clload = 2 pF | 0.26 | — | 0.5 | ns |
| Transition High to Low Time ¹ | t _{THL} | | 0.26 | — | 0.5 | |
| Operating Frequency | f | — | — | 300 | — | MHz |
| Offset voltage imbalance | Vos | — | — | — | 150 | mV |

¹ Measurement levels are 20–80% from output voltage.

4.6 System Modules Timing

This section contains the timing and electrical parameters for the modules in the i.MX53xD processor.

4.6.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 31 lists the timing parameters.

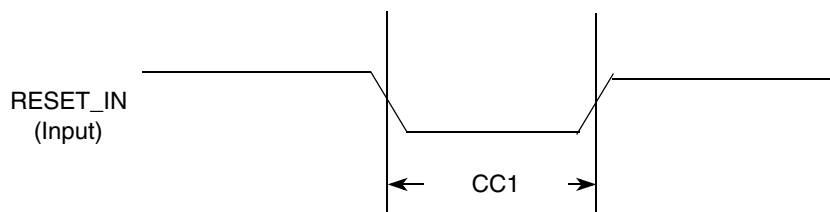


Figure 8. Reset Timing Diagram

Table 31. Reset Timing Parameters

| ID | Parameter | Min | Max | Unit |
|-----|--|-----|-----|------|
| CC1 | Duration of RESET_IN to be qualified as valid (input slope = 5 ns) | 50 | — | ns |

4.6.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 32 lists the timing parameters.

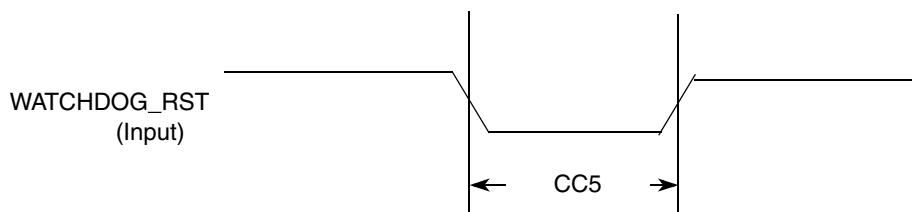


Figure 9. WATCHDOG_RST Timing Diagram

Table 32. WATCHDOG_RST Timing Parameters

| ID | Parameter | Min | Max | Unit |
|-----|--------------------------------------|-----|-----|------------|
| CC5 | Duration of WATCHDOG_RESET Assertion | 1 | — | T_{CKIL} |

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 μ s.

4.6.3 Clock Amplifier Parameters (CKIH1, CKIH2)

The input to Clock Amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required.

Electrical Characteristics

Table 33 shows the electrical parameters of CAMP.

Table 33. CAMP Electrical Parameters (CKIH1, CKIH2)

| Parameter | Min | Typ | Max | Unit |
|--|------------------|-----|-----------|------|
| Input frequency | 8.0 | — | 40.0 | MHz |
| VIL (for square wave input) | 0 | — | 0.3 | V |
| VIH (for square wave input) ¹ | NVCC_CKIH - 0.25 | — | NVCC_CKIH | V |
| Sinusoidal input amplitude | 0.4 | — | VDD | Vp-p |
| Output duty cycle | 45 | 50 | 55 | % |

¹ NVCC_CKIH is the supply voltage of CAMP.

4.6.4 DPLL Electrical Parameters

Table 34 shows the electrical parameters of digital phase-locked loop (DPLL).

Table 34. DPLL Electrical Parameters

| Parameter | Test Conditions/Remarks | Min | Typ | Max | Unit |
|--|--|-----------|------|---|---------------------|
| Reference clock frequency range ¹ | — | 10 | — | 100 | MHz |
| Reference clock frequency range after pre-divider | — | 10 | — | 40 | MHz |
| Output clock frequency range (dpdck_2) | — | 300 | — | 1025 | MHz |
| Pre-division factor ² | — | 1 | — | 16 | — |
| Multiplication factor integer part | — | 5 | — | 15 | — |
| Multiplication factor numerator ³ | Should be less than denominator | -67108862 | — | 67108862 | — |
| Multiplication factor denominator ² | — | 1 | — | 67108863 | — |
| Output Duty Cycle | — | 48.5 | 50 | 51.5 | % |
| Frequency lock time ⁴ (FOL mode or non-integer MF) | — | — | — | 398 | T _{apdref} |
| Phase lock time | — | — | — | 100 | μs |
| Frequency jitter ⁵ (peak value) | — | — | 0.02 | 0.04 | T _{dck} |
| Phase jitter (peak value) | FPL mode, integer and fractional MF | — | 2.0 | 3.5 | ns |
| Power dissipation | f _{dck} = 300 MHz at avdd = 1.8 V, dvdd = 1.2 V f _{dck} = 650 MHz at avdd = 1.8 V, dvdd = 1.2 V | — | — | 0.65 (avdd) 0.92 (dvdd) 1.98 (avdd) 1.8 (dvdd) | mW |

¹ Device input range cannot exceed the electrical specifications of the CAMP, see Table 33.

² The values specified here are internal to DPLL. Inside the DPLL, a “1” is added to the value specified by the user. Therefore, the user has to enter a value “1” less than the desired value at the inputs of DPLL for PDF and MFD.

³ The maximum total multiplication factor (MFI + MFN/MFD) allowed is 15. Therefore, if the MFI value is 15, MFN value must be zero.

- ⁴ T_{dpdref} is the time period of the reference clock after predivider. According to the specification, the maximum lock time in FOL mode is 398 cycles of divided reference clock when DPLL starts after full reset.
- ⁵ T_{dck} is the time period of the output clock, $dpdck_2$.

4.6.5 NAND Flash Controller (NFC) Parameters

This section provides the relative timing requirements among various signals of NFC at the module level, in each operational mode.

Timing parameters in [Figure 10](#), [Figure 11](#), [Figure 12](#), [Figure 13](#), [Figure 15](#), and [Table 36](#) show the default NFC mode (asymmetric mode) using two Flash clock cycles per one access of RE_B and WE_B.

Timing parameters in [Figure 10](#), [Figure 11](#), [Figure 12](#), [Figure 14](#), [Figure 15](#), and [Table 36](#) show symmetric NFC mode using one Flash clock cycle per one access of RE_B and WE_B.

With reference to the timing diagrams, a high is defined as 80% of signal value and low is defined as 20% of signal value. All parameters are given in nanoseconds. The BGA contact load used in calculations is 20 pF (except for NF16— 40 pF) and there is maximum drive strength on all contacts.

All timing parameters are a function of T, which is the period of the flash_clk clock (“enfc_clk” at system level). This clock frequency can be controlled by the user, configuring CCM (SoC clock controller). The clock is derived from emi_slow_clk after single divider.

[Figure 35](#) demonstrates several examples of clock frequency settings.

Table 35. NFC Clock Settings Examples

| emi_slow_clk (MHz) | nfc_podf (Division Factor) | enfc_clk (MHz) | T-Clock Period (ns) |
|--------------------|----------------------------|--------------------|---------------------|
| 100 (Boot mode) | 7 ¹ | 14.29 | 70 |
| | 3 ² | 33.33 | 30 |
| 133 | 4 | 33.33 | 30 |
| | 3 | 44.33 ³ | 22.5 |
| | 2 | 66 ³ | 15 |

¹ Boot value NFC_FREQ_SEL Fuse High (burned)

² Boot value NFC_FREQ_SEL Fuse Low

³ For RBB_MODE=1, using NANDF_RB0 signal for ready/busy indication. This mode require setting the delay line. See the Reference Manual for details.

NOTE

A potential limitation for minimum clock frequency may exist for some devices. When the clock frequency is too low, the data bus capturing might occur after the specified t_{rthoh} (RE_B high to output hold) period. Setting the clock frequency above 25.6 MHz (that is, $T = 39$ ns) guaranties a proper operation for devices having $t_{rthoh} > 15$ ns. It is also recommended that the NFC_FREQ_SEL Fuse be set accordingly to initiate the boot with 33.33 MHz clock.

Lower frequency operation can be supported for most available devices in the market, relying on data lines Bus-Keeper logic. This depends on device behavior on the data bus in the time interval between data output valid to data output high-Z state. In NAND device parameters this period is marked between $t_{r\text{hoh}}$ and $t_{r\text{hz}}$ (RE_B high to output high-Z). In most devices, the data transition from valid value to high-Z occurs without going through other states. Setting the data bus pads to Bus-Keeper mode in the IOMUXC registers, keeps the data bus valid internally after the specified hold time, allowing proper capturing with slower clock.

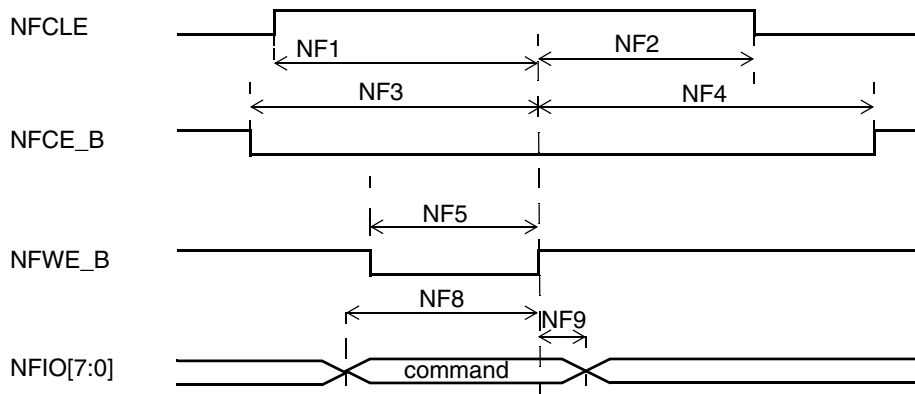


Figure 10. Command Latch Cycle Timing

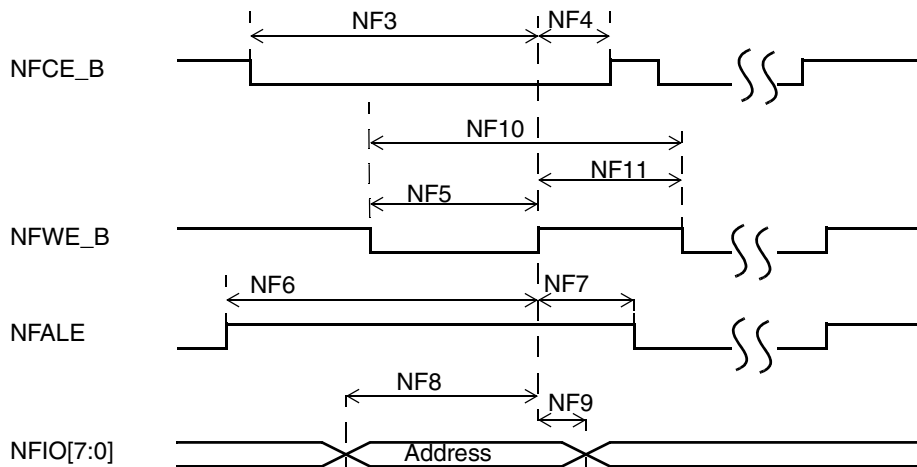


Figure 11. Address Latch Cycle Timing

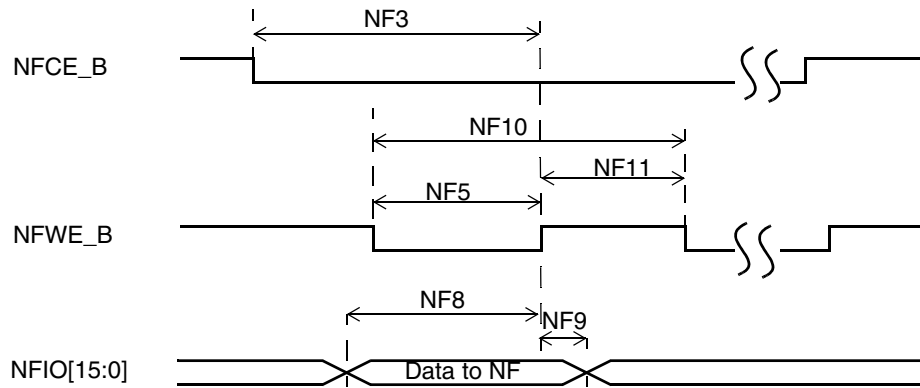


Figure 12. Write Data Latch Timing

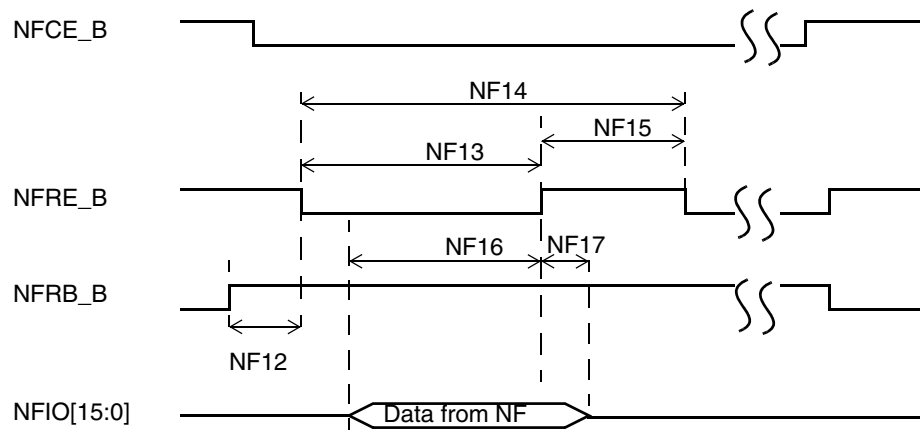


Figure 13. Read Data Latch Timing, Asymmetric Mode

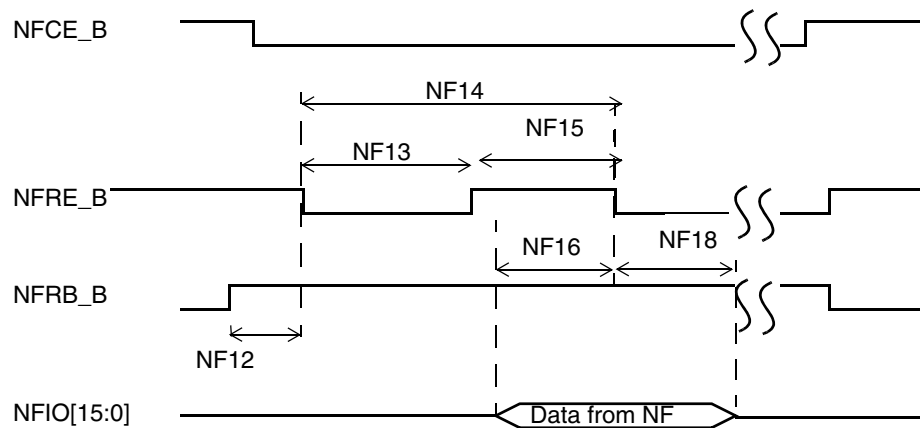


Figure 14. Read Data Latch Timing, Symmetric Mode

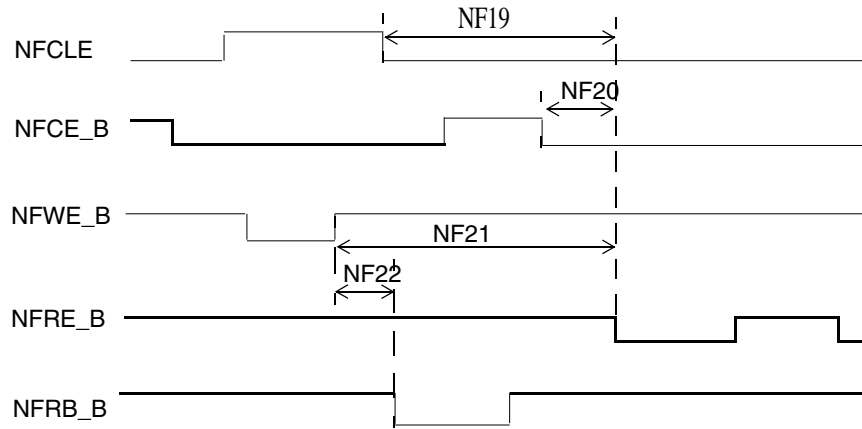


Figure 15. Other Timing Parameters

Table 36. NFC—Timing Characteristics

| ID | Parameter | Symbol | Asymmetric Mode Min | Symmetric Mode Min | Max |
|-------------------|-----------------------|--------|--------------------------------|-------------------------|-----------------------|
| NF1 | NFCLE setup Time | tCLS | 2T + 0.1 | 2T + 0.1 | — |
| NF2 | NFCLE Hold Time | tCLH | T - 4.45 | T - 4.45 | — |
| NF3 ¹ | NFCE_B Setup Time | tCS | 3T + 0.95 | 3T+0.95 | — |
| NF4 | NFCE_B Hold Time | tCH | 2T-5.55 | 1.5T-5.55 | — |
| NF5 | NFWE_B Pulse Width | tWP | T - 1.4 | 0.5T - 1.4 | — |
| NF6 | NFALE Setup Time | tALS | 2T + 0.1 | 2T + 0.1 | — |
| NF7 | NFALE Hold Time | tALH | T - 4.45 | T - 4.45 | — |
| NF8 | Data Setup Time | tDS | T - 0.9 | 0.5T - 0.9 | — |
| NF9 | Data Hold Time | tDH | T - 5.55 | 0.5T - 5.55 | — |
| NF10 | Write Cycle Time | tWC | 2T | T-0.5 | — |
| NF11 | NFWE_B Hold Time | tWH | T - 1.15 | 0.5T - 1.15 | — |
| NF12 | Ready to NFRE_B Low | tRR | 9T + 8.9 | 9T + 8.9 | — |
| NF13 | NFRE_B Pulse Width | tRP | 1.5T | 0.5T-1 | — |
| NF14 | READ Cycle Time | tRC | 2T | T | — |
| NF15 | NFRE_B High Hold Time | tREH | 0.5T - 1.15 | 0.5T - 1.15 | — |
| NF16 ² | Data Setup on READ | tDSR | 11.2 + 0.5T - Tdl ³ | 11.2 - Tdl ³ | — |
| NF17 ⁴ | Data Hold on READ | tDHR | 0 | — | 2T _{ack} + T |
| NF18 ⁵ | Data Hold on READ | tDHR | — | Tdl ³ - 11.2 | 2T _{ack} + T |
| NF19 | CLE to RE delay | tCLR | 9T | 9T | — |
| NF20 | CE to RE delay | tCRE | T - 3.45 | T - 3.45 | T + 0.3 |
| NF21 | WE high to RE low | tWHR | 10.5T | 10.5T | — |
| NF22 | WE high to busy | tWB | — | — | 6T |

¹ In case of NUM_OF_DEVICES is greater than 0 (for example, interleaved mode), then only during the data phase of symmetric mode the setup time will equal 1.5T + 0.95.

² t_{DSR} is calculated by the following formula:

$$\text{Asymmetric mode: } t_{DSR} = t_{REpd} + t_{Dpd} + \frac{1}{2}T - Tdl^3$$

$$\text{Symmetric mode: } t_{DSR} = t_{REpd} + t_{Dpd} - Tdl^3$$

$$t_{REpd} + t_{Dpd} = 11.2 \text{ ns (including clock skew)}$$

where t_{REpd} is RE propagation delay in the chip including I/O pad delay, and t_{Dpd} is Data propagation delay from I/O pad to EXTMC including I/O pad delay.

t_{DSR} can be used to determine t_{REA} max parameter with the following formula: t_{REA} = 1.5T - t_{DSR}.

³ Tdl is composed of 4 delay-line units each generates an equal delay with min 1.25 ns and max 1 aclk period (T_{ack}). Default is 1/4 aclk period for each delay-line unit, so all 4 delay lines together generates a total of 1 aclk period. T_{ack} is “emi_slow_clk” of the system, which default value is 7.5 ns (133 MHz).

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⁴ NF17 is defined only in asymmetric operation mode.

NF17 max value is equivalent to max t_{RHZ} value that can be used with NFC.

T_{ack} is “emi_slow_clk” of the system.

⁵ NF18 is defined only in Symmetric operation mode.

t_{DHR} (MIN) is calculated by the following formula: $T_{dl}^3 - (t_{REpd} + t_{Dpd})$

where t_{REpd} is RE propagation delay in the chip including I/O pad delay, and t_{Dpd} is Data propagation delay from I/O pad to EXTMC including I/O pad delay.

NF18 max value is equivalent to max t_{RHZ} value that can be used with NFC.

T_{ack} is “emi_slow_clk” of the system.

4.6.6 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.6.6.1 EIM Signal Cross Reference

Table 37 is a guide intended to help the user identify signals in the External Interface Module Chapter of the Reference Manual which are identical to those mentioned in this data sheet.

Table 37. EIM Signal Cross Reference

| Reference Manual EIM Chapter Nomenclature | Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature |
|--|---|
| BCLK | EIM_BCLK |
| CSx | EIM_CSx |
| WE_B | EIM_RW |
| OE_B | EIM_OE |
| BEy_B | EIM_EBx |
| ADV | EIM_LBA |
| ADDR | EIM_A[25:16], EIM_DA[15:0] |
| ADDR/M_DATA | EIM_DAx (Addr/Data muxed mode) |
| DATA | EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus) |
| WAIT_B | EIM_WAIT |

4.6.6.2 EIM Interface Pads Allocation

EIM supports 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. In some of the modes the EIM and the NAND FLASH have shared data bus. Table 38 provides EIM interface pads allocation in different modes.

Table 38. EIM Internal Module Multiplexing

| Setup | Non Multiplexed Address/Data Mode | | | | | | Multiplexed Address/Data mode | |
|--------------------------|-----------------------------------|--------------------------------|-----------------------|--------------------------------|-----------------------|-------------------------------|-------------------------------|-------------------------------|
| | 8 Bit | | | 16 Bit | | 32 Bit | 16 Bit | 32 Bit |
| | MUM = 0, DSZ = 100 | MUM = 0, DSZ = 101 | MUM = 0, DSZ = 111 | MUM = 0, DSZ = 001 | MUM = 0, DSZ = 010 | MUM = 0, DSZ = 011 | MUM = 1, DSZ = 001 | MUM = 1, DSZ = 011 |
| A[15:0] | EIM_DA [15:0] | EIM_DA [15:0] | EIM_DA [15:0] | EIM_DA [15:0] | EIM_DA [15:0] | EIM_DA [15:0] | EIM_DA [15:0] | EIM_DA [15:0] |
| A[25:16] | EIM_A [25:16] | EIM_A [25:16] | EIM_A [25:16] | EIM_A [25:16] | EIM_A [25:16] | EIM_A [24:16] ¹ | EIM_A [25:16] | NANDF_D [8:0] ¹ |
| D[7:0], EIM_EB 0 | NANDF_D [7:0] ² | — | — | NANDF_D [7:0] ² | — | NANDF_D [7:0] | EIM_DA [7:0] | EIM_DA [7:0] |
| D[15:8], EIM_EB 1 | — | NANDF_D [15:8] ³ | — | NANDF_D [15:8] ³ | — | NANDF_D [15:8] | EIM_DA [15:8] | EIM_DA [15:8] |
| D[23:16], EIM_EB 2 | — | — | — | — | EIM_D [23:16] | EIM_D [23:16] | — | NANDF_D [7:0] |
| D[31:24], EIM_EB 3 | — | — | EIM_D [31:24] | — | EIM_D [31:24] | EIM_D [31:24] | — | NANDF_D [15:8] |

¹ For 32-bit mode, the address range is A[24:0], due to address space allocation in memory map.

² NANDF_D[7:0] multiplexed on ALT3 mode of PATA_DATA[7:0]

³ NANDF_D[15:8] multiplexed on ALT3 mode of PATA_DATA[15:8]

4.6.6.3 General EIM Timing-Synchronous Mode

Figure 16, Figure 17, and Table 39 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

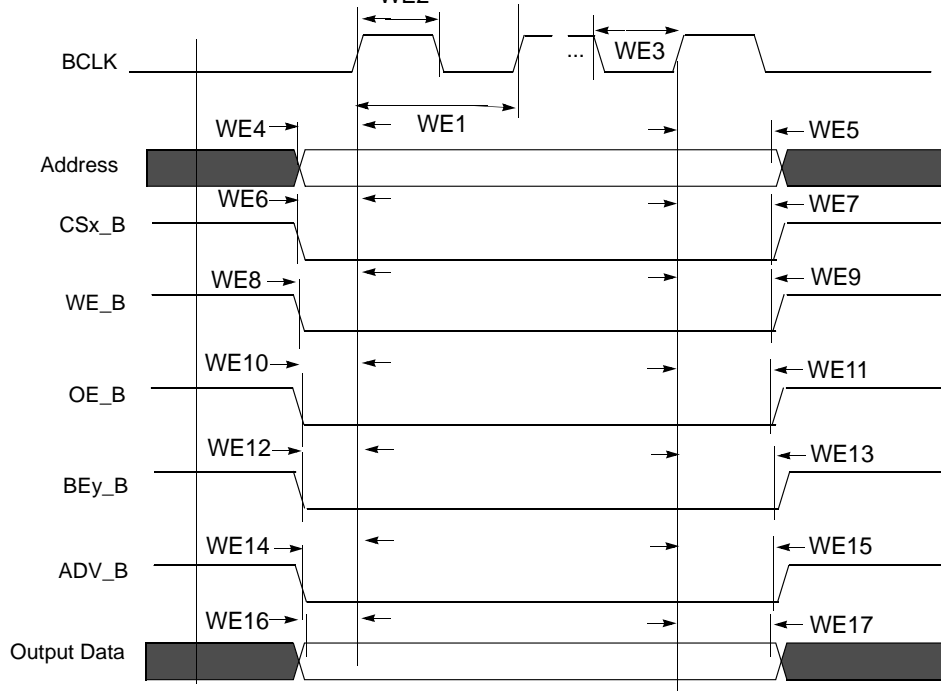


Figure 16. EIM Outputs Timing Diagram

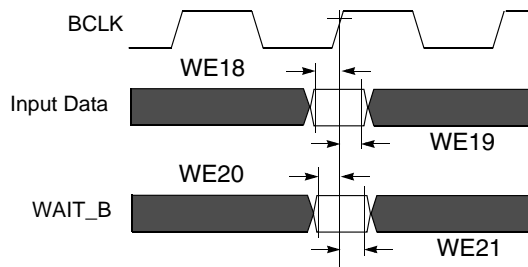


Figure 17. EIM Inputs Timing Diagram

Table 39. EIM Bus Timing Parameters ¹

| ID | Parameter | BCD = 0 | | BCD = 1 | | BCD = 2 | | BCD = 3 | |
|-----|------------------------------|---------|-----|---------|-----|---------|-----|---------|-----|
| | | Min | Max | Min | Max | Min | Max | Min | Max |
| WE1 | BCLK Cycle time ² | t | | 2 x t | | 3 x t | | 4 x t | |
| WE2 | BCLK Low Level Width | 0.4 x t | | 0.8 x t | | 1.2 x t | | 1.6 x t | |

Table 39. EIM Bus Timing Parameters (continued)¹

| ID | Parameter | BCD = 0 | | BCD = 1 | | BCD = 2 | | BCD = 3 | |
|------|--|------------------------|------------------------|----------------|------------|------------------------|------------------------|----------------------|----------------------|
| | | Min | Max | Min | Max | Min | Max | Min | Max |
| WE3 | BCLK High Level Width | $0.4 \times t$ | | $0.8 \times t$ | | $1.2 \times t$ | | $1.6 \times t$ | |
| WE4 | Clock rise to address valid ³ | $-0.5 \times t - 1.25$ | $-0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $-1.5 \times t - 1.25$ | $-1.5 \times t + 1.75$ | $-2 \times t - 1.25$ | $-2 \times t + 1.75$ |
| WE5 | Clock rise to address invalid | $0.5 \times t - 1.25$ | $0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $1.5 \times t - 1.25$ | $1.5 \times t + 1.75$ | $2 \times t - 1.25$ | $2 \times t + 1.75$ |
| WE6 | Clock rise to CSx_B valid | $-0.5 \times t - 1.25$ | $-0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $-1.5 \times t - 1.25$ | $-1.5 \times t + 1.75$ | $-2 \times t - 1.25$ | $-2 \times t + 1.75$ |
| WE7 | Clock rise to CSx_B invalid | $0.5 \times t - 1.25$ | $0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $1.5 \times t - 1.25$ | $1.5 \times t + 1.75$ | $2 \times t - 1.25$ | $2 \times t + 1.75$ |
| WE8 | Clock rise to WE_B Valid | $-0.5 \times t - 1.25$ | $-0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $-1.5 \times t - 1.25$ | $-1.5 \times t + 1.75$ | $-2 \times t - 1.25$ | $-2 \times t + 1.75$ |
| WE9 | Clock rise to WE_B Invalid | $0.5 \times t - 1.25$ | $0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $1.5 \times t - 1.25$ | $1.5 \times t + 1.75$ | $2 \times t - 1.25$ | $2 \times t + 1.75$ |
| WE10 | Clock rise to OE_B Valid | $-0.5 \times t - 1.25$ | $-0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $-1.5 \times t - 1.25$ | $-1.5 \times t + 1.75$ | $-2 \times t - 1.25$ | $-2 \times t + 1.75$ |
| WE11 | Clock rise to OE_B Invalid | $0.5 \times t - 1.25$ | $0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $1.5 \times t - 1.25$ | $1.5 \times t + 1.75$ | $2 \times t - 1.25$ | $2 \times t + 1.75$ |
| WE12 | Clock rise to BEy_B Valid | $-0.5 \times t - 1.25$ | $-0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $-1.5 \times t - 1.25$ | $-1.5 \times t + 1.75$ | $-2 \times t - 1.25$ | $-2 \times t + 1.75$ |
| WE13 | Clock rise to BEy_B Invalid | $0.5 \times t - 1.25$ | $0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $1.5 \times t - 1.25$ | $1.5 \times t + 1.75$ | $2 \times t - 1.25$ | $2 \times t + 1.75$ |
| WE14 | Clock rise to ADV_B Valid | $-0.5 \times t - 1.25$ | $-0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $-1.5 \times t - 1.25$ | $-1.5 \times t + 1.75$ | $-2 \times t - 1.25$ | $-2 \times t + 1.75$ |
| WE15 | Clock rise to ADV_B Invalid | $0.5 \times t - 1.25$ | $0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $1.5 \times t - 1.25$ | $1.5 \times t + 1.75$ | $2 \times t - 1.25$ | $2 \times t + 1.75$ |
| WE16 | Clock rise to Output Data Valid | $-0.5 \times t - 1.25$ | $-0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $-1.5 \times t - 1.25$ | $-1.5 \times t + 1.75$ | $-2 \times t - 1.25$ | $-2 \times t + 1.75$ |
| WE17 | Clock rise to Output Data Invalid | $0.5 \times t - 1.25$ | $0.5 \times t + 1.75$ | $t - 1.25$ | $t + 1.75$ | $1.5 \times t - 1.25$ | $1.5 \times t + 1.75$ | $2 \times t - 1.25$ | $2 \times t + 1.75$ |
| WE18 | Input Data setup time to Clock rise | 2 | — | 4 | — | — | — | — | — |
| WE19 | Input Data hold time from Clock rise | 2 | — | 2 | — | — | — | — | — |
| WE20 | WAIT_B setup time to Clock rise | 2 | — | 4 | — | — | — | — | — |
| WE21 | WAIT_B hold time from Clock rise | 2 | — | 2 | — | — | — | — | — |

Electrical Characteristics

- ¹ t is the maximal EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed BCLK frequency is 104 MHz. As a result, if BCD = 0, axi_clk must be ≤ 104 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a BCLK of 66.5 MHz. When the clock branch to EIM is decreased to 104 MHz, other busses are impacted which are clocked from this source. See the CCM chapter of the i.MX53 Reference Manual for a detailed clock tree description.
- ² BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.
- ³ For signal measurements “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

4.6.6.4 Examples of EIM Synchronous Accesses

Figure 18 to Figure 21 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

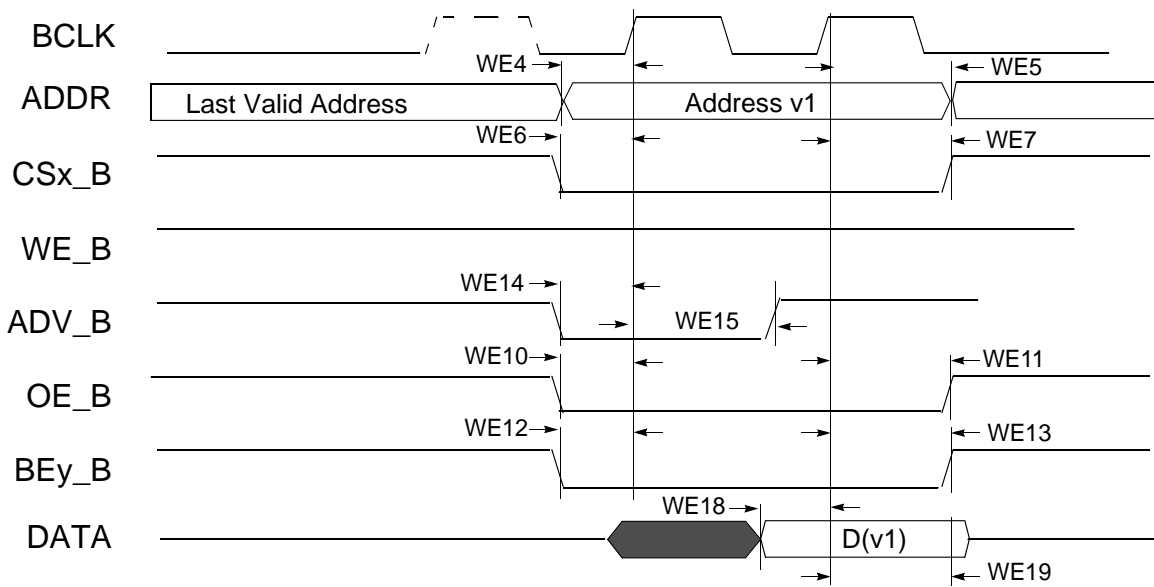


Figure 18. Synchronous Memory Read Access, WSC=1

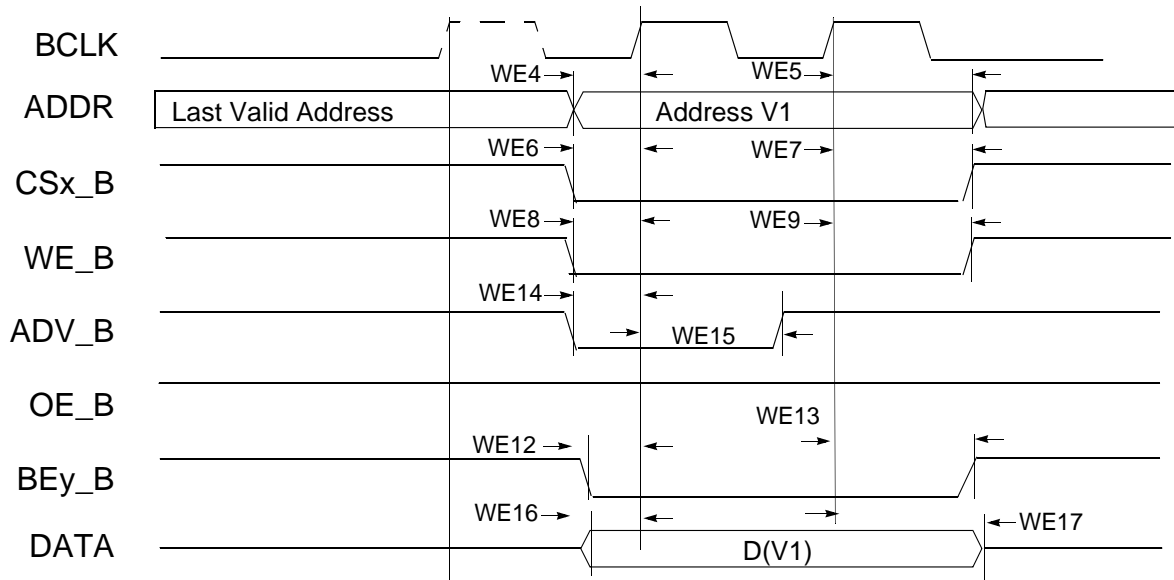


Figure 19. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

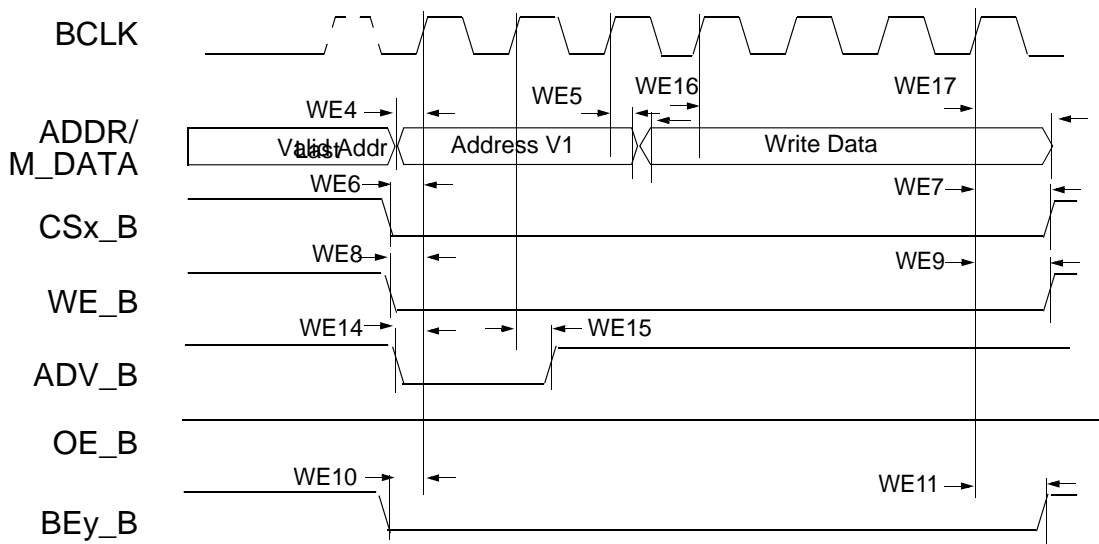


Figure 20. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

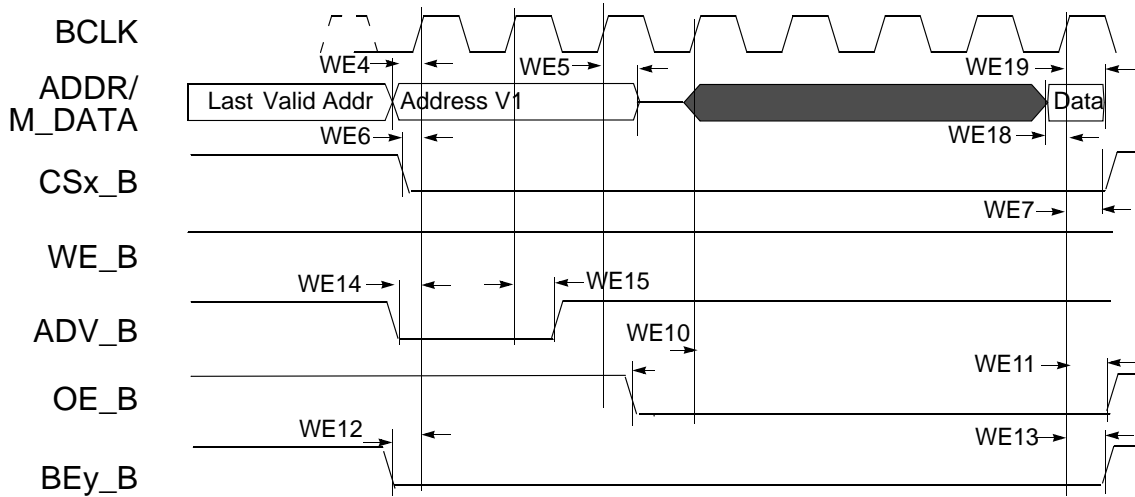


Figure 21. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, and OEA=0

4.6.6.5 General EIM Timing-Asynchronous Mode

Figure 22 through Figure 27, and Table 40 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 22 through Figure 25 as RWSC, OEN, and CSN is configured differently. Refer to i.MX53xD RM for the EIM programming model.

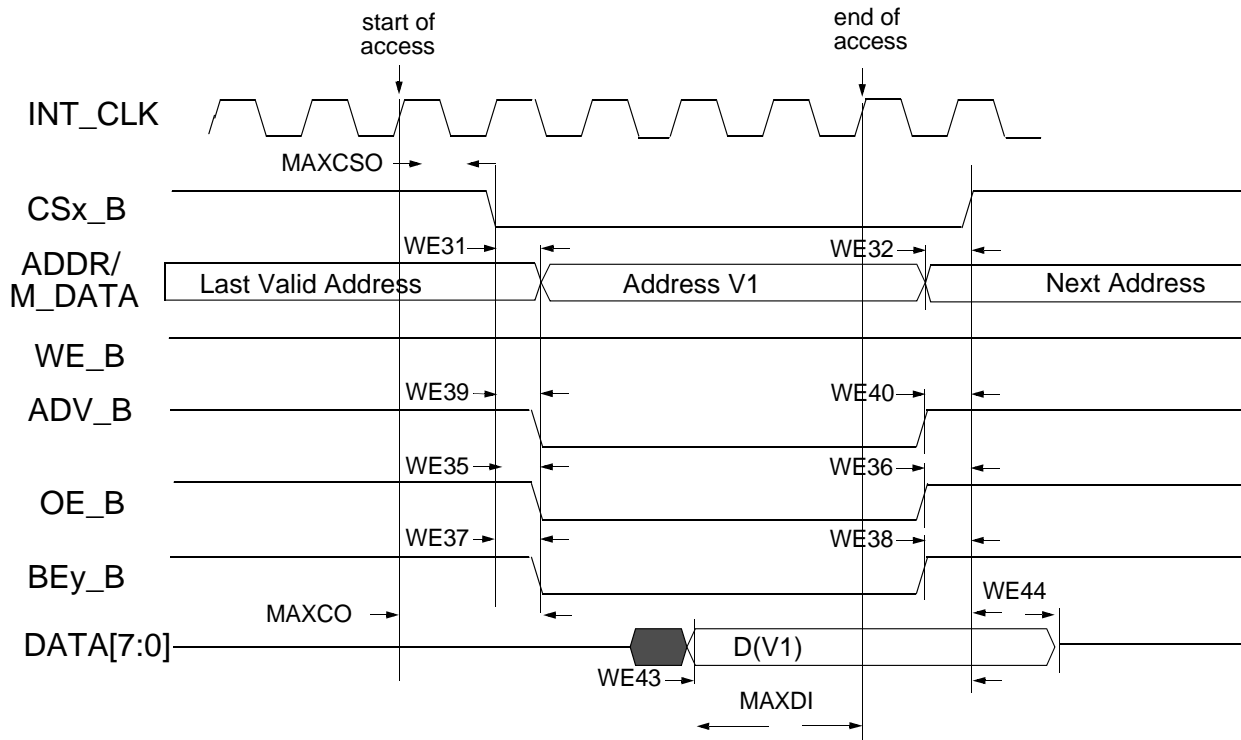


Figure 22. Asynchronous Memory Read Access (RWSC = 5)

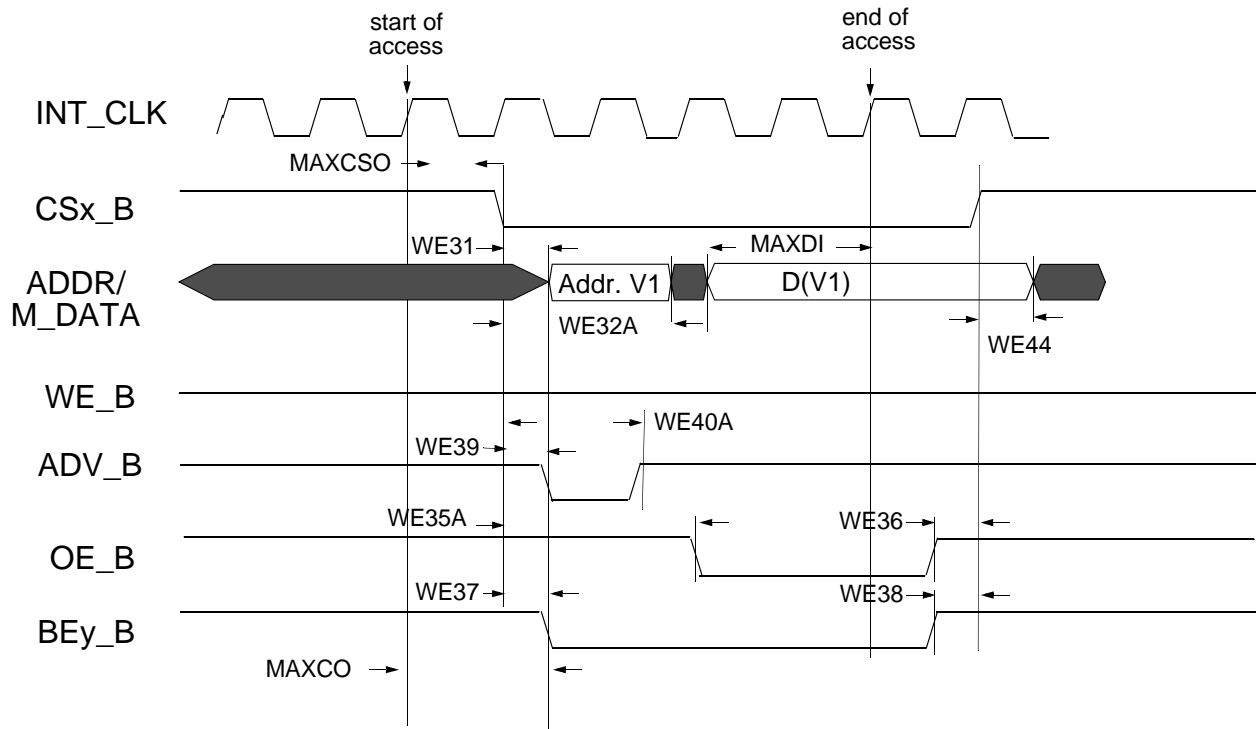


Figure 23. Asynchronous A/D Muxed Read Access (RWSC = 5)

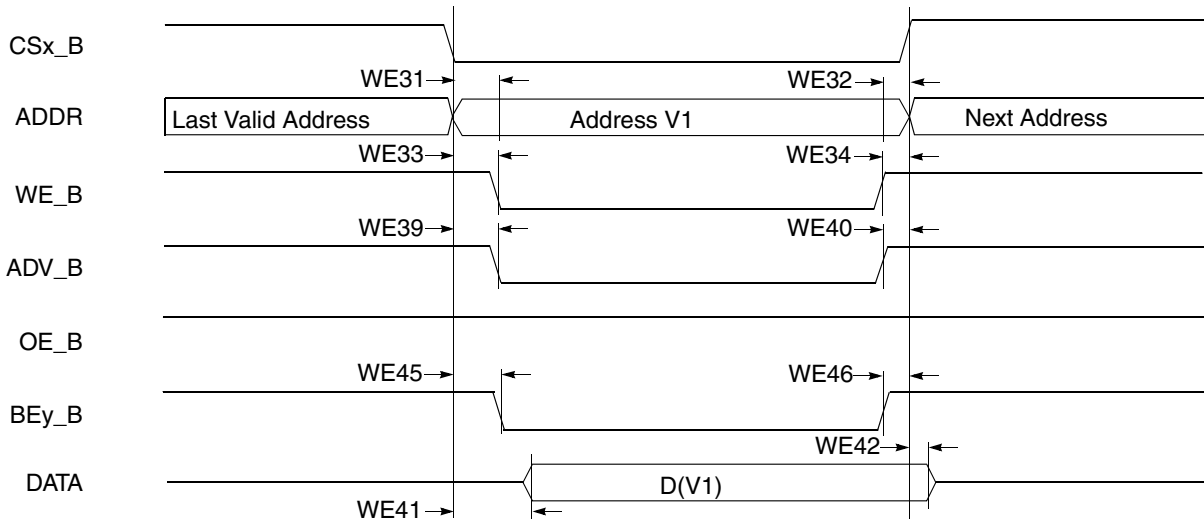


Figure 24. Asynchronous Memory Write Access

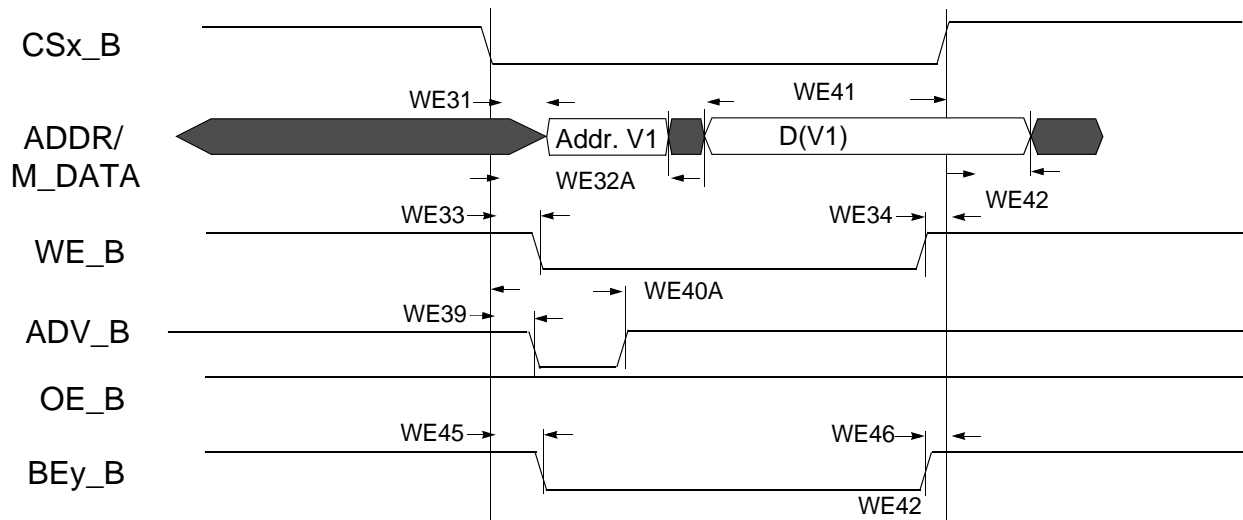


Figure 25. Asynchronous A/D Muxed Write Access

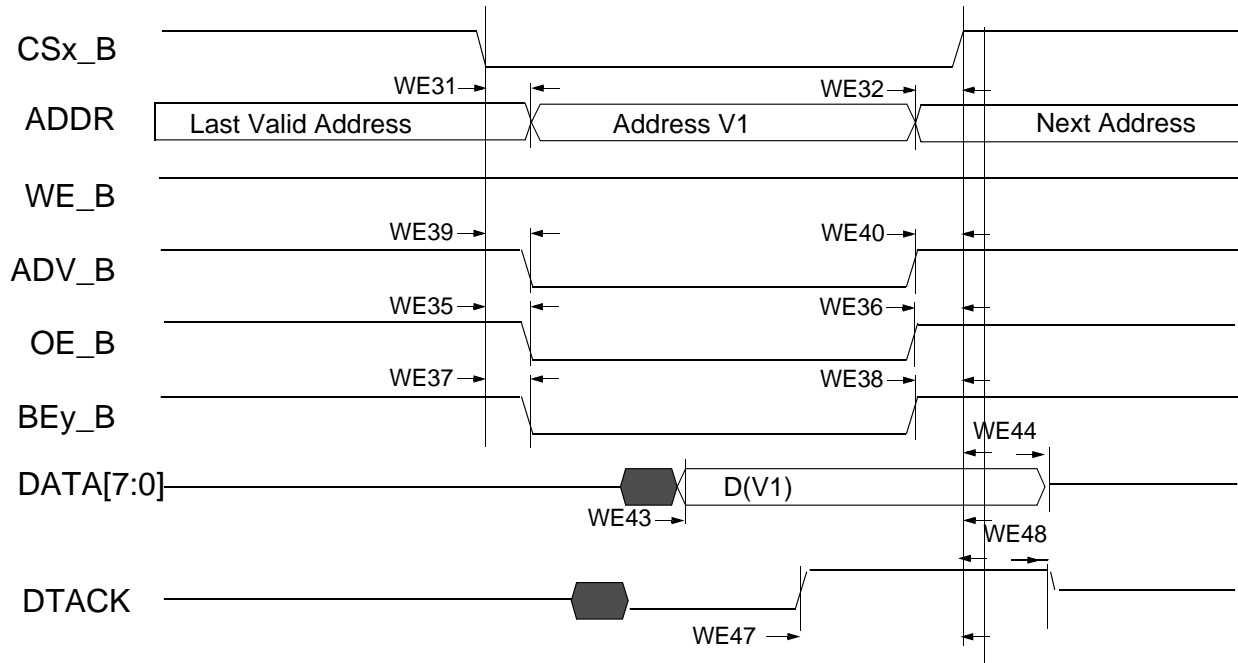


Figure 26. DTACK Read Access (DAP=0)

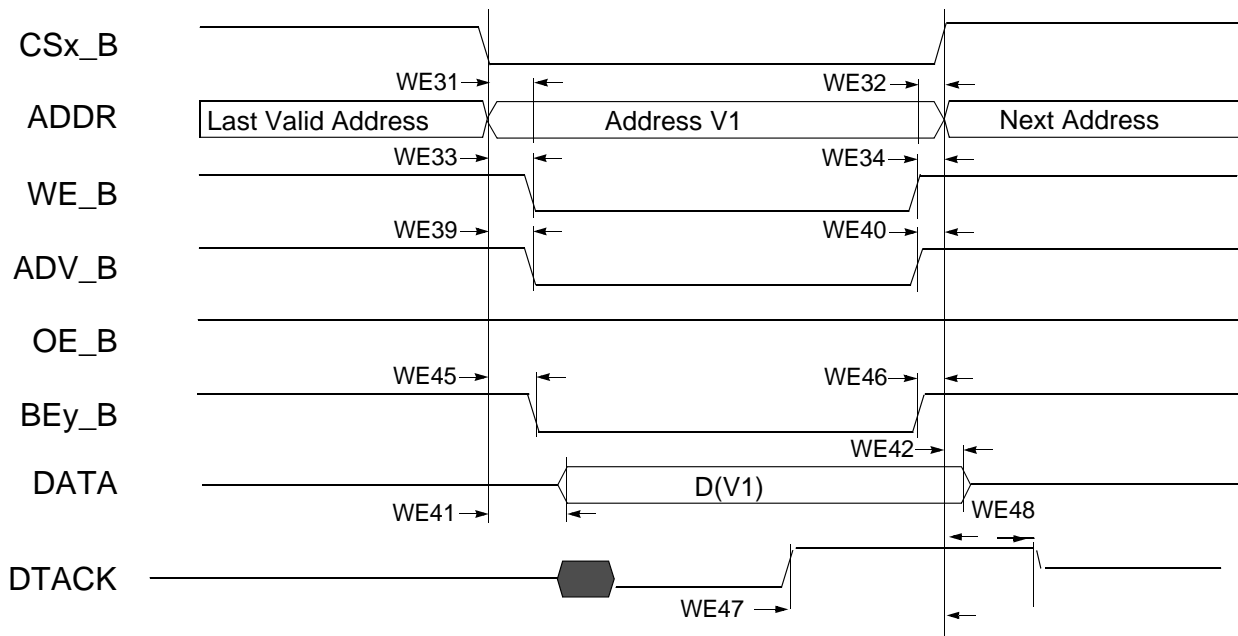


Figure 27. DTACK Write Access (DAP=0)

Electrical Characteristics

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip Select

| Ref No. | Parameter | Determination by Synchronous measured parameters ¹² | Min | Max (If 133 MHz is supported by SOC) | Unit |
|------------------|---|--|--|---|------|
| WE31 | CSx_B valid to Address Valid | WE4 - WE6 - CSA ³ | — | 3 - CSA | ns |
| WE32 | Address Invalid to CSx_B invalid | WE7 - WE5 - CSN ⁴ | — | 3 - CSN | ns |
| WE32A(muxed A/D) | CSx_B valid to Address Invalid | $t^5 + WE4 - WE7 + (ADV_N + ADVA + 1 - CSA^3)$ | -3 + (ADV_N + ADVA + 1 - CSA) | — | ns |
| WE33 | CSx_B Valid to WE_B Valid | WE8 - WE6 + (WEA - CSA) | — | 3 + (WEA - CSA) | ns |
| WE34 | WE_B Invalid to CSx_B Invalid | WE7 - WE9 + (WEN - CSN) | — | 3 - (WEN - CSN) | ns |
| WE35 | CSx_B Valid to OE_B Valid | WE10 - WE6 + (OEA - CSA) | — | 3 + (OEA - CSA) | ns |
| WE35A(muxed A/D) | CSx_B Valid to OE_B Valid | WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - CSA) | -3 + (OEA + RADVN + RADVA + ADH + 1 - CSA) | 3 + (OEA + RADVN + RADVA + ADH + 1 - CSA) | ns |
| WE36 | OE_B Invalid to CSx_B Invalid | WE7 - WE11 + (OEN - CSN) | — | 3 - (OEN - CSN) | ns |
| WE37 | CSx_B Valid to BEy_B Valid (Read access) | WE12 - WE6 + (RBEA - CSA) | — | 3 + (RBEA ⁶ - CSA) | ns |
| WE38 | BEy_B Invalid to CSx_B Invalid (Read access) | WE7 - WE13 + (RBEN - CSN) | — | 3 - (RBEN ⁷ - CSN) | ns |
| WE39 | CSx_B Valid to ADV_B Valid | WE14 - WE6 + (ADVA - CSA) | — | 3 + (ADVA - CSA) | ns |
| WE40 | ADV_B Invalid to CSx_B Invalid (ADVL is asserted) | WE7 - WE15 - CSN | — | 3 - CSN | ns |
| WE40A(muxed A/D) | CSx_B Valid to ADV_B Invalid | WE14 - WE6 + (ADV_N + ADVA + 1 - CSA) | -3 + (ADV_N + ADVA + 1 - CSA) | 3 + (ADV_N + ADVA + 1 - CSA) | ns |
| WE41 | CSx_B Valid to Output Data Valid | WE16 - WE6 - WCSA | — | 3 - WCSA | ns |
| WE41A(muxed A/D) | CSx_B Valid to Output Data Valid | WE16 - WE6 + (WADV_N + WADVA + ADH + 1 - WCSA) | — | 3 + (WADV_N + WADVA + ADH + 1 - WCSA) | ns |
| WE42 | Output Data Invalid to CSx_B Invalid | WE17 - WE7 - CSN | — | 3 - CSN | ns |
| MAXCO | Output max. delay from internal driving ADDR/control FFs to chip outputs. | 10 | — | — | ns |
| MAXCSO | Output max. delay from CSx internal driving FFs to CSx out. | 10 | — | — | |
| MAXDI | DATA MAXIMUM delay from chip input data to its internal FF | 5 | — | — | |

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip Select

| Ref No. | Parameter | Determination by Synchronous measured parameters ¹² | Min | Max (If 133 MHz is supported by SOC) | Unit |
|---------|---|--|-------------------------|--------------------------------------|------|
| WE43 | Input Data Valid to CSx_B Invalid | MAXCO - MAXCSO + MAXDI | MAXCO - MAXCSO + MAXDI | — | ns |
| WE44 | CSx_B Invalid to Input Data invalid | 0 | 0 | — | ns |
| WE45 | CSx_B Valid to BEy_B Valid (Write access) | WE12 - WE6 + (WBEA - CSA) | — | 3 + (WBEA - CSA) | ns |
| WE46 | BEy_B Invalid to CSx_B Invalid (Write access) | WE7 - WE13 + (WBEN - CSN) | — | -3 + (WBEN - CSN) | ns |
| MAXDTI | DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization | | — | — | — |
| WE47 | Dtack Active to CSx_B Invalid | MAXCO - MAXCSO + MAXDTI | MAXCO - MAXCSO + MAXDTI | — | ns |
| WE48 | CSx_B Invalid to Dtack invalid | 0 | 0 | — | ns |

¹ Parameters WE4... WE21 value see column BCD = 0 in Table 39.

² All config. parameters (CSA,CSN,WBEA,WBEN,ADVA,ADVN,OEN,OEA,RBEA & RBEN) are in cycle units.

³ CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

⁴ CS Negation. This bit field determines when CS signal is negated during read/write cycles.

⁵ t is axi_clk cycle time.

⁶ BE Assertion. This bit field determines when BE signal is asserted during read cycles.

⁷ BE Negation. This bit field determines when BE signal is negated during read cycles.

4.6.7 DDR SDRAM Specific Parameters (DDR2/LVDDR2, LPDDR2, and DDR3)

The DDR2/LVDDR2 interface fully complies with JESD79-2E – DDR2 JEDEC release April, 2008, supporting DDR2-800 and LVDDR2-800.

The DDR3 interface fully complies with JESD79-3D – DDR3 JEDEC release April 2008 supporting DDR3-800.

The LPDDR2 interface fully complies with JESD209-2B, supporting LPDDR2-800.

Electrical Characteristics

Figure 28 and Table 41 show the address and control timing parameters for DDR2 and DDR3.

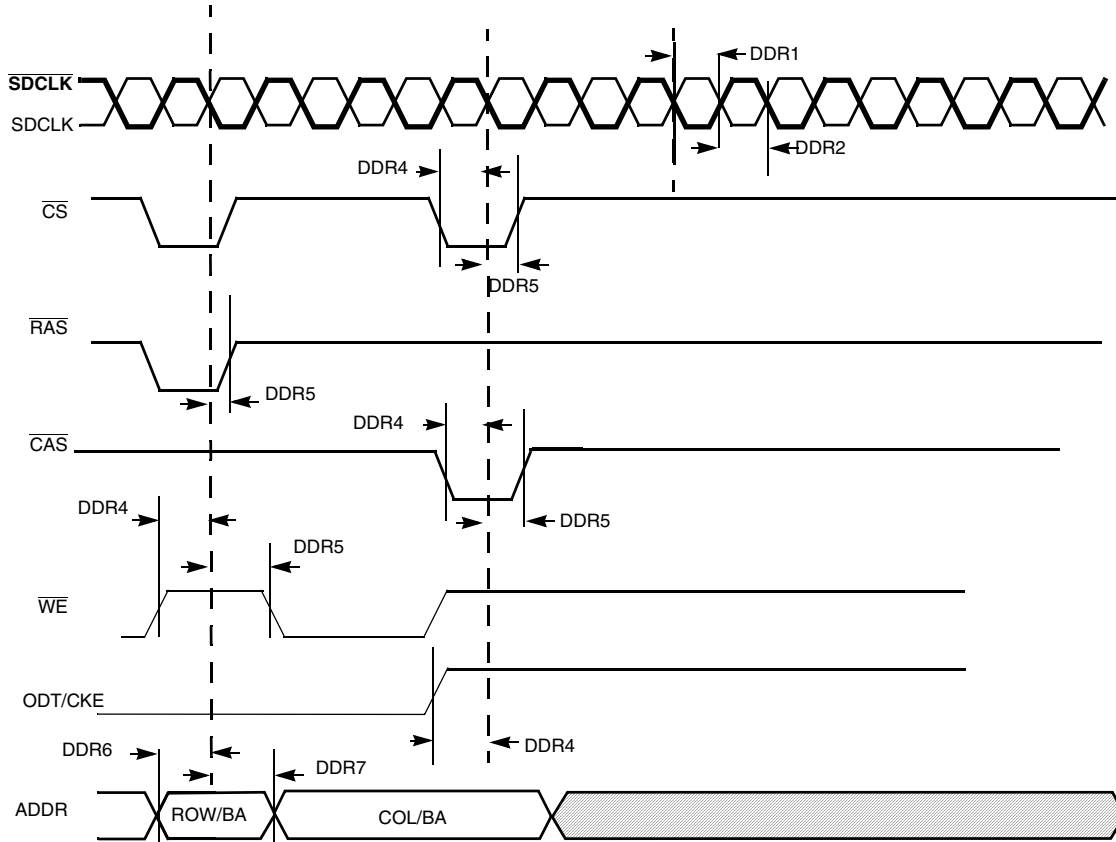


Figure 28. DDR SDRAM Address and Control Parameters for DDR2 and DDR3

Table 41. DDR SDRAM Timing Parameter Table^{1 2}

| ID | Parameter | Symbol | SDCLK = 400 MHz | | Units |
|------|---------------------------------------|--------|-----------------|------|-------|
| | | | Min | Max | |
| DDR1 | SDRAM clock high-level width | tCH | 0.48 | 0.52 | tck |
| DDR2 | SDRAM clock low-level width | tCL | 0.48 | 0.52 | tck |
| DDR4 | CS, RAS, CAS, CKE, WE, ODT setup time | tIS | 0.6 | — | ns |
| DDR5 | CS, RAS, CAS, CKE, WE, ODT hold time | tIH | 0.6 | — | ns |
| DDR6 | Address output setup time | tIS | 0.6 | — | ns |
| DDR7 | Address output hold time | tIH | 0.6 | — | ns |

¹ All timings are refer to Vref level cross point.

² Reference load model is 25 Ω resistor from each of the DDR outputs to VDD_REF.

Figure 29 and Table 42 show the address and control timing parameters for LPDDR2.

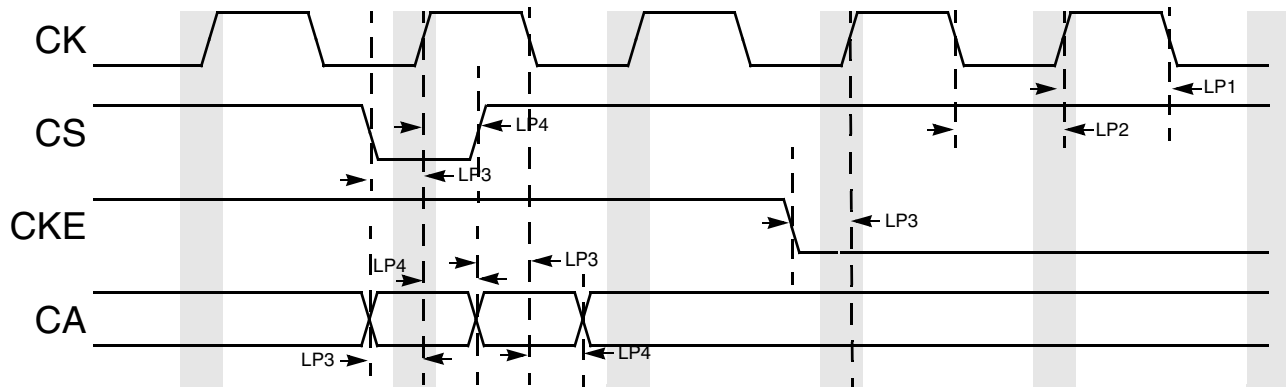


Figure 29. DDR SDRAM Address and Control Timing Parameters for LPDDR2

Table 42. DDR SDRAM Timing Parameter Table for LPDDR2^{1 2}

| ID | Parameter | Symbol | SDCLK = 400 MHz | | Units |
|-----|------------------------------|--------|-----------------|------|-------|
| | | | Min | Max | |
| LP1 | SDRAM clock high-level width | tCH | 0.45 | 0.55 | tCK |
| LP2 | SDRAM clock low-level width | tCL | 0.45 | 0.55 | tCK |
| LP3 | CS, CKE setup time | tIS | 0.3 | — | ns |
| LP4 | CS, CKE hold time | tIH | 0.3 | — | ns |
| LP3 | CA setup time | tIS | 0.3 | — | ns |
| LP4 | CA hold time | tIH | 0.3 | — | ns |

¹ All timings are refer to Vref level cross point.

² Reference load model is 25 Ω resistor from each of the DDR outputs to VDD_REF.

Figure 30 and Table 43 show the data write timing parameters.

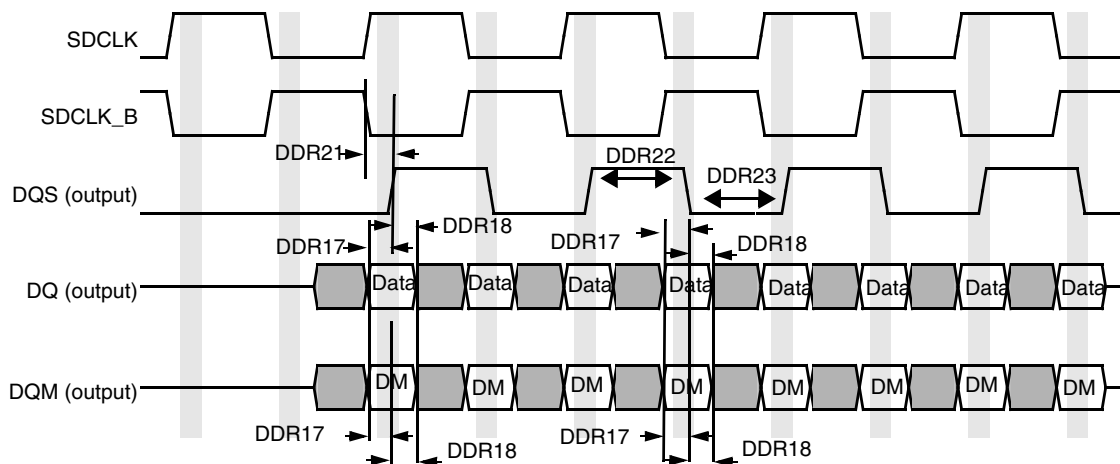


Figure 30. DDR SDRAM Data Write Cycle

Table 43. DDR SDRAM Write Cycle ^{1 2 3}

| ID | Parameter | Symbol | SDCLK = 400 MHz | | Unit |
|-------|---|-------------------|-----------------|-------|------|
| | | | Min | Max | |
| DDR17 | DQ and DQM setup time to DQS (differential strobe) | t _{DS} | 0.285 | — | ns |
| DDR18 | DQ and DQM hold time to DQS (differential strobe) | t _{DH} | 0.285 | — | ns |
| DDR21 | DQS latching rising transitions to associated clock edges | t _{DQSS} | -0.25 | +0.25 | tCK |
| DDR22 | DQS high level width | t _{DQSH} | 0.45 | 0.55 | tCK |
| DDR23 | DQS low level width | t _{DQSL} | 0.45 | 0.55 | tCK |

¹ All timings are refer to Vref level cross point.

² Reference load model is 25 Ω resistor from each of the DDR outputs to VDD_REF.

³ To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

Figure 31 and Table 44 show the data read timing parameters.

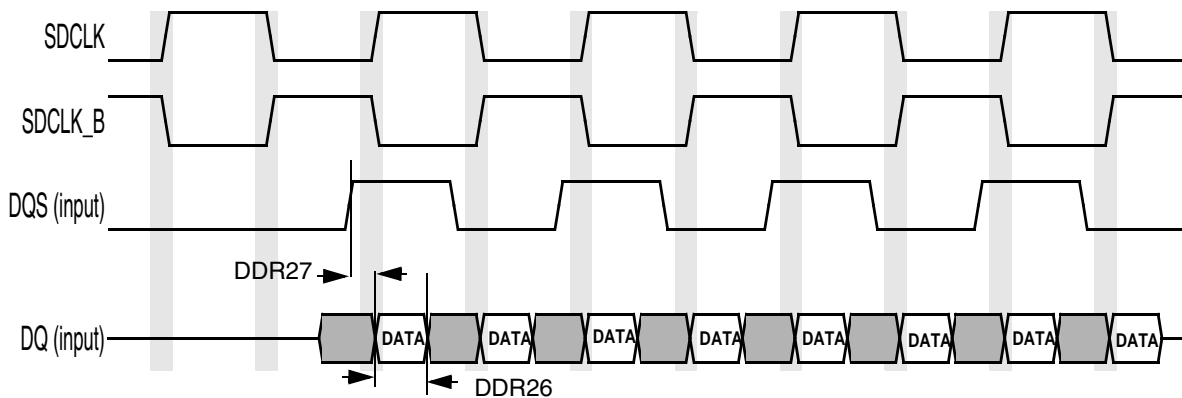


Figure 31. DDR SDRAM DQ vs. DQS and SDCLK Read Cycle

Table 44. DDR SDRAM Read Cycle ¹

| ID | Parameter | Symbol | SDCLK = 400 MHz | | Unit |
|----------------|---|--------|-----------------|-------|------|
| | | | Min | Max | |
| DDR26 | Minimum required DQ valid window width except from LPDDR2 | — | 0.6 | — | ns |
| DDR26(LP DDR2) | Minimum required DQ valid window width for LPDDR2 | — | 0.425 | — | ns |
| DDR27 | DQS to DQ valid data | — | 0.275 | 0.475 | ns |

¹ To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

4.7 External Peripheral Interfaces Parameters

The following subsections provide information on external peripheral interfaces.

4.7.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.7.2 CSPI and ECSPi Timing Parameters

This section describes the timing parameters of the CSPI and ECSPi blocks. The CSPI and ECSPi have separate timing parameters for master and slave modes. The nomenclature used with the CSPI / ECSPi modules and the respective routing of these signals is shown in [Table 45](#).

Table 45. CSPI Nomenclature and Routing

| Block Instance | I/O Access |
|----------------|---|
| ECSPi-1 | GPIO, KPP, DISP0_DAT, CSI0_DAT and EIM_D through IOMUXC |
| ECSPi-2 | DISP0_DAT, CSI0_DAT and EIM through IOMUXC |
| CSPI | DISP0_DAT, EIM_A/D, SD1 and SD2 through IOMUXC |

4.7.2.1 CSPI Master Mode Timing

[Figure 32](#) depicts the timing of CSPI in master mode. [Table 46](#) lists the CSPI master mode timing characteristics.

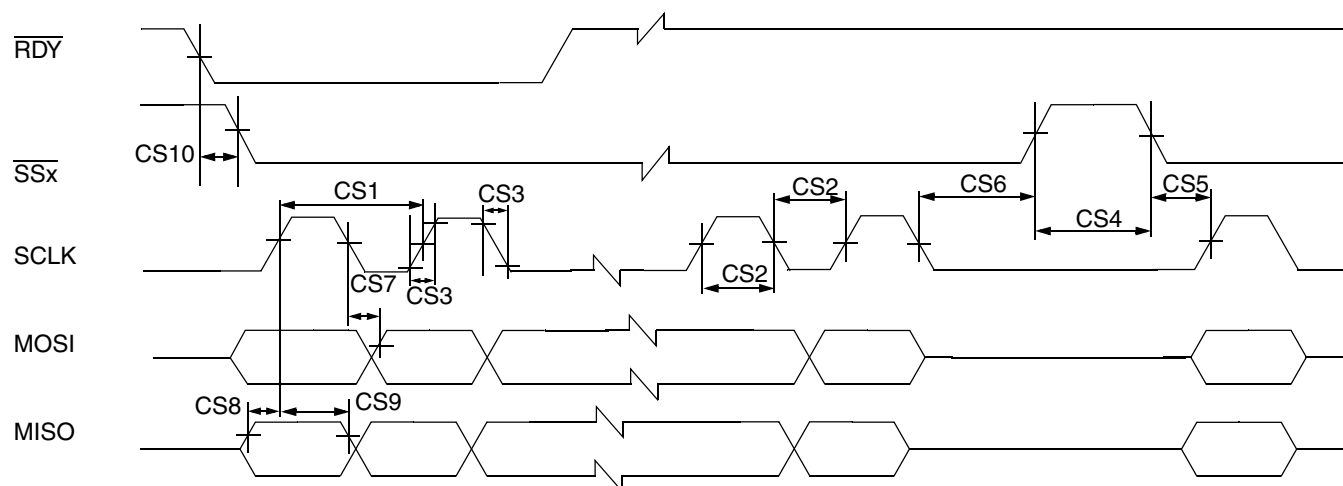


Figure 32. CSPI/ECSPi Master Mode Timing Diagram

Table 46. CSPI Master Mode Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|------|--|-----------------|-----|-----|------|
| CS1 | SCLK Cycle Time | t_{clk} | 60 | — | ns |
| CS2 | SCLK High or Low Time | t_{sw} | 26 | — | ns |
| CS3 | SCLK Rise or Fall ¹ | $t_{RISE/FALL}$ | — | — | ns |
| CS4 | SSx pulse width | t_{CSLH} | 26 | — | ns |
| CS5 | SSx Lead Time (Slave Select setup time) | t_{SCS} | 26 | — | ns |
| CS6 | SSx Lag Time (SS hold time) | t_{HCS} | 26 | — | ns |
| CS7 | MOSI Propagation Delay ($C_{LOAD} = 20\text{ pF}$) | t_{pDmosi} | -1 | 21 | ns |
| CS8 | MISO Setup Time | t_{Smiso} | 5 | — | ns |
| CS9 | MISO Hold Time | t_{Hmiso} | 5 | — | ns |
| CS10 | RDY to SSx Time ² | t_{SDRY} | 5 | — | ns |

¹ See specific I/O AC parameters [Section 4.5, "I/O AC Parameters"](#)

² SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.2.2 CSPI Slave Mode Timing

Figure 33 depicts the timing of CSPI in slave mode. Timing characteristics were not available at the time of publication.

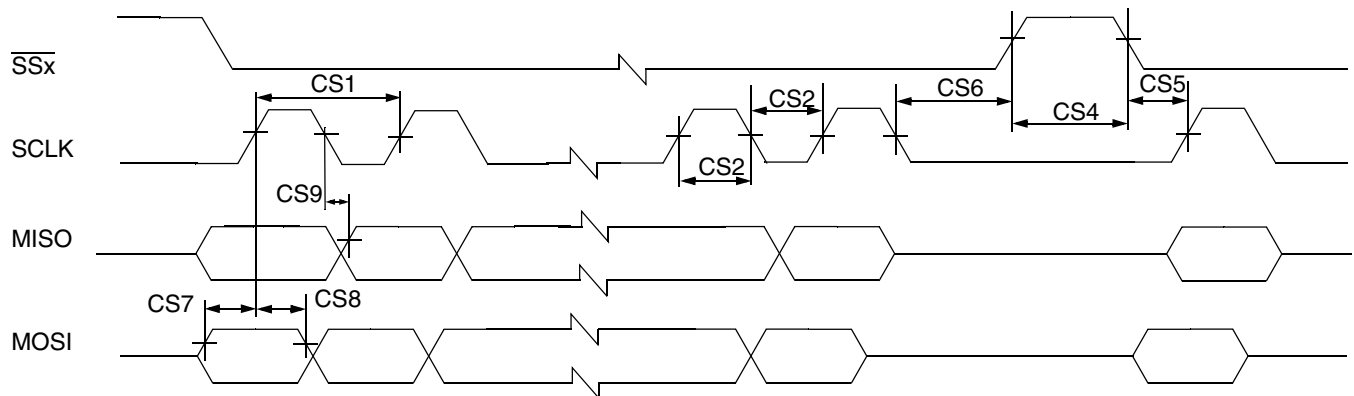


Figure 33. CSPI/ECSPI Slave Mode Timing Diagram

4.7.2.3 ECSPi Master Mode Timing

Figure 32 depicts the timing of ECSPi in master mode. Table 47 lists the ECSPi master mode timing characteristics.

Table 47. ECSPi Master Mode Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|------|---|-----------------|------------------|-----|------|
| CS1 | SCLK Cycle Time—Read SCLK Cycle Time—Write | t_{clk} | 30 15 | — | ns |
| CS2 | SCLK High or Low Time—Read SCLK High or Low Time—Write | t_{sw} | 14 7 | — | ns |
| CS3 | SCLK Rise or Fall ¹ | $t_{RISE/FALL}$ | — | — | ns |
| CS4 | SSx pulse width | t_{CSLH} | Half SCLK period | — | ns |
| CS5 | SSx Lead Time (CS setup time) | t_{SCS} | 5 | — | ns |
| CS6 | SSx Lag Time (CS hold time) | t_{HCS} | 5 | — | ns |
| CS7 | MOSI Propagation Delay ($C_{LOAD} = 20$ pF) | t_{PDmosi} | -0.5 | 2.5 | ns |
| CS8 | MISO Setup Time | t_{Smiso} | 8.5 | — | ns |
| CS9 | MISO Hold Time | t_{Hmiso} | 0 | — | ns |
| CS10 | RDY to SSx Time ² | t_{SDRY} | 5 | — | ns |

¹ See specific I/O AC parameters Section 4.5, “I/O AC Parameters”

² SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.2.4 ECSPi Slave Mode Timing

Figure 33 depicts the timing of ECSPi in slave mode. Table 48 lists the ECSPi slave mode timing characteristics.

Table 48. ECSPi Slave Mode Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---|--------------|------------------|-----|------|
| CS1 | SCLK Cycle Time—Read SCLK Cycle Time—Write | t_{clk} | 15 40 | — | ns |
| CS2 | SCLK High or Low Time—Read SCLK High or Low Time—Write | t_{sw} | 7 20 | — | ns |
| CS4 | SSx pulse width | t_{CSLH} | Half SCLK period | — | ns |
| CS5 | SSx Lead Time (CS setup time) | t_{SCS} | 5 | — | ns |
| CS6 | SSx Lag Time (CS hold time) | t_{HCS} | 5 | — | ns |
| CS7 | MOSI Setup Time | t_{Smosi} | 4 | — | ns |
| CS8 | MOSI Hold Time | t_{Hmosi} | 4 | — | ns |
| CS9 | MISO Propagation Delay ($C_{LOAD} = 20$ pF) | t_{PDmiso} | 4 | 17 | ns |

4.7.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 49 shows the interface timing values. The number field in the table refers to timing signals found in Figure 34 and Figure 35.

Table 49. Enhanced Serial Audio Interface (ESAI) Timing

| No. | Characteristics ^{1,2,3} | Symbol | Expression ³ | Min | Max | Condition ⁴ | Unit |
|-----|---|-------------|--|--------------|--------------|------------------------|------|
| 62 | Clock cycle ⁵ | t_{SSICC} | $4 \times T_C$ $4 \times T_C$ | 30.0 30.0 | — — | i ck i ck | ns |
| 63 | Clock high period • For internal clock • For external clock | — — | $2 \times T_C - 9.0$ $2 \times T_C$ | 6 15 | — — | — — | ns |
| 64 | Clock low period • For internal clock • For external clock | — — | $2 \times T_C - 9.0$ $2 \times T_C$ | 6 15 | — — | — — | ns |
| 65 | SCKR rising edge to FSR out (bl) high | — — | — — | — — | 17.0 7.0 | x ck i ck a | ns |
| 66 | SCKR rising edge to FSR out (bl) low | — — | — — | — — | 17.0 7.0 | x ck i ck a | ns |
| 67 | SCKR rising edge to FSR out (wr) high ⁶ | — — | — — | — — | 19.0 9.0 | x ck i ck a | ns |
| 68 | SCKR rising edge to FSR out (wr) low ⁶ | — — | — — | — — | 19.0 9.0 | x ck i ck a | ns |
| 69 | SCKR rising edge to FSR out (wl) high | — — | — — | — — | 16.0 6.0 | x ck i ck a | ns |
| 70 | SCKR rising edge to FSR out (wl) low | — — | — — | — — | 17.0 7.0 | x ck i ck a | ns |
| 71 | Data in setup time before SCKR (SCK in synchronous mode) falling edge | — — | — — | 12.0 19.0 | — — | x ck i ck | ns |
| 72 | Data in hold time after SCKR falling edge | — — | — — | 3.5 9.0 | — — | x ck i ck | ns |
| 73 | FSR input (bl, wr) high before SCKR falling edge ⁶ | — — | — — | 2.0 12.0 | — — | x ck i ck a | ns |
| 74 | FSR input (wl) high before SCKR falling edge | — — | — — | 2.0 12.0 | — — | x ck i ck a | ns |
| 75 | FSR input hold time after SCKR falling edge | — — | — — | 2.5 8.5 | — — | x ck i ck a | ns |
| 78 | SCKT rising edge to FST out (bl) high | — — | — — | — — | 18.0 8.0 | x ck i ck | ns |
| 79 | SCKT rising edge to FST out (bl) low | — — | — — | — — | 20.0 10.0 | x ck i ck | ns |

Table 49. Enhanced Serial Audio Interface (ESAI) Timing (continued)

| No. | Characteristics ^{1,2,3} | Symbol | Expression ³ | Min | Max | Condition ⁴ | Unit |
|-----|---|--------|-------------------------|-------------|--------------|------------------------|------|
| 80 | SCKT rising edge to FST out (wr) high ⁶ | — — | — — | — — | 20.0 10.0 | x ck i ck | ns |
| 81 | SCKT rising edge to FST out (wr) low ⁶ | — — | — — | — — | 22.0 12.0 | x ck i ck | ns |
| 82 | SCKT rising edge to FST out (wl) high | — — | — — | — — | 19.0 9.0 | x ck i ck | ns |
| 83 | SCKT rising edge to FST out (wl) low | — — | — — | — — | 20.0 10.0 | x ck i ck | ns |
| 84 | SCKT rising edge to data out enable from high impedance | — — | — — | — — | 22.0 17.0 | x ck i ck | ns |
| 86 | SCKT rising edge to data out valid | — — | — — | — — | 18.0 13.0 | x ck i ck | ns |
| 87 | SCKT rising edge to data out high impedance ⁷⁷ | — — | — — | — — | 21.0 16.0 | x ck i ck | ns |
| 89 | FST input (bl, wr) setup time before SCKT falling edge ⁶ | — — | — — | 2.0 18.0 | — — | x ck i ck | ns |
| 90 | FST input (wl) setup time before SCKT falling edge | — — | — — | 2.0 18.0 | — — | x ck i ck | ns |
| 91 | FST input hold time after SCKT falling edge | — — | — — | 4.0 5.0 | — — | x ck i ck | ns |
| 95 | HCKR/HCKT clock cycle | — | $2 \times T_C$ | 15 | — | — | ns |
| 96 | HCKT input rising edge to SCKT output | — | — | — | 18.0 | — | ns |
| 97 | HCKR input rising edge to SCKR output | — | — | — | 18.0 | — | ns |

¹ V_{CORE_VDD} = 1.00 ± 0.10V
T_j = -40 °C to 125 °C
C_L = 50 pF

² i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

³ bl = bit length
wl = word length
wr = word length relative

⁴ SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

⁵ For the internal clock, the external clock cycle is defined by l_{cyc} and the ESAI control register.

Electrical Characteristics

- ⁶ The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.
- ⁷ Periodically sampled and not 100% tested.

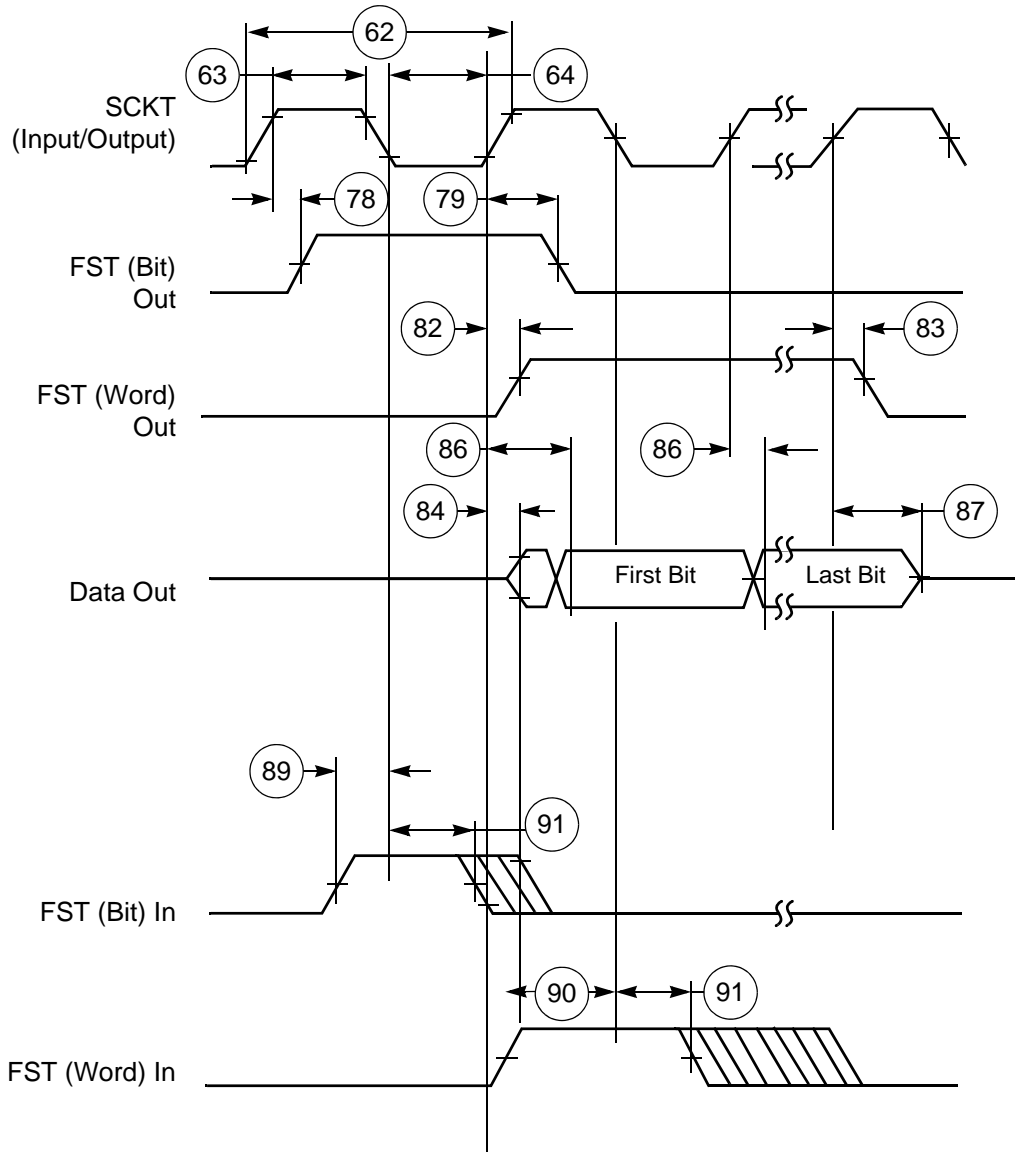


Figure 34. ESAI Transmitter Timing

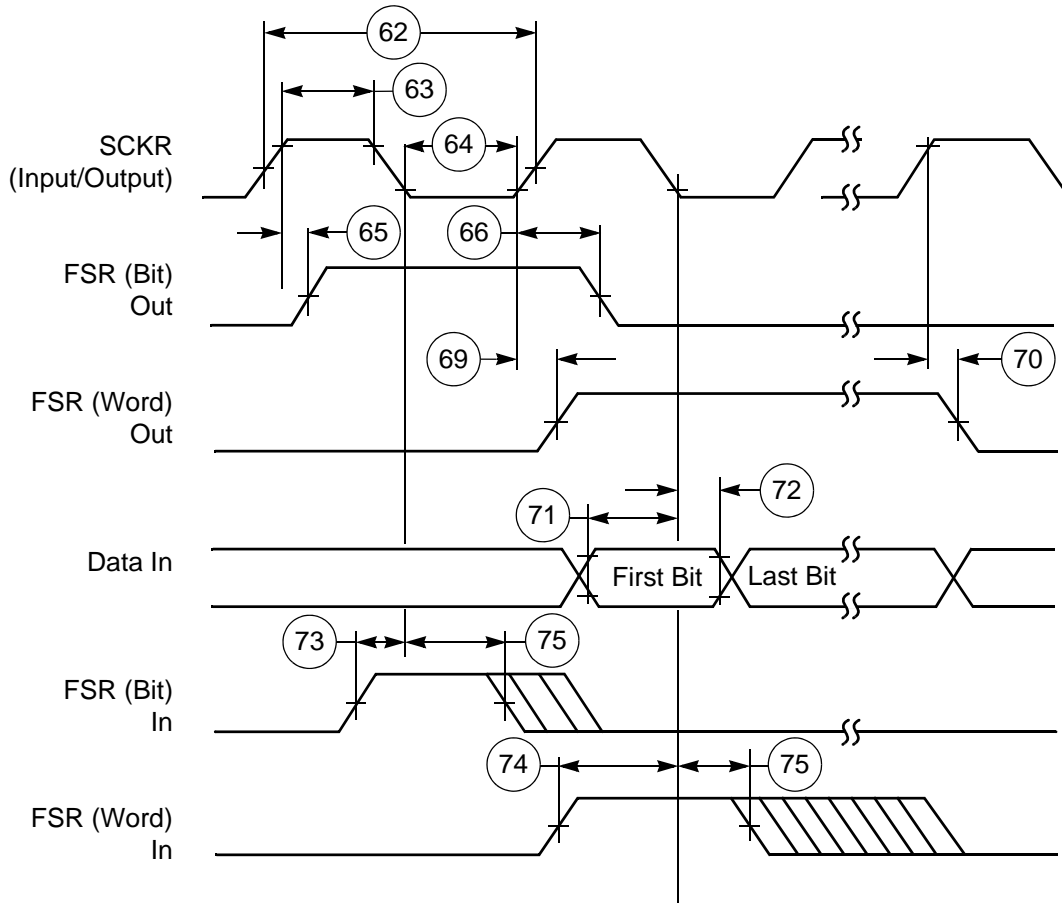


Figure 35. ESAI Receiver Timing

4.7.4 Enhanced Secured Digital Host Controller(eSDHCv2/v3) AC timing

This section describes the electrical information of the eSDHCv2/v3, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Data Rate) timing.

4.7.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 36 depicts the timing of SD/eMMC4.3, and Table 50 lists the SD/eMMC4.3 timing characteristics.

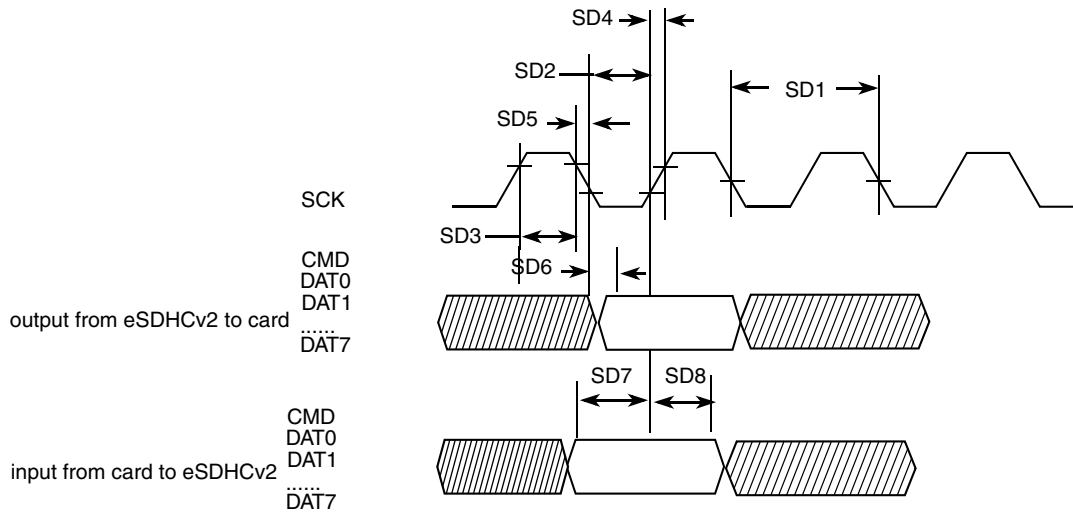


Figure 36. SD/eMMC4.3 Timing

Table 50. SD/eMMC4.3 Interface Timing Specification

| ID | Parameter | Symbols | Min | Max | Unit |
|---|---|------------|------|-------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | f_{PP}^1 | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed/High Speed) | f_{PP}^2 | 0 | 25/50 | MHz |
| | Clock Frequency (MMC Full Speed/High Speed) | f_{PP}^3 | 0 | 20/52 | MHz |
| | Clock Frequency (Identification Mode) | f_{OD} | 100 | 400 | kHz |
| SD2 | Clock Low Time | t_{WL} | 7 | — | ns |
| SD3 | Clock High Time | t_{WH} | 7 | — | ns |
| SD4 | Clock Rise Time | t_{TLH} | — | 3 | ns |
| SD5 | Clock Fall Time | t_{THL} | — | 3 | ns |
| eSDHC Output/Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| SD6 | eSDHCv2 Output Delay (port 1, 2, and 4) | t_{OD} | -3.5 | 3.5 | ns |
| | eSDHCv3 Output Delay (port 3) | t_{OD} | -4.5 | 4.5 | ns |

Table 50. SD/eMMC4.3 Interface Timing Specification (continued)

| ID | Parameter | Symbols | Min | Max | Unit |
|---|------------------------------------|-----------|-----|-----|------|
| eSDHC Input/Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD7 | eSDHC Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD8 | eSDHC Input Hold Time ⁴ | t_{IH} | 2.5 | — | ns |

¹ In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

² In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

³ In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

⁴To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.7.4.2 eMMC4.4 (Dual Data Rate) eSDHCv3 AC Timing

Figure 37 depicts the timing of eMMC4.4. Table 51 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

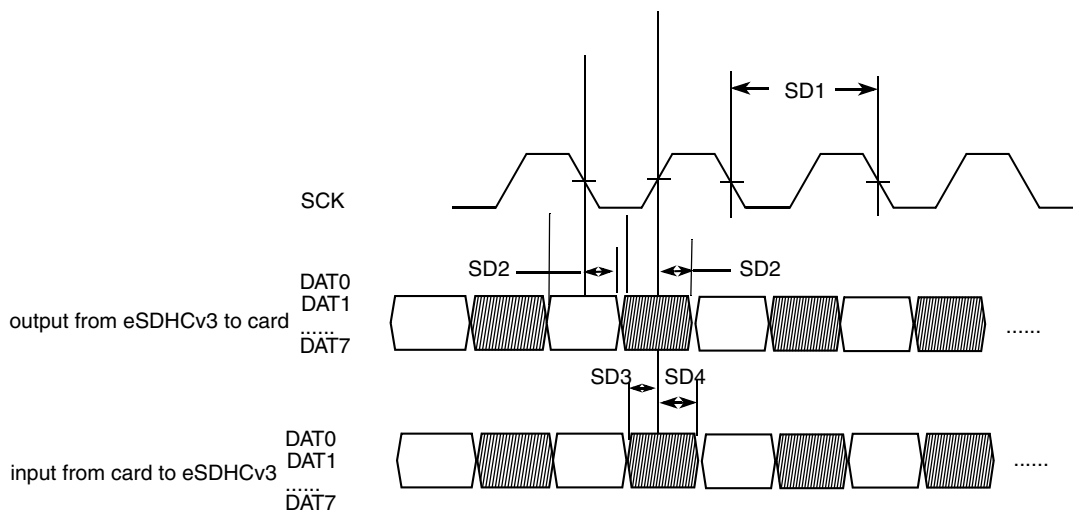


Figure 37. eMMC4.4 Timing

Table 51. eMMC4.4 Interface Timing Specification

| ID | Parameter | Symbols | Min | Max | Unit |
|---|---|----------|------|-----|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (MMC Full Speed/High Speed) | f_{PP} | 0 | 52 | MHz |
| eSDHC Output / Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| SD2 | eSDHC Output Delay | t_{OD} | -4.5 | 4.5 | ns |

Table 51. eMMC4.4 Interface Timing Specification (continued)

| ID | Parameter | Symbols | Min | Max | Unit |
|--|------------------------|-----------|-----|-----|------|
| eSDHC Input / Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD3 | eSDHC Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD4 | eSDHC Input Hold Time | t_{IH} | 2.5 | — | ns |

4.7.5 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII (18 pins in total) and the 10 Mbps (only 7-wire interface, which uses 7 of the MII pins), for connection to an external Ethernet transceiver. For the pin list of MII and 7-wire, see the i.MX53 Reference Manual.

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.7.5.1 MII Receive Signal Timing

The MII receive signal timing involves the FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK signals. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement but the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 52 lists the MII receive channel signal timing parameters and Figure 38 shows MII receive signal timings.

Table 52. MII Receive Signal Timing

| No. | Characteristics ^{1 2} | Min | Max | Unit |
|-----|--|-----|-----|-------------------|
| M1 | FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup | 5 | — | ns |
| M2 | FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold | 5 | — | ns |
| M3 | FEC_RX_CLK pulse width high | 35% | 65% | FEC_RX_CLK period |
| M4 | FEC_RX_CLK pulse width low | 35% | 65% | FEC_RX_CLK period |

¹ FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have same timing in 10 Mbps 7-wire interface mode.

² Test conditions: 25pF on each output signal.

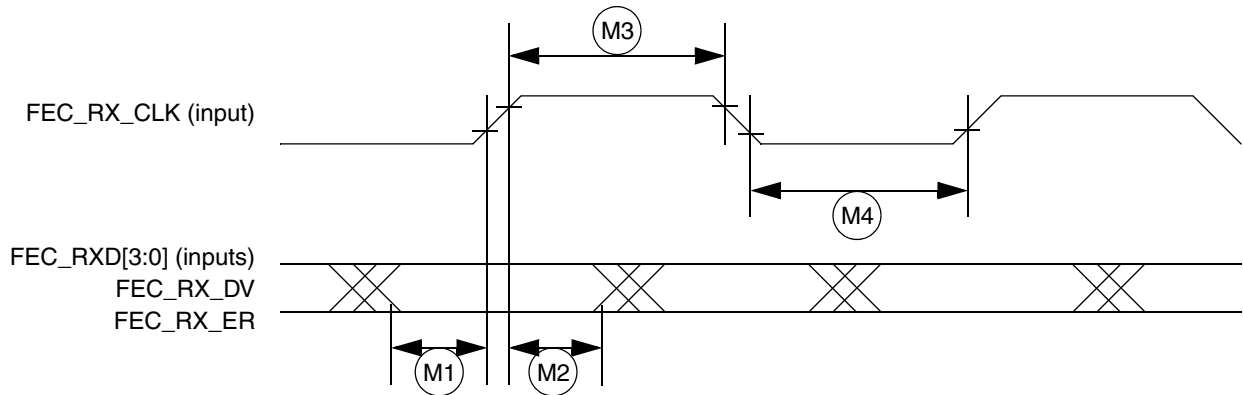


Figure 38. MII Receive Signal Timing Diagram

4.7.5.2 MII Transmit Signal Timing

The MII transmit signal timing affects the FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK signals. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Table 53 lists MII transmit channel timing parameters. Figure 39 shows MII transmit signal timing diagram for the values listed in Table 53.

Table 53. MII Transmit Signal Timing

| Num | Characteristic ^{1 2} | Min | Max | Unit |
|-----|--|-----|-----|-------------------|
| M5 | FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid | 5 | — | ns |
| M6 | FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid | — | 20 | ns |
| M7 | FEC_TX_CLK pulse width high | 35% | 65% | FEC_TX_CLK period |
| M8 | FEC_TX_CLK pulse width low | 35% | 65% | FEC_TX_CLK period |

¹ FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

² Test conditions: 25pF on each output signal.

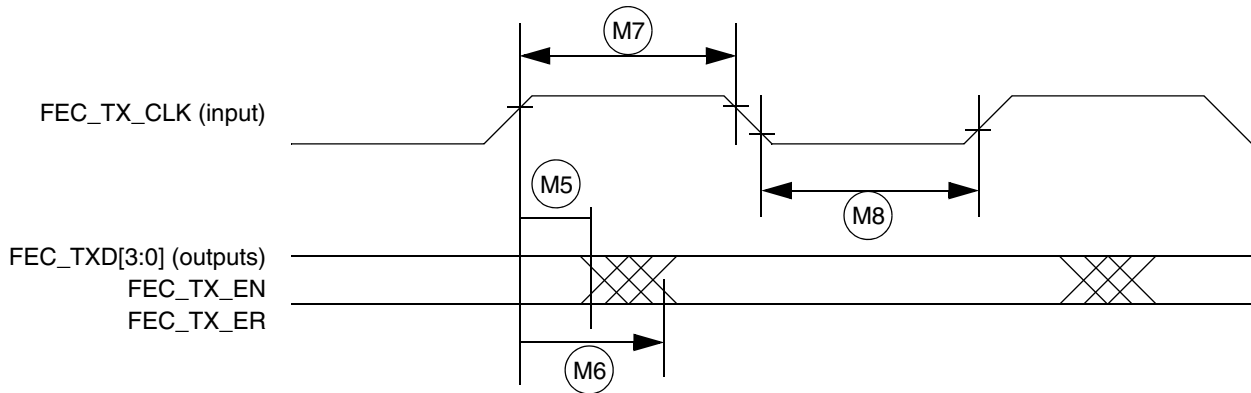


Figure 39. MII Transmit Signal Timing Diagram

4.7.5.3 MII Async Inputs Signal Timing (FEC_CRIS and FEC_COL)

Table 54 lists MII asynchronous inputs signal timing information. Figure 40 shows MII asynchronous input timings listed in Table 54.

Table 54. MII Async Inputs Signal Timing

| Num | Characteristic ¹ | Min | Max | Unit |
|-----------------|---|-----|-----|-------------------|
| M9 ² | FEC_CRIS to FEC_COL minimum pulse width | 1.5 | — | FEC_TX_CLK period |

¹ Test conditions: 25pF on each output signal.

² FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

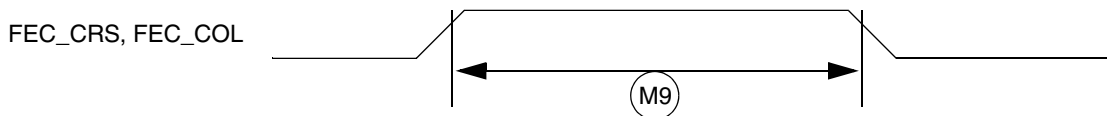


Figure 40. MII Async Inputs Timing Diagram

4.7.5.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 55 lists MII serial management channel timings. Figure 41 shows MII serial management channel timings listed in Table 55. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However, the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 55. MII Transmit Signal Timing

| ID | Characteristics ¹ | Min | Max | Unit |
|-----|---|-----|-----|------|
| M10 | FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay) | — | 5 | ns |
| M12 | FEC_MDIO (input) to FEC_MDC rising edge setup | 18 | — | ns |

Table 55. MII Transmit Signal Timing (continued)

| ID | Characteristics ¹ | Min | Max | Unit |
|-----|--|------|-----|----------------|
| M13 | FEC_MDIO (input) to FEC_MDC rising edge hold | 0 | — | ns |
| M14 | FEC_MDC pulse width high | 40 % | 60% | FEC_MDC period |
| M15 | FEC_MDC pulse width low | 40 % | 60% | FEC_MDC period |

¹ Test conditions: 25pF on each output signal.

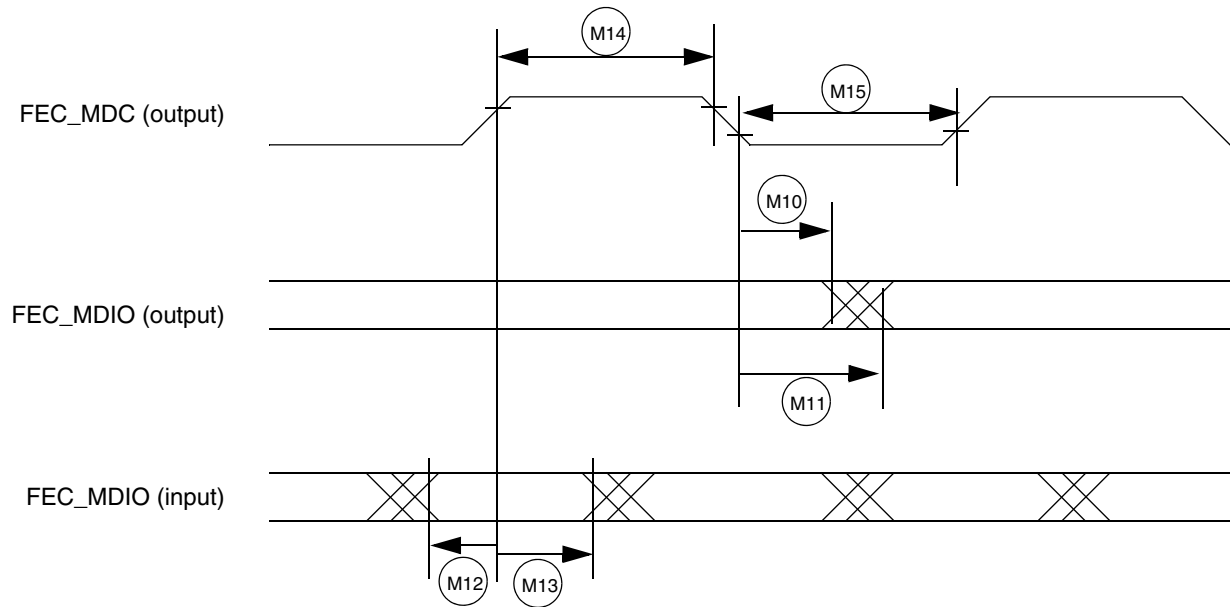


Figure 41. MII Serial Management Channel Timing Diagram

4.7.5.5 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz \pm 50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and optional FEC_RX_ER.

The RMII mode timings are shown in [Table 56](#) and [Figure 42](#).

Table 56. RMII Signal Timing

| No. | Characteristics ¹ | Min | Max | Unit |
|-----|--|-----|-----|----------------|
| M16 | REF_CLK(FEC_TX_CLK) pulse width high | 35% | 65% | REF_CLK period |
| M17 | REF_CLK(FEC_TX_CLK) pulse width low | 35% | 65% | REF_CLK period |
| M18 | REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid | 2 | — | ns |
| M19 | REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid | — | 16 | ns |

Table 56. RMII Signal Timing (continued)

| No. | Characteristics ¹ | Min | Max | Unit |
|-----|---|-----|-----|------|
| M20 | FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup | 4 | — | ns |
| M21 | REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold | 2 | — | ns |

¹ Test conditions: 25pF on each output signal.

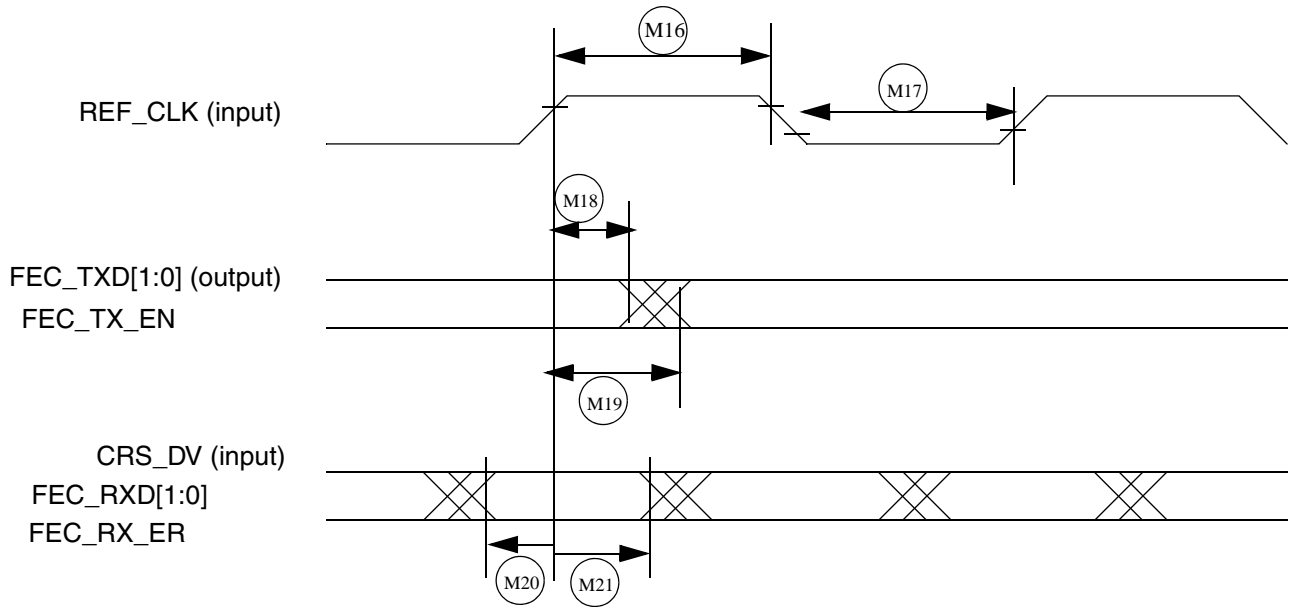


Figure 42. RMII Mode Signal Timing Diagram

4.7.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver external to i.MX53xD such as MC33902 from Freescale. The i.MX53xD has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the i.MX53 Reference Manual to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

4.7.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 43 depicts the timing of I²C module, and Table 57 lists the I²C module timing characteristics.

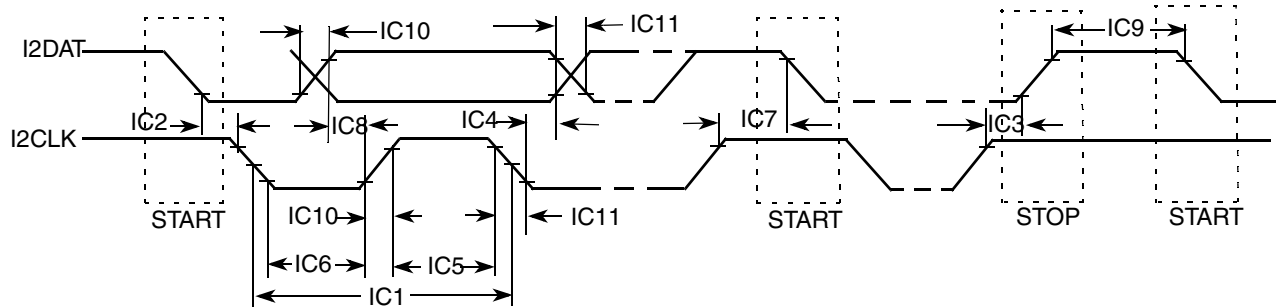


Figure 43. I²C Bus Timing

Table 57. I²C Module Timing Parameters

| ID | Parameter | Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V | | Fast Mode Supply Voltage = 2.7 V–3.3 V | | Unit |
|------|---|---|-------------------|--|------------------|------|
| | | Min | Max | Min | Max | |
| IC1 | I2CLK cycle time | 10 | — | 2.5 | — | μs |
| IC2 | Hold time (repeated) START condition | 4.0 | — | 0.6 | — | μs |
| IC3 | Set-up time for STOP condition | 4.0 | — | 0.6 | — | μs |
| IC4 | Data hold time | 0 ¹ | 3.45 ² | 0 ¹ | 0.9 ² | μs |
| IC5 | HIGH Period of I2CLK Clock | 4.0 | — | 0.6 | — | μs |
| IC6 | LOW Period of the I2CLK Clock | 4.7 | — | 1.3 | — | μs |
| IC7 | Set-up time for a repeated START condition | 4.7 | — | 0.6 | — | μs |
| IC8 | Data set-up time | 250 | — | 100 ³ | — | ns |
| IC9 | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | μs |
| IC10 | Rise time of both I2DAT and I2CLK signals | — | 1000 | 20 + 0.1C _b ⁴ | 300 | ns |
| IC11 | Fall time of both I2DAT and I2CLK signals | — | 300 | 20 + 0.1C _b ⁴ | 300 | ns |
| IC12 | Capacitive load for each bus line (C _b) | — | 400 | — | 400 | pF |

¹ A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

² The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

³ A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line $\text{max_rise_time (IC9)} + \text{data_setup_time (IC7)} = 1000 + 250 = 1250$ ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

⁴ C_b = total capacitance of one bus line in pF.

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.7.8.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. [Table 58](#) defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 58. Camera Input Signal Cross Reference, Format and Bits per Cycle

| Signal Name ¹ | RGB565 8 bits 2 cycles | RGB565 ² 8 bits 3 cycles | RGB666 ³ 8 bits 3 cycles | RGB888 8 bits 3 cycles | YCbCr 8 bits 2 cycles | RGB565 ⁴ 16 bits 2 cycles | YCbCr ⁵ 16 bits 1 cycle | YCbCr ⁶ 16 bits 1 cycle | YCbCr ⁷ 20 bits 1 cycle |
|--------------------------|------------------------------|---|---|------------------------------|-----------------------------|--|--|--|--|
| CSIx_DAT0 | — | — | — | — | — | — | — | 0 | C[0] |
| CSIx_DAT1 | — | — | — | — | — | — | — | 0 | C[1] |
| CSIx_DAT2 | — | — | — | — | — | — | — | C[0] | C[2] |
| CSIx_DAT3 | — | — | — | — | — | — | — | C[1] | C[3] |
| CSIx_DAT4 | — | — | — | — | — | B[0] | C[0] | C[2] | C[4] |
| CSIx_DAT5 | — | — | — | — | — | B[1] | C[1] | C[3] | C[5] |
| CSIx_DAT6 | — | — | — | — | — | B[2] | C[2] | C[4] | C[6] |
| CSIx_DAT7 | — | — | — | — | — | B[3] | C[3] | C[5] | C[7] |
| CSIx_DAT8 | — | — | — | — | — | B[4] | C[4] | C[6] | C[8] |
| CSIx_DAT9 | — | — | — | — | — | G[0] | C[5] | C[7] | C[9] |
| CSIx_DAT10 | — | — | — | — | — | G[1] | C[6] | 0 | Y[0] |
| CSIx_DAT11 | — | — | — | — | — | G[2] | C[7] | 0 | Y[1] |
| CSIx_DAT12 | B[0], G[3] | R[2],G[4],B[2] | R/G/B[4] | R/G/B[0] | Y/C[0] | G[3] | Y[0] | Y[0] | Y[2] |
| CSIx_DAT13 | B[1], G[4] | R[3],G[5],B[3] | R/G/B[5] | R/G/B[1] | Y/C[1] | G[4] | Y[1] | Y[1] | Y[3] |
| CSIx_DAT14 | B[2], G[5] | R[4],G[0],B[4] | R/G/B[0] | R/G/B[2] | Y/C[2] | G[5] | Y[2] | Y[2] | Y[4] |
| CSIx_DAT15 | B[3], R[0] | R[0],G[1],B[0] | R/G/B[1] | R/G/B[3] | Y/C[3] | R[0] | Y[3] | Y[3] | Y[5] |
| CSIx_DAT16 | B[4], R[1] | R[1],G[2],B[1] | R/G/B[2] | R/G/B[4] | Y/C[4] | R[1] | Y[4] | Y[4] | Y[6] |
| CSIx_DAT17 | G[0], R[2] | R[2],G[3],B[2] | R/G/B[3] | R/G/B[5] | Y/C[5] | R[2] | Y[5] | Y[5] | Y[7] |
| CSIx_DAT18 | G[1], R[3] | R[3],G[4],B[3] | R/G/B[4] | R/G/B[6] | Y/C[6] | R[3] | Y[6] | Y[6] | Y[8] |
| CSIx_DAT19 | G[2], R[4] | R[4],G[5],B[4] | R/G/B[5] | R/G/B[7] | Y/C[7] | R[4] | Y[7] | Y[7] | Y[9] |

¹ CSIx stands for CSI1 or CSI2

- ² The MSB bits are duplicated on LSB bits implementing color extension
- ³ The two MSB bits are duplicated on LSB bits implementing color extension
- ⁴ RGB 16 bits— Supported in two ways: (1) As a “generic data” input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
- ⁵ YCbCr 16 bits— Supported as a “generic-data” input, with no on-the-fly processing.
- ⁶ YCbCr 16 bits— Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
- ⁷ YCbCr, 20 bits— Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.7.8.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.7.8.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.7.8.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See [Figure 44](#).

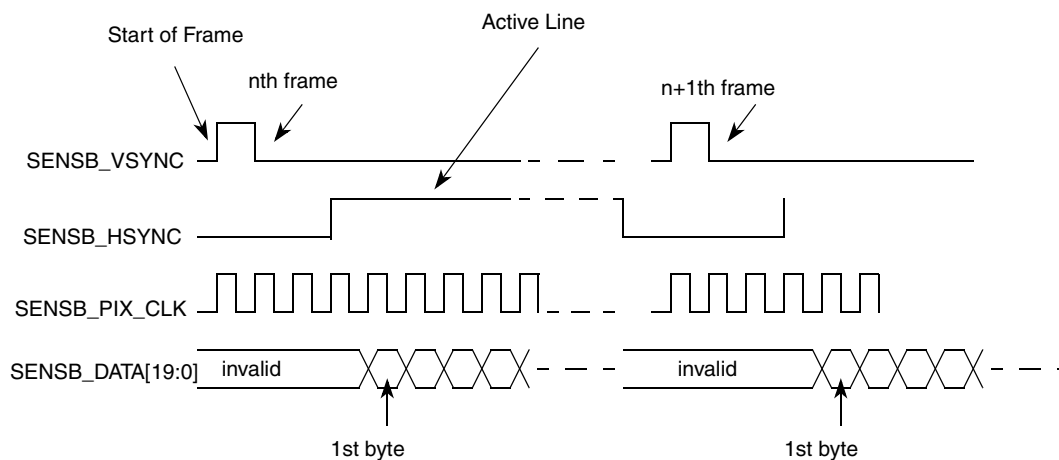


Figure 44. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks.

Electrical Characteristics

SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.7.8.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in [Section 4.7.8.2.2, “Gated Clock Mode,”](#)) except for the SENSB_HSYNC signal, which is not used (see [Figure 45](#)). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

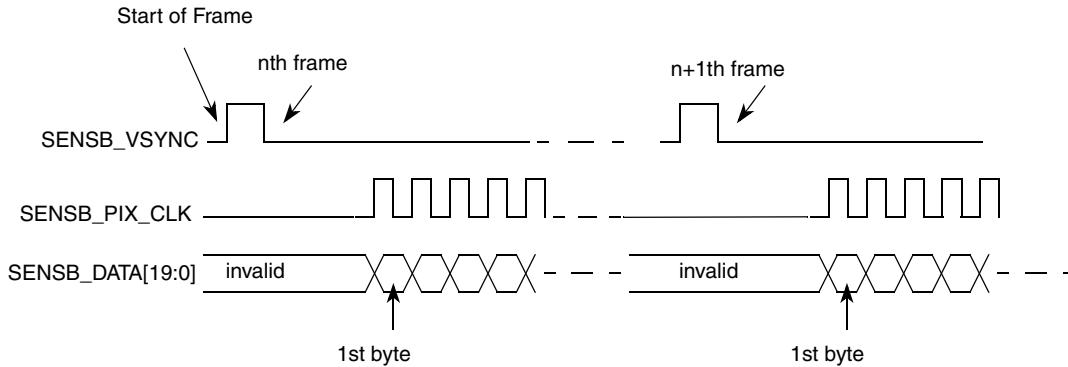


Figure 45. Non-Gated Clock Mode Timing Diagram

The timing described in [Figure 45](#) is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.7.8.3 Electrical Characteristics

[Figure 46](#) depicts the sensor interface timing. SENSB_MCLK signal described here is not generated by the IPU. [Table 59](#) lists the sensor interface timing characteristics.

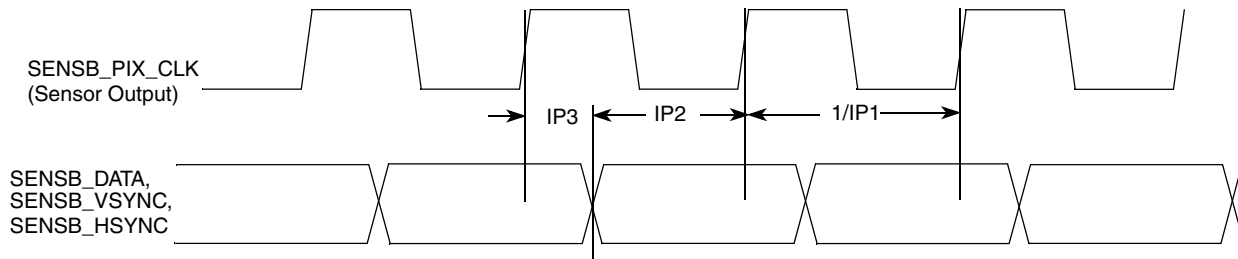


Figure 46. Sensor Interface Timing Diagram

Table 59. Sensor Interface Timing Characteristics

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---------------------------------------|--------|------|-----|------|
| IP1 | Sensor output (pixel) clock frequency | Fpck | 0.01 | 180 | MHz |
| IP2 | Data and control setup time | Tsu | 2 | — | ns |
| IP3 | Data and control holdup time | Thd | 1 | — | ns |

4.7.8.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. [Table 60](#) defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 60. Video Signal Cross-Reference

| i.MX53xD | LCD | | | | | | | | Comment ¹ |
|-----------------------|-------------------------------------|------------------------------------|---------------|---------------|-----------------------------|-----------------|-----------------|----------------|--|
| Port Name (x=0, 1) | RGB, Signal Name (General) | RGB/TV Signal Allocation (Example) | | | | | | Smart | |
| | | 16-bit RGB | 18-bit RGB | 24 Bit RGB | 8-bit YCrCb ² | 16-bit YCrCb | 20-bit YCrCb | Signal Name | |
| DISPx_DAT0 | DAT[0] | B[0] | B[0] | B[0] | Y/C[0] | C[0] | C[0] | DAT[0] | The restrictions are as follows: a) There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. b) The bit order is expressed in each of the bit groups, for example B[0] = least significant blue pixel bit |
| DISPx_DAT1 | DAT[1] | B[1] | B[1] | B[1] | Y/C[1] | C[1] | C[1] | DAT[1] | |
| DISPx_DAT2 | DAT[2] | B[2] | B[2] | B[2] | Y/C[2] | C[2] | C[2] | DAT[2] | |
| DISPx_DAT3 | DAT[3] | B[3] | B[3] | B[3] | Y/C[3] | C[3] | C[3] | DAT[3] | |
| DISPx_DAT4 | DAT[4] | B[4] | B[4] | B[4] | Y/C[4] | C[4] | C[4] | DAT[4] | |
| DISPx_DAT5 | DAT[5] | G[0] | B[5] | B[5] | Y/C[5] | C[5] | C[5] | DAT[5] | |
| DISPx_DAT6 | DAT[6] | G[1] | G[0] | B[6] | Y/C[6] | C[6] | C[6] | DAT[6] | |
| DISPx_DAT7 | DAT[7] | G[2] | G[1] | B[7] | Y/C[7] | C[7] | C[7] | DAT[7] | |
| DISPx_DAT8 | DAT[8] | G[3] | G[2] | G[0] | — | Y[0] | C[8] | DAT[8] | |
| DISPx_DAT9 | DAT[9] | G[4] | G[3] | G[1] | — | Y[1] | C[9] | DAT[9] | |
| DISPx_DAT10 | DAT[10] | G[5] | G[4] | G[2] | — | Y[2] | Y[0] | DAT[10] | |
| DISPx_DAT11 | DAT[11] | R[0] | G[5] | G[3] | — | Y[3] | Y[1] | DAT[11] | |
| DISPx_DAT12 | DAT[12] | R[1] | R[0] | G[4] | — | Y[4] | Y[2] | DAT[12] | |
| DISPx_DAT13 | DAT[13] | R[2] | R[1] | G[5] | — | Y[5] | Y[3] | DAT[13] | |
| DISPx_DAT14 | DAT[14] | R[3] | R[2] | G[6] | — | Y[6] | Y[4] | DAT[14] | |
| DISPx_DAT15 | DAT[15] | R[4] | R[3] | G[7] | — | Y[7] | Y[5] | DAT[15] | |
| DISPx_DAT16 | DAT[16] | — | R[4] | R[0] | — | — | Y[6] | — | |
| DISPx_DAT17 | DAT[17] | — | R[5] | R[1] | — | — | Y[7] | — | |
| DISPx_DAT18 | DAT[18] | — | — | R[2] | — | — | Y[8] | — | |
| DISPx_DAT19 | DAT[19] | — | — | R[3] | — | — | Y[9] | — | |
| DISPx_DAT20 | DAT[20] | — | — | R[4] | — | — | — | — | |
| DISPx_DAT21 | DAT[21] | — | — | R[5] | — | — | — | — | |

Table 60. Video Signal Cross-Reference (continued)

| i.MX53xD | LCD | | | | | | | | Comment ¹ |
|-----------------------|-------------------------------------|------------------------------------|---------------|---------------|-----------------------------|-----------------|-----------------|----------------|---|
| Port Name (x=0, 1) | RGB, Signal Name (General) | RGB/TV Signal Allocation (Example) | | | | | | Smart | |
| | | 16-bit RGB | 18-bit RGB | 24 Bit RGB | 8-bit YCrCb ² | 16-bit YCrCb | 20-bit YCrCb | Signal Name | |
| DISPx_DAT22 | DAT[22] | — | — | R[6] | — | — | — | — | — |
| DISPx_DAT23 | DAT[23] | — | — | R[7] | — | — | — | — | — |
| Dlx_DISP_CLK | PixCLK | | | | | | | — | — |
| Dlx_PIN1 | — | | | | | | | VSYNC_IN | May be required for anti-tearing |
| Dlx_PIN2 | HSYNC | | | | | | | — | — |
| Dlx_PIN3 | VSYNC | | | | | | | — | VSYNC out |
| Dlx_PIN4 | — | | | | | | | — | Additional frame/row synchronous signals with programmable timing |
| Dlx_PIN5 | — | | | | | | | — | |
| Dlx_PIN6 | — | | | | | | | — | |
| Dlx_PIN7 | — | | | | | | | — | |
| Dlx_PIN8 | — | | | | | | | — | |
| Dlx_D0_CS | — | | | | | | | CS0 | — |
| Dlx_D1_CS | — | | | | | | | CS1 | Alternate mode of PWM output for contrast or brightness control |
| Dlx_PIN11 | — | | | | | | | WR | — |
| Dlx_PIN12 | — | | | | | | | RD | — |
| Dlx_PIN13 | — | | | | | | | RS1 | Register select signal |
| Dlx_PIN14 | — | | | | | | | RS2 | Optional RS2 |
| Dlx_PIN15 | DRDY/DV | | | | | | | DRDY | Data validation/blank, data enable |
| Dlx_PIN16 | — | | | | | | | — | Additional data synchronous signals with programmable features/timing |
| Dlx_PIN17 | Q | | | | | | | — | |

¹ Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

² This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 60 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.7.8.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordingly.

4.7.8.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The `ipp_disp_clk` is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The `ipp_pin_1–ipp_pin_7` are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as HSYNC/VSYCN and so on) calculation. The internal event (local start point) is synchronized with internal `DI_CLK`. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half `DI_CLK` resolution. A full description of the counters system can be found in the IPU chapter of the i.MX53 Reference Manual.

4.7.8.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The `ipp_d0_cs` and `ipp_d1_cs` pins are dedicated to provide chip select signals to two displays.
- The `ipp_pin_11–ipp_pin_17` are general purpose asynchronous pins, that can be used to provide WR, RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half `DI_CLK` resolution.

4.7.8.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.7.8.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.7.8.6.2 LCD Interface Functional Description

Figure 47 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock, used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off. (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

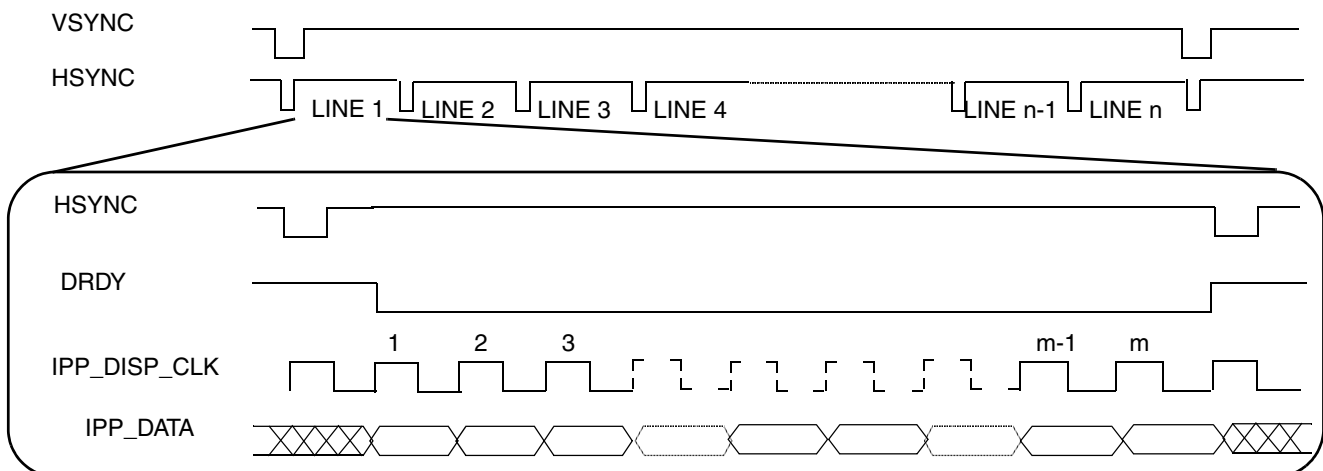


Figure 47. Interface Timing Diagram for TFT (Active Matrix) Panels

4.7.8.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 48 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

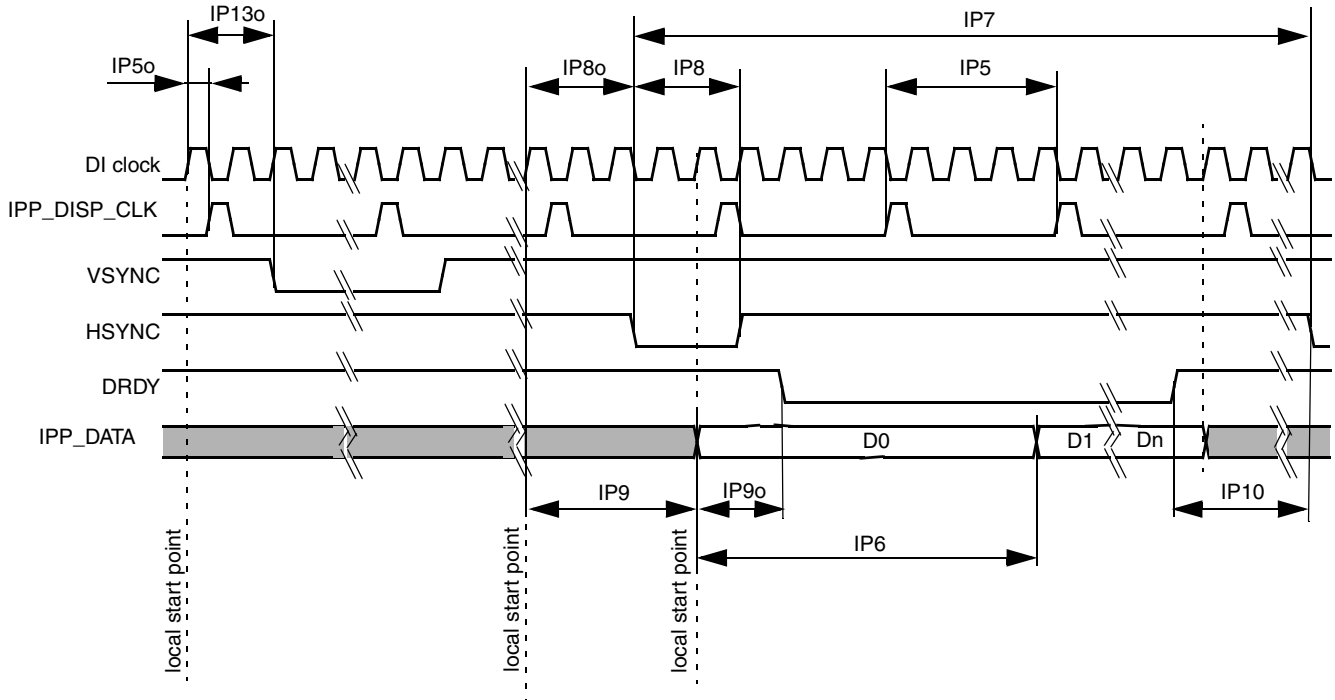


Figure 48. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 49 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

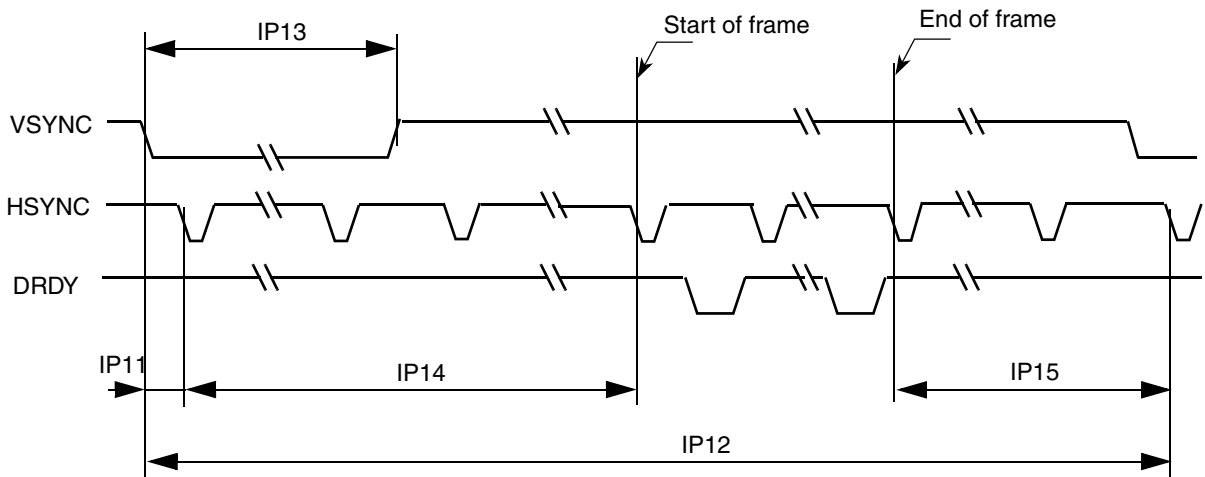


Figure 49. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 61 shows timing characteristics of signals presented in Figure 48 and Figure 49.

Table 61. Synchronous Display Interface Timing Characteristics (Pixel Level)

| ID | Parameter | Symbol | Value | Description | Unit |
|------|--------------------------------|--------|---------------------------------------|---|------|
| IP5 | Display interface clock period | Tdicp | (¹) | Display interface clock. IPP_DISP_CLK | ns |
| IP6 | Display pixel clock period | Tdpcp | DISP_CLK_PER_PIXEL × Tdicp | Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to n components. | ns |
| IP7 | Screen width time | Tsw | (SCREEN_WIDTH) × Tdicp | SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter ² . | ns |
| IP8 | HSYNC width time | Thsw | (HSYNC_WIDTH) | HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter. | ns |
| IP9 | Horizontal blank interval 1 | Thbi1 | BGXP × Tdicp | BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter. | ns |
| IP10 | Horizontal blank interval 2 | Thbi2 | (SCREEN_WIDTH - BGXP - FW) × Tdicp | Width a horizontal blanking after a last active data in a line (in interface clocks) FW—width of active line in interface clocks. The FW should be built by suitable DI's counter. | ns |
| IP12 | Screen height | Tsh | (SCREEN_HEIGHT) × Tsw | SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter. | ns |
| IP13 | VSYNC width | Tvsw | VSYNC_WIDTH | VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter | ns |
| IP14 | Vertical blank interval 1 | Tvbi1 | BGYP × Tsw | BGYP—width of first Vertical blanking interval in line.The BGYP should be built by suitable DI's counter. | ns |
| IP15 | Vertical blank interval 2 | Tvbi2 | (SCREEN_HEIGHT - BGYP - FH) × Tsw | Width of second Vertical blanking interval in line.The FH should be built by suitable DI's counter. | ns |

Table 61. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

| ID | Parameter | Symbol | Value | Description | Unit |
|-------|------------------------|--------|-----------------------------|--|------|
| IP50 | Offset of IPP_DISP_CLK | Todicp | DISP_CLK_OFFSET × Tdiclk | DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution) Defined by DISP_CLK counter | ns |
| IP130 | Offset of VSYNC | Tovs | VSYNC_OFFSET × Tdiclk | VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter. | ns |
| IP80 | Offset of HSYNC | Tohs | HSYNC_OFFSET × Tdiclk | HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter. | ns |
| IP90 | Offset of DRDY | Todrdy | DRDY_OFFSET × Tdiclk | DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI's counter. | ns |

¹ Display interface clock period immediate value.

$$T_{dicp} = \begin{cases} T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}, & \text{for integer } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \\ T_{diclk} \left(\text{floor} \left[\frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \right] + 0.5 \pm 0.5 \right), & \text{for fractional } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}_{dicp} = T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}$$

² DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$\text{Accuracy} = (0.5 \times T_{diclk}) \pm 0.62\text{ns}$$

The maximal accuracy of UP/DOWN edge of IPP_DATA is:

$$\text{Accuracy} = T_{\text{diclk}} \pm 0.62\text{ns}$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed through the registers.

Figure 50 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 62 lists the synchronous display interface timing characteristics.

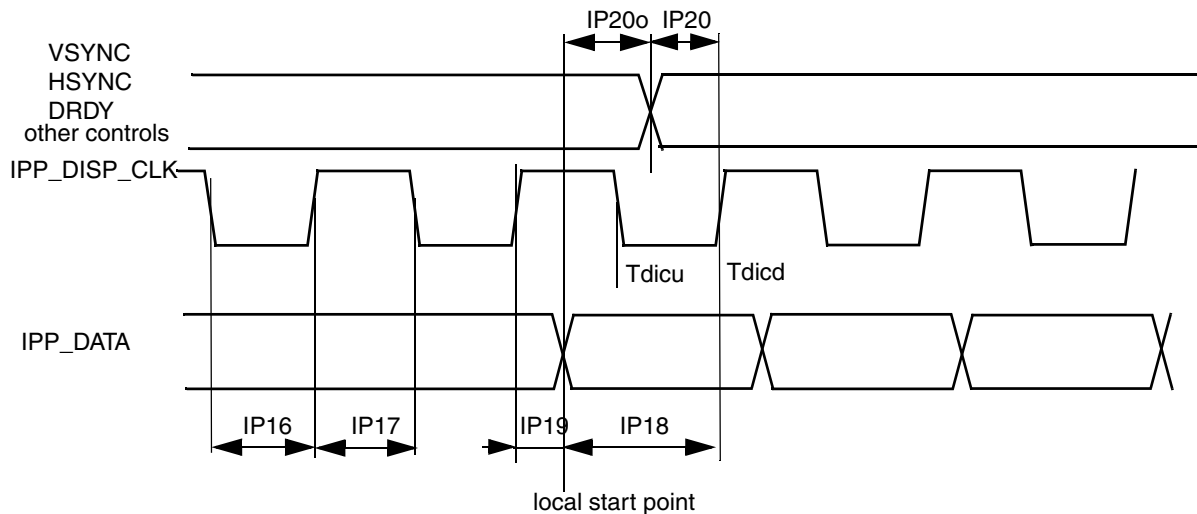


Figure 50. Synchronous Display Interface Timing Diagram—Access Level

Table 62. Synchronous Display Interface Timing Characteristics (Access Level)

| ID | Parameter | Symbol | Min | Typ ¹ | Max | Unit |
|-------|--|--------|------------------------|--|-----------------------|------|
| IP16 | Display interface clock low time | Tckl | Tdicd-Tdicu-1.24 | Tdicd ² -Tdicu ³ | Tdicd-Tdicu+1.24 | ns |
| IP17 | Display interface clock high time | Tckh | Tdicp-Tdicd+Tdicu-1.24 | Tdicp-Tdicd+Tdicu | Tdicp-Tdicd+Tdicu+1.2 | ns |
| IP18 | Data setup time | Tdsu | Tdicd-1.24 | Tdicu | — | ns |
| IP19 | Data holdup time | Tdhd | Tdicp-Tdicd-1.24 | Tdicp-Tdicu | — | ns |
| IP20o | Control signals offset times (defines for each pin) | Tocsu | Tocsu-1.24 | Tocsu | Tocsu+1.24 | ns |
| IP20 | Control signals setup time to display interface clock (defines for each pin) | Tcsu | Tdicd-1.24-Tocsu%Tdicp | Tdicu | — | ns |

¹The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

Electrical Characteristics

² Display interface clock down time

$$T_{dicd} = \frac{1}{2} \left(T_{diclk} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_DOWN}}{\text{DI_CLK_PERIOD}} \right] \right)$$

³ Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

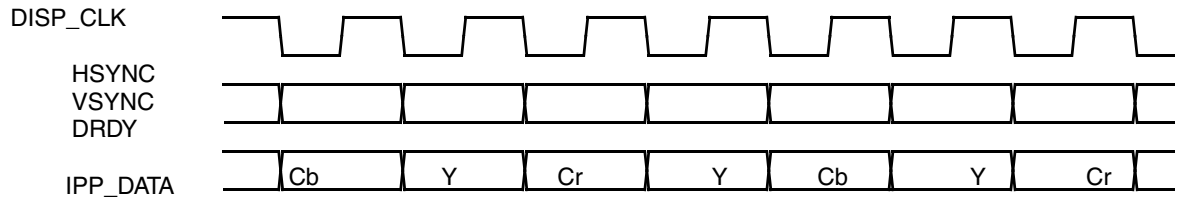
$$T_{dicu} = \frac{1}{2} \left(T_{diclk} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_UP}}{\text{DI_CLK_PERIOD}} \right] \right)$$

4.7.8.7 Interface to a TV Encoder (TVDAC)

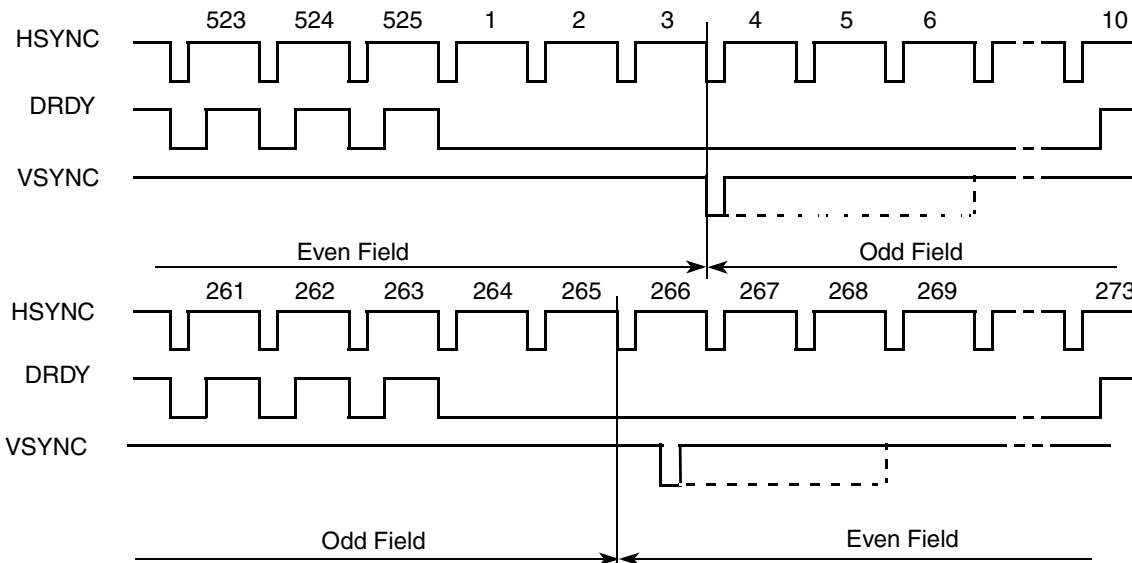
The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The timing of the interface is described in [Figure 51](#).

NOTE

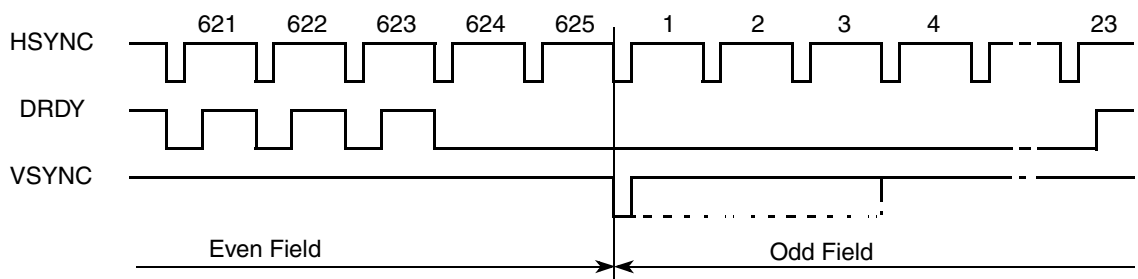
- The frequency of the clock DISP_CLK is 27 MHz (within 10%)
- The HSYNC, VSYNC signals are active low.
- The DRDY signal is shown as active high.
- The transition to the next row is marked by the negative edge of the HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the VSYNC signal. It remains low for at least one clock cycles.
 - At a transition to an odd field (of the next frame), the negative edges of VSYNC and HSYNC coincide.
 - At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the HSYNC signal being high.



Pixel Data Timing



Line and Field Timing - NTSC



Line and Field Timing - PAL

Figure 51. TV Encoder Interface Timing Diagram

4.7.8.7.1 TVEv2 TV Encoder Performance Specifications

The TV encoder output specifications are shown in [Table 63](#). All the parameters in the table are defined under the following conditions:

- $R_{\text{set}} = 1.05 \text{ k}\Omega \pm 1\%$, resistor on TVDAC_VREF pin to GND
- $R_{\text{load}} = 37.5 \text{ }\Omega \pm 1\%$, output load to the GND

Table 63. TV Encoder Video Performance Specifications

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|------|-------|------|----------|
| DAC STATIC PERFORMANCE | | | | | |
| Resolution ¹ | — | — | 10 | — | Bits |
| Integral Nonlinearity (INL) ² | — | — | 1 | 2 | LSBs |
| Differential Nonlinearity (DNL) ² | — | — | 0.6 | 1 | LSBs |
| Channel-to-channel gain matching ² | — | — | 2 | — | % |
| Full scale output voltage ² | $R_{\text{set}} = 1.05 \text{ k}\Omega \pm 1\%$ $R_{\text{load}} = 37.5 \text{ }\Omega \pm 1\%$ | 1.24 | 1.306 | 1.37 | V |
| DAC DYNAMIC PERFORMANCE | | | | | |
| Spurious Free Dynamic Range (SFDR) | $F_{\text{out}} = 3.38 \text{ MHz}$ $F_{\text{samp}} = 216 \text{ MHz}$ | — | 59 | — | dBc |
| Spurious Free Dynamic Range (SFDR) | $F_{\text{out}} = 8.3 \text{ MHz}$ $F_{\text{samp}} = 297 \text{ MHz}$ | — | 54 | — | dBc |
| VIDEO PERFORMANCE IN SD MODE² | | | | | |
| Short Term Jitter (Line to Line) | — | — | 2.5 | — | ±ns |
| Long Term Jitter (Field to Field) | — | — | 3.5 | — | ±ns |
| Frequency Response | 0–4.0 MHz | -0.1 | — | 0.1 | dB |
| | 5.75 MHz | -0.7 | — | 0 | dB |
| Luminance Nonlinearity | — | — | 0.5 | — | ±% |
| Differential Gain | — | — | 0.35 | — | % |
| Differential Phase | — | — | 0.6 | — | Degrees |
| Signal-to-Noise Ratio (SNR) | Flat field full bandwidth | — | 75 | — | dB |
| Hue Accuracy | — | — | 0.8 | — | ±Degrees |
| Color Saturation Accuracy | — | — | 1.5 | — | ±% |
| Chroma AM Noise | — | — | -70 | — | dB |
| Chroma PM Noise | — | — | -47 | — | dB |
| Chroma Nonlinear Phase | — | — | 0.5 | — | ±Degrees |
| Chroma Nonlinear Gain | — | — | 2.5 | — | ±% |
| Chroma/Luma Intermodulation | — | — | 0.1 | — | ±% |
| Chroma/Luma Gain Inequality | — | — | 1.0 | — | ±% |

Table 63. TV Encoder Video Performance Specifications (continued)

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|--------------------------|------|-----|-----|------|
| Chroma/Luma Delay Inequality | — | — | 1.0 | — | ±ns |
| VIDEO PERFORMANCE IN HD MODE² | | | | | |
| Luma Frequency Response | 0–30 MHz | -0.2 | — | 0.2 | dB |
| Chroma Frequency Response | 0–15 MHz, YCbCr 422 mode | -0.2 | — | 0.2 | dB |
| Luma Nonlinearity | — | — | 3.2 | — | % |
| Chroma Nonlinearity | — | — | 3.4 | — | % |
| Luma Signal-to-Noise Ratio | 0–30 MHz | — | 62 | — | dB |
| Chroma Signal-to-Noise Ratio | 0–15 MHz | — | 72 | — | dB |

¹ Guaranteed by design.

² Guaranteed by characterization.

4.7.8.8 Asynchronous Interfaces

The following sections describes the types of asynchronous interfaces.

4.7.8.8.1 Standard Parallel Interfaces

The IPU has four signal generator machines for asynchronous signal. Each machine generates IPU's internal control levels (0 or 1) by UP and DOWN that are defined in registers. Each asynchronous pin has a dynamic connection with one of the signal generators. This connection is redefined again with a new display access (pixel/component). The IPU can generate control signals according to system 80/68 requirements. The burst length is received as a result from predefined behavior of the internal signal generator machines.

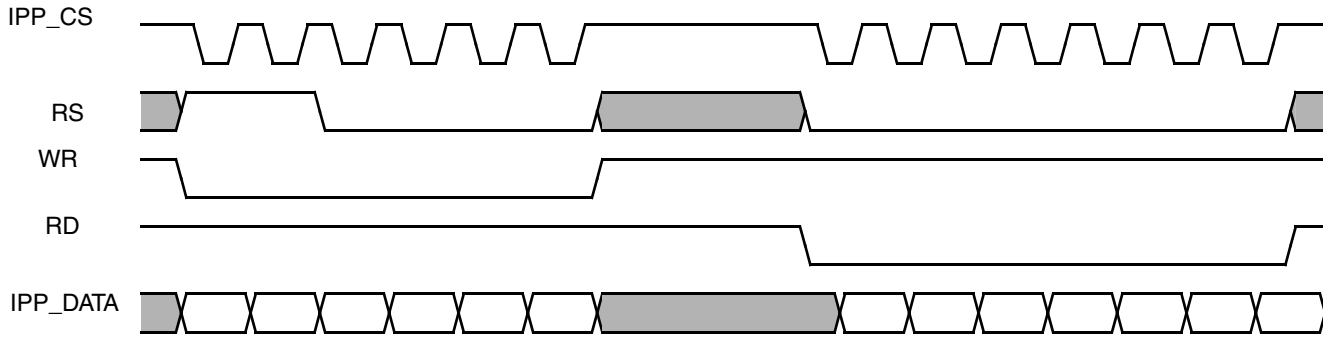
The access to a display is realized by the following:

- CS (IPP_CS) chip select
- WR (IPP_PIN_11) write strobe
- RD (IPP_PIN_12) read strobe
- RS (IPP_PIN_13) Register select (A0)

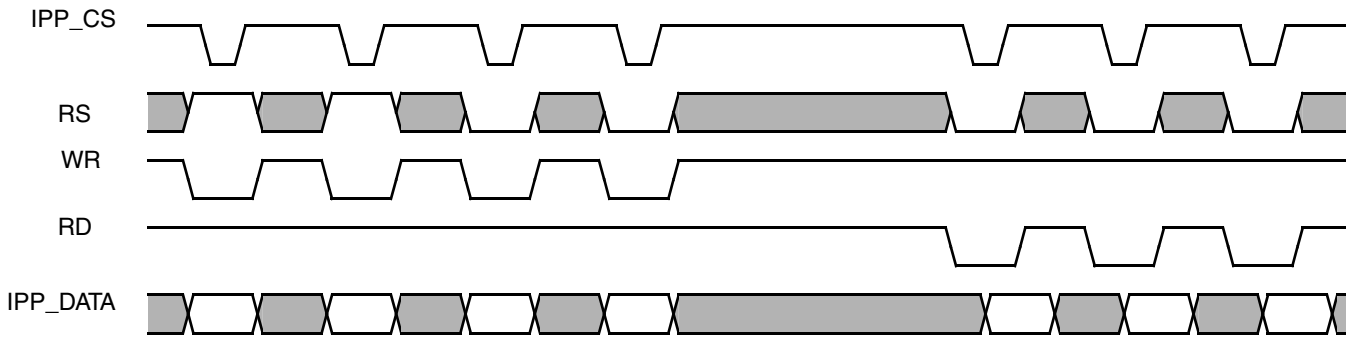
Both system 80 and system 68k interfaces are supported for all described modes as depicted in [Figure 52](#), [Figure 53](#), [Figure 54](#), and [Figure 55](#). The timing images correspond to active-low IPP_CS, WR and RD signals.

Each asynchronous access is defined by an access size parameter. This parameter can be different between different kinds of accesses. This parameter defines a length of windows, when suitable controls of the current access are valid. A pause between two different display accesses can be guaranteed by programing suitable access sizes. There are no minimal/maximal hold/setup times hard defined by DI. Each control signal can be switched at any time during access size.

Electrical Characteristics

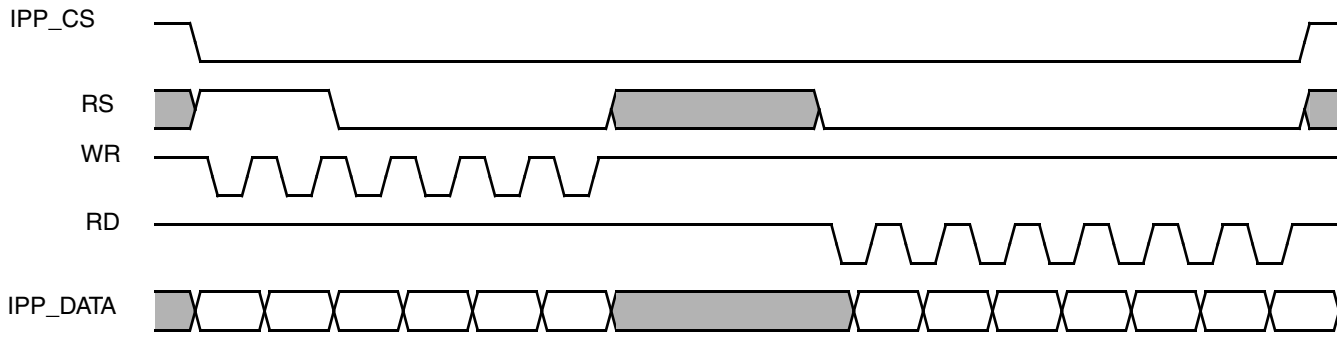


Burst access mode with sampling by CS signal

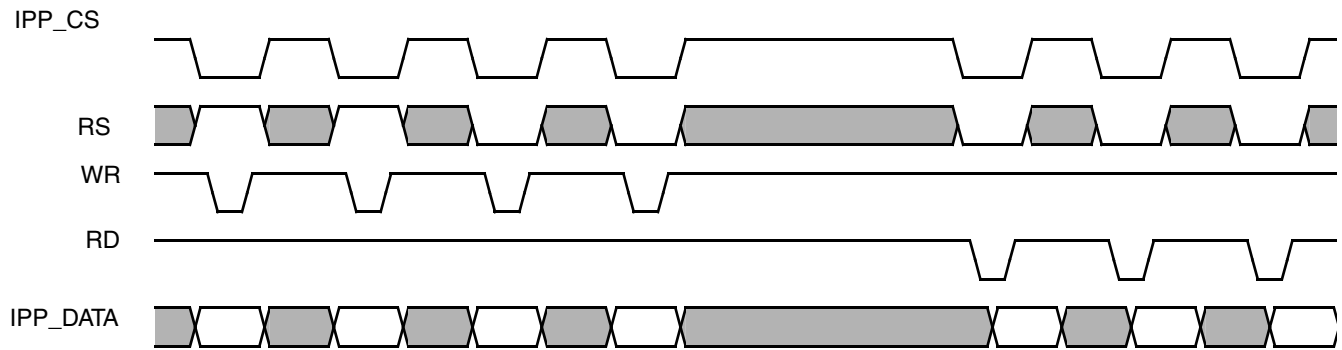


Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 52. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram



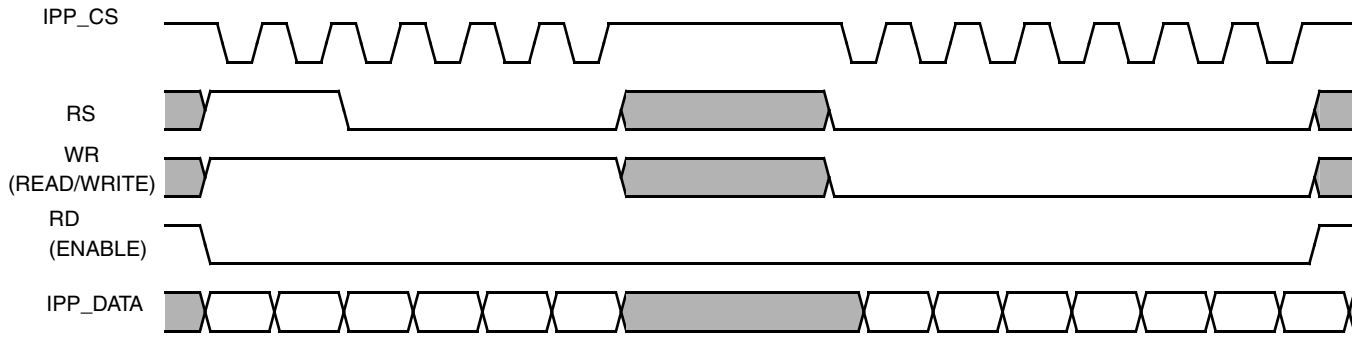
Burst access mode with sampling by WR/RD signals



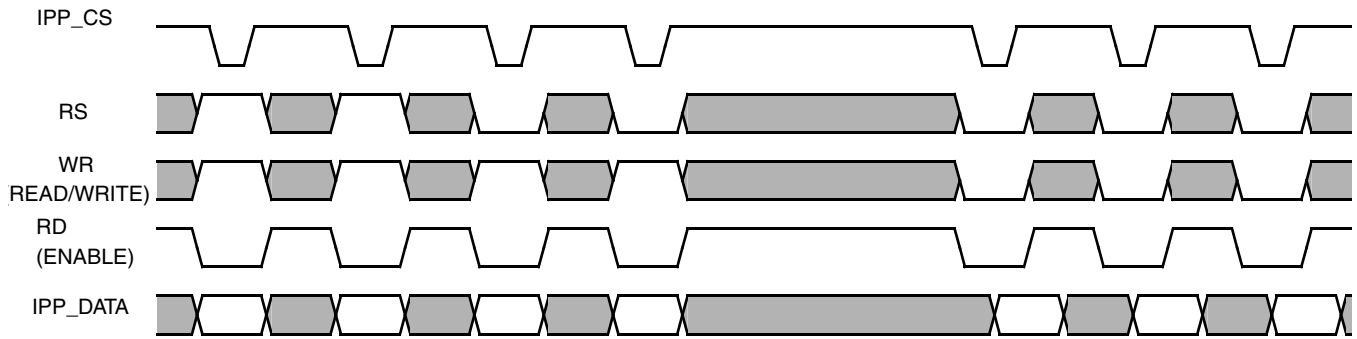
Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 53. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

Electrical Characteristics

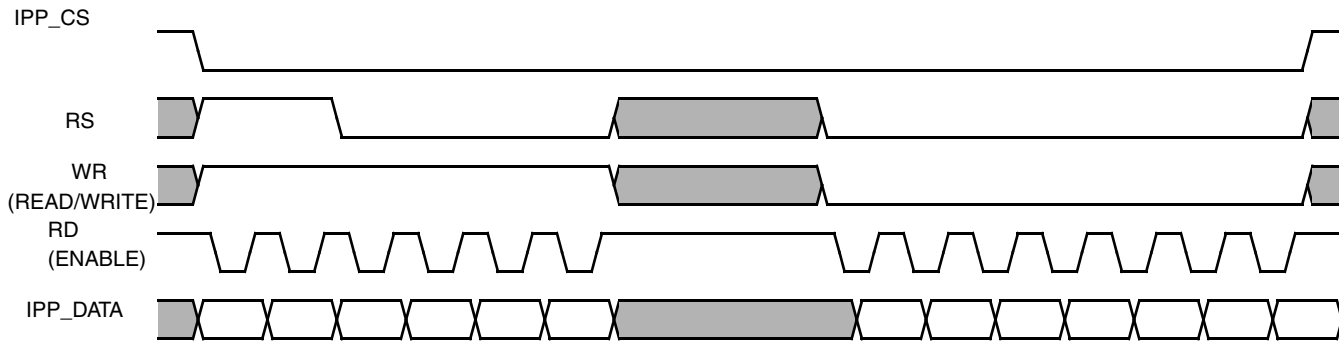


Burst access mode with sampling by CS signal

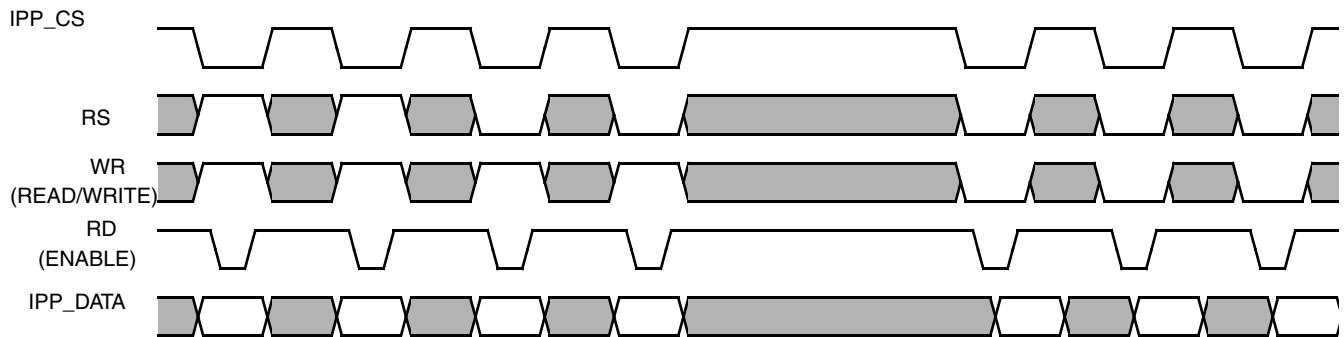


Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 54. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram



Burst access mode with sampling by ENABLE signal



Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 55. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Display operation can be performed with IPP_WAIT signal. The DI reacts to the incoming IPP_WAIT signal with 2 DI_CLK delay. The DI finishes a current access and a next access is postponed until IPP_WAIT release. [Figure 56](#) shows timing of the parallel interface with IPP_WAIT control.

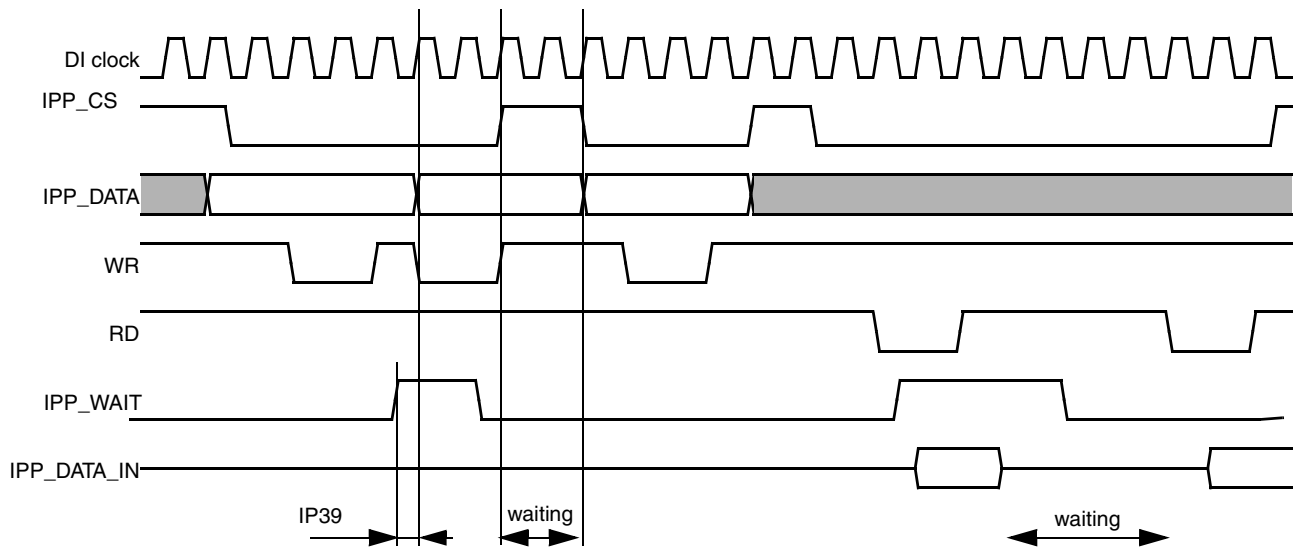


Figure 56. Parallel Interface Timing Diagram—Read Wait States

4.7.8.8.2 Asynchronous Parallel Interface Timing Parameters

Figure 57 depicts timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 65 shows timing characteristics at display access level. All timing diagrams are based on active low control signals (signals polarity is controlled through the DI_DISP_SIG_POL register).

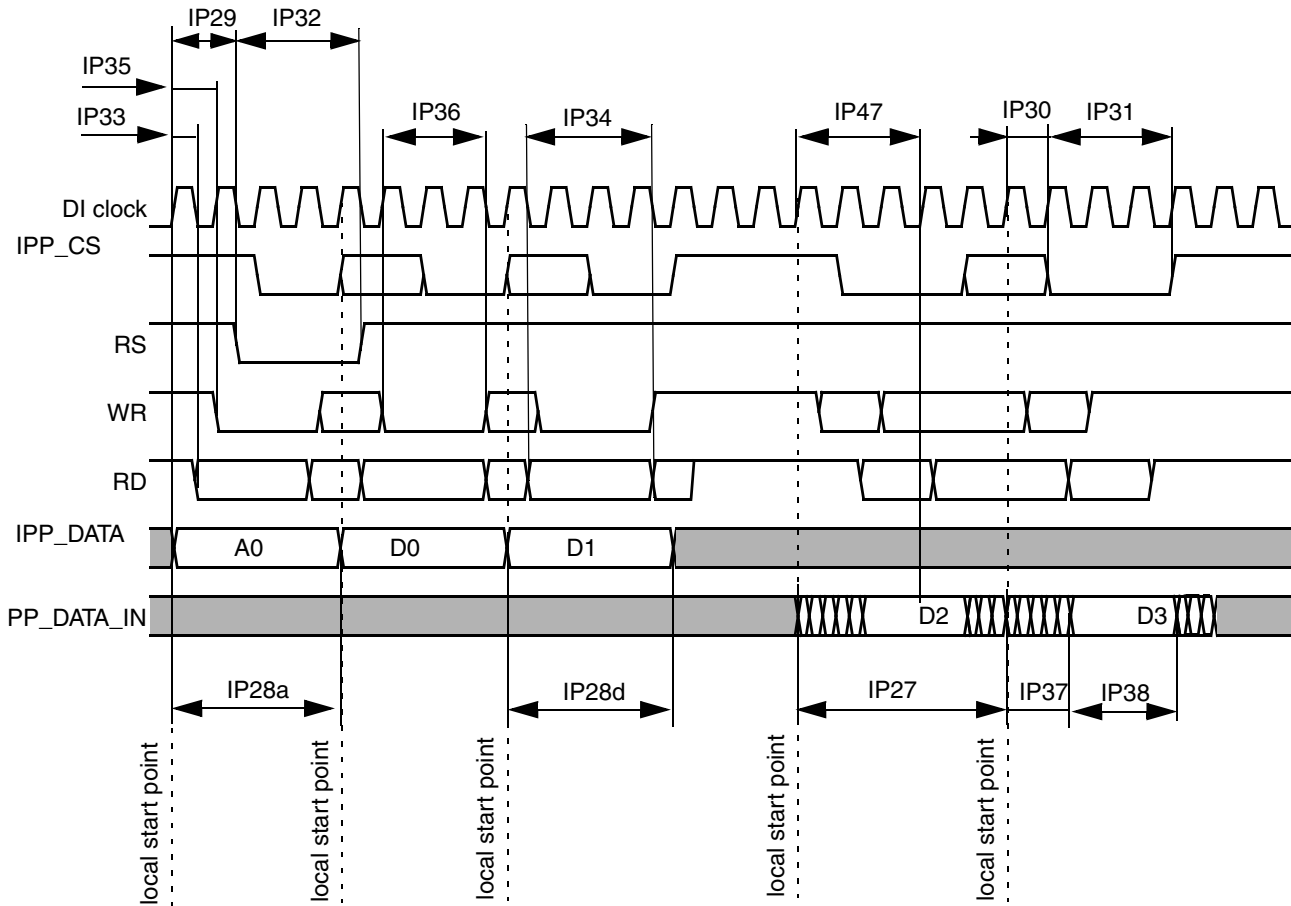


Figure 57. Asynchronous Parallel Interface Timing Diagram

Table 64. Asynchronous Display Interface Timing Parameters (Pixel Level)

| ID | Parameter | Symbol | Value | Description | Unit |
|-------|---------------------------------|--------|---------------|---|------|
| IP28a | Address Write system cycle time | Tcycwa | ACCESS_SIZE_# | predefined value in DI REGISTER | ns |
| IP28d | Data Write system cycle time | Tcycwd | ACCESS_SIZE_# | predefined value in DI REGISTER | ns |
| IP29 | RS start | Tdcrr | UP# | RS strobe switch, predefined value in DI REGISTER | ns |
| IP30 | CS start | Tdcsc | UP# | CS strobe switch, predefined value in DI REGISTER | ns |
| IP31 | CS hold | Tdchc | DOWN# | CS strobe release, predefined value in DI REGISTER | — |
| IP32 | RS hold | Tdchrr | DOWN# | RS strobe release, predefined value in DI REGISTER | — |
| IP35 | Write start | Tdcsw | UP# | write strobe switch, predefined value in DI REGISTER | ns |
| IP36 | Controls hold time for write | Tdchw | DOWN# | write strobe release, predefined value in DI REGISTER | ns |

Table 65. Asynchronous Parallel Interface Timing Parameters (Access Level)

| ID | Parameter | Symbol | Min | Typ ¹ | Max | Unit |
|------|--|--------|--------------------------------|--|------------------------|------|
| IP28 | Write system cycle time | Tcycw | Tdicpw - 1.24 | Tdicpw ² | Tdicpw+1.24 | ns |
| IP29 | RS start | Tdcsrr | Tdicurs - 1.24 | Tdicurs | Tdicurs+1.24 | ns |
| IP30 | CS start | Tdcsc | Tdicucs - 1.24 | Tdicur | Tdicucs+1.24 | ns |
| IP31 | CS hold | Tdchc | Tdicdcs - Tdicucs - 1.24 | Tdicdcs ³ -Tdicucs ⁴ | Tdicdcs - Tdicucs+1.24 | ns |
| IP32 | RS hold | Tdchrr | Tdicdrs - Tdicurs - 1.24 | Tdicdrs ⁵ -Tdicurs ⁶ | Tdicdrs - Tdicurs+1.24 | ns |
| IP35 | Controls setup time for write | Tdcsw | Tdicuw - 1.24 | Tdicuw | Tdicuw+1.24 | ns |
| IP36 | Controls hold time for write | Tdchw | Tdicdw - Tdicuw - 1.24 | Tdicpw ⁷ -Tdicuw ⁸ | Tdicdw-Tdicuw+1.24 | ns |
| IP38 | Slave device data hold time ⁸ | Troh | Tdrp - Tlbd - Tdicdr+1.24 4 | — | Tdicpr - Tdicdr - 1.24 | ns |

¹The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

²Display period value for write

$$Tdicpw = T_{DI_CLK} \times \text{ceil} \left[\frac{DI_ACCESS_SIZE_#}{DI_CLK_PERIOD} \right]$$

ACCESS_SIZE is predefined in REGISTER.

³Display control down for CS

$$Tdicdcs = \frac{1}{2} \left(T_{DI_CLK} \times \text{ceil} \left[\frac{2 \times DISP_DOWN_#}{DI_CLK_PERIOD} \right] \right)$$

DISP_DOWN is predefined in REGISTER.

⁴Display control up for CS

$$Tdicucs = \frac{1}{2} \left(T_{DI_CLK} \times \text{ceil} \left[\frac{2 \times DISP_UP_#}{DI_CLK_PERIOD} \right] \right)$$

DISP_UP is predefined in REGISTER.

⁵Display control down for RS

$$Tdicdrs = \frac{1}{2} \left(T_{DI_CLK} \times \text{ceil} \left[\frac{2 \times DISP_DOWN_#}{DI_CLK_PERIOD} \right] \right)$$

DISP_DOWN is predefined in REGISTER.

⁶Display control up for RS

$$Tdicurs = \frac{1}{2} \left(T_{DI_CLK} \times \text{ceil} \left[\frac{2 \times DISP_UP_#}{DI_CLK_PERIOD} \right] \right)$$

DISP_UP is predefined in REGISTER.

⁷Display control down for read

$$T_{dicdrw} = \frac{1}{2} \left(T_{DI_CLK} \times \text{ceil} \left[\frac{2 \times \text{DISP_DOWN_}\#}{DI_CLK_PERIOD} \right] \right)$$

DISP_DOWN is predefined in REGISTER.

⁸Display control up for write

$$T_{dicuw} = \frac{1}{2} \left(T_{DI_CLK} \times \text{ceil} \left[\frac{2 \times \text{DISP_UP_}\#}{DI_CLK_PERIOD} \right] \right)$$

DISP_UP is predefined in REGISTER.

4.7.9 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits”.

4.7.10 One-Wire (OWIRE) Timing Parameters

Figure 58 depicts the RPP timing, and Table 66 lists the RPP timing parameters.

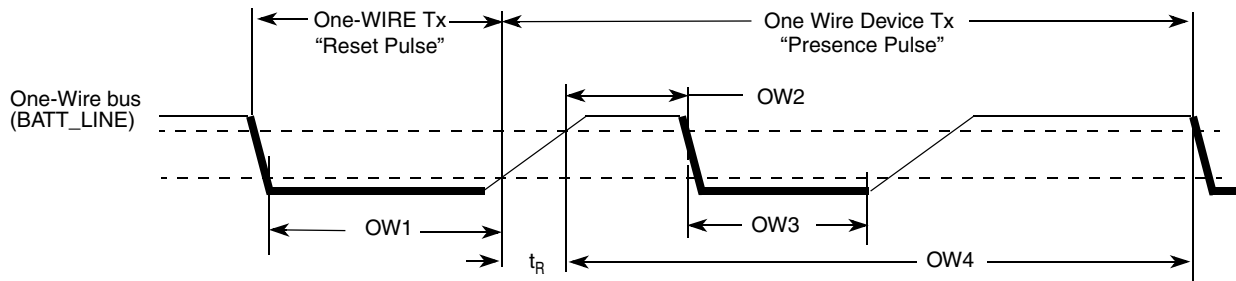


Figure 58. Reset and Presence Pulses (RPP) Timing Diagram

Table 66. RPP Sequence Delay Comparisons Timing Parameters

| ID | Parameters | Symbol | Min | Typ | Max | Unit |
|-----|---|-------------------|-----|-----|----------------|------|
| OW1 | Reset Time Low | t _{RSTL} | 480 | 511 | — ¹ | μs |
| OW2 | Presence Detect High | t _{PDH} | 15 | — | 60 | μs |
| OW3 | Presence Detect Low | t _{PDL} | 60 | — | 240 | μs |
| OW4 | Reset Time High (includes recovery time) | t _{RSTH} | 480 | 512 | — | μs |

¹ In order not to mask signaling by other devices on the 1-Wire bus, t_{RSTL} + t_R should always be less than 960 μs.

Figure 59 depicts Write 0 Sequence timing, and Table 67 lists the timing parameters.

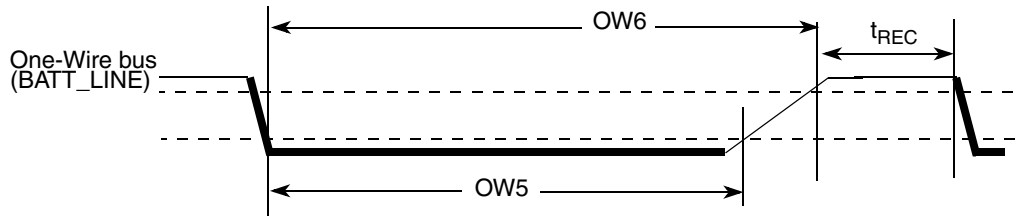


Figure 59. Write 0 Sequence Timing Diagram

Table 67. WR0 Sequence Timing Parameters

| ID | Parameter | Symbol | Min | Typ | Max | Unit |
|-----|------------------------|-------------------|-----|-----|-----|------|
| OW5 | Write 0 Low Time | t _{LOW0} | 60 | 100 | 120 | μs |
| OW6 | Transmission Time Slot | t _{SLOT} | OW5 | 117 | 120 | μs |
| | Recovery time | t _{REC} | 1 | — | — | μs |

Figure 60 depicts Write 1 Sequence timing, Figure 61 depicts the Read Sequence timing, and Table 68 lists the timing parameters.

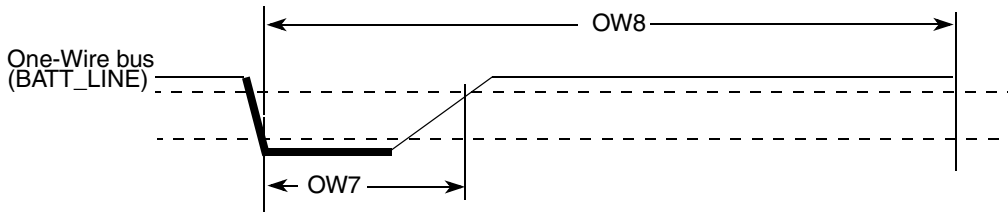


Figure 60. Write 1 Sequence Timing Diagram

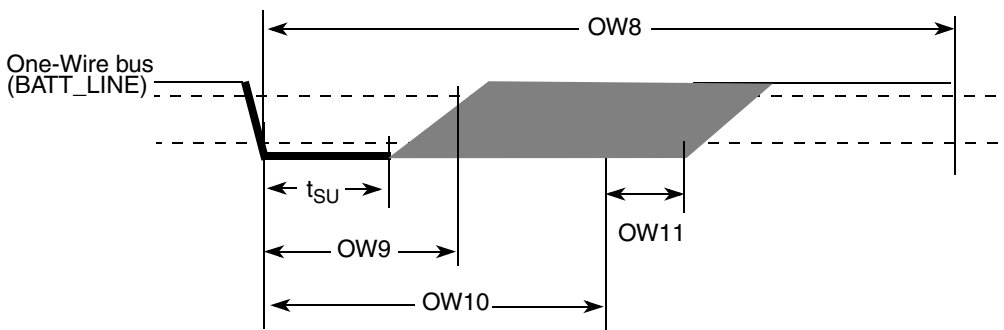


Figure 61. Read Sequence Timing Diagram

Table 68. WR1 /RD Timing Parameters

| ID | Parameter | Symbol | Min | Typ | Max | Unit |
|------|------------------------|---------------|-----|-----|-----|---------------|
| OW7 | Write 1 Low Time | t_{LOW1} | 1 | 5 | 15 | μs |
| OW8 | Transmission Time Slot | t_{SLOT} | 60 | 117 | 120 | μs |
| | Read Data Setup | t_{SU} | — | — | 1 | μs |
| OW9 | Read Low Time | t_{LOWR} | 1 | 5 | 15 | μs |
| OW10 | Read Data Valid | t_{RDV} | — | 15 | — | μs |
| OW11 | Release Time | $t_{RELEASE}$ | 0 | — | 45 | μs |

4.7.11 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 62 depicts the timing of the PWM, and Table 69 lists the PWM timing parameters.

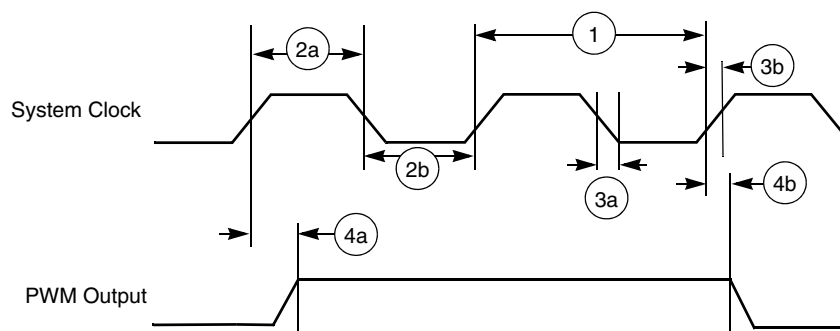


Figure 62. PWM Timing

Table 69. PWM Output Timing Parameter

| Ref. No. | Parameter | Min | Max | Unit |
|----------|-----------------------------------|-------|---------|------|
| 1 | System CLK frequency ¹ | 0 | ipg_clk | MHz |
| 2a | Clock high time | 12.29 | — | ns |
| 2b | Clock low time | 9.91 | — | ns |
| 3a | Clock fall time | — | 0.5 | ns |
| 3b | Clock rise time | — | 0.5 | ns |
| 4a | Output delay time | — | 9.37 | ns |
| 4b | Output setup time | 8.71 | — | ns |

¹ CL of PWMO = 30 pF

4.7.12 PATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-6 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100MB/s. Parallel ATA module interface consist of a total of 29 pins. Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-6 specification and these requirements are configurable by the ATA module registers.

Table 70 and Figure 63 define the AC characteristics of all the PATA interface signals in all data transfer modes.

ATA Interface Signals

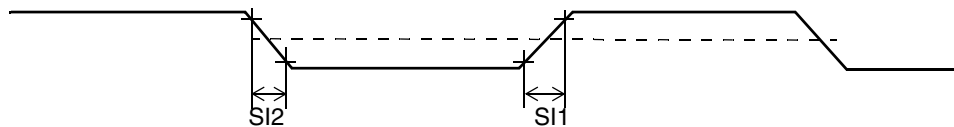


Figure 63. PATA Interface Signals Timing Diagram

Table 70. AC Characteristics of All Interface Signals

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---|-------------------|-----|------|------|
| SI1 | Rising edge slew rate for any signal on ATA interface ¹ | S _{rise} | — | 1.25 | V/ns |
| SI2 | Falling edge slew rate for any signal on ATA interface ¹ | S _{fall} | — | 1.25 | V/ns |
| SI3 | Host interface signal capacitance at the host connector | C _{host} | — | 20 | pF |

¹ SRISE and SFALL shall meet this requirement when measured at the sender’s connector from 10–90% of full signal amplitude with all capacitive loads from 15–40 pF where all signals have the same capacitive load value.

The user must use level shifters for 5.0 V compatibility on the ATA interface. The i.MX53xD PATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX53xD PATA interface on silicon, the bus buffer used, the cable delay and cable skew. [Table 71](#) shows ATA timing parameters.

Table 71. PATA Timing Parameters

| Name | Description | Value/ Contributing Factor ¹ |
|---------|--|--|
| T | Bus clock period (AHB_CLK_ROOT) | Peripheral clock frequency (7.5 ns for 133 MHz clock) |
| ti_ds | Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5 | 15 ns 10 ns 7 ns 5 ns 4 ns |
| ti_dh | Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5 | 5.0 ns 4.6 ns |
| tco | Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en | 12.0 ns |
| tsu | Set-up time ata_data to bus clock L-to-H | 8.5 ns |
| tsui | Set-up time ata_iordy to bus clock H-to-L | 8.5 ns |
| thi | Hold time ata_iordy to bus clock H to L | 2.5 ns |
| tskew1 | Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | 7 ns |
| tskew2 | Max difference in buffer propagation delay for any of following signals: ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | Transceiver |
| tskew3 | Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read) | Transceiver |
| tbuf | Max buffer propagation delay | Transceiver |
| tcable1 | Cable propagation delay for ata_data | Cable |
| tcable2 | Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack | Cable |
| tskew4 | Max difference in cable propagation delay between ata_iordy and ata_data (read) | Cable |
| tskew5 | Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write) | Cable |
| tskew6 | Max difference in cable propagation delay without accounting for ground bounce | Cable |

¹ Values provided where applicable.

4.7.12.1 PIO Mode Read Timing

Figure 64 shows timing for PIO read. Table 72 lists the timing parameters for PIO read.

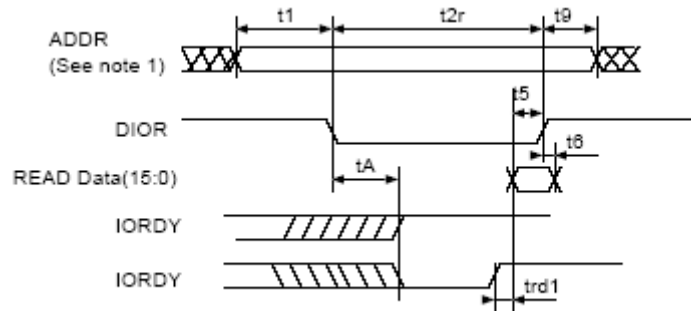


Figure 64. PIO Read Timing Diagram

Table 72. PIO Read Timing Parameters

| ATA Parameter | Parameter from Figure 64 | Value | Controlling Variable |
|---------------|--------------------------|--|---|
| t1 | t1 | $t1(\text{min}) = \text{time_1} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_1 |
| t2 (read) | t2r | $t2(\text{min}) = \text{time_2r} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_2r |
| t9 | t9 | $t9(\text{min}) = \text{time_9} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$ | time_9 |
| t5 | t5 | $t5(\text{min}) = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable2}$ | time_2 (affects t _{su} and t _{co}) |
| t6 | t6 | 0 | — |
| tA | tA | $tA(\text{min}) = (1.5 + \text{time_ax}) \times T - (t_{co} + t_{sui} + t_{cable2} + t_{cable2} + 2 \times t_{buf})$ | time_ax |
| trd | trd1 | $trd1(\text{max}) = (-trd) + (\text{tskew3} + \text{tskew4})$ $trd1(\text{min}) = (\text{time_pio_rdx} - 0.5) \times T - (t_{su} + t_{hi})$ $(\text{time_pio_rdx} - 0.5) \times T > t_{su} + t_{hi} + \text{tskew3} + \text{tskew4}$ | time_pio_rdx |
| t0 | — | $t0(\text{min}) = (\text{time_1} + \text{time_2r} + \text{time_9}) \times T$ | time_1, time_2r, time_9 |

Figure 65 shows timing for PIO write. Table 73 lists the timing parameters for PIO write.

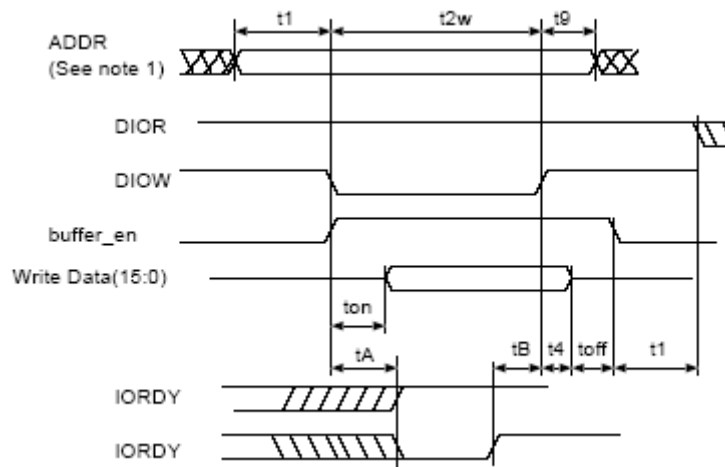


Figure 65. Multi-word DMA (MDMA) Timing

Table 73. PIO Write Timing Parameters

| ATA Parameter | Parameter from Figure 65 | Value | Controlling Variable |
|---------------|--------------------------|---|------------------------------|
| t1 | t1 | $t1(\min) = \text{time_1} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_1 |
| t2 (write) | t2w | $t2(\min) = \text{time_2w} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | time_2w |
| t9 | t9 | $t9(\min) = \text{time_9} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$ | time_9 |
| t3 | — | $t3(\min) = (\text{time_2w} - \text{time_on}) \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$ | If not met, increase time_2w |
| t4 | t4 | $t4(\min) = \text{time_4} \times T - \text{tskew1}$ | time_4 |
| tA | tA | $tA = (1.5 + \text{time_ax}) \times T - (\text{tco} + \text{tsui} + \text{tcable2} + \text{tcable2} + 2 \times \text{tbuf})$ | time_ax |
| t0 | — | $t0(\min) = (\text{time_1} + \text{time_2} + \text{time_9}) \times T$ | time_1, time_2r, time_9 |
| — | — | Avoid bus contention when switching buffer on by making ton long enough | — |
| — | — | Avoid bus contention when switching buffer off by making toff long enough | — |

Electrical Characteristics

Figure 66 shows timing for MDMA read, Figure 67 shows timing for MDMA write, and Table 74 lists the timing parameters for MDMA read and write.

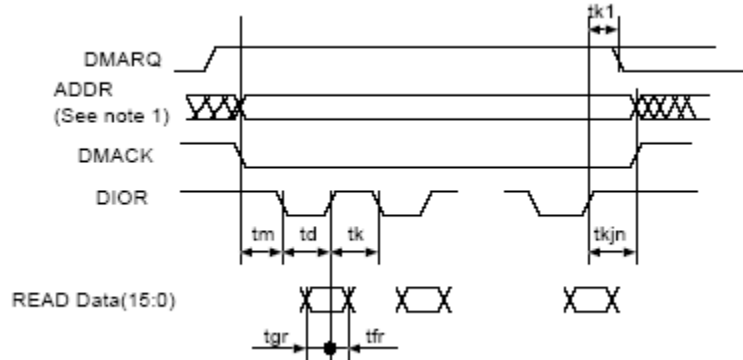


Figure 66. MDMA Read Timing Diagram

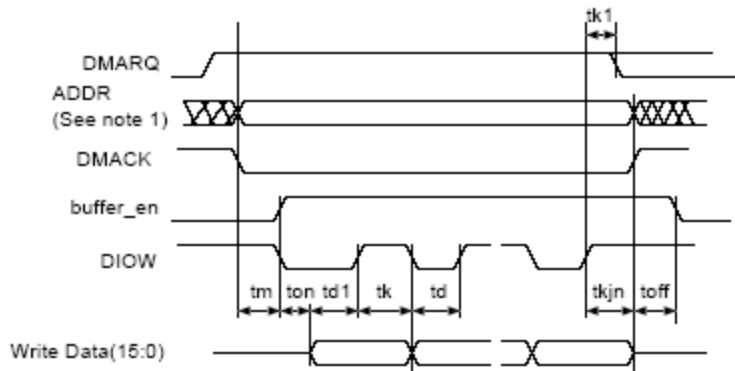


Figure 67. MDMA Write Timing Diagram

Table 74. MDMA Read and Write Timing Parameters

| ATA Parameter | Parameter from Figure 66 (Read), Figure 67 (Write) | Value | Controlling Variable |
|---------------|--|---|-----------------------------|
| tm, ti | tm | $tm(min) = ti(min) = time_m \times T - (tskew1 + tskew2 + tskew5)$ | time_m |
| td | td, td1 | $td1(min) = td(min) = time_d \times T - (tskew1 + tskew2 + tskew6)$ | time_d |
| tk | tk ¹ | $tk(min) = time_k \times T - (tskew1 + tskew2 + tskew6)$ | time_k |
| t0 | — | $t0(min) = (time_d + time_k) \times T$ | time_d, time_k |
| tg(read) | tgr | $tgr(min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2$ $tgr(min-drive) = td - te(drive)$ | time_d |
| tf(read) | tfr | $tfr(min) = 5\text{ ns}$ | — |
| tg(write) | — | $tg(min-write) = time_d \times T - (tskew1 + tskew2 + tskew5)$ | time_d |
| tf(write) | — | $tf(min-write) = time_k \times T - (tskew1 + tskew2 + tskew6)$ | time_k |
| tL | — | $tL\text{ (max)} = (time_d + time_k - 2) \times T - (tsu + tco + 2 \times tbuf + 2 \times tcable2)$ | time_d, time_k ² |

Table 74. MDMA Read and Write Timing Parameters (continued)

| ATA Parameter | Parameter from Figure 66 (Read), Figure 67 (Write) | Value | Controlling Variable |
|---------------|--|--|----------------------|
| tn, tj | tkjn | $tn = tj = tkjn = time_jn \times T - (tskew1 + tskew2 + tskew6)$ | time_jn |
| — | ton toff | ton = $time_on \times T - tskew1$ toff = $time_off \times T - tskew1$ | — |

¹ tk1 in the MDMA figures (Figure 66 and Figure 67) equals $(tk - 2 \times T)$.

² tk1 in the MDMA figures equals $(tk - 2 \times T)$.

4.7.12.2 Ultra DMA (UDMA) Input Timing

Figure 68 shows timing when the UDMA in transfer starts, Figure 69 shows timing when the UDMA in host terminates transfer, Figure 70 shows timing when the UDMA in device terminates transfer, and Table 75 lists the timing parameters for UDMA in burst.

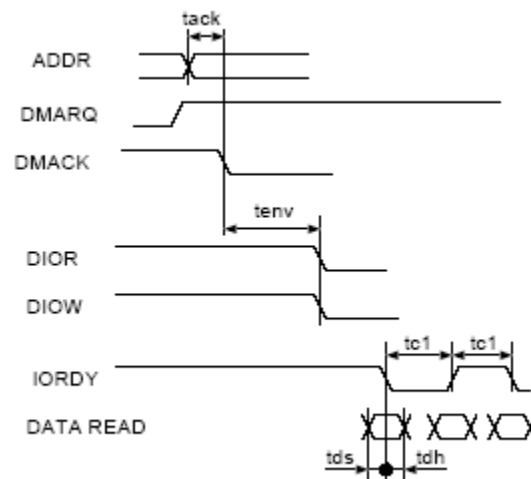


Figure 68. UDMA in Transfer Starts Timing Diagram

Table 75. UDMA in Burst Timing Parameters (continued)

| ATA Parameter | Parameter from Figure 68, Figure 69, and Figure 70 | Description | Controlling Variable |
|---------------|--|--|----------------------|
| tcyc | tc1 | $(tcyc - tskew) > T$ | T big enough |
| trp | trp | $trp (min) = time_rp \times T - (tskew1 + tskew2 + tskew6)$ | time_rp |
| — | tx1 ¹ | $(time_rp \times T) - (tco + tsu + 3T + 2 \times tbuf + 2 \times tcable2) > trfs (drive)$ | time_rp |
| tmli | tmli1 | $tmli1 (min) = (time_mlix + 0.4) \times T$ | time_mlix |
| tzah | tzah | $tzah (min) = (time_zah + 0.4) \times T$ | time_zah |
| tdzfs | tdzfs | $tdzfs = (time_dzfs \times T) - (tskew1 + tskew2)$ | time_dzfs |
| tcvh | tcvh | $tcvh = (time_cvh \times T) - (tskew1 + tskew2)$ | time_cvh |
| — | ton toff ² | ton = time_on × T - tskew1 toff = time_off × T - tskew1 | — |

¹ There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

² Make ton and toff big enough to avoid bus contention.

4.7.12.3 UDMA Output Timing

Figure 71 shows timing when the UDMA out transfer starts, Figure 72 shows timing when the UDMA out host terminates transfer, Figure 73 shows timing when the UDMA out device terminates transfer, and Table 76 lists the timing parameters for UDMA out burst.

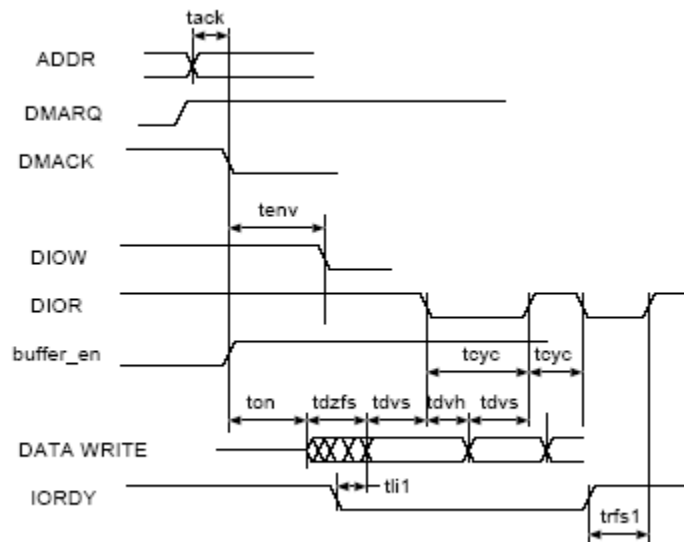


Figure 71. UDMA Out Transfer Starts Timing Diagram

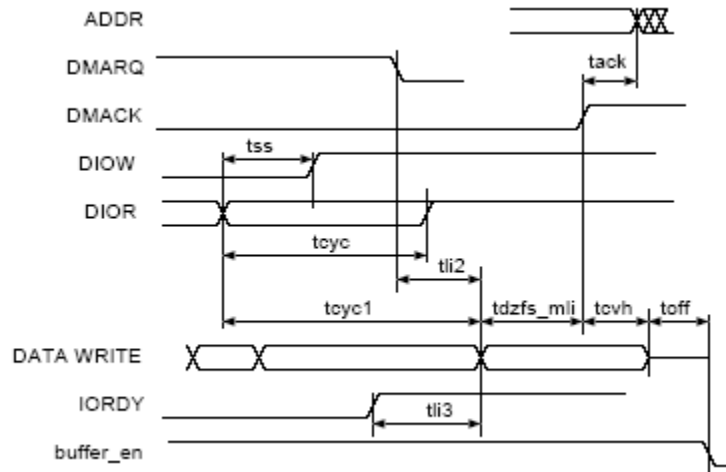


Figure 72. UDMA Out Host Terminates Transfer Timing Diagram

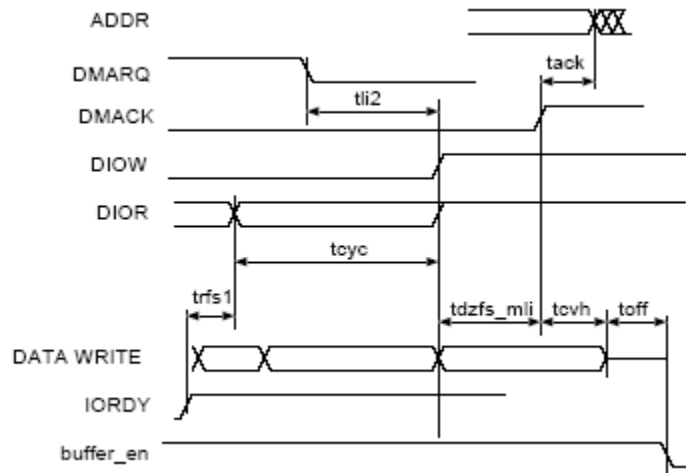


Figure 73. UDMA Out Device Terminates Transfer Timing Diagram

Table 76. UDMA Out Burst Timing Parameters

| ATA Parameter | Parameter from Figure 71, Figure 72, Figure 73 | Value | Controlling Variable |
|---------------|--|--|----------------------|
| tack | tack | $tack (min) = (time_ack \times T) - (tskew1 + tskew2)$ | time_ack |
| tenv | tenv | $tenv (min) = (time_env \times T) - (tskew1 + tskew2)$ $tenv (max) = (time_env \times T) + (tskew1 + tskew2)$ | time_env |
| tdvs | tdvs | $tdvs = (time_dvs \times T) - (tskew1 + tskew2)$ | time_dvs |
| tdvh | tdvh | $tdvh = (time_dvh \times T) - (tskew1 + tskew2)$ | time_dvh |
| tcyc | tcyc | $tcyc = time_cyc \times T - (tskew1 + tskew2)$ | time_cyc |
| t2cyc | — | $t2cyc = time_cyc \times 2 \times T$ | time_cyc |

Table 76. UDMA Out Burst Timing Parameters (continued)

| ATA Parameter | Parameter from Figure 71, Figure 72, Figure 73 | Value | Controlling Variable |
|---------------|--|--|----------------------|
| trfs1 | trfs | $trfs = 1.6 \times T + tsui + tco + tbuf + tbuf$ | — |
| — | tdzfs | $tdzfs = time_dzfs \times T - (tskew1)$ | time_dzfs |
| tss | tss | $tss = time_ss \times T - (tskew1 + tskew2)$ | time_ss |
| tmli | tdzfs_mli | $tdzfs_mli = \max(time_dzfs, time_mli) \times T - (tskew1 + tskew2)$ | — |
| tli | tli1 | $tli1 > 0$ | — |
| tli | tli2 | $tli2 > 0$ | — |
| tli | tli3 | $tli3 > 0$ | — |
| tcvh | tcvh | $tcvh = (time_cvh \times T) - (tskew1 + tskew2)$ | time_cvh |
| — | ton toff | $ton = time_on \times T - tskew1$ $toff = time_off \times T - tskew1$ | — |

4.7.13 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.7.13.1 Reference Clock Electrical and Jitter Specifications

The refclk signal is differential and supports frequencies of 25 MHz or 50-156.25 MHz (100 MHz and 125 MHz are common frequencies). The frequency is pin-selectable (for more information about the signal, see “Per-Transceiver Control and Status Signals” in the SATA PHY chapter in the Reference Manual).

Table 77 provides the SATA PHY reference clock specifications.

Table 77. Reference Clock Specifications

| Parameters | Test Conditions | Min | Max | Unit |
|--|---|-----|--------|--------|
| Differential peak voltage (typically 0.71 V) | — | 350 | 850 | mV |
| Common mode voltage (refclk_p + refclk_m) / 2 | — | 175 | 2,000 | mV |
| Total phase jitter | For information about total phase jitter, see following section | — | 3 | ps RMS |
| Minimum/maximum duty cycle | — | 40 | 60 | % UI |
| Frequency range | — | 25 | 156.25 | MHz |

4.7.13.1.1 Reference Clock Jitter Measurement

The total phase jitter on the reference clock is specified at 3 ps RMS. There are numerous ways to measure the reference clock jitter, one of which is as follows.

Using a high-speed sampling scope (20 GSamples/s), 1 million samples of the differential reference clock are taken, and the zero-crossing times of each rising edge are calculated. From the zero-crossing data, an average reference clock period is calculated. This average reference clock period is subtracted from each sequential, instantaneous period to find the difference between each reference clock rising edge and the ideal placement to produce the phase jitter sequence. The power spectral density (PSD) of the phase jitter is calculated and integrated after being weighted with the transfer function shown in Figure 74. The square root of the resultant integral is the RMS total phase jitter.

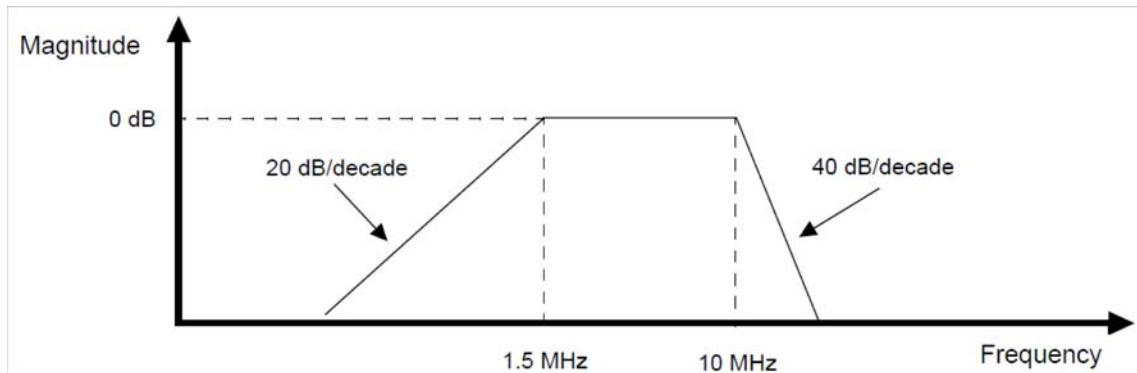


Figure 74. Weighting Function for RMS Phase Jitter Calculation

4.7.13.2 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specification. The following subsections provide values obtained from a combination of simulations and silicon characterization.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

4.7.13.2.1 SATA PHY Transmitter Characteristics

Table 78 provides specifications for SATA PHY transmitter characteristics.

Table 78. SATA2 PHY Transmitter Characteristics

| Parameters | Symbol | Min | Typ | Max | Unit |
|--|-----------|------|-----|-----|------|
| Transmit common mode voltage | V_{CTM} | 0.4 | — | 0.6 | V |
| Transmitter pre-emphasis accuracy (measured change in de-emphasized bit) | — | -0.5 | — | 0.5 | dB |

4.7.13.2.2 SATA PHY Receiver Characteristics

Table 79 provides specifications for SATA PHY receiver characteristics.

Table 79. SATA PHY Receiver Characteristics

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|--------------------------------|------|-----|-----|------|
| Minimum Rx eye height (differential peak-to-peak) | V _{MIN_RX_EYE_HEIGHT} | — | — | 175 | mV |
| Tolerance | PPM | -400 | — | 400 | ppm |

4.7.13.3 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.7.13.4 SATA Connectivity When Not in Use

NOTE

The Temperature Sensor is part of the SATA module. If SATA IP is disabled, the Temperature Sensor will not work as well. Temperature Sensor functionality is important in supporting high performance applications without overheating the device (at high ambient temp).

When both SATA and thermal sensor are not required, connect VP and VPH supplies to ground. The rest of the ports, both inputs and outputs (SATA_REFCLKM, SATA_REFCLKP, SATA_REXT, SATA_RXM, SATA_RXP, SATA_TXM) can be left floating. It is not recommended to turn off the VPH while the VP is active.

When SATA is not in use but thermal sensor is still required, both VP and VPH supplies must be powered on according to their nominal voltage levels. The reference clock input frequency must fall within the specified range of 25 MHz to 156.25 MHz. SATA_REXT does not need to be connected, as the termination impedance is not of consequence.

4.7.14 SCAN JTAG Controller (SJC) Timing Parameters

Figure 75 depicts the SJC test clock input timing. Figure 76 depicts the SJC boundary scan timing. Figure 77 depicts the SJC test access port. Signal parameters are listed in Table 80.

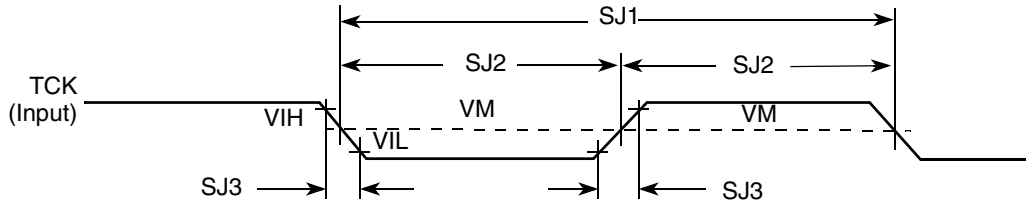


Figure 75. Test Clock Input Timing Diagram

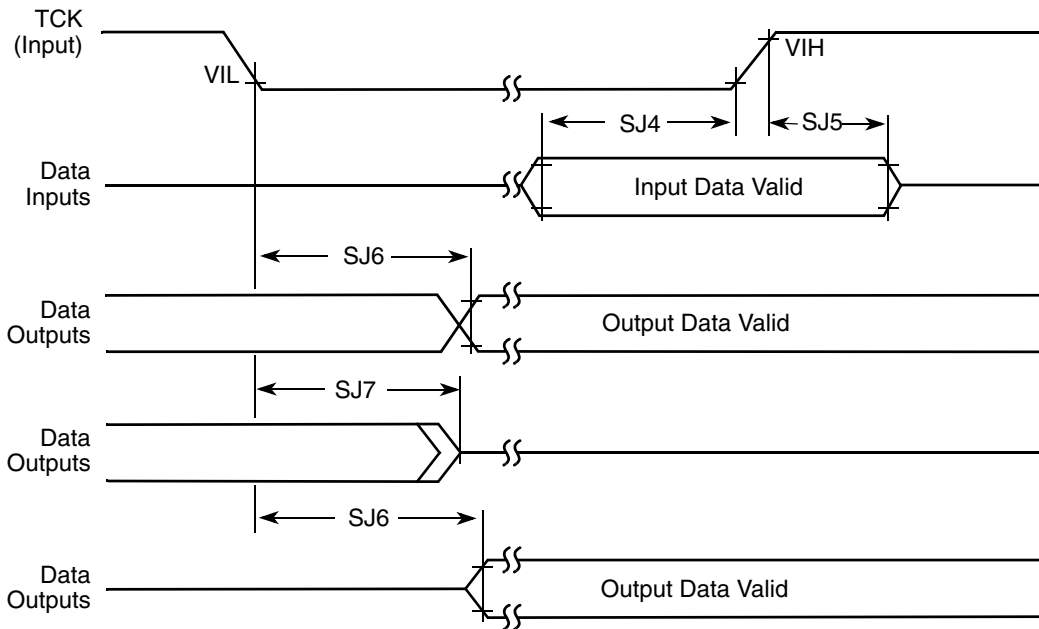


Figure 76. Boundary Scan (JTAG) Timing Diagram

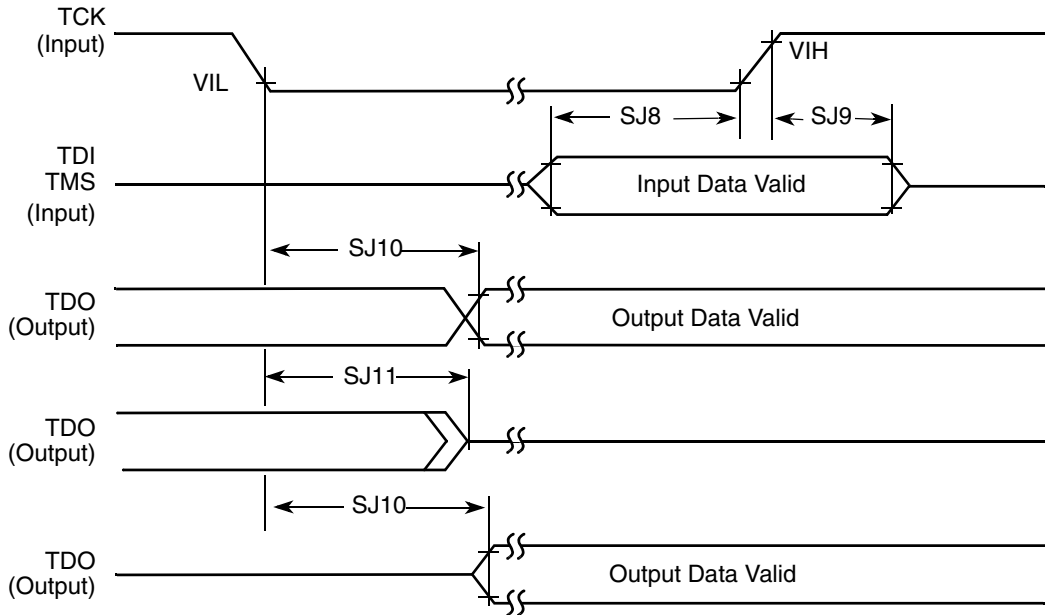


Figure 77. Test Access Port Timing Diagram

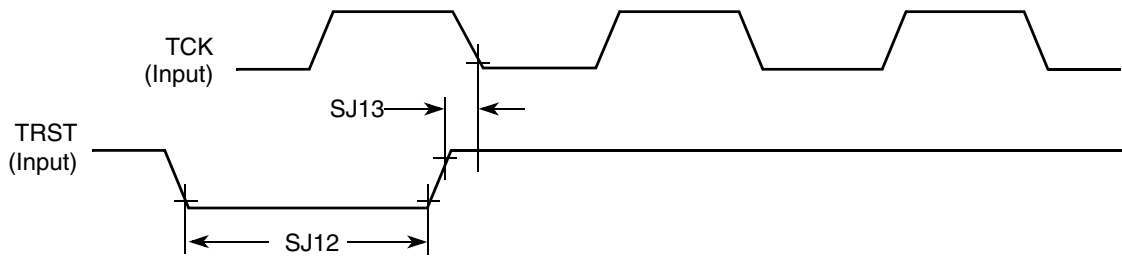


Figure 78. $\overline{\text{TRST}}$ Timing Diagram

Table 80. JTAG Timing

| ID | Parameter ^{1,2} | All Frequencies | | Unit |
|-----|---|-----------------|-----|------|
| | | Min | Max | |
| SJ0 | TCK frequency of operation $1/(3 \cdot T_{DC})^1$ | 0.001 | 22 | MHz |
| SJ1 | TCK cycle time in crystal mode | 45 | — | ns |
| SJ2 | TCK clock pulse width measured at V_M^2 | 22.5 | — | ns |
| SJ3 | TCK rise and fall times | — | 3 | ns |
| SJ4 | Boundary scan input data set-up time | 5 | — | ns |
| SJ5 | Boundary scan input data hold time | 24 | — | ns |
| SJ6 | TCK low to output data valid | — | 40 | ns |
| SJ7 | TCK low to output high impedance | — | 40 | ns |
| SJ8 | TMS, TDI data set-up time | 5 | — | ns |

Table 80. JTAG Timing (continued)

| ID | Parameter ^{1,2} | All Frequencies | | Unit |
|------|---|-----------------|-----|------|
| | | Min | Max | |
| SJ9 | TMS, TDI data hold time | 25 | — | ns |
| SJ10 | TCK low to TDO data valid | — | 44 | ns |
| SJ11 | TCK low to TDO high impedance | — | 44 | ns |
| SJ12 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| SJ13 | $\overline{\text{TRST}}$ set-up time to TCK low | 40 | — | ns |

¹ T_{DC} = target frequency of SJC

² V_M = mid-point voltage

4.7.15 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 81 and Figures , show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 81. SPDIF Timing Parameters

| Characteristics | Symbol | Timing Parameter Range | | Units |
|---|---------|------------------------|------|-------|
| | | Min | Max | |
| SPDIFIN Skew: asynchronous inputs, no specs apply | — | — | 0.7 | ns |
| SPDIFOUT output (Load = 50pf) | | | | |
| • Skew | — | — | 1.5 | ns |
| • Transition rising | — | — | 24.2 | |
| • Transition falling | — | — | 31.3 | |
| SPDIFOUT1 output (Load = 30pf) | | | | |
| • Skew | — | — | 1.5 | ns |
| • Transition rising | — | — | 13.6 | |
| • Transition falling | — | — | 18.0 | |
| Modulating Rx clock (SRCK) period | srckp | 40.0 | — | ns |
| SRCK high period | srckph | 16.0 | — | ns |
| SRCK low period | srckpl | 16.0 | — | ns |
| Modulating Tx clock (STCLK) period | stclkp | 40.0 | — | ns |
| STCLK high period | stclkph | 16.0 | — | ns |
| STCLK low period | stclkpl | 16.0 | — | ns |

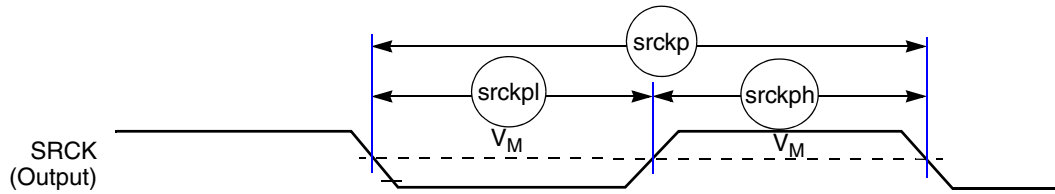


Figure 79. SPDIF Timing Diagram

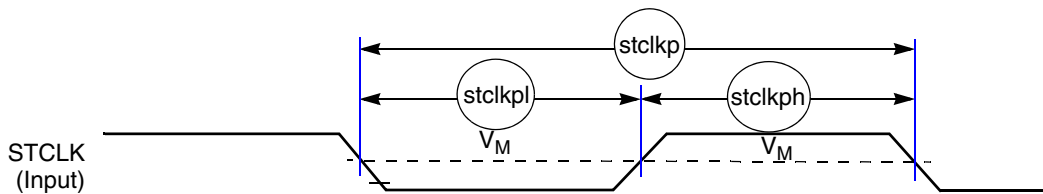


Figure 80. STCLK Timing

4.7.16 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in [Table 82](#).

Table 82. AUDMUX Port Allocation

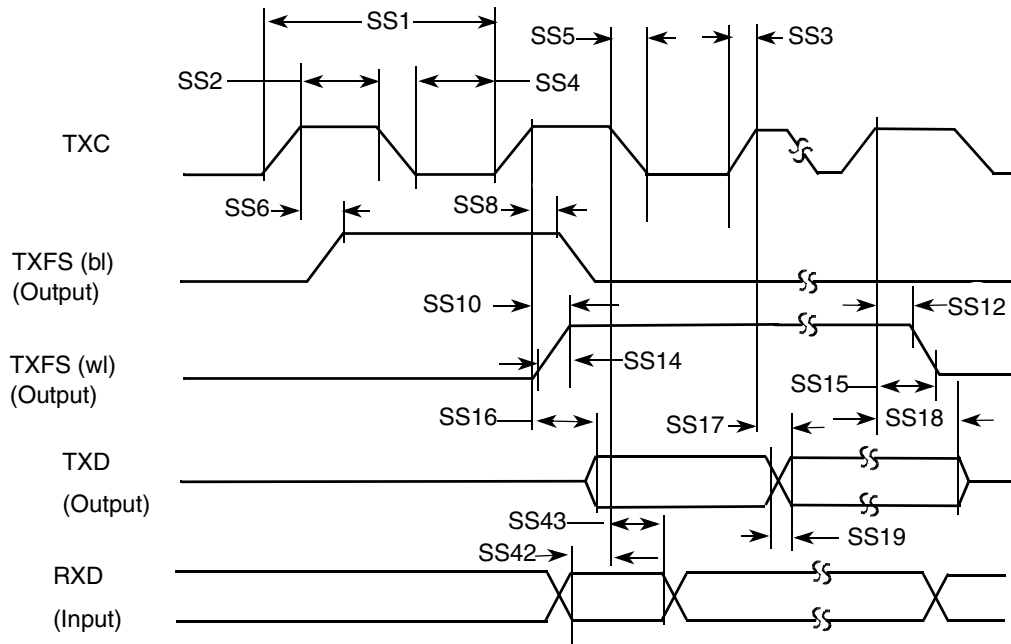
| Port | Signal Nomenclature | Type and Access |
|---------------|---------------------|---|
| AUDMUX port 1 | SSI 1 | Internal |
| AUDMUX port 2 | SSI 2 | Internal |
| AUDMUX port 3 | AUD3 | External— AUD3 I/O |
| AUDMUX port 4 | AUD4 | External— EIM or CSPI1 I/O through IOMUXC |
| AUDMUX port 5 | AUD5 | External— EIM or SD1 I/O through IOMUXC |
| AUDMUX port 6 | AUD6 | External— EIM or DISP2 through IOMUXC |
| AUDMUX port 7 | SSI 3 | Internal |

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the i.MX53 Reference Manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.7.16.1 SSI Transmitter Timing with Internal Clock

Figure 81 depicts the SSI transmitter internal clock timing and Table 83 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only
 : SRXD input in synchronous mode only

Figure 81. SSI Transmitter Internal Clock Timing Diagram

Table 83. SSI Transmitter Timing with Internal Clock

| ID | Parameter | Min | Max | Unit |
|---------------------------------|--|------|------|------|
| Internal Clock Operation | | | | |
| SS1 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS2 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS3 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS4 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS5 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS6 | (Tx) CK high to FS (bl) high | — | 15.0 | ns |
| SS8 | (Tx) CK high to FS (bl) low | — | 15.0 | ns |
| SS10 | (Tx) CK high to FS (wl) high | — | 15.0 | ns |
| SS12 | (Tx) CK high to FS (wl) low | — | 15.0 | ns |
| SS14 | (Tx/Rx) Internal FS rise time | — | 6.0 | ns |
| SS15 | (Tx/Rx) Internal FS fall time | — | 6.0 | ns |
| SS16 | (Tx) CK high to STXD valid from high impedance | — | 15.0 | ns |

Table 83. SSI Transmitter Timing with Internal Clock (continued)

| ID | Parameter | Min | Max | Unit |
|---|-------------------------------------|------|------|------|
| SS17 | (Tx) CK high to STXD high/low | — | 15.0 | ns |
| SS18 | (Tx) CK high to STXD high impedance | — | 15.0 | ns |
| SS19 | STXD rise/fall time | — | 6.0 | ns |
| Synchronous Internal Clock Operation | | | | |
| SS42 | SRXD setup before (Tx) CK falling | 10.0 | — | ns |
| SS43 | SRXD hold after (Tx) CK falling | 0.0 | — | ns |
| SS52 | Loading | — | 25.0 | pF |

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.16.2 SSI Receiver Timing with Internal Clock

Figure 82 depicts the SSI receiver internal clock timing and Table 84 lists the timing parameters for the receiver timing with the internal clock

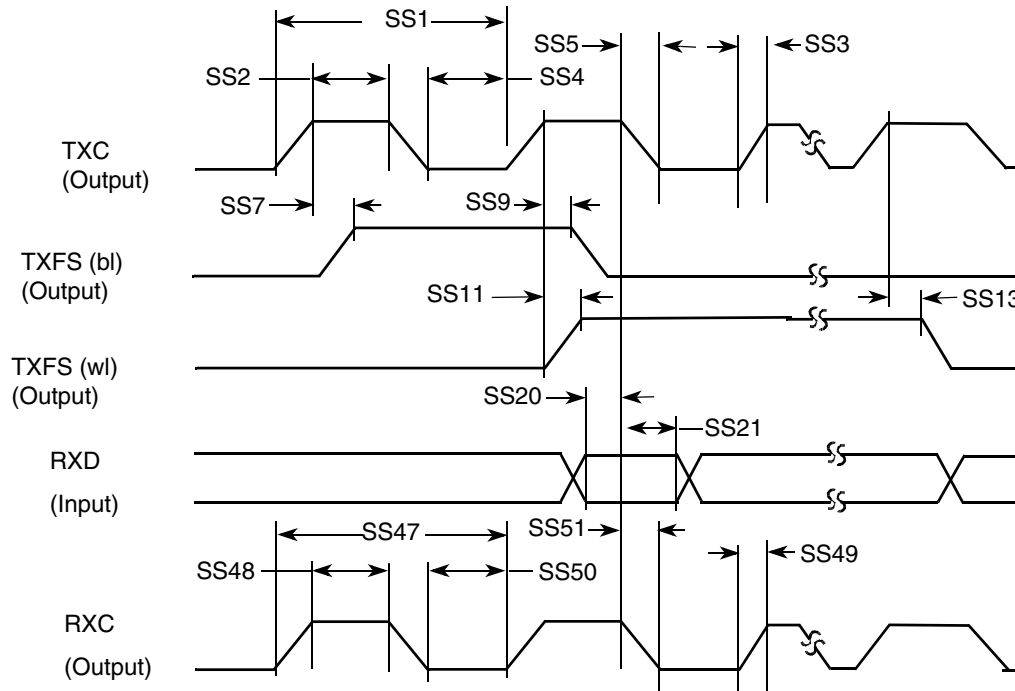


Figure 82. SSI Receiver Internal Clock Timing Diagram

Table 84. SSI Receiver Timing with Internal Clock

| ID | Parameter | Min | Max | Unit |
|---------------------------------|------------------------------------|------|------|------|
| Internal Clock Operation | | | | |
| SS1 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS2 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS3 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS4 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS5 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS7 | (Rx) CK high to FS (bl) high | — | 15.0 | ns |
| SS9 | (Rx) CK high to FS (bl) low | — | 15.0 | ns |
| SS11 | (Rx) CK high to FS (wl) high | — | 15.0 | ns |
| SS13 | (Rx) CK high to FS (wl) low | — | 15.0 | ns |
| SS20 | SRXD setup time before (Rx) CK low | 10.0 | — | ns |
| SS21 | SRXD hold time after (Rx) CK low | 0.0 | — | ns |

Table 84. SSI Receiver Timing with Internal Clock (continued)

| ID | Parameter | Min | Max | Unit |
|-------------------------------------|--------------------------------|-------|-----|------|
| Oversampling Clock Operation | | | | |
| SS47 | Oversampling clock period | 15.04 | — | ns |
| SS48 | Oversampling clock high period | 6.0 | — | ns |
| SS49 | Oversampling clock rise time | — | 3.0 | ns |
| SS50 | Oversampling clock low period | 6.0 | — | ns |
| SS51 | Oversampling clock fall time | — | 3.0 | ns |

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.16.3 SSI Transmitter Timing with External Clock

Figure 83 depicts the SSI transmitter external clock timing and Table 85 lists the timing parameters for the transmitter timing with the external clock

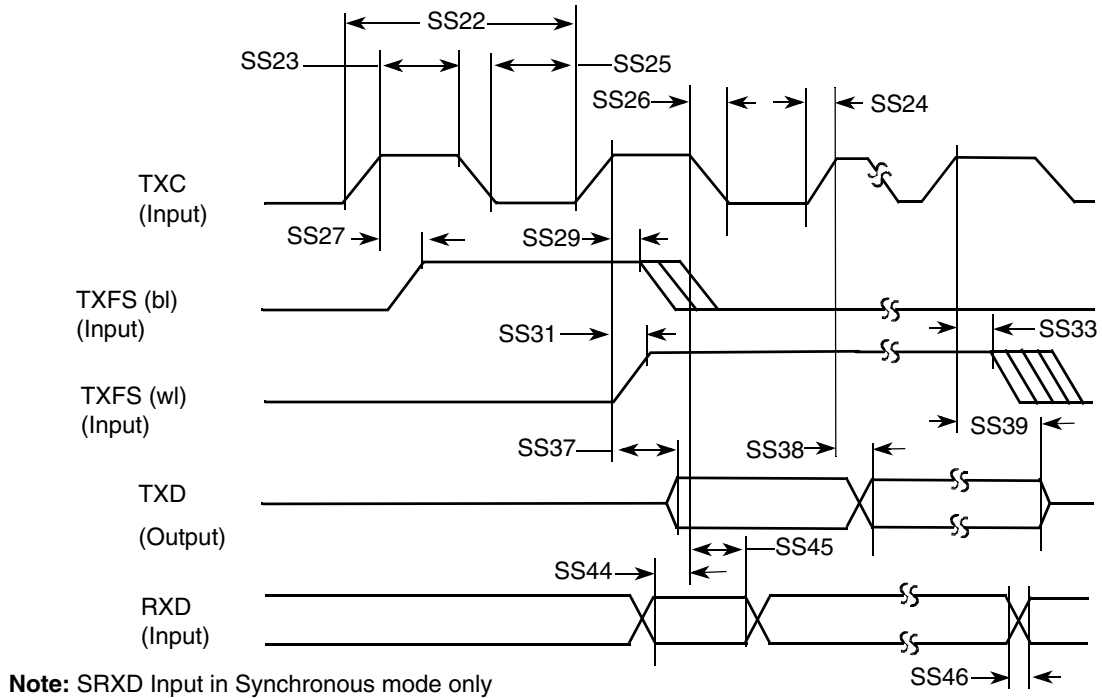


Figure 83. SSI Transmitter External Clock Timing Diagram

Table 85. SSI Transmitter Timing with External Clock

| ID | Parameter | Min | Max | Unit |
|---------------------------------|--|-------|------|------|
| External Clock Operation | | | | |
| SS22 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS23 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS24 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS25 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS26 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS27 | (Tx) CK high to FS (bl) high | -10.0 | 15.0 | ns |
| SS29 | (Tx) CK high to FS (bl) low | 10.0 | — | ns |
| SS31 | (Tx) CK high to FS (wl) high | -10.0 | 15.0 | ns |
| SS33 | (Tx) CK high to FS (wl) low | 10.0 | — | ns |
| SS37 | (Tx) CK high to STXD valid from high impedance | — | 15.0 | ns |
| SS38 | (Tx) CK high to STXD high/low | — | 15.0 | ns |

Table 85. SSI Transmitter Timing with External Clock (continued)

| ID | Parameter | Min | Max | Unit |
|---|-------------------------------------|------|------|------|
| SS39 | (Tx) CK high to STXD high impedance | — | 15.0 | ns |
| Synchronous External Clock Operation | | | | |
| SS44 | SRXD setup before (Tx) CK falling | 10.0 | — | ns |
| SS45 | SRXD hold after (Tx) CK falling | 2.0 | — | ns |
| SS46 | SRXD rise/fall time | — | 6.0 | ns |

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.16.4 SSI Receiver Timing with External Clock

Figure 84 depicts the SSI receiver external clock timing and Table 86 lists the timing parameters for the receiver timing with the external clock.

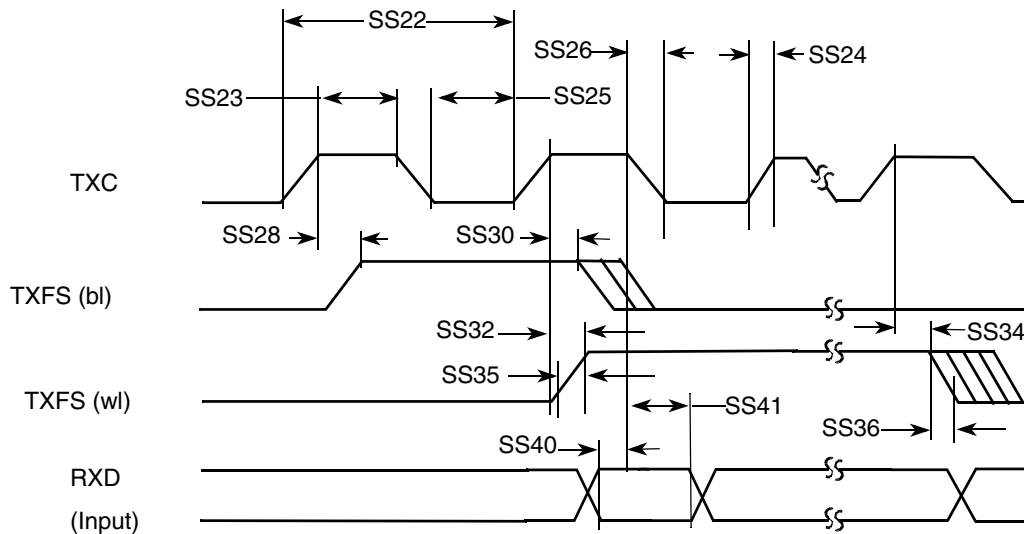


Figure 84. SSI Receiver External Clock Timing Diagram

Table 86. SSI Receiver Timing with External Clock

| ID | Parameter | Min | Max | Unit |
|---------------------------------|------------------------------------|------|------|------|
| External Clock Operation | | | | |
| SS22 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS23 | (Tx/Rx) CK clock high period | 36 | — | ns |
| SS24 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS25 | (Tx/Rx) CK clock low period | 36 | — | ns |
| SS26 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS28 | (Rx) CK high to FS (bl) high | -10 | 15.0 | ns |
| SS30 | (Rx) CK high to FS (bl) low | 10 | — | ns |
| SS32 | (Rx) CK high to FS (wl) high | -10 | 15.0 | ns |
| SS34 | (Rx) CK high to FS (wl) low | 10 | — | ns |
| SS35 | (Tx/Rx) External FS rise time | — | 6.0 | ns |
| SS36 | (Tx/Rx) External FS fall time | — | 6.0 | ns |
| SS40 | SRXD setup time before (Rx) CK low | 10 | — | ns |
| SS41 | SRXD hold time after (Rx) CK low | 2 | — | ns |

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.17 UART I/O Configuration and Timing Parameters**4.7.17.1 UART RS-232 I/O Configuration in Different Modes**

The i.MX53xD UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 — DCE mode). [Table 87](#) shows the UART I/O configuration based on the enabled mode.

Table 87. UART I/O Configuration vs. Mode

| Port | DTE Mode | | DCE Mode | |
|---------|-----------|-----------------------------|-----------|-----------------------------|
| | Direction | Description | Direction | Description |
| RTS | Output | RTS from DTE to DCE | Input | RTS from DTE to DCE |
| CTS | Input | CTS from DCE to DTE | Output | CTS from DCE to DTE |
| DTR | Output | DTR from DTE to DCE | Input | DTR from DTE to DCE |
| DSR | Input | DSR from DCE to DTE | Output | DSR from DCE to DTE |
| DCD | Input | DCD from DCE to DTE | Output | DCD from DCE to DTE |
| RI | Input | RING from DCE to DTE | Output | RING from DCE to DTE |
| TXD_MUX | Input | Serial data from DCE to DTE | Output | Serial data from DCE to DTE |
| RXD_MUX | Output | Serial data from DTE to DCE | Input | Serial data from DTE to DCE |

4.7.17.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.7.17.2.1 UART Transmitter

[Figure 85](#) depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. [Table 88](#) lists the UART RS-232 serial mode transmit timing characteristics.

Electrical Characteristics

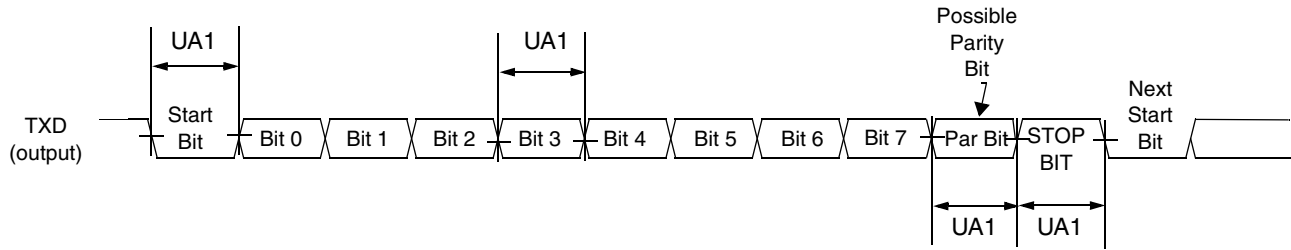


Figure 85. UART RS-232 Serial Mode Transmit Timing Diagram

Table 88. RS-232 Serial Mode Transmit Timing Parameters

| ID | Parameter | Symbol | Min | Max | Units |
|-----|-------------------|------------|---|---|-------|
| UA1 | Transmit Bit Time | t_{Tbit} | $\frac{1}{F_{baud_rate}} - \frac{1}{T_{ref_clk}}$ | $\frac{1}{F_{baud_rate}} + \frac{1}{T_{ref_clk}}$ | — |

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

4.7.17.2.2 UART Receiver

Figure 86 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 89 lists serial mode receive timing characteristics.

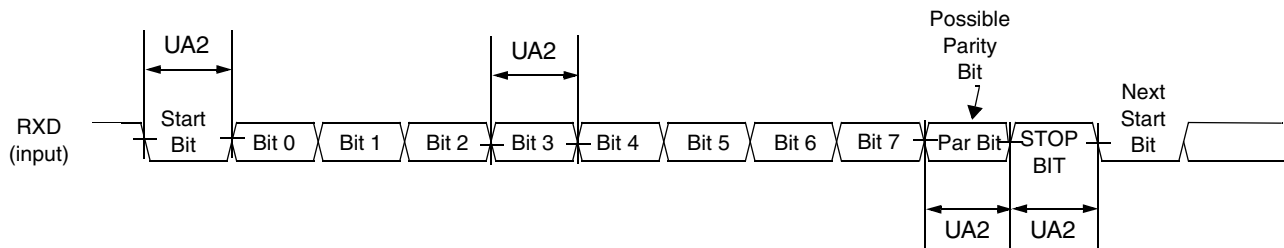


Figure 86. UART RS-232 Serial Mode Receive Timing Diagram

Table 89. RS-232 Serial Mode Receive Timing Parameters

| ID | Parameter | Symbol | Min | Max | Units |
|-----|-------------------------------|------------|---|---|-------|
| UA2 | Receive Bit Time ¹ | t_{Rbit} | $\frac{1}{F_{baud_rate}} - \frac{1}{(16 \times F_{baud_rate})}$ | $\frac{1}{F_{baud_rate}} + \frac{1}{(16 \times F_{baud_rate})}$ | — |

¹ The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

4.7.17.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.7.17.3.3 UART IrDA Mode Transmitter

Figure 87 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 90 lists the transmit timing characteristics.

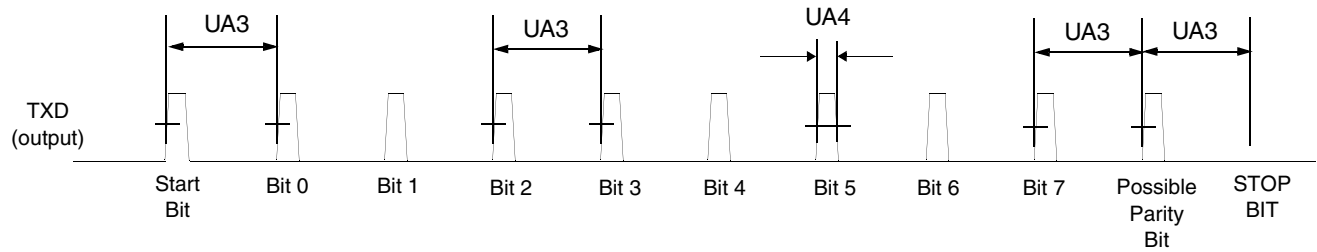


Figure 87. UART IrDA Mode Transmit Timing Diagram

Table 90. IrDA Mode Transmit Timing Parameters

| ID | Parameter | Symbol | Min | Max | Units |
|-----|--------------------------------|----------------|---|---|-------|
| UA3 | Transmit Bit Time in IrDA mode | t_{TIRbit} | $1/F_{baud_rate}^1 - T_{ref_clk}^2$ | $1/F_{baud_rate} + T_{ref_clk}$ | — |
| UA4 | Transmit IR Pulse Duration | $t_{TIRpulse}$ | $(3/16) \times (1/F_{baud_rate}) - T_{ref_clk}$ | $(3/16) \times (1/F_{baud_rate}) + T_{ref_clk}$ | — |

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

4.7.17.3.4 UART IrDA Mode Receiver

Figure 88 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 91 lists the receive timing characteristics.

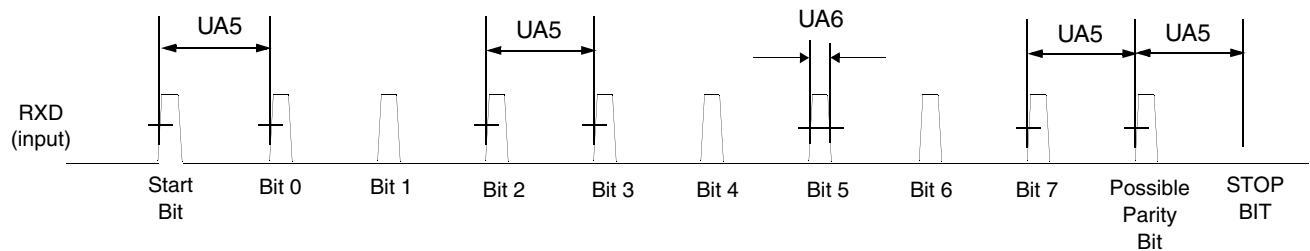


Figure 88. UART IrDA Mode Receive Timing Diagram

Table 91. IrDA Mode Receive Timing Parameters

| ID | Parameter | Symbol | Min | Max | Units |
|-----|--|----------------|---|---|-------|
| UA5 | Receive Bit Time ¹ in IrDA mode | t_{RIRbit} | $1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$ | $1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$ | — |
| UA6 | Receive IR Pulse Duration | $t_{RIRpulse}$ | 1.41 μ s | $(5/16) \times (1/F_{baud_rate})$ | — |

¹ The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

4.7.18 USB-OH-3 Parameters

This section describes the electrical parameters of the USB OTG port and USB HOST ports. For on-chip USB PHY parameters see [Section 4.7.19, “USB PHY Parameters.”](#)

4.7.18.1 Serial Interface

In order to support four serial different interfaces, the USB serial transceiver can be configured to operate in one of four modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

4.7.18.1.1 DAT_SE0 Bidirectional Mode

Table 92. Signal Definitions — DAT_SE0 Bidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|--|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out In | TX data when USB_TXOE_B is low Differential RX data when USB_TXOE_B is high |
| USB_SE0_VM | Out In | SE0 drive when USB_TXOE_B is low SE0 RX indicator when USB_TXOE_B is high |

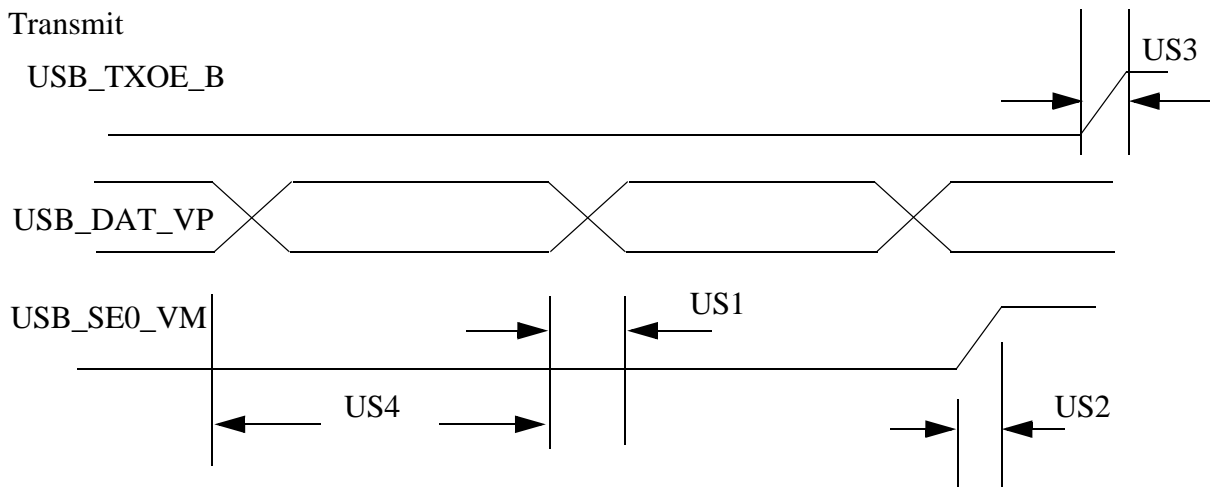


Figure 89. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

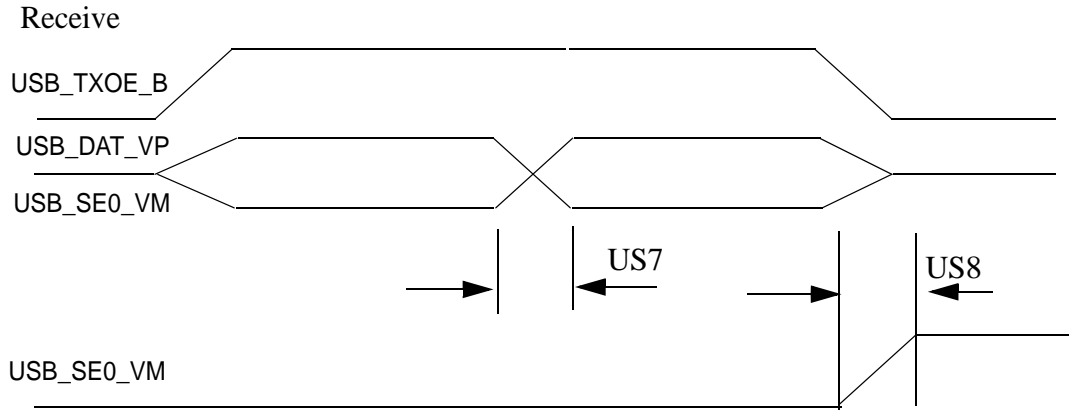


Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 93. Definitions of USB Waveform in DAT_SE0 Bi — Directional Mode

| No. | Parameter | Signal Name | Direction | Min | Max | Unit | Conditions / Reference Signal |
|-----|-------------------|-------------|-----------|------|------|------|-------------------------------|
| US1 | TX Rise/Fall Time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US2 | TX Rise/Fall Time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| US3 | TX Rise/Fall Time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| US4 | TX Duty Cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US7 | RX Rise/Fall Time | USB_DAT_VP | In | — | 3.0 | ns | 35 pF |
| US8 | RX Rise/Fall Time | USB_SE0_VM | In | — | 3.0 | ns | 35 pF |

4.7.18.1.2 DAT_SE0 Unidirectional Mode

Table 94. Signal Definitions — DAT_SE0 Unidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|---|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out | TX data when USB_TXOE_B is low |
| USB_SE0_VM | Out | SE0 drive when USB_TXOE_B is low |
| USB_VP1 | In | Buffered data on DP when USB_TXOE_B is high |
| USB_VM1 | In | Buffered data on DM when USB_TXOE_B is high |

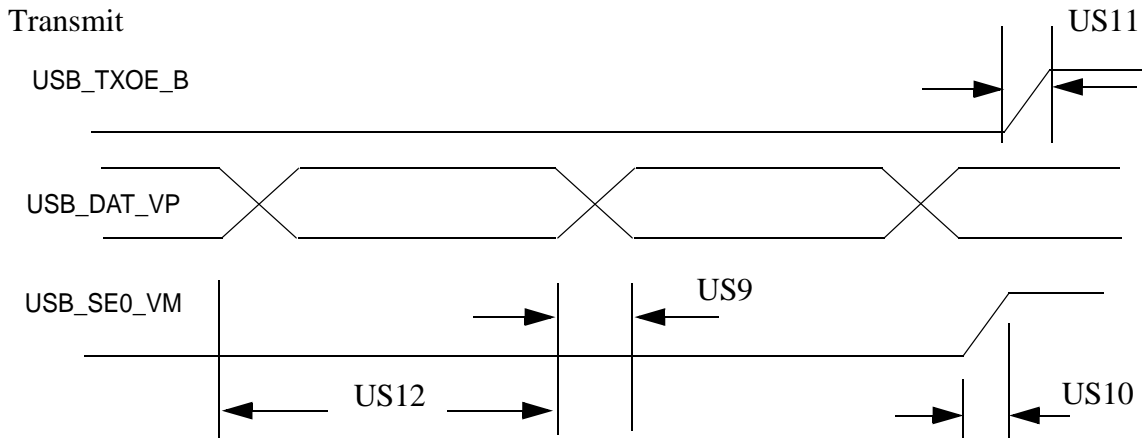


Figure 91. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

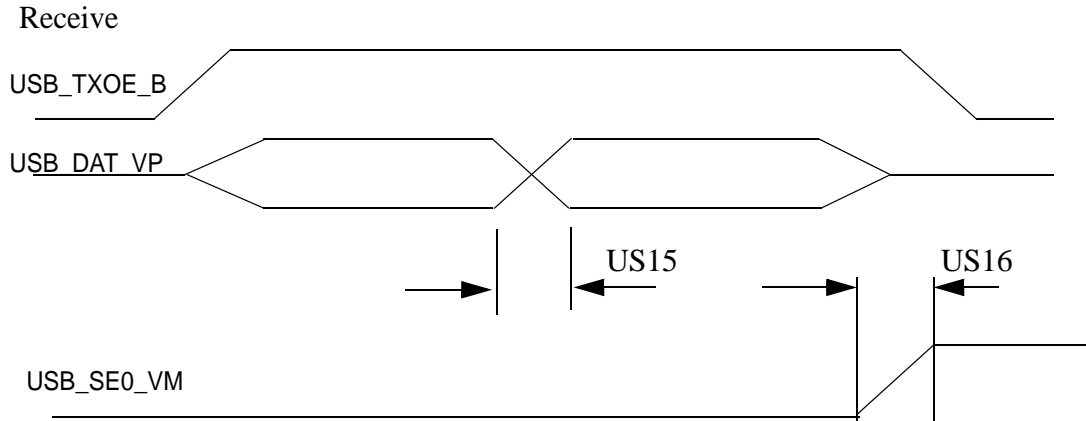


Figure 92. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 95. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

| No. | Parameter | Signal Name | Signal Source | Min | Max | Unit | Condition / Reference Signal |
|------|-------------------|-------------|---------------|------|------|------|------------------------------|
| US9 | TX Rise/Fall Time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US10 | TX Rise/Fall Time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| US11 | TX Rise/Fall Time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| US12 | TX Duty Cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US15 | RX Rise/Fall Time | USB_VP1 | In | — | 3.0 | ns | 35 pF |
| US16 | RX Rise/Fall Time | USB_VM1 | In | — | 3.0 | ns | 35 pF |

4.7.18.1.3 VP_VM Bidirectional Mode

Table 96. Signal Definitions — VP_VM Bidirectional Mode

| Name | Direction | Signal Description |
|------------|---------------------|---|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out (Tx) In (Rx) | TX VP data when USB_TXOE_B is low RX VP data when USB_TXOE_B is high |
| USB_SE0_VM | Out (Tx) In (Rx) | TX VM data when USB_TXOE_B low RX VM data when USB_TXOE_B high |

Transmit

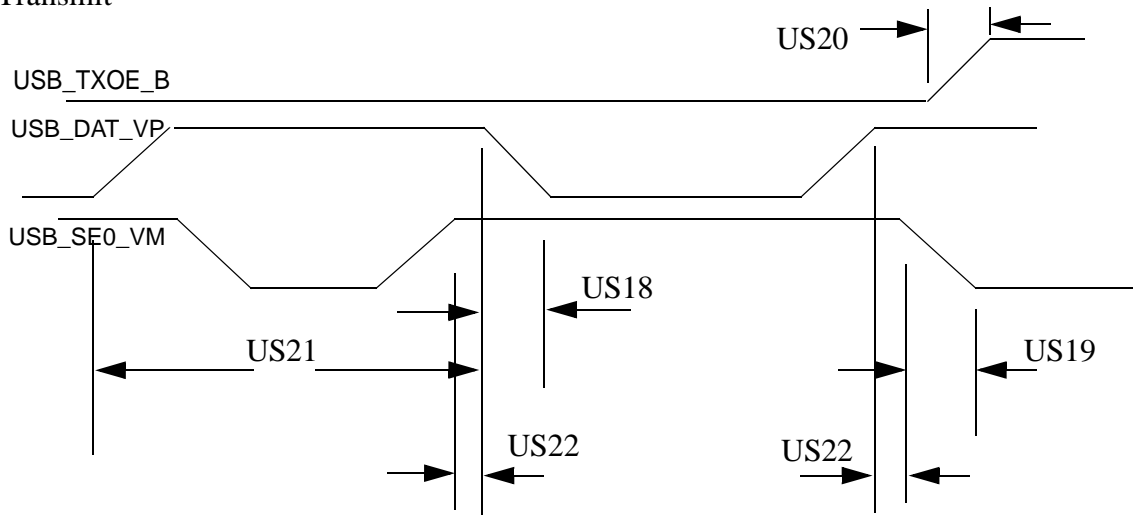


Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

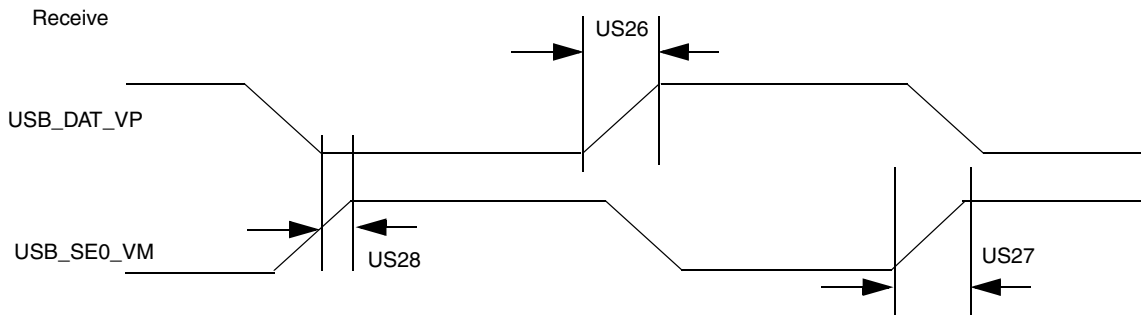


Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode

Table 97. USB Port Timing Specification in VP_VM Bidirectional Mode

| No. | Parameter | Signal Name | Direction | Min | Max | Unit | Condition / Reference Signal |
|------|-------------------|-------------|-----------|------|------|------|------------------------------|
| US18 | TX Rise/Fall Time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US19 | TX Rise/Fall Time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| US20 | TX Rise/Fall Time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| US21 | TX Duty Cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US22 | TX Overlap | USB_SE0_VM | Out | -3.0 | +3.0 | ns | USB_DAT_VP |
| US26 | RX Rise/Fall Time | USB_DAT_VP | In | — | 3.0 | ns | 35 pF |
| US27 | RX Rise/Fall Time | USB_SE0_VM | In | — | 3.0 | ns | 35 pF |
| US28 | RX Skew | USB_DAT_VP | In | -4.0 | +4.0 | ns | USB_SE0_VM |

4.7.18.1.4 VP_VM Unidirectional Mode

Table 98. Signal Definitions — VP_VM Unidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|------------------------------------|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out | TX VP data when USB_TXOE_B is low |
| USB_SE0_VM | Out | TX VM data when USB_TXOE_B is low |
| USB_VP1 | In | RX VP data when USB_TXOE_B is high |
| USB_VM1 | In | RX VM data when USB_TXOE_B is high |

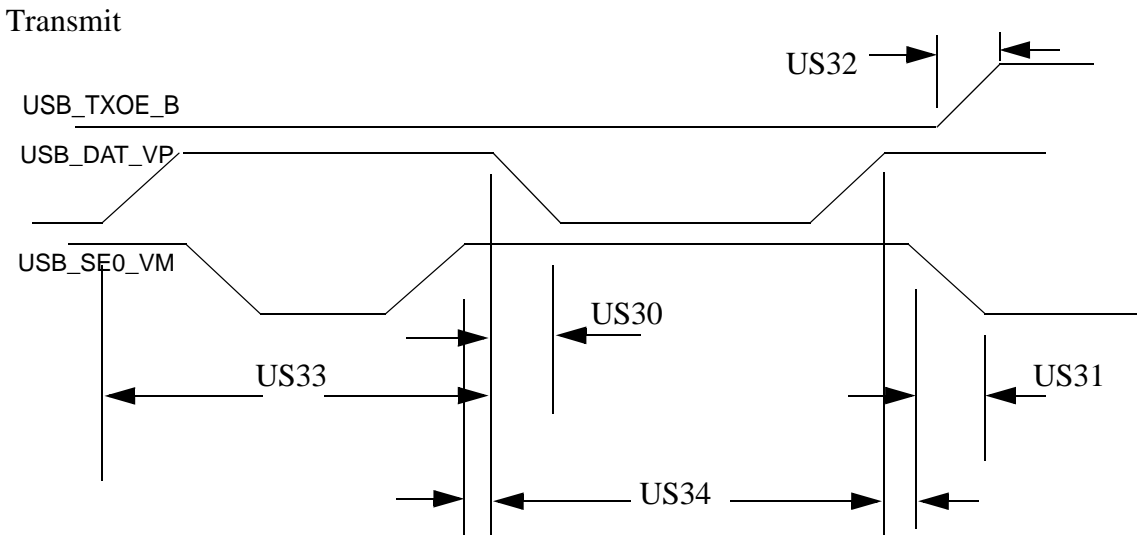


Figure 95. USB Transmit Waveform in VP_VM Unidirectional Mode

Receive

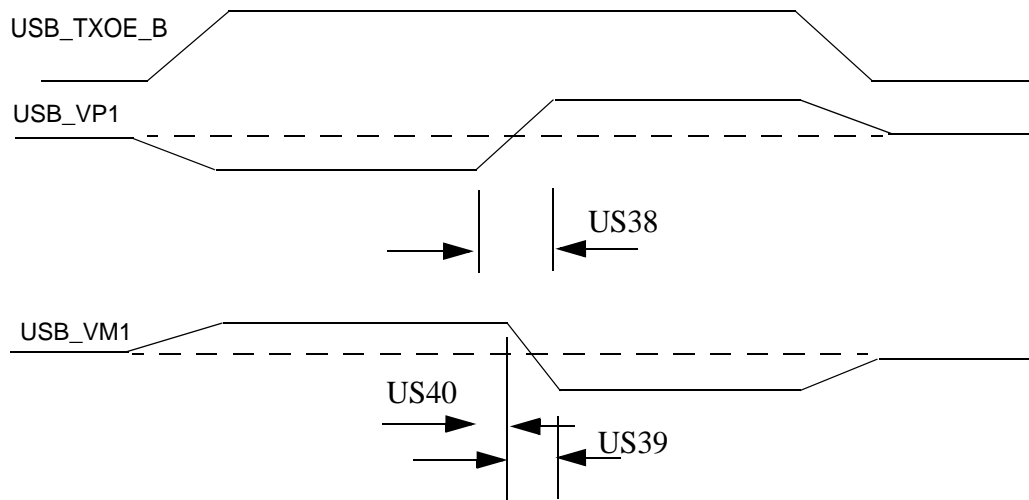


Figure 96. USB Receive Waveform in VP_VM Unidirectional Mode

Table 99. USB Timing Specification in VP_VM Unidirectional Mode

| No. | Parameter | Signal | Direction | Min | Max | Unit | Conditions / Reference Signal |
|------|-------------------|----------------|-----------|------|------|------|-------------------------------|
| US30 | TX Rise/Fall Time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US31 | TX Rise/Fall Time | USB_SE0_V M | Out | — | 5.0 | ns | 50 pF |
| US32 | TX Rise/Fall Time | USB_TXOE_ B | Out | — | 5.0 | ns | 50 pF |
| US33 | TX Duty Cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US34 | TX Overlap | USB_SE0_V M | Out | -3.0 | 3.0 | ns | USB_DAT_VP |
| US38 | RX Rise/Fall Time | USB_VP1 | In | — | 3.0 | ns | 35 pF |
| US39 | RX Rise/Fall Time | USB_VM1 | In | — | 3.0 | ns | 35 pF |
| US40 | RX Skew | USB_VP1 | In | -4.0 | +4.0 | ns | USB_VM1 |

4.7.18.2 Parallel Interface (Normal ULPI) Timing

Electrical and timing specifications of Parallel Interface (Normal ULPI) for Host Port2 and Port3 are presented in the subsequent sections.

Table 100. Signal Definitions — Parallel Interface (Normal ULPI)

| Name | Direction | Signal Description |
|---------------|-----------|--|
| USB_Clk | In | Interface clock. All interface signals are synchronous to Clock. |
| USB_Data[7:0] | I/O | Bi-directional data bus, driven low by the link during idle. Bus ownership is determined by Dir. |
| USB_Dir | In | Direction. Control the direction of the Data bus. |
| USB_Stp | Out | Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus. |
| USB_Nxt | In | Next. The PHY asserts this signal to throttle the data. |

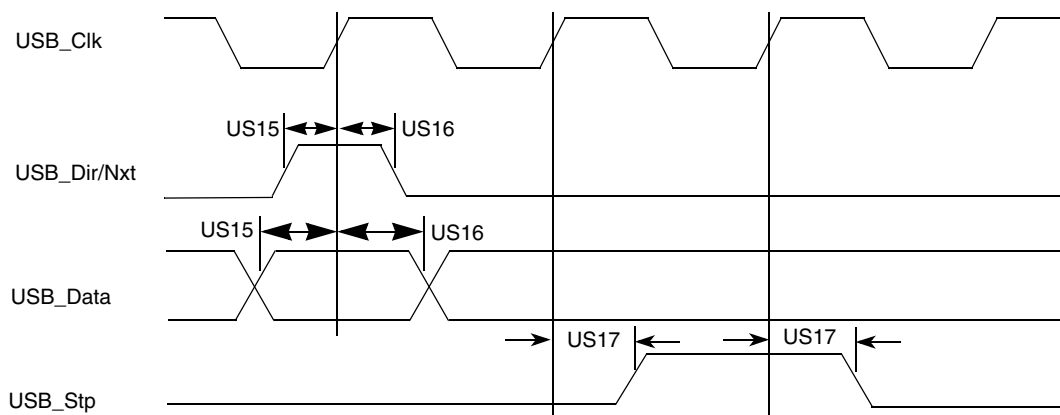


Figure 97. USB Transmit/Receive Waveform in Parallel Mode

Table 101. USB Timing Specification for Normal ULPI Mode

| ID | Parameter | Min | Max | Unit | Conditions / Reference Signal |
|------|---------------------------------------|-----|-----|------|-------------------------------|
| US15 | Setup Time (Dir&Nxt in, Data in) | 6.0 | — | ns | 10 pF |
| US16 | Hold Time (Dir&Nxt in, Data in) | 0.0 | — | ns | 10 pF |
| US17 | Output Delay Time (Stp out, Data out) | — | 9.0 | ns | 10 pF |

4.7.19 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

4.7.19.1 USB PHY AC Parameters

Table 102 lists the AC timing parameters for USB PHY.

Table 102. USB PHY AC Timing Parameters

| Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|------------|-----|-----|-----|------|
| trise | 1.5 Mbps | 75 | — | 300 | ns |
| | 12 Mbps | 4 | | 20 | |
| | 480 Mbps | 0.5 | | | |
| tfall | 1.5 Mbps | 75 | — | 300 | ns |
| | 12 Mbps | 4 | | 20 | |
| | 480 Mbps | 0.5 | | | |
| Jitter | 1.5 Mbps | — | — | 10 | ns |
| | 12 Mbps | | | 1 | |
| | 480 Mbps | | | 0.2 | |

4.7.19.2 USB PHY Additional Electrical Parameters

Table 103 lists the parameters for additional electrical characteristics for USB PHY.

Table 103. Additional Electrical Characteristics for USB PHY

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|-----------------------|--------------|-----|------------|------|
| Vcm DC (dc level measured at receiver connector) | HS Mode LS/FS Mode | -0.05 0.8 | — | 0.5 2.5 | V |
| Crossover Voltage | LS Mode FS Mode | 1.3 1.3 | — | 2 2 | V |
| Power supply ripple noise (analog 3.3 V) | < 160 MHz | -50 | 0 | 50 | mV |
| Power supply ripple noise (analog 2.5 V) | < 1.2 MHz | -10 | 0 | 10 | mV |
| | > 1.2 MHz | -50 | 0 | 50 | |
| Power supply ripple noise (Digital 1.2 V) | All conditions | -50 | 0 | 50 | mV |

4.7.19.3 USB PHY System Clocking (SYSCLK)

Table 104 lists the USB PHY system clocking parameters.

Table 104. USB PHY System Clocking Parameters

| Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|-------------------------------------|------|-----|-----|------|
| Clock deviation | Reference Clock frequency 24 MHz | -150 | — | 150 | ppm |
| Rise/fall time | — | — | — | 200 | ps |
| Jitter (peak-peak) | < 1.2 MHz | 0 | — | 50 | ps |
| Jitter (peak-peak) | > 1.2 MHz | 0 | — | 100 | ps |
| Duty-cycle | Reference Clock frequency 24 MHz | 40 | — | 60 | % |

4.7.19.4 USB PHY Voltage Thresholds

Table 105 lists the USB PHY voltage thresholds.

Table 105. VBUS Comparators Thresholds

| Parameter | Conditions | Min | Typ | Max | Unit |
|--|------------|-----|------|------|------|
| A-Device Session Valid | — | 0.8 | 1.4 | 2.0 | V |
| B-Device Session Valid | — | 0.8 | 1.4 | 4.0 | V |
| B-Device Session End | — | 0.2 | 0.45 | 0.8 | V |
| VBUS Valid Comparator Threshold ¹ | — | 4.4 | 4.6 | 4.75 | V |

¹ For VBUS maximum rating, see Table 4 on page 17

4.7.19.5 USB PHY Termination

USB driver impedance in FS and HS modes is $45\ \Omega \pm 10\%$ (steady state). No external resistors required.

4.8 XTAL Electrical Specifications

Table 106 shows the XTALOSC electrical specifications.

Table 107 shows the XTALOSC_32K electrical specifications.

Table 106. XTALOSC Electrical Specifications

| Parameter | Min | Typ | Max | Units |
|-----------|-----|-----|-----|-------|
| Frequency | 22 | 24 | 27 | MHz |

Table 107. XTALOSC_32K Electrical Specifications

| Parameter | Min | Typ | Max | Units |
|-----------|-----|--------------------------|-----|-------|
| Frequency | — | 32.768/32.0 ¹ | — | kHz |

¹ Recommended nominal frequency 32.768 kHz.

4.9 Integrated LDO Voltage Regulators Parameters

The PLL supplies VDD_DIG_PLL and VDD_ANA_PLL can be powered ON from internal LDO voltage regulator (default case). In this case VDD_REG is used as internal regulator's power source. The regulator's output can be used as a supply for other domains such as VDDA and VDDAL1.

Table 108 shows the VDD_DIG_PLL and VDD_ANA_PLL Integrated Voltage Regulators Parameters.

Table 108. LDO Voltage Regulators Electrical Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|---|--|------|-----|------|-------|
| VDD_DIG_PLL functional Voltage Range ¹ | V _{VID_DIG_PLL} | 1.15 | 1.2 | 1.3 | V |
| VDD_ANA_PLL functional Voltage Range ¹ | V _{VDD_ANA_PLL} | 1.7 | 1.8 | 1.95 | V |
| VDD_DIG_PLL and VDD_ANA_PLL accuracy | — | — | — | ±3 | % |
| VDD_DIG_PLL power-supply rejection ratio ² | — | — | -18 | — | dB |
| VDD_ANA_PLL power-supply rejection ratio ² | — | — | -15 | — | dB |
| Output current ³ | I _{VDD_DIG_PLL} + I _{VDD_ANA_PLL} | — | — | 125 | mA |

¹ VDD_DIG_PLL and VDD_ANA_PLL voltages are programmable, but should not be set outside the target functional range for proper PLL operation.

² The gain or attenuation from the input supply variation to the output of the LDO (by design).

³ The limitation is for sum of the VDD_DIG_PLL and VDD_ANA_PLL current.

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 109 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, please refer to the i.MX53xD Fuse Map document and Boot chapter in i.MX53 Reference Manual.

Table 109. Fuses and Associated Pins Used for Boot

| Pin | Direction at Reset | eFuse Name | Details |
|--------------|--------------------|------------|---------------------|
| BOOT_MODE[1] | Input | N/A | Boot Mode selection |
| BOOT_MODE[0] | Input | | |

Table 109. Fuses and Associated Pins Used for Boot (continued)

| Pin | Direction at Reset | eFuse Name | Details |
|----------|--------------------|----------------------------------|--|
| EIM_A22 | Input | BOOT_CFG1[7]/Test Mode Selection | Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0' . Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses. |
| EIM_A21 | Input | BOOT_CFG1[6]/Test Mode Selection | |
| EIM_A20 | Input | BOOT_CFG1[5]/Test Mode Selection | |
| EIM_A19 | Input | BOOT_CFG1[4] | |
| EIM_A18 | Input | BOOT_CFG1[3] | |
| EIM_A17 | Input | BOOT_CFG1[2] | |
| EIM_A16 | Input | BOOT_CFG1[1] | |
| EIM_LBA | Input | BOOT_CFG1[0] | |
| EIM_EB0 | Input | BOOT_CFG2[7] | |
| EIM_EB1 | Input | BOOT_CFG2[6] | |
| EIM_DA0 | Input | BOOT_CFG2[5] | |
| EIM_DA1 | Input | BOOT_CFG2[4] | |
| EIM_DA2 | Input | BOOT_CFG2[3] | |
| EIM_DA3 | Input | BOOT_CFG2[2] | |
| EIM_DA4 | Input | BOOT_CFG3[7] | |
| EIM_DA5 | Input | BOOT_CFG3[6] | |
| EIM_DA6 | Input | BOOT_CFG3[5] | |
| EIM_DA7 | Input | BOOT_CFG3[4] | |
| EIM_DA8 | Input | BOOT_CFG3[3] | |
| EIM_DA9 | Input | BOOT_CFG3[2] | |
| EIM_DA10 | Input | BOOT_CFG3[1] | |

5.2 Boot Devices Interfaces Allocation

Table 110 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface’s specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 110. Interfaces Allocation During Boot

| Interface | IP Instance | Allocated Pads During Boot | Comment |
|-----------|-------------|------------------------------------|-----------------------|
| SPI | CSPI | EIM_A25, EIM_D21, EIM_D22, EIM_D28 | Only SS1 is supported |
| SPI | ECSPI-1 | EIM_D[19:16] | Only SS1 is supported |
| SPI | ECSPI-2 | CSI_DAT[10:8], EIM_LBA | Only SS1 is supported |

Table 110. Interfaces Allocation During Boot (continued)

| Interface | IP Instance | Allocated Pads During Boot | Comment |
|------------|-------------|---|--|
| EIM | EIM | EIM | <ul style="list-style-type: none"> Lower 16-bit data bus A/D multiplexed or upper 16 bit data bus non multiplexed Only CS0 is supported. |
| NAND Flash | EXTMC | NAND | <ul style="list-style-type: none"> 8/16-bit NAND data can be muxed either over EIM data or PATA data Only CS0 is supported |
| SD/MMC | eSDHCv2-1 | PATA_DATA[11:8], SD1_DATA[3:0], SD1_CMD, SD1_CLK | 1, 4, or 8 bit |
| SD/MMC | eSDHCv2-2 | PATA_DATA[15:12], SD2_CLK, SD2_CMD, SD2_DATA[3:0] | 1, 4, or 8 bit |
| SD/MMC | eSDHCv3-3 | PATA_RESET_B, PATA_IORDY, PATA_DA_0, PATA_DATA[3:0], PATA_DATA[11:8] | 1, 4, or 8 bit |
| SD/MMC | eSDHCv2-4 | PATA_DA1, PATA_DA_2, PATA_DATA[7:4], PATA_DATA[15:12] | 1, 4, or 8 bit |
| I2C | I2C-1 | EIM_D21, EIM_D28 | — |
| I2C | I2C-2 | EIM_D16, EIM_EB2 | — |
| I2C | I2C-3 | EIM_D[18:17] | — |
| PATA | PATA | PATA_DIOW, PATA_DMACK, PATA_DMARQ, PATA_BUFFER_EN, PATA_INTRQ, PATA_DIOR, PATA_RESET_B, PATA_IORDY, PATA_DA_[2:0], PATA_CS_[1:0], PATA_DATA[15:0] | — |
| SATA | SATA_PHY | SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT, SATA_REFCLKM, SATA_REFCLKP | — |
| UART | UARTv2-1 | CSI0_DAT[11:10] | RXD/TXD only |
| UART | UARTv2-2 | PATA_DMARQ, PATA_BUFFER_EN | RXD/TXD only |
| UART | UARTv2-3 | EIM_D24, EIM_D25 | RXD/TXD only |
| UART | UARTv2-4 | CSI0_DAT[13:12] | RXD/TXD only |
| UART | UARTv2-5 | CSI0_DAT[15:14] | RXD/TXD only |
| USB | USB-OTG PHY | USB_H1_GPANAIO USB_H1_RREFEXT USB_H1_DP USB_H1_DN USB_H1_VBUS | — |

5.3 Power Setup During Boot

By default, VDD_DIG_PLL is driven from internal on-die 1.2 V linear regulator (LDO). In order to achieve the standard operating mode (see VDD_DIG_PLL on Table 7), LDO output to VDD_DIG_PLL should be configured by software by boot code after power-up to 1.3 V output. This is done by programming the PLL1P2_VREG bits.

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 19x19 mm Package Information

This section contains the outline drawing, signal assignment map, ground/power reference ID (by ball grid location) for the 19 × 19 mm, 0.8 mm pitch package.

6.1.1 Case TEPBGA-2, 19 x 19 mm, 0.8 mm Pitch, 23 x 23 Ball Matrix

Figure 98 shows the top view of the 19×19 mm package, Figure 99 shows the bottom view and the ball location (529 solder balls) of the 19×19 mm package, and Figure 100 shows the side view of the 19×19 mm package.

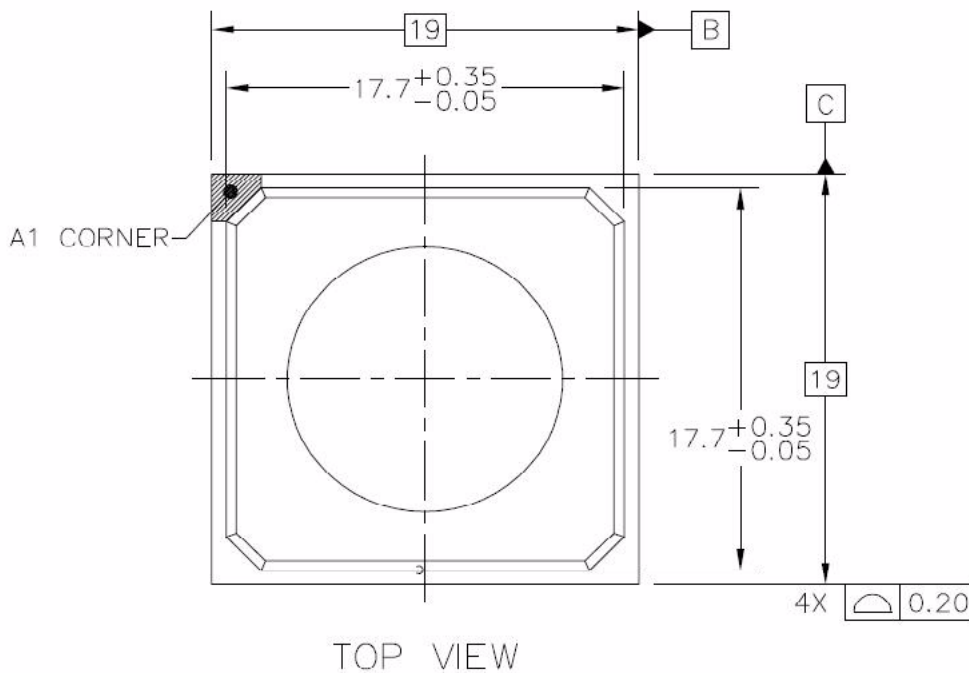
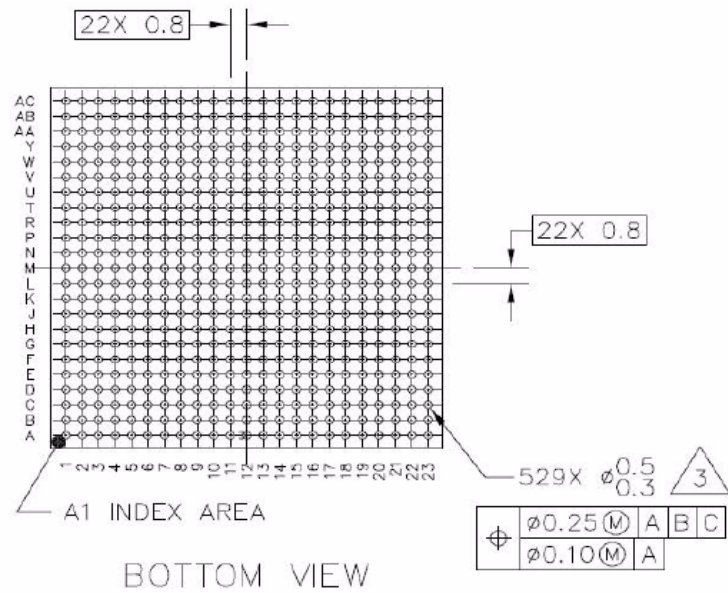
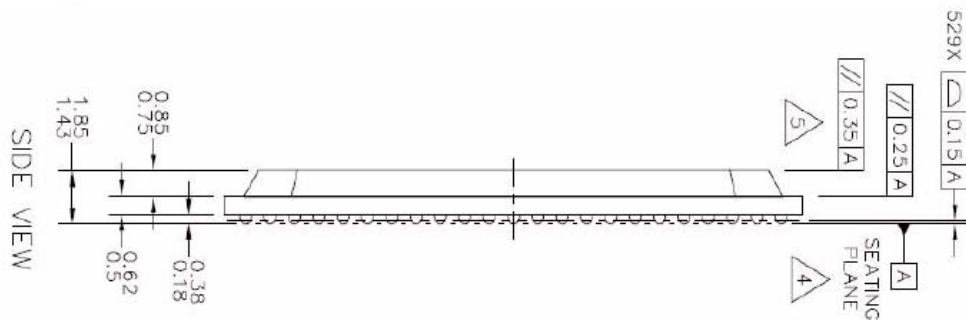


Figure 98. 19 x 19 mm Package Top View



$\triangle 3$. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

Figure 99. 19 x 19 mm Package, 529 Solder Balls, Bottom View



- $\triangle 4$. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- $\triangle 5$. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 100. 19 x 19 mm Package Side View

The following notes apply to [Figure 98](#), [Figure 99](#), and [Figure 100](#).

1. All dimensions are in millimeters.
2. Dimensions and tolerancing per ASME Y14.5M1–994.

6.1.2 19 x 19 mm Signal Assignments, Power Rails, and I/O

[Table 111](#) shows the device connection list for ground, power, sense, and reference contact signals.

[Table 112](#) displays an alpha-sorted list of the signal assignments including associated power supplies. The table also includes out of reset pad state. [Table 113](#) shows the package ball map.

6.1.2.1 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

[Table 111](#) shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 111. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

| Contact Name | Package Contact Assignment(s) |
|---------------|--|
| DDR_VREF | L17 |
| GND | A1, A11, A13, A18, A2, A22, A23, AA11, AA15, AA20, AA21, AB1, AB18, AB2, AB22, AB23, AC1, AC18, AC2, AC22, AC23, B1, B11, B13, B18, B23, C12, C20, C21, D19, E19, F19, F20, F21, F22, G19, G7, H10, H12, H8, J11, J13, J15, J17, J20, J9, K10, K12, K14, K16, K21, K8, L11, L13, L15, L7, L9, M10, M12, M14, M16, M8, N11, N13, N15, N9, P10, P12, P14, P16, P21, P7, P8, R11, R13, R15, R17, R20, R9, T10, T14, T16, T8, U15, U19, V15, V18, V19, V20, V21, V22, W19, Y14, Y15, Y19 |
| NVCC_CKIH | G17 |
| NVCC_CSI | R7 |
| NVCC_EIM_MAIN | U10, U9 |
| NVCC_EIM_SEC | U7 |
| NVCC_EMI_DRAM | H18, K17, N17, P17, T18 |
| NVCC_FEC | F11 |
| NVCC_GPIO | F8 |
| NVCC_JTAG | G9 |
| NVCC_KEYPAD | F7 |
| NVCC_LCD | J6, J7 |
| NVCC_LVDS | U13 |
| NVCC_LVDS_BG | U14 |
| NVCC_NANDF | T12 |
| NVCC_PATA | N7 |
| NVCC_RESET | H16 |
| NVCC_SD1 | H15 |

Package Information and Contact Assignments

Table 111. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

| Contact Name | Package Contact Assignment(s) |
|----------------|--|
| NVCC_SD2 | H14 |
| NVCC_SRTC_POW | V11 |
| NVCC_XTAL | V12 |
| SVCC | B22 |
| SVDDGP | B2 |
| TVDAC_AHVDDRGB | U17, V16 |
| TVDAC_DHVDD | U16 |
| USB_H1_VDDA25 | F13 |
| USB_H1_VDDA33 | G13 |
| USB_OTG_VDDA25 | F14 |
| USB_OTG_VDDA33 | G14 |
| VCC | H13, J14, J16, K13, K15, L14, L16, M11, M13, M15, M9, N10, N12, N14, N16, N8, P11, P13, P15, P9, R10, R12, R14, R16, R8, T11, T13, T15, T17, T7, T9, U18, U8 |
| VDDA | G12, M17, M7, U12 |
| VDDAL1 | F9 |
| VDD_ANA_PLL | G16 |
| VDD_DIG_PLL | H17 |
| VDD_FUSE | G15 |
| VDDGP | G10, G11, G8, H11, H7, H9, J10, J12, J8, K11, K7, K9, L10, L12, L8 |
| VDD_REG | G18 |
| VP | A15, B15 |
| VPH | A9, B9 |

Table 112 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|--------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|------------------|-----------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| BOOT_MODE0 | C18 | NVCC_RESET | LVIO | ALT0 | SRC | src_BOOT_MODE[0] | Input | 100 K Ω PD |
| BOOT_MODE1 | B20 | NVCC_RESET | LVIO | ALT0 | SRC | src_BOOT_MODE[1] | Input | 100 K Ω PD |
| CKIH1 | B21 | NVCC_CKIH | ANALOG | ALT0 | CAMP-1 | camp1_CKIH | Input | Analog |
| CKIH2 | D18 | NVCC_CKIH | ANALOG | ALT0 | CAMP-2 | camp2_CKIH | Input | Analog |
| CKIL | AB10 | NVCC_SRTC_POW | ANALOG | — | SRCT | CKIL | — | — |
| CSI0_DAT10 | R5 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[28] | Input | 100 K Ω PU |
| CSI0_DAT11 | T2 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[29] | Input | 100 K Ω PU |
| CSI0_DAT12 | T3 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[30] | Input | 360 K Ω PD |
| CSI0_DAT13 | T6 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[31] | Input | 360 K Ω PD |
| CSI0_DAT14 | U1 | NVCC_CSI | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[0] | Input | 360 K Ω PD |
| CSI0_DAT15 | U2 | NVCC_CSI | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[1] | Input | 360 K Ω PD |
| CSI0_DAT16 | T4 | NVCC_CSI | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[2] | Input | 360 K Ω PD |
| CSI0_DAT17 | T5 | NVCC_CSI | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[3] | Input | 360 K Ω PD |
| CSI0_DAT18 | U3 | NVCC_CSI | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[4] | Input | 360 K Ω PD |
| CSI0_DAT19 | U4 | NVCC_CSI | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[5] | Input | 360 K Ω PD |
| CSI0_DAT4 | R1 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[22] | Input | 100 K Ω PU |
| CSI0_DAT5 | R2 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[23] | Input | 360 K Ω PD |
| CSI0_DAT6 | R6 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[24] | Input | 100 K Ω PU |
| CSI0_DAT7 | R3 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[25] | Input | 100 K Ω PU |
| CSI0_DAT8 | T1 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[26] | Input | 100 K Ω PU |
| CSI0_DAT9 | R4 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[27] | Input | 360 K Ω PD |
| CSI0_DATA_EN | P3 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[20] | Input | 100 K Ω PU |
| CSI0_MCLK | P2 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[19] | Input | 100 K Ω PU |
| CSI0_PIXCLK | P1 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[18] | Input | 100 K Ω PU |
| CSI0_VSYNC | P4 | NVCC_CSI | UHVIO | ALT1 | GPIO-5 | gpio5_GPIO[21] | Input | 100 K Ω PU |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|--------------|----------------------------|------------|-----------------|-------------------------------------|----------------|----------------|-----------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| DI0_DISP_CLK | H4 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[16] | Input | 100 K Ω PU |
| DI0_PIN15 | E4 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[17] | Input | 100 K Ω PU |
| DI0_PIN2 | D3 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[18] | Input | 100 K Ω PU |
| DI0_PIN3 | C2 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[19] | Input | 100 K Ω PU |
| DI0_PIN4 | D2 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[20] | Input | 100 K Ω PU |
| DISP0_DAT0 | J5 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[21] | Input | 100 K Ω PD |
| DISP0_DAT1 | J4 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[22] | Input | 100 K Ω PD |
| DISP0_DAT10 | G3 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[31] | Input | 100 K Ω PU |
| DISP0_DAT11 | H5 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[5] | Input | 100 K Ω PD |
| DISP0_DAT12 | H1 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[6] | Input | 100 K Ω PU |
| DISP0_DAT13 | E1 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[7] | Input | 100 K Ω PU |
| DISP0_DAT14 | F2 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[8] | Input | 100 K Ω PU |
| DISP0_DAT15 | F3 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[9] | Input | 100 K Ω PU |
| DISP0_DAT16 | D1 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[10] | Input | 100 K Ω PU |
| DISP0_DAT17 | F5 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[11] | Input | 100 K Ω PU |
| DISP0_DAT18 | G4 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[12] | Input | 100 K Ω PU |
| DISP0_DAT19 | G5 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[13] | Input | 100 K Ω PU |
| DISP0_DAT2 | H2 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[23] | Input | 100 K Ω PD |
| DISP0_DAT20 | F4 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[14] | Input | 100 K Ω PU |
| DISP0_DAT21 | C1 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[15] | Input | 100 K Ω PU |
| DISP0_DAT22 | E3 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[16] | Input | 100 K Ω PU |
| DISP0_DAT23 | C3 | NVCC_LCD | GPIO | ALT1 | GPIO-5 | gpio5_GPIO[17] | Input | 100 K Ω PU |
| DISP0_DAT3 | F1 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[24] | Input | 100 K Ω PD |
| DISP0_DAT4 | G2 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[25] | Input | 100 K Ω PD |
| DISP0_DAT5 | H3 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[26] | Input | 100 K Ω PD |
| DISP0_DAT6 | G1 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[27] | Input | 100 K Ω PD |
| DISP0_DAT7 | H6 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[28] | Input | 100 K Ω PD |
| DISP0_DAT8 | G6 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[29] | Input | 100 K Ω PU |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|------------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|---|-----------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| DISP0_DAT9 | E2 | NVCC_LCD | GPIO | ALT1 | GPIO-4 | gpio4_GPIO[30] | Input | 100 K Ω PU |
| DRAM_A0 | M19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[0] | Output | Low |
| DRAM_A1 | L21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[1] | Output | Low |
| DRAM_A10 | K19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[10] | Output | Low |
| DRAM_A11 | L22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[11] | Output | Low |
| DRAM_A12 | L20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[12] | Output | Low |
| DRAM_A13 | L23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[13] | Output | Low |
| DRAM_A14 | N18 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[14] | Output | Low |
| DRAM_A15 | M18 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[15] | Output | Low |
| DRAM_A2 | M20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[2] | Output | Low |
| DRAM_A3 | N20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[3] | Output | Low |
| DRAM_A4 | K20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[4] | Output | Low |
| DRAM_A5 | N21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[5] | Output | Low |
| DRAM_A6 | M22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[6] | Output | Low |
| DRAM_A7 | N22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[7] | Output | Low |
| DRAM_A8 | N23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[8] | Output | Low |
| DRAM_A9 | M21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_A[9] | Output | Low |
| DRAM_CALIBRATION | M23 | NVCC_EMI_DRAM | special | — | — | (used in DRAM driver calibration. See Special Signal Considerations {add xref} above) | Input | — |
| DRAM_CAS | L18 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_CAS | Output | High |
| DRAM_CS0 | K18 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_CS[0] | Output | High |
| DRAM_CS1 | P19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_CS[1] | Output | High |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|--------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|----------------|-----------|----------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| DRAM_D0 | H20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[0] | Output | High |
| DRAM_D1 | G21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[1] | Output | High |
| DRAM_D10 | E22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[10] | Output | High |
| DRAM_D11 | D20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[11] | Output | High |
| DRAM_D12 | E23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[12] | Output | High |
| DRAM_D13 | C23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[13] | Output | High |
| DRAM_D14 | F23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[14] | Output | High |
| DRAM_D15 | C22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[15] | Output | High |
| DRAM_D16 | U20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[16] | Output | High |
| DRAM_D17 | T21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[17] | Output | High |
| DRAM_D18 | U21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[18] | Output | High |
| DRAM_D19 | R21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[19] | Output | High |
| DRAM_D2 | J21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[2] | Output | High |
| DRAM_D20 | U23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[20] | Output | High |
| DRAM_D21 | R22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[21] | Output | High |
| DRAM_D22 | U22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[22] | Output | High |
| DRAM_D23 | R23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[23] | Output | High |
| DRAM_D24 | Y20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[24] | Output | High |
| DRAM_D25 | W21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[25] | Output | High |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|----------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|----------------------|-----------|----------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| DRAM_D26 | Y21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[26] | Output | High |
| DRAM_D27 | W22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[27] | Output | High |
| DRAM_D28 | AA23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[28] | Output | High |
| DRAM_D29 | V23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[29] | Output | High |
| DRAM_D3 | G20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[3] | Output | High |
| DRAM_D30 | AA22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[30] | Output | High |
| DRAM_D31 | W23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[31] | Output | High |
| DRAM_D4 | J23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[4] | Output | High |
| DRAM_D5 | G23 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[5] | Output | High |
| DRAM_D6 | J22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[6] | Output | High |
| DRAM_D7 | G22 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[7] | Output | High |
| DRAM_D8 | E21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[8] | Output | High |
| DRAM_D9 | D21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_D[9] | Output | High |
| DRAM_DQM0 | H21 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_DQ M[0] | Output | Low |
| DRAM_DQM1 | E20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_DQ M[1] | Output | Low |
| DRAM_DQM2 | T20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_DQ M[2] | Output | Low |
| DRAM_DQM3 | W20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_DQ M[3] | Output | Low |
| DRAM_RAS | J19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_RAS | Output | High |
| DRAM_RESE T | P18 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_RES ET | Output | Low |
| DRAM_SDBA 0 | R19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_SDB A[0] | Output | Low |
| DRAM_SDBA 1 | P20 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_SDB A[1] | Output | Low |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|-----------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|---------------------|-----------|----------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| DRAM_SDBA 2 | N19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_SDB A[2] | Output | Low |
| DRAM_SDCK E0 | H19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_SDC KE[0] | Output | Low |
| DRAM_SDCK E1 | T19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_SDC KE[1] | Output | Low |
| DRAM_SDCL K_0 | K23 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDC LK0 | Output | Floating |
| DRAM_SDCL K_0_B | K22 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDC LK0_B | Output | Floating |
| DRAM_SDCL K_1 | P22 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDC LK1 | Output | Floating |
| DRAM_SDCL K_1_B | P23 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDC LK1_B | Output | Floating |
| DRAM_SDOD T0 | J18 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_ODT [0] | Output | Low |
| DRAM_SDOD T1 | R18 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_ODT [1] | Output | Low |
| DRAM_SDQS 0 | H23 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDQ S[0] | Input | Low |
| DRAM_SDQS 0_B | H22 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDQ S_B[0] | Input | High |
| DRAM_SDQS 1 | D23 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDQ S[1] | Input | Low |
| DRAM_SDQS 1_B | D22 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDQ S_B[1] | Input | High |
| DRAM_SDQS 2 | T22 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDQ S[2] | Input | Low |
| DRAM_SDQS 2_B | T23 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDQ S_B[2] | Input | High |
| DRAM_SDQS 3 | Y22 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDQ S[3] | Input | Low |
| DRAM_SDQS 3_B | Y23 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | EXTMC | emi_DRAM_SDQ S_B[3] | Input | High |
| DRAM_SDWE | L19 | NVCC_EMI_DRAM | DDR3 | ALT0 | EXTMC | emi_DRAM_SD WE | Output | High |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|--------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|---|---------------------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| ECKIL | AC10 | NVCC_SRTC_POW | ANALOG | — | SRTC | ECKIL {no block I/O by this name in RM} | — | — |
| EIM_A16 | AA5 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[16] | Output ² | — |
| EIM_A17 | V7 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[17] | Output ² | — |
| EIM_A18 | AB3 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[18] | Output ² | — |
| EIM_A19 | W7 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[19] | Output ² | — |
| EIM_A20 | Y6 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[20] | Output ² | — |
| EIM_A21 | AA4 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[21] | Output ² | — |
| EIM_A22 | AA3 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[22] | Output ² | — |
| EIM_A23 | V6 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[23] | Output | — |
| EIM_A24 | Y5 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[24] | Output | — |
| EIM_A25 | W6 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_A[25] | Output | — |
| EIM_BCLK | W11 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_BCLK | Output | — |
| EIM_CS0 | W8 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_CS[0] | Output | — |
| EIM_CS1 | Y7 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_CS[1] | Output | — |
| EIM_D16 | U6 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[16] | Input | 100 K Ω PU |
| EIM_D17 | U5 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[17] | Input | 100 K Ω PU |
| EIM_D18 | V1 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[18] | Input | 100 K Ω PU |
| EIM_D19 | V2 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[19] | Input | 100 K Ω PU |
| EIM_D20 | W1 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[20] | Input | 100 K Ω PU |
| EIM_D21 | V3 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[21] | Input | 100 K Ω PU |
| EIM_D22 | W2 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[22] | Input | 360 K Ω PD |
| EIM_D23 | Y1 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[23] | Input | 100 K Ω PU |
| EIM_D24 | Y2 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[24] | Input | 100 K Ω PU |
| EIM_D25 | W3 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[25] | Input | 100 K Ω PU |
| EIM_D26 | V5 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[26] | Input | 100 K Ω PU |
| EIM_D27 | V4 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[27] | Input | 100 K Ω PU |
| EIM_D28 | AA1 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[28] | Input | 100 K Ω PU |
| EIM_D29 | AA2 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[29] | Input | 100 K Ω PU |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|--------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|---------------------|---------------------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| EIM_D30 | W4 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[30] | Input | 100 K Ω PU |
| EIM_D31 | W5 | NVCC_EIM_SEC | UHVIO | ALT1 | GPIO-3 | gpio3_GPIO[31] | Input | 360 K Ω PD |
| EIM_DA0 | Y8 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[0] | Input ² | 100 K Ω PU |
| EIM_DA1 | AC4 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[1] | Input ² | 100 K Ω PU |
| EIM_DA10 | AB7 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[10] | Input ² | 100 K Ω PU |
| EIM_DA11 | AC6 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[11] | Input | 100 K Ω PU |
| EIM_DA12 | V10 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[12] | Input | 100 K Ω PU |
| EIM_DA13 | AC7 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[13] | Input | 100 K Ω PU |
| EIM_DA14 | Y10 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[14] | Input | 100 K Ω PU |
| EIM_DA15 | AA9 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[15] | Input | 100 K Ω PU |
| EIM_DA2 | AA7 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[2] | Input ² | 100 K Ω PU |
| EIM_DA3 | W9 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[3] | Input ² | 100 K Ω PU |
| EIM_DA4 | AB6 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[4] | Input ² | 100 K Ω PU |
| EIM_DA5 | V9 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[5] | Input ² | 100 K Ω PU |
| EIM_DA6 | Y9 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[6] | Input ² | 100 K Ω PU |
| EIM_DA7 | AC5 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[7] | Input ² | 100 K Ω PU |
| EIM_DA8 | AA8 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[8] | Input ² | 100 K Ω PU |
| EIM_DA9 | W10 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_NAND_EIM_DA[9] | Input ² | 100 K Ω PU |
| EIM_EB0 | AC3 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_EB[0] | Output ² | — |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|--------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|---------------------------|---------------------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| EIM_EB1 | AB5 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_EB[1] | Output ² | — |
| EIM_EB2 | Y3 | NVCC_EIM_MAIN | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[30] | Input | 100 K Ω PU |
| EIM_EB3 | Y4 | NVCC_EIM_MAIN | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[31] | Input | 100 K Ω PU |
| EIM_LBA | AA6 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_LBA | Output ² | — |
| EIM_OE | V8 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_OE | Output | — |
| EIM_RW | AB4 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_RW | Output | — |
| EIM_WAIT | AB9 | NVCC_EIM_MAIN | UHVIO | ALT0 | EXTMC | emi_EIM_WAIT | Output | — |
| EXTAL | AB11 | NVCC_XTAL | ANALOG | — | EXTAL OSC | EXTAL | — | — |
| FASTR_ANA | E18 | NVCC_CKIH | ANALOG | — | — | (reserved, tie to ground) | — | — |
| FASTR_DIG | E17 | NVCC_CKIH | ANALOG | — | — | (reserved, tie to ground) | — | — |
| FEC_CRSDV | D11 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[25] | Input | 100 K Ω PU |
| FEC_MDC | E10 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[31] | Input | 100 K Ω PU |
| FEC_MDIO | D12 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[22] | Input | 100 K Ω PU |
| FEC_REF_CLK | E12 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[23] | Input | 100 K Ω PU |
| FEC_RX_ER | F12 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[24] | Input | 100 K Ω PU |
| FEC_RXD0 | C11 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[27] | Input | 100 K Ω PU |
| FEC_RXD1 | E11 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[26] | Input | 100 K Ω PU |
| FEC_TX_EN | C10 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[28] | Input | 360 K Ω PD |
| FEC_TXD0 | F10 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[30] | Input | 100 K Ω PU |
| FEC_TXD1 | D10 | NVCC_FEC | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[29] | Input | 100 K Ω PU |
| GPIO_0 | C8 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[0] | Input | 360 K Ω PD |
| GPIO_1 | B7 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[1] | Input | 360 K Ω PD |
| GPIO_10 | W16 | TVDAC_AHVDDRB | GPIO | ALT0 | GPIO-4 | gpio4_GPIO[0] | Input | 100 K Ω PU |
| GPIO_11 | V17 | TVDAC_AHVDDRB | GPIO | ALT0 | GPIO-4 | gpio4_GPIO[1] | Input | 100 K Ω PU |
| GPIO_12 | W17 | TVDAC_AHVDDRB | GPIO | ALT0 | GPIO-4 | gpio4_GPIO[2] | Input | 100 K Ω PU |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|--------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|----------------|--------------------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| GPIO_13 | AA18 | TVDAC_AHVDDRB | GPIO | ALT0 | GPIO-4 | gpio4_GPIO[3] | Input | 100 K Ω PU |
| GPIO_14 | W18 | TVDAC_AHVDDRB | GPIO | ALT0 | GPIO-4 | gpio4_GPIO[4] | Input | 100 K Ω PU |
| GPIO_16 | C6 | NVCC_GPIO | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[11] | Input | 360 K Ω PD |
| GPIO_17 | A3 | NVCC_GPIO | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[12] | Input | 360 K Ω PD |
| GPIO_18 | D7 | NVCC_GPIO | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[13] | Input | 360 K Ω PD |
| GPIO_19 | B4 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[5] | Input ³ | 100 K Ω PU |
| GPIO_2 | C7 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[2] | Input | 360 K Ω PD |
| GPIO_3 | A6 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[3] | Input | 360 K Ω PD |
| GPIO_4 | D8 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[4] | Input | 100 K Ω PU |
| GPIO_5 | A5 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[5] | Input | 360 K Ω PD |
| GPIO_6 | B6 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[6] | Input | 360 K Ω PD |
| GPIO_7 | A4 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[7] | Input | 360 K Ω PD |
| GPIO_8 | B5 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[8] | Input | 360 K Ω PD |
| GPIO_9 | E8 | NVCC_GPIO | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[9] | Input | 100 K Ω PU |
| JTAG_MOD | C9 | NVCC_JTAG | GPIO | ALT0 | SJC | sjc_MOD | Input | 100 K Ω PU |
| JTAG_TCK | D9 | NVCC_JTAG | GPIO | ALT0 | SJC | sjc_TCK | Input | 100 K Ω PD |
| JTAG_TDI | B8 | NVCC_JTAG | GPIO | ALT0 | SJC | sjc_TDI | Input | 47 K Ω PU |
| JTAG_TDO | A7 | NVCC_JTAG | GPIO | ALT0 | SJC | sjc_TDO | Input | Keeper |
| JTAG_TMS | A8 | NVCC_JTAG | GPIO | ALT0 | SJC | sjc_TMS | Input | 47 K Ω PU |
| JTAG_TRSTB | E9 | NVCC_JTAG | GPIO | ALT0 | SJC | sjc_TRSTB | Input | 47 K Ω PU |
| KEY_COL0 | C5 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[6] | Input ⁴ | 100 K Ω PU |
| KEY_COL1 | E7 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[8] | Input | 100 K Ω PU |
| KEY_COL2 | C4 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[10] | Input | 100 K Ω PU |
| KEY_COL3 | F6 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[12] | Input | 100 K Ω PU |
| KEY_COL4 | E5 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[14] | Input | 100 K Ω PU |
| KEY_ROW0 | B3 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[7] | Input | 360 K Ω PD |
| KEY_ROW1 | D6 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[9] | Input | 100 K Ω PU |
| KEY_ROW2 | D5 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[11] | Input | 100 K Ω PU |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|-----------------|----------------------------|--------------|-----------------|-------------------------------------|----------------|----------------|-----------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| KEY_ROW3 | D4 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[13] | Input | 100 K Ω PU |
| KEY_ROW4 | E6 | NVCC_KEYPAD | UHVIO | ALT1 | GPIO-4 | gpio4_GPIO[15] | Input | 360 K Ω PD |
| LVDS_BG_RE S | AA14 | NVCC_LVDS_BG | ANALOG | — | LDB | LVDS_BG_RES | — | — |
| LVDS0_CLK_ N | AB16 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[25] | Input | Floating |
| LVDS0_CLK_ P | AC16 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[24] | Input | Floating |
| LVDS0_TX0_ N | Y17 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[31] | Input | Floating |
| LVDS0_TX0_P | AA17 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[30] | Input | Floating |
| LVDS0_TX1_ N | AB17 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[29] | Input | Floating |
| LVDS0_TX1_P | AC17 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[28] | Input | Floating |
| LVDS0_TX2_ N | Y16 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[27] | Input | Floating |
| LVDS0_TX2_P | AA16 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[26] | Input | Floating |
| LVDS0_TX3_ N | AB15 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[23] | Input | Floating |
| LVDS0_TX3_P | AC15 | NVCC_LVDS | LVDS | ALT0 | GPIO-7 | gpio7_GPI[22] | Input | Floating |
| LVDS1_CLK_ N | AA13 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[27] | Input | Floating |
| LVDS1_CLK_ P | Y13 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[26] | Input | Floating |
| LVDS1_TX0_ N | AC14 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[31] | Input | Floating |
| LVDS1_TX0_P | AB14 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[30] | Input | Floating |
| LVDS1_TX1_ N | AC13 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[29] | Input | Floating |
| LVDS1_TX1_P | AB13 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[28] | Input | Floating |
| LVDS1_TX2_ N | AC12 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[25] | Input | Floating |
| LVDS1_TX2_P | AB12 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[24] | Input | Floating |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|----------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|----------------|-----------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| LVDS1_TX3_N | AA12 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[23] | Input | Floating |
| LVDS1_TX3_P | Y12 | NVCC_LVDS | LVDS | ALT0 | GPIO-6 | gpio6_GPI[22] | Input | Floating |
| NANDF_ALE | Y11 | NVCC_NANDF | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[8] | Input | 100 K Ω PU |
| NANDF_CLE | AA10 | NVCC_NANDF | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[7] | Input | 100 K Ω PU |
| NANDF_CS0 | W12 | NVCC_NANDF | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[11] | Input | 100 K Ω PU |
| NANDF_CS1 | V13 | NVCC_NANDF | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[14] | Input | 100 K Ω PU |
| NANDF_CS2 | V14 | NVCC_NANDF | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[15] | Input | 100 K Ω PU |
| NANDF_CS3 | W13 | NVCC_NANDF | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[16] | Input | 100 K Ω PU |
| NANDF_RB0 | U11 | NVCC_NANDF | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[10] | Input | 100 K Ω PU |
| NANDF_RE_B | AC8 | NVCC_EIM_MAIN | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[13] | Input | 100 K Ω PU |
| NANDF_WE_B | AB8 | NVCC_EIM_MAIN | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[12] | Input | 100 K Ω PU |
| NANDF_WP_B | AC9 | NVCC_NANDF | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[9] | Input | 100 K Ω PU |
| PATA_BUFFER_EN | K4 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[1] | Input | 100 K Ω PU |
| PATA_CS_0 | L5 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[9] | Input | 100 K Ω PU |
| PATA_CS_1 | L2 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[10] | Input | 100 K Ω PU |
| PATA_DA_0 | K6 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[6] | Input | 100 K Ω PU |
| PATA_DA_1 | L3 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[7] | Input | 100 K Ω PU |
| PATA_DA_2 | L4 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[8] | Input | 100 K Ω PU |
| PATA_DATA0 | L1 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[0] | Input | 100 K Ω PU |
| PATA_DATA1 | M1 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[1] | Input | 100 K Ω PU |
| PATA_DATA10 | N4 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[10] | Input | 100 K Ω PU |
| PATA_DATA11 | M6 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[11] | Input | 100 K Ω PU |
| PATA_DATA12 | N5 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[12] | Input | 100 K Ω PU |
| PATA_DATA13 | N6 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[13] | Input | 100 K Ω PU |
| PATA_DATA14 | P6 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[14] | Input | 100 K Ω PU |
| PATA_DATA15 | P5 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[15] | Input | 100 K Ω PU |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|---------------|----------------------------|---------------|-----------------|-------------------------------------|----------------|--------------------|-----------|-------------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| PATA_DATA2 | L6 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[2] | Input | 100 K Ω PU |
| PATA_DATA3 | M2 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[3] | Input | 100 K Ω PU |
| PATA_DATA4 | M3 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[4] | Input | 100 K Ω PU |
| PATA_DATA5 | M4 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[5] | Input | 100 K Ω PU |
| PATA_DATA6 | N1 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[6] | Input | 100 K Ω PU |
| PATA_DATA7 | M5 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[7] | Input | 100 K Ω PU |
| PATA_DATA8 | N2 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[8] | Input | 100 K Ω PU |
| PATA_DATA9 | N3 | NVCC_PATA | UHVIO | ALT1 | GPIO-2 | gpio2_GPIO[9] | Input | 100 K Ω PU |
| PATA_DIOR | K3 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[3] | Input | 100 K Ω PU |
| PATA_DIOW | J3 | NVCC_PATA | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[17] | Input | 100 K Ω PU |
| PATA_DMACK | J2 | NVCC_PATA | UHVIO | ALT1 | GPIO-6 | gpio6_GPIO[18] | Input | 100 K Ω PU |
| PATA_DMARQ | J1 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[0] | Input | 100 K Ω PU |
| PATA_INTRQ | K5 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[2] | Input | 100 K Ω PU |
| PATA_IORDY | K1 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[5] | Input | 100 K Ω PU |
| PATA_RESET_B | K2 | NVCC_PATA | UHVIO | ALT1 | GPIO-7 | gpio7_GPIO[4] | Input | 100 K Ω PU |
| PMIC_ON_REQ | W14 | NVCC_SRTC_POW | GPIO | ALT0 | SRTC | srtc_SRTCALAR M | Output | — |
| PMIC_STBY_REQ | W15 | NVCC_SRTC_POW | GPIO | ALT0 | CCM | ccm_PMIC_VSTBY_REQ | Output | — |
| POR_B | C19 | NVCC_RESET | LVIO | ALT0 | SRC | src_POR_B | Input | 100 K Ω PU |
| RESET_IN_B | A21 | NVCC_RESET | LVIO | ALT0 | SRC | src_RESET_B | Input | 100 K Ω PU |
| SATA_REFCLKM | A14 | VPH | ANALOG | — | SATA | SATA_REFCLKM | — | — |
| SATA_REFCLKP | B14 | VPH | ANALOG | — | SATA | SATA_REFCLKP | — | — |
| SATA_REXT | C13 | VPH | ANALOG | — | SATA | SATA_REXT | — | — |
| SATA_RXM | A12 | VPH | ANALOG | — | SATA | SATA_RXM | — | — |
| SATA_RXP | B12 | VPH | ANALOG | — | SATA | SATA_RXP | — | — |
| SATA_TXM | B10 | VPH | ANALOG | — | SATA | SATA_TXM | — | — |
| SATA_TXP | A10 | VPH | ANALOG | — | SATA | SATA_TXP | — | — |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|-----------------|----------------------------|------------------------------|-----------------|-------------------------------------|----------------|-----------------|-----------|----------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| SD1_CLK | E16 | NVCC_SD1 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[20] | Input | 100 KΩ PU |
| SD1_CMD | F18 | NVCC_SD1 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[18] | Input | 100 KΩ PU |
| SD1_DATA0 | A20 | NVCC_SD1 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[16] | Input | 100 KΩ PU |
| SD1_DATA1 | C17 | NVCC_SD1 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[17] | Input | 100 KΩ PU |
| SD1_DATA2 | F17 | NVCC_SD1 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[19] | Input | 100 KΩ PU |
| SD1_DATA3 | F16 | NVCC_SD1 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[21] | Input | 100 KΩ PU |
| SD2_CLK | E14 | NVCC_SD2 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[10] | Input | 100 KΩ PU |
| SD2_CMD | C15 | NVCC_SD2 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[11] | Input | 100 KΩ PU |
| SD2_DATA0 | D13 | NVCC_SD2 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[15] | Input | 100 KΩ PU |
| SD2_DATA1 | C14 | NVCC_SD2 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[14] | Input | 100 KΩ PU |
| SD2_DATA2 | D14 | NVCC_SD2 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[13] | Input | 100 KΩ PU |
| SD2_DATA3 | E13 | NVCC_SD2 | UHVIO | ALT1 | GPIO-1 | gpio1_GPIO[12] | Input | 100 KΩ PU |
| TEST_MODE | D17 | NVCC_RESET | LVIO | ALT0 | | tcu_TEST_MODE | Input | 100 KΩ PD |
| TVCDC_IJOB_BACK | AB19 | TVDAC_AHVDDRB | ANALOG | — | TVE | TVCDC_IJOB_BACK | — | — |
| TVCDC_IJOG_BACK | AC20 | TVDAC_AHVDDRB | ANALOG | — | TVE | TVCDC_IJOG_BACK | — | — |
| TVCDC_IJOR_BACK | AB21 | TVDAC_AHVDDRB | ANALOG | — | TVE | TVCDC_IJOR_BACK | — | — |
| TVDAC_COMP | AA19 | TVDAC_AHVDDRB | ANALOG | — | TVE | TVDAC_COMP | — | — |
| TVDAC_IJOB | AC19 | TVDAC_AHVDDRB | ANALOG | — | TVE | TVDAC_IJOB | — | — |
| TVDAC_IJOG | AB20 | TVDAC_AHVDDRB | ANALOG | — | TVE | TVDAC_IJOG | — | — |
| TVDAC_IJOR | AC21 | TVDAC_AHVDDRB | ANALOG | — | TVE | TVDAC_IJOR | — | — |
| TVDAC_VREF | Y18 | TVDAC_AHVDDRB | ANALOG | — | TVE | TVDAC_VREF | — | — |
| USB_H1_DN | B17 | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG50 | — | USB | USB_H1_DN | — | — |

Table 112. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | | |
|---------------------|----------------------------|-----------------------------------|-----------------|-------------------------------------|----------------|---------------------|-----------|----------------|
| | | | | Alt. Mode | Block Instance | Block I/O | Direction | Config./ Value |
| USB_H1_DP | A17 | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG50 | — | USB | USB_H1_DP | — | — |
| USB_H1_GPA NAIO | A16 | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG25 | — | USB | USB_H1_GPANA IO | — | — |
| USB_H1_RRE FEXT | B16 | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG25 | — | USB | USB_H1_RREFE XT | — | — |
| USB_H1_VBU S | D15 | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG50 | — | USB | USB_H1_VBUS | — | — |
| USB_OTG_D N | A19 | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG50 | — | USB | USB_OTG_DN | — | — |
| USB_OTG_DP | B19 | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG50 | — | USB | USB_OTG_DP | — | — |
| USB_OTG_G PANAIO | F15 | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG25 | — | USB | USB_OTG_GPA NAIO | — | — |
| USB_OTG_ID | C16 | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG25 | — | USB | USB_OTG_ID | — | — |
| USB_OTG_R REFEXT | D16 | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG25 | — | USB | USB_OTG_RRE FEXT | — | — |
| USB_OTG_VB US | E15 | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG50 | — | USB | USB_OTG_VBU S | — | — |
| XTAL | AC11 | NVCC_XTAL | ANALOG | — | XTALO SC | XTAL | — | — |

¹ The state immediately after reset and before ROM firmware or software has executed.

² During power-on reset, this port acts as input for fuse override. See [Section 5.1, “Boot Mode Configuration Pins”](#) for details. For appropriate resistor values, see Chapter 1 of *i.MX53 System Development User's Guide (MX53UG)*.

³ During power-on reset, this port acts as output for diagnostic signal INT_BOOT

⁴ During power-on reset, this port acts as output for diagnostic signal ANY_PU_RST

NOTE

KEY_COL0 and GPIO_19 act as output for diagnostic signals during power-on reset.

6.2 19 x 19 mm, 0.8 Pitch Ball Map

Table 113 shows the 19 × 19 mm, 0.8 pitch ball map.

Table 113. 19 x 19 mm, 0.8 Pitch Ball Map

| | E | D | C | B | A |
|----|--------------|-----------------|-------------|----------------|----------------|
| 1 | DISP0_DAT13 | DISP0_DAT16 | DISP0_DAT21 | GND | GND |
| 2 | DISP0_DAT9 | DIO_PIN4 | DIO_PIN3 | SVDDGP | GND |
| 3 | DISP0_DAT22 | DIO_PIN2 | DISP0_DAT23 | KEY_ROW0 | GPIO_17 |
| 4 | DIO_PIN15 | KEY_ROW3 | KEY_COL2 | GPIO_19 | GPIO_7 |
| 5 | KEY_COL4 | KEY_ROW2 | KEY_COLO | GPIO_8 | GPIO_5 |
| 6 | KEY_ROW4 | KEY_ROW1 | GPIO_16 | GPIO_6 | GPIO_3 |
| 7 | KEY_COL1 | GPIO_18 | GPIO_2 | GPIO_1 | JTAG_TDO |
| 8 | GPIO_9 | GPIO_4 | GPIO_0 | JTAG_TDI | JTAG_TMS |
| 9 | JTAG_TRSTB | JTAG_TCK | JTAG_MOD | VPH | VPH |
| 10 | FEC_MDC | FEC_TXD1 | FEC_TX_EN | SATA_TXM | SATA_TXP |
| 11 | FEC_RXD1 | FEC_CRS_DV | FEC_RXD0 | GND | GND |
| 12 | FEC_REF_CLK | FEC_MDIO | GND | SATA_RXP | SATA_RXM |
| 13 | SD2_DATA3 | SD2_DATA0 | SATA_REXT | GND | GND |
| 14 | SD2_CLK | SD2_DATA2 | SD2_DATA1 | SATA_REFCLKP | SATA_REFCLKM |
| 15 | USB_OTG_VBUS | USB_H1_VBUS | SD2_CMD | VP | VP |
| 16 | SD1_CLK | USB_OTG_PREFEXT | USB_OTG_ID | USB_H1_RREFEXT | USB_H1_GPANAIO |
| 17 | FASTR_DIG | TEST_MODE | SD1_DATA1 | USB_H1_DN | USB_H1_DP |
| 18 | FASTR_ANA | CKIH2 | BOOT_MODE0 | GND | GND |
| 19 | GND | GND | POR_B | USB_OTG_DP | USB_OTG_DN |
| 20 | DRAM_DQM1 | DRAM_D11 | GND | BOOT_MODE1 | SD1_DATA0 |
| 21 | DRAM_D8 | DRAM_D9 | GND | CKIH1 | RESET_IN_B |
| 22 | DRAM_D10 | DRAM_SDQS1_B | DRAM_D15 | SVCC | GND |
| 23 | DRAM_D12 | DRAM_SDQS1 | DRAM_D13 | GND | GND |
| | E | D | C | B | A |

Table 113. 19 x 19 mm, 0.8 Pitch Ball Map

| | L | K | J | H | G | F |
|----|------------|----------------|-------------|---------------|----------------|-----------------|
| 1 | PATA_DATA0 | PATA_IORDY | PATA_DMARQ | DISP0_DAT12 | DISP0_DAT6 | DISP0_DAT3 |
| 2 | PATA_CS_1 | PATA_RESET_B | PATA_DMACK | DISP0_DAT2 | DISP0_DAT4 | DISP0_DAT14 |
| 3 | PATA_DA_1 | PATA_DIOR | PATA_DIOW | DISP0_DAT5 | DISP0_DAT10 | DISP0_DAT15 |
| 4 | PATA_DA_2 | PATA_BUFFER_EN | DISP0_DAT1 | DIO_DISP_CLK | DISP0_DAT18 | DISP0_DAT20 |
| 5 | PATA_CS_0 | PATA_INTRQ | DISP0_DAT0 | DISP0_DAT11 | DISP0_DAT19 | DISP0_DAT17 |
| 6 | PATA_DATA2 | PATA_DA_0 | NVCC_LCD | DISP0_DAT7 | DISP0_DAT8 | KEY_COL3 |
| 7 | GND | VDDGP | NVCC_LCD | VDDGP | GND | NVCC_KEYPAD |
| 8 | VDDGP | GND | VDDGP | GND | VDDGP | NVCC_GPIO |
| 9 | GND | VDDGP | GND | VDDGP | NVCC_JTAG | VDDAL1 |
| 10 | VDDGP | GND | VDDGP | GND | VDDGP | FEC_TXD0 |
| 11 | GND | VDDGP | GND | VDDGP | VDDGP | NVCC_FEC |
| 12 | VDDGP | GND | VDDGP | GND | VDDA | FEC_RX_ER |
| 13 | GND | VCC | GND | VCC | USB_H1_VDDA33 | USB_H1_VDDA25 |
| 14 | VCC | GND | VCC | NVCC_SD2 | USB_OTG_VDDA33 | USB_OTG_VDDA25 |
| 15 | GND | VCC | GND | NVCC_SD1 | VDD_FUSE | USB_OTG_GPANAIO |
| 16 | VCC | GND | VCC | NVCC_RESET | VDD_ANA_PLL | SD1_DATA3 |
| 17 | DDR_VREF | NVCC_EMI_DRAM | GND | VDD_DIG_PLL | NVCC_CKIH | SD1_DATA2 |
| 18 | DRAM_CAS | DRAM_CS0 | DRAM_SDODT0 | NVCC_EMI_DRAM | VDD_REG | SD1_CMD |
| 19 | DRAM_SDWE | DRAM_A10 | DRAM_RAS | DRAM_SDCKE0 | GND | GND |
| 20 | DRAM_A12 | DRAM_A4 | GND | DRAM_D0 | DRAM_D3 | GND |
| 21 | DRAM_A1 | GND | DRAM_D2 | DRAM_DQM0 | DRAM_D1 | GND |
| 22 | DRAM_A11 | DRAM_SDCLK_0_B | DRAM_D6 | DRAM_SDQS0_B | DRAM_D7 | GND |
| 23 | DRAM_A13 | DRAM_SDCLK_0 | DRAM_D4 | DRAM_SDQS0 | DRAM_D5 | DRAM_D14 |
| | L | K | J | H | G | F |

Table 113. 19 x 19 mm, 0.8 Pitch Ball Map

| | U | T | R | P | N | M |
|----|----------------|---------------|-------------|----------------|---------------|------------------|
| 1 | CSIO_DAT14 | CSIO_DAT8 | CSIO_DAT4 | CSIO_PIXCLK | PATA_DATA6 | PATA_DATA1 |
| 2 | CSIO_DAT15 | CSIO_DAT11 | CSIO_DAT5 | CSIO_MCLK | PATA_DATA8 | PATA_DATA3 |
| 3 | CSIO_DAT18 | CSIO_DAT12 | CSIO_DAT7 | CSIO_DATA_EN | PATA_DATA9 | PATA_DATA4 |
| 4 | CSIO_DAT19 | CSIO_DAT16 | CSIO_DAT9 | CSIO_VSYNC | PATA_DATA10 | PATA_DATA5 |
| 5 | EIM_D17 | CSIO_DAT17 | CSIO_DAT10 | PATA_DATA15 | PATA_DATA12 | PATA_DATA7 |
| 6 | EIM_D16 | CSIO_DAT13 | CSIO_DAT6 | PATA_DATA14 | PATA_DATA13 | PATA_DATA11 |
| 7 | NVCC_EIM_SEC | VCC | NVCC_CSI | GND | NVCC_PATA | VDDA |
| 8 | VCC | GND | VCC | GND | VCC | GND |
| 9 | NVCC_EIM_MAIN | VCC | GND | VCC | GND | VCC |
| 10 | NVCC_EIM_MAIN | GND | VCC | GND | VCC | GND |
| 11 | NANDF_RB0 | VCC | GND | VCC | GND | VCC |
| 12 | VDDA | NVCC_NANDF | VCC | GND | VCC | GND |
| 13 | NVCC_LVDS | VCC | GND | VCC | GND | VCC |
| 14 | NVCC_LVDS_BG | GND | VCC | GND | VCC | GND |
| 15 | GND | VCC | GND | VCC | GND | VCC |
| 16 | TVDAC_DHVDD | GND | VCC | GND | VCC | GND |
| 17 | TVDAC_AHVDDRGB | VCC | GND | NVCC_EMI_DRAM | NVCC_EMI_DRAM | VDDA |
| 18 | VCC | NVCC_EMI_DRAM | DRAM_SDODT1 | DRAM_RESET | DRAM_A14 | DRAM_A15 |
| 19 | GND | DRAM_SDCKE1 | DRAM_SDBA0 | DRAM_CS1 | DRAM_SDBA2 | DRAM_A0 |
| 20 | DRAM_D16 | DRAM_DQM2 | GND | DRAM_SDBA1 | DRAM_A3 | DRAM_A2 |
| 21 | DRAM_D18 | DRAM_D17 | DRAM_D19 | GND | DRAM_A5 | DRAM_A9 |
| 22 | DRAM_D22 | DRAM_SDQS2 | DRAM_D21 | DRAM_SDCLK_1 | DRAM_A7 | DRAM_A6 |
| 23 | DRAM_D20 | DRAM_SDQS2_B | DRAM_D23 | DRAM_SDCLK_1_B | DRAM_A8 | DRAM_CALIBRATION |
| | U | T | R | P | N | M |

Table 113. 19 x 19 mm, 0.8 Pitch Ball Map

| | AC | AB | AA | Y | W | V |
|----|----------------|----------------|-------------|--------------|---------------|----------------|
| 1 | GND | GND | EIM_D28 | EIM_D23 | EIM_D20 | EIM_D18 |
| 2 | GND | GND | EIM_D29 | EIM_D24 | EIM_D22 | EIM_D19 |
| 3 | EIM_EB0 | EIM_A18 | EIM_A22 | EIM_EB2 | EIM_D25 | EIM_D21 |
| 4 | EIM_DA1 | EIM_RW | EIM_A21 | EIM_EB3 | EIM_D30 | EIM_D27 |
| 5 | EIM_DA7 | EIM_EB1 | EIM_A16 | EIM_A24 | EIM_D31 | EIM_D26 |
| 6 | EIM_DA11 | EIM_DA4 | EIM_LBA | EIM_A20 | EIM_A25 | EIM_A23 |
| 7 | EIM_DA13 | EIM_DA10 | EIM_DA2 | EIM_CS1 | EIM_A19 | EIM_A17 |
| 8 | NANDF_RE_B | NANDF_WE_B | EIM_DA8 | EIM_DA0 | EIM_CS0 | EIM_OE |
| 9 | NANDF_WP_B | EIM_WAIT | EIM_DA15 | EIM_DA6 | EIM_DA3 | EIM_DA5 |
| 10 | ECKIL | CKIL | NANDF_CLE | EIM_DA14 | EIM_DA9 | EIM_DA12 |
| 11 | XTAL | EXTAL | GND | NANDF_ALE | EIM_BCLK | NVCC_SRTC_POW |
| 12 | LVDS1_TX2_N | LVDS1_TX2_P | LVDS1_TX3_N | LVDS1_TX3_P | NANDF_CS0 | NVCC_XTAL |
| 13 | LVDS1_TX1_N | LVDS1_TX1_P | LVDS1_CLK_N | LVDS1_CLK_P | NANDF_CS3 | NANDF_CS1 |
| 14 | LVDS1_TX0_N | LVDS1_TX0_P | LVDS_BG_RES | GND | PMIC_ON_REQ | NANDF_CS2 |
| 15 | LVDS0_TX3_P | LVDS0_TX3_N | GND | GND | PMIC_STBY_REQ | GND |
| 16 | LVDS0_CLK_P | LVDS0_CLK_N | LVDS0_TX2_P | LVDS0_TX2_N | GPIO_10 | TVDAC_AHVDDRGB |
| 17 | LVDS0_TX1_P | LVDS0_TX1_N | LVDS0_TX0_P | LVDS0_TX0_N | GPIO_12 | GPIO_11 |
| 18 | GND | GND | GPIO_13 | TVDAC_VREF | GPIO_14 | GND |
| 19 | TVDAC_IOB | TVCDC_JOB_BACK | TVDAC_COMP | GND | GND | GND |
| 20 | TVCDC_I0G_BACK | TVDAC_I0G | GND | DRAM_D24 | DRAM_DQM3 | GND |
| 21 | TVDAC_I0R | TVCDC_I0R_BACK | GND | DRAM_D26 | DRAM_D25 | GND |
| 22 | GND | GND | DRAM_D30 | DRAM_SDQS3 | DRAM_D27 | GND |
| 23 | GND | GND | DRAM_D28 | DRAM_SDQS3_B | DRAM_D31 | DRAM_D29 |
| | AC | AB | AA | Y | W | V |

6.3 12 x 12 mm Package on Package (PoP) Information

This section contains the outline drawing, signal assignment map, ground/power reference ID (by ball grid location) for the 12 x 12 mm, 0.4 mm pitch PoP package.

6.3.1 Case PoP, 0.4 mm Pitch, 12 x 12 Ball Matrix

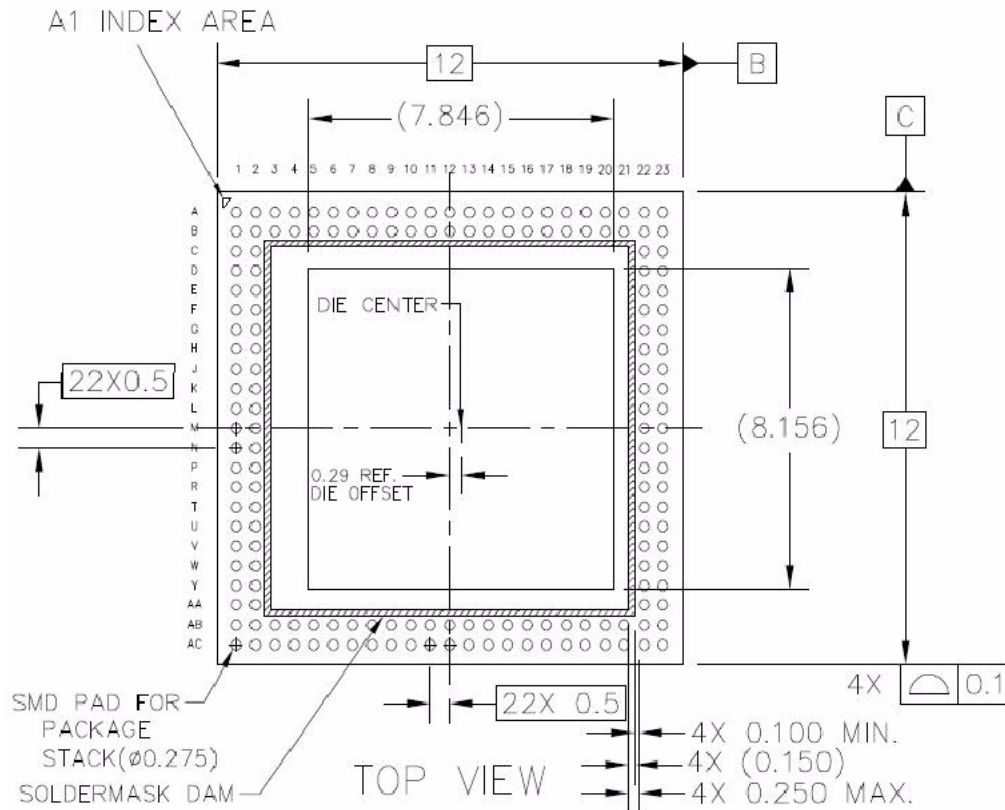
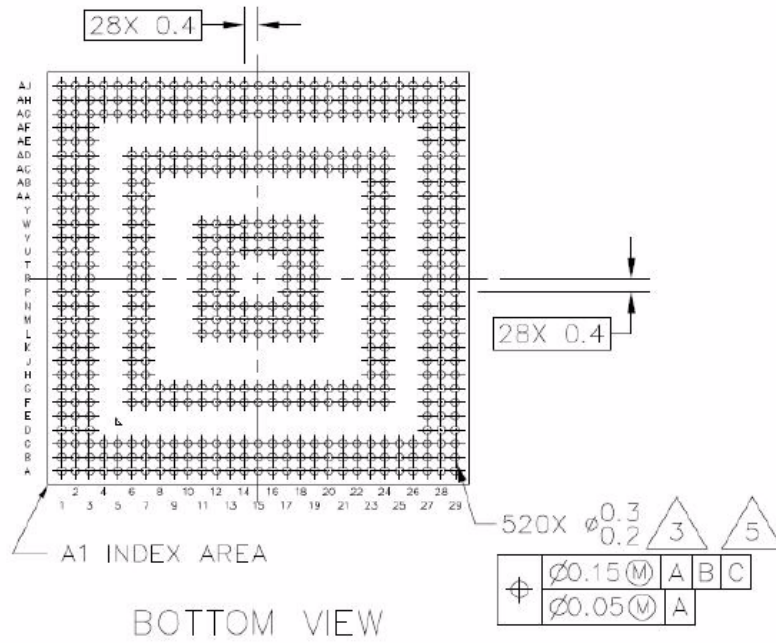


Figure 101. 12x12 mm PoP Top View



- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 5. REFLOW BALL DIAMETER.

Figure 102. 12 x 12 mm PoP, Bottom View

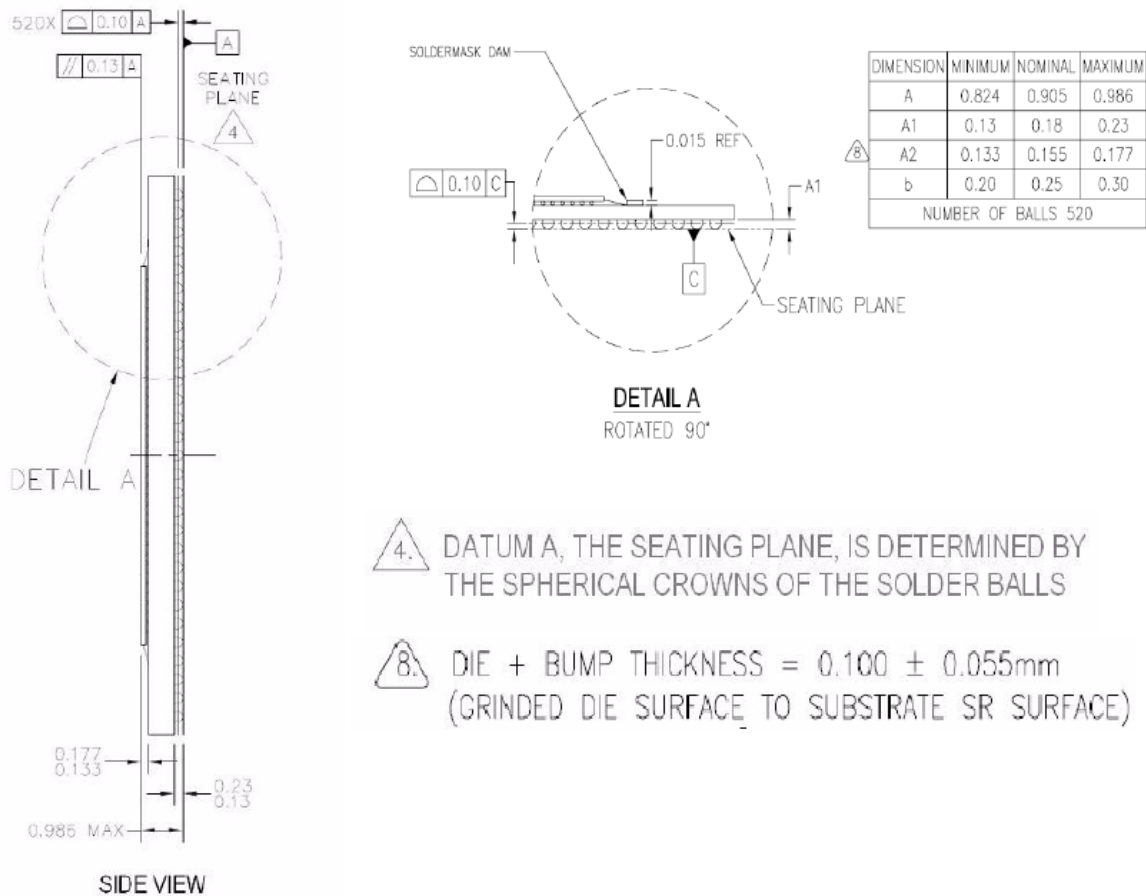


Figure 103. 12 x 12 mm PoP, Side View

The following notes apply to Figure 101, Figure 102, and Figure 103.

- 1 All dimensions are in millimeters.
- 2 Dimensions and tolerancing per ASME Y14.5M–1994.
- 3 Terminal position designation per JESD 95-1, SPP-010
- 4 Compliant to JESD 95-1 design guide 4.22, no exact variation, and with exception to dimension 'A'
- 5 Raw solder ball size during assembly is 0.25mm

6.3.2 12x 12 PoP Signal Assignments, Power Rails, and I/O

Table 114 and Table 115 show the device connection list for ground, power, sense, and reference contact signals.

Table 118 displays an alpha-sorted list of the signal assignments including associated power supplies. The table also includes out of reset pad state. Table 119 and Table 120 show the package ball maps.

6.3.2.1 12 x 12 mm PoP Ground, Power, Sense, and Reference Contact Assignments

Table 114 and Table 115 show the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 114. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments

| Contact Name | Contact Assignment |
|-------------------|--|
| DDR_VREF | U23 |
| GND | A1, A2, A28, A29, B1, B2, B28, B29, C17, L14, L15, L16, M14, M15, M16, N14, N15, N16, P11, P12, P13, P17, P18, P19, R11, R12, R13, R17, R18, R19, T11, T12, T13, T17, T18, T19, U14, U15, U16, V14, V15, V16, W14, W15, W16, AH1, AH15, AH29, AJ1, AJ2, AJ15, AJ28, AJ29 |
| NVCC_CKIH | AD22 |
| NVCC_CSI | J6 |
| NVCC_EIM_MAIN | G9 |
| NVCC_EIM_SEC | G6 |
| NVCC_EMI_DRAM | F24, G24, H24, K24, L24, N24, P24, R24, U24, V24, W24, AC24, AD24 |
| NVCC_EMI_DRAM_2P5 | K23, Y24 |
| NVCC_FEC | AC14 |
| NVCC_GPIO | AD9 |
| NVCC_JTAG | AD11 |
| NVCC_KEYPAD | AD6 |
| NVCC_LCD | W7, Y7 |
| NVCC_LVDS | F19 |
| NVCC_LVDS_BG | F18 |
| NVCC_NANDF | G12 |
| NVCC_PATA | N6 |
| NVCC_RESET | AD18 |
| NVCC_SD1 | AC20 |
| NVCC_SD2 | AC16 |
| NVCC_SRTC_POW | F13 |
| NVCC_XTAL | F14 |
| POP_VACC | AG14 |
| POP_VCCMM | C8, L3 |
| POP_VCCQMM | C11 |
| POP_VCCQMM1 | H3 |
| POP_VDD1 | C3, C13, C26, T3, T27, AG6, AG26 |

Package Information and Contact Assignments

Table 114. 12 x 12 mm PoP Bottom Ground, Power, Sense, and Reference Contact Assignments (continued)

| Contact Name | Contact Assignment |
|----------------|---|
| POP_VDD2 | C14, C27, D3, P27, W3, AF3, AG12, AG27 |
| POP_VDDCA | AA3, AD3, AG10 |
| POP_VDDMM | AG13 |
| POP_VDDQ | C16, C20, C24, E27, J27, N27, W27, AB27, AF27, AG16, AG20, AG24 |
| POP_ZQ | U3 |
| SVCC | AH28 |
| SVDDGP | AH2 |
| TVDAC_AHVDDRGB | G22, G23 |
| TVDAC_DHVDD | F23 |
| TVDAC_VREF | A27 |
| USB_H1_VDDA25 | AD19 |
| USB_H1_VDDA33 | AC18 |
| USB_OTG_VDDA25 | AC19 |
| USB_OTG_VDDA33 | AD20 |
| VCC | L11, L12, L13, L17, L18, L19, M11, M12, M13, M17, M18, M19, N11, N12, N13, N17, N18, N19, U17, U18, U19, V17, V18, V19, W17, W18, W19 |
| VDD_ANA_PLL | AC22 |
| VDD_DIG_PLL | AC23 |
| VDD_FUSE | AC21 |
| VDD_REG | AD23 |
| VDDA | F16, M6, R6, T24, AD14 |
| VDDAL1 | AC8 |
| VDDGP | U11, U12, U13, V11, V12, V13, W11, W12, W13 |
| VP | AH19, AJ19 |
| VPH | AH13, AJ13 |

Table 115. 12 x 12 mm PoP Top Ground, Power, Sense, and Reference Contact Assignments

| Contact Name | Contact Assignment |
|--------------|--|
| DDR_VREF | P2, M22 |
| GND | A12, A15, A18, A21, B5, B8, B10, C1, C23, F2, F23, J2, J23, M2, M23, P23, R1, U23, V1, Y23, AA1, AB7, AB11, AC5, AC9, AC12, AC15, AC18, AC21 |
| POP_VACC | AC11 |

Table 115. 12 x 12 mm PoP Top Ground, Power, Sense, and Reference Contact Assignments (continued)

| Contact Name | Contact Assignment |
|--------------|--|
| POP_VCCMM | A6, J1 |
| POP_VCCQMM | A9 |
| POP_VCCQMM1 | F1 |
| POP_VDD1 | A11, A20, B3, N2, N22, AB5, AC20 |
| POP_VDD2 | B11, B21, C2, L22, R2, AA2, AB10, AB21 |
| POP_VDDCA | U2, W2, AC8 |
| POP_VDDMM | AC10 |
| POP_VDDQ | B13, B16, B19, D22, G22, K22, R22, V22, AA22, AB13, AB16, AB19 |
| POP_ZQ | P1 |

6.3.2.2 PoP Memory Support and Signal Cross Reference

Support is provided for 8- and 16-bit MLC NAND Flash mounted on the top of the package. To ensure JESD209 compliance, dedicated PCB connections are required per [Table 116](#). With NAND flash selected as the boot source, NANDF_CLE and the EIM signals are configured as outputs. The PATA signals are configured as inputs with weak pull-ups (default) which allows the NANDF_CLE and the EIM signals to drive them. Note that the 16-bit NAND flash is on the EIM bus only.

EIM_DA[4:7] and EIM_DA[12:15] are assigned to top balls and require no PCB connections.

Table 116. Additional PCB connections for PoP NAND Flash

| Suggested PCB Net Name | First i.MX53 I/O on Net | Second i.MX53 I/O on Net | Associated Top Ball | Required for 8-bit NAND Flash? | Required for 16-bit NAND Flash? |
|------------------------|-------------------------|--------------------------|---------------------|--------------------------------|---------------------------------|
| NANDF_CLE | NANDF_CLE | PATA_DA_0 | PATA_DA_0 | Yes | Yes |
| NANDF_D0 | EIM_DA10 | PATA_DATA0 | PATA_DATA0 | Yes | Yes |
| NANDF_D1 | EIM_DA2 | PATA_DATA1 | PATA_DATA1 | Yes | Yes |
| NANDF_D2 | EIM_DA11 | PATA_DATA2 | PATA_DATA2 | Yes | Yes |
| NANDF_D3 | EIM_DA3 | PATA_DATA3 | PATA_DATA3 | Yes | Yes |
| NANDF_D8 | EIM_DA8 | PATA_DATA8 | PATA_DATA8 | No | Yes |
| NANDF_D9 | EIM_DA0 | PATA_DATA9 | PATA_DATA9 | No | Yes |
| NANDF_D10 | EIM_DA9 | PATA_DATA10 | PATA_DATA10 | No | Yes |
| NANDF_D11 | EIM_DA1 | PATA_DATA11 | PATA_DATA11 | No | Yes |

Package Information and Contact Assignments

To support eMMC per the JESD209 option, top ball signals per [Table 117](#) are provided. IOMUX mode ALT2 is invoked for these I/O.

Table 117. Additional Top Ball Connections for PoP eMMC

| eMMC Signal on Port eSDHC3 | Associated Top Ball |
|----------------------------|---------------------|
| RST | PATA_DAO |
| CLK | PATA_IORDY |
| CMD | PATA_RESETB |

i.MX53 PoP supports 16- and 32-bit LPDDR2-800 per JESD209 with no additional PCB digital signal connections. No signal cross reference is needed. The designer must ensure that the PCB routes power to POP_VDD1, POP_VDD2, POP_VDDQ, POP_VDDCA, POP_VACC, and POP_VCCQMM, POP_VCCMM, and POP_VDDMM. Appropriate discrete components must be employed for POP_ZQ, DRAM_CALIBRATION, DDR_VREF, and POP_VCCQMM1.

6.3.2.3 PoP 12 x 12 mm, Signal Assignments, Power Rails, and I/O

[Table 118](#) displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|--------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|------------------|-----------|-------------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| BOOT_MODE0 | AA28 | — | NVCC_RESET | LVIO | ALT0 | src_BOOT_MODE[0] | Input | 100 K Ω PD |
| BOOT_MODE1 | AB29 | — | NVCC_RESET | LVIO | ALT0 | src_BOOT_MODE[1] | Input | 100 K Ω PD |
| CKIH1 | AC29 | — | NVCC_CKIH | ANALOG | ALT0 | camp1_CKIH | Input | Analog |
| CKIH2 | AC28 | — | NVCC_CKIH | ANALOG | ALT0 | camp2_CKIH | Input | Analog |
| CKIL | G13 | — | NVCC_SRTC_POW | ANALOG | — | CKIL | — | — |
| CSI0_DAT10 | R2 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[28] | Input | 100 K Ω PU |
| CSI0_DAT11 | R7 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[29] | Input | 100 K Ω PU |
| CSI0_DAT12 | U1 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[30] | Input | 360 K Ω PD |
| CSI0_DAT13 | R1 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[31] | Input | 360 K Ω PD |
| CSI0_DAT14 | T1 | — | NVCC_CSI | UHVIO | ALT1 | gpio6_GPIO[0] | Input | 360 K Ω PD |
| CSI0_DAT15 | P1 | — | NVCC_CSI | UHVIO | ALT1 | gpio6_GPIO[1] | Input | 360 K Ω PD |
| CSI0_DAT16 | M1 | — | NVCC_CSI | UHVIO | ALT1 | gpio6_GPIO[2] | Input | 360 K Ω PD |
| CSI0_DAT17 | N1 | — | NVCC_CSI | UHVIO | ALT1 | gpio6_GPIO[3] | Input | 360 K Ω PD |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|--------------|---------------------------------------|------------------------------------|------------|-----------------|-------------------------------------|----------------|-----------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| CSI0_DAT18 | L2 | — | NVCC_CSI | UHVIO | ALT1 | gpio6_GPIO[4] | Input | 360 KΩ PD |
| CSI0_DAT19 | L1 | — | NVCC_CSI | UHVIO | ALT1 | gpio6_GPIO[5] | Input | 360 KΩ PD |
| CSI0_DAT4 | T7 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[22] | Input | 100 KΩ PU |
| CSI0_DAT5 | R3 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[23] | Input | 360 KΩ PD |
| CSI0_DAT6 | P7 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[24] | Input | 100 KΩ PU |
| CSI0_DAT7 | N7 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[25] | Input | 100 KΩ PU |
| CSI0_DAT8 | U2 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[26] | Input | 100 KΩ PU |
| CSI0_DAT9 | P3 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[27] | Input | 360 KΩ PD |
| CSI0_DATA_EN | P6 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[20] | Input | 100 KΩ PU |
| CSI0_MCLK | T6 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[19] | Input | 100 KΩ PU |
| CSI0_PIXCLK | U6 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[18] | Input | 100 KΩ PU |
| CSI0_VSYNC | U7 | — | NVCC_CSI | UHVIO | ALT1 | gpio5_GPIO[21] | Input | 100 KΩ PU |
| DI0_DISP_CLK | AF2 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[16] | Input | 100 KΩ PU |
| DI0_PIN15 | AH6 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[17] | Input | 100 KΩ PU |
| DI0_PIN2 | AD7 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[18] | Input | 100 KΩ PU |
| DI0_PIN3 | AC7 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[19] | Input | 100 KΩ PU |
| DI0_PIN4 | AC6 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[20] | Input | 100 KΩ PU |
| DISP0_DAT0 | AD1 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[21] | Input | 100 KΩ PD |
| DISP0_DAT1 | AC3 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[22] | Input | 100 KΩ PD |
| DISP0_DAT10 | AG2 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[31] | Input | 100 KΩ PU |
| DISP0_DAT11 | AE3 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[5] | Input | 100 KΩ PD |
| DISP0_DAT12 | AC1 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[6] | Input | 100 KΩ PU |
| DISP0_DAT13 | AH3 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[7] | Input | 100 KΩ PU |
| DISP0_DAT14 | AG3 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[8] | Input | 100 KΩ PU |
| DISP0_DAT15 | AH4 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[9] | Input | 100 KΩ PU |
| DISP0_DAT16 | AG5 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[10] | Input | 100 KΩ PU |
| DISP0_DAT17 | AB6 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[11] | Input | 100 KΩ PU |
| DISP0_DAT18 | AJ4 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[12] | Input | 100 KΩ PU |
| DISP0_DAT19 | AA7 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[13] | Input | 100 KΩ PU |
| DISP0_DAT2 | AC2 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[23] | Input | 100 KΩ PD |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|------------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|------------------|-----------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| DISP0_DAT20 | AJ5 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[14] | Input | 100 KΩ PU |
| DISP0_DAT21 | AB7 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[15] | Input | 100 KΩ PU |
| DISP0_DAT22 | AH5 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[16] | Input | 100 KΩ PU |
| DISP0_DAT23 | AJ6 | — | NVCC_LCD | GPIO | ALT1 | gpio5_GPIO[17] | Input | 100 KΩ PU |
| DISP0_DAT3 | AE2 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[24] | Input | 100 KΩ PD |
| DISP0_DAT4 | AF1 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[25] | Input | 100 KΩ PD |
| DISP0_DAT5 | AE1 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[26] | Input | 100 KΩ PD |
| DISP0_DAT6 | AD2 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[27] | Input | 100 KΩ PD |
| DISP0_DAT7 | AG1 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[28] | Input | 100 KΩ PD |
| DISP0_DAT8 | AG4 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[29] | Input | 100 KΩ PU |
| DISP0_DAT9 | AJ3 | — | NVCC_LCD | GPIO | ALT1 | gpio4_GPIO[30] | Input | 100 KΩ PU |
| DRAM_A0 | W23 | AC6 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[0] | Output | Low |
| DRAM_A1 | Y23 | AB6 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[1] | Output | Low |
| DRAM_A10 | M28 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[10] | Output | Low |
| DRAM_A11 | J29 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[11] | Output | Low |
| DRAM_A12 | L28 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[12] | Output | Low |
| DRAM_A13 | M27 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[13] | Output | Low |
| DRAM_A14 | L27 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[14] | Output | Low |
| DRAM_A15 | D27 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[15] | Output | Low |
| DRAM_A2 | V23 | AC7 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[2] | Output | Low |
| DRAM_A3 | L23 | AB8 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[3] | Output | Low |
| DRAM_A4 | AA24 | AB9 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[4] | Output | Low |
| DRAM_A5 | M23 | W1 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[5] | Output | Low |
| DRAM_A6 | P23 | V2 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[6] | Output | Low |
| DRAM_A7 | N23 | U1 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[7] | Output | Low |
| DRAM_A8 | M24 | T2 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[8] | Output | Low |
| DRAM_A9 | T23 | T1 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_A[9] | Output | Low |
| DRAM_CALIBRATION | R23 | — | NVCC_EMI_DRAM | CALIBRATION | | DRAM_CALIBRATION | Input | — |
| DRAM_CAS | AA23 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_CAS | Output | High |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|--------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|----------------|-----------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| DRAM_CS0 | AB23 | AB3 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_CS[0] | Output | High |
| DRAM_CS1 | J24 | AB4 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_CS[1] | Output | High |
| DRAM_D0 | T29 | W22 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[0] | Output | High |
| DRAM_D1 | V27 | AA23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[1] | Output | High |
| DRAM_D10 | AG22 | AC13 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[10] | Output | High |
| DRAM_D11 | AG29 | AC17 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[11] | Output | High |
| DRAM_D12 | AG23 | AB14 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[12] | Output | High |
| DRAM_D13 | AF29 | AB15 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[13] | Output | High |
| DRAM_D14 | AG28 | AB12 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[14] | Output | High |
| DRAM_D15 | AJ27 | AC16 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[15] | Output | High |
| DRAM_D16 | D29 | C22 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[16] | Output | High |
| DRAM_D17 | E29 | E23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[17] | Output | High |
| DRAM_D18 | D28 | D23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[18] | Output | High |
| DRAM_D19 | F28 | G23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[19] | Output | High |
| DRAM_D2 | R29 | U22 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[2] | Output | High |
| DRAM_D20 | F27 | F22 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[20] | Output | High |
| DRAM_D21 | G27 | H22 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[21] | Output | High |
| DRAM_D22 | E28 | E22 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[22] | Output | High |
| DRAM_D23 | F29 | H23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[23] | Output | High |
| DRAM_D24 | F21 | A17 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[24] | Output | High |
| DRAM_D25 | C19 | A14 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[25] | Output | High |
| DRAM_D26 | G21 | B17 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[26] | Output | High |
| DRAM_D27 | G18 | A13 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[27] | Output | High |
| DRAM_D28 | G20 | B15 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[28] | Output | High |
| DRAM_D29 | F17 | B12 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[29] | Output | High |
| DRAM_D3 | U27 | Y22 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[3] | Output | High |
| DRAM_D30 | F20 | A16 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[30] | Output | High |
| DRAM_D31 | G19 | B14 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[31] | Output | High |
| DRAM_D4 | R27 | T23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[4] | Output | High |
| DRAM_D5 | R28 | V23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[5] | Output | High |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|----------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|--------------------|-----------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| DRAM_D6 | P29 | T22 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[6] | Output | High |
| DRAM_D7 | T28 | W23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[7] | Output | High |
| DRAM_D8 | AF28 | AC14 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[8] | Output | High |
| DRAM_D9 | AE29 | AB17 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_D[9] | Output | High |
| DRAM_DQM0 | N28 | N23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_DQM[0] | Output | Low |
| DRAM_DQM1 | AD27 | AB20 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_DQM[1] | Output | Low |
| DRAM_DQM2 | H29 | L23 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_DQM[2] | Output | Low |
| DRAM_DQM3 | C23 | B20 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_DQM[3] | Output | Low |
| DRAM_RAS | M29 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_RAS | Output | High |
| DRAM_RESET | J28 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_RESET | Output | Low |
| DRAM_SDBA0 | H27 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_SDBA[0] | Output | Low |
| DRAM_SDBA1 | K27 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_SDBA[1] | Output | Low |
| DRAM_SDBA2 | K28 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_SDBA[2] | Output | Low |
| DRAM_SDCKE0 | AB24 | AC3 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_SDCKE[0] | Output | Low |
| DRAM_SDCKE1 | F22 | AC4 | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_SDCKE[1] | Output | Low |
| DRAM_SDCLK_1 | H23 | Y2 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDCLK_1 | Output | Floating |
| DRAM_SDCLK_1_B | J23 | Y1 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDCLK_1_B | Output | Floating |
| DRAM_SDODT_0 | L29 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_ODT[0] | Output | Low |
| DRAM_SDODT_1 | H28 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_ODT[1] | Output | Low |
| DRAM_SDQS0 | N29 | R23 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDQS[0] | Input | Low |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|--------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|--------------------|---------------------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| DRAM_SDQS0_B | P28 | P22 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDQS_B[0] | Input | High |
| DRAM_SDQS1 | AE28 | AB18 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDQS[1] | Input | Low |
| DRAM_SDQS1_B | AE27 | AC19 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDQS_B[1] | Input | High |
| DRAM_SDQS2 | G28 | J22 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDQS[2] | Input | Low |
| DRAM_SDQS2_B | G29 | K23 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDQS_B[2] | Input | High |
| DRAM_SDQS3 | C22 | B18 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDQS[3] | Input | Low |
| DRAM_SDQS3_B | C21 | A19 | NVCC_EMI_DRAM | DDR3CLK | ALT0 | emi_DRAM_SDQS_B[3] | Input | High |
| DRAM_SDWE | K29 | — | NVCC_EMI_DRAM | DDR3 | ALT0 | emi_DRAM_SDWE | Output | High |
| ECKIL | G14 | — | NVCC_SRTC_POW | ANALOG | | ECKIL | — | — |
| EIM_A16 | A7 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[16] | Output ₂ | — |
| EIM_A17 | G8 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[17] | Output ₂ | — |
| EIM_A18 | F8 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[18] | Output ₂ | — |
| EIM_A19 | A6 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[19] | Output ₂ | — |
| EIM_A20 | B7 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[20] | Output ₂ | — |
| EIM_A21 | C6 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[21] | Output ₂ | — |
| EIM_A22 | C2 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[22] | Output ₂ | — |
| EIM_A23 | B3 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[23] | Output | — |
| EIM_A24 | A4 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[24] | Output | — |
| EIM_A25 | A3 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_A[25] | Output | — |
| EIM_BCLK | F11 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_BCLK | Output | — |
| EIM_CS0 | G10 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_CS[0] | Output | — |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|--------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|----------------------|--------------------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| EIM_CS1 | C4 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_CS[1] | Output | — |
| EIM_D16 | H1 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[16] | Input | 100 KΩ PU |
| EIM_D17 | G3 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[17] | Input | 100 KΩ PU |
| EIM_D18 | H2 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[18] | Input | 100 KΩ PU |
| EIM_D19 | G2 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[19] | Input | 100 KΩ PU |
| EIM_D20 | M7 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[20] | Input | 100 KΩ PU |
| EIM_D21 | H6 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[21] | Input | 100 KΩ PU |
| EIM_D22 | G1 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[22] | Input | 360 KΩ PD |
| EIM_D23 | F1 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[23] | Input | 100 KΩ PU |
| EIM_D24 | F9 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[24] | Input | 100 KΩ PU |
| EIM_D25 | E1 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[25] | Input | 100 KΩ PU |
| EIM_D26 | D1 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[26] | Input | 100 KΩ PU |
| EIM_D27 | C10 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[27] | Input | 100 KΩ PU |
| EIM_D28 | D2 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[28] | Input | 100 KΩ PU |
| EIM_D29 | C7 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[29] | Input | 100 KΩ PU |
| EIM_D30 | C1 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[30] | Input | 100 KΩ PU |
| EIM_D31 | F7 | — | NVCC_EIM_SEC | UHVIO | ALT1 | gpio3_GPIO[31] | Input | 360 KΩ PD |
| EIM_DA0 | K1 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[0] | Input ² | 100 KΩ PU |
| EIM_DA1 | G11 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[1] | Input ² | 100 KΩ PU |
| EIM_DA10 | L7 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[10] | Input ² | 100 KΩ PU |
| EIM_DA11 | K7 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[11] | Input | 100 KΩ PU |
| EIM_DA12 | E2 | D1 | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[12] | Input | 100 KΩ PU |
| EIM_DA13 | F2 | E1 | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[13] | Input | 100 KΩ PU |
| EIM_DA14 | J2 | G1 | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[14] | Input | 100 KΩ PU |
| EIM_DA15 | K2 | H1 | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[15] | Input | 100 KΩ PU |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|--------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|---------------------|---------------------|-------------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| EIM_DA2 | F10 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[2] | Input ² | 100 K Ω PU |
| EIM_DA3 | A8 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[3] | Input ² | 100 K Ω PU |
| EIM_DA4 | E3 | D2 | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[4] | Input ² | 100 K Ω PU |
| EIM_DA5 | F3 | E2 | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[5] | Input ² | 100 K Ω PU |
| EIM_DA6 | J3 | G2 | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[6] | Input ² | 100 K Ω PU |
| EIM_DA7 | K3 | H2 | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[7] | Input ² | 100 K Ω PU |
| EIM_DA8 | A10 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[8] | Input ² | 100 K Ω PU |
| EIM_DA9 | K6 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_NAND_EIM_D A[9] | Input ² | 100 K Ω PU |
| EIM_EB0 | J1 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_EB[0] | Output ₂ | — |
| EIM_EB1 | G7 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_EB[1] | Output ₂ | — |
| EIM_EB2 | J7 | — | NVCC_EIM_MAIN | UHVIO | ALT1 | gpio2_GPIO[30] | Input | 100 K Ω PU |
| EIM_EB3 | F6 | — | NVCC_EIM_MAIN | UHVIO | ALT1 | gpio2_GPIO[31] | Input | 100 K Ω PU |
| EIM_LBA | A5 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_LBA | Output ₂ | — |
| EIM_OE | A9 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_OE | Output | — |
| EIM_RW | H7 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_RW | Output | — |
| EIM_WAIT | L6 | — | NVCC_EIM_MAIN | UHVIO | ALT0 | emi_EIM_WAIT | Output | — |
| EXTAL | G15 | — | NVCC_XTAL | ANALOG | — | EXTAL | — | — |
| FASTR_ANA | AD29 | — | NVCC_CKIH | ANALOG | — | FASTR_ANA | — | — |
| FASTR_DIG | AD28 | — | NVCC_CKIH | ANALOG | — | FASTR_DIG | — | — |
| FEC_CRD_DV | Y27 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[25] | Input | 100 K Ω PU |
| FEC_MDC | U28 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[31] | Input | 100 K Ω PU |
| FEC_MDIO | AA29 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[22] | Input | 100 K Ω PU |
| FEC_REF_CLK | Y29 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[23] | Input | 100 K Ω PU |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|--------------|---------------------------------------|------------------------------------|-----------------|-----------------|-------------------------------------|----------------|--------------------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| FEC_RX_ER | Y28 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[24] | Input | 100 KΩ PU |
| FEC_RXD0 | W28 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[27] | Input | 100 KΩ PU |
| FEC_RXD1 | W29 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[26] | Input | 100 KΩ PU |
| FEC_TX_EN | V29 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[28] | Input | 360 KΩ PD |
| FEC_TXD0 | U29 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[30] | Input | 100 KΩ PU |
| FEC_TXD1 | V28 | — | NVCC_FEC | UHVIO | ALT1 | gpio1_GPIO[29] | Input | 100 KΩ PU |
| GPIO_0 | AD12 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[0] | Input | 360 KΩ PD |
| GPIO_1 | AH12 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[1] | Input | 360 KΩ PD |
| GPIO_10 | B25 | — | TVDAC_AHVDDRG B | GPIO | ALT0 | gpio4_GPIO[0] | Input | 100 KΩ PU |
| GPIO_11 | B26 | — | TVDAC_AHVDDRG B | GPIO | ALT0 | gpio4_GPIO[1] | Input | 100 KΩ PU |
| GPIO_12 | A26 | — | TVDAC_AHVDDRG B | GPIO | ALT0 | gpio4_GPIO[2] | Input | 100 KΩ PU |
| GPIO_13 | C25 | — | TVDAC_AHVDDRG B | GPIO | ALT0 | gpio4_GPIO[3] | Input | 100 KΩ PU |
| GPIO_14 | B27 | — | TVDAC_AHVDDRG B | GPIO | ALT0 | gpio4_GPIO[4] | Input | 100 KΩ PU |
| GPIO_16 | AH10 | — | NVCC_GPIO | UHVIO | ALT1 | gpio7_GPIO[11] | Input | 360 KΩ PD |
| GPIO_17 | AC10 | — | NVCC_GPIO | UHVIO | ALT1 | gpio7_GPIO[12] | Input | 360 KΩ PD |
| GPIO_18 | AC9 | — | NVCC_GPIO | UHVIO | ALT1 | gpio7_GPIO[13] | Input | 360 KΩ PD |
| GPIO_19 | AJ10 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[5] | Input ³ | 100 KΩ PU |
| GPIO_2 | AG11 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[2] | Input | 360 KΩ PD |
| GPIO_3 | AC12 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[3] | Input | 360 KΩ PD |
| GPIO_4 | AH11 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[4] | Input | 100 KΩ PU |
| GPIO_5 | AJ11 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[5] | Input | 360 KΩ PD |
| GPIO_6 | AJ12 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[6] | Input | 360 KΩ PD |
| GPIO_7 | AC11 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[7] | Input | 360 KΩ PD |
| GPIO_8 | AD10 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[8] | Input | 360 KΩ PD |
| GPIO_9 | AC13 | — | NVCC_GPIO | UHVIO | ALT1 | gpio1_GPIO[9] | Input | 100 KΩ PU |
| JTAG_MOD | AD15 | — | NVCC_JTAG | GPIO | ALT0 | sjc_MOD | Input | 100 KΩ PU |
| JTAG_TCK | AD13 | — | NVCC_JTAG | GPIO | ALT0 | sjc_TCK | Input | 100 KΩ PD |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|--------------|---------------------------------------|------------------------------------|--------------|-----------------|-------------------------------------|----------------|--------------------|-------------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| JTAG_TDI | AC15 | — | NVCC_JTAG | GPIO | ALT0 | sjc_TDI | Input | 47 K Ω PU |
| JTAG_TDO | AG15 | — | NVCC_JTAG | GPIO | ALT0 | sjc_TDO | Input | Keeper |
| JTAG_TMS | AD16 | — | NVCC_JTAG | GPIO | ALT0 | sjc_TMS | Input | 47 K Ω PU |
| JTAG_TRSTB | AC17 | — | NVCC_JTAG | GPIO | ALT0 | sjc_TRSTB | Input | 47 K Ω PU |
| KEY_COL0 | AG9 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[6] | Input ⁴ | 100 K Ω PU |
| KEY_COL1 | AJ9 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[8] | Input | 100 K Ω PU |
| KEY_COL2 | AG8 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[10] | Input | 100 K Ω PU |
| KEY_COL3 | AJ8 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[12] | Input | 100 K Ω PU |
| KEY_COL4 | AH7 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[14] | Input | 100 K Ω PU |
| KEY_ROW0 | AH9 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[7] | Input | 360 K Ω PD |
| KEY_ROW1 | AH8 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[9] | Input | 100 K Ω PU |
| KEY_ROW2 | AJ7 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[11] | Input | 100 K Ω PU |
| KEY_ROW3 | AG7 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[13] | Input | 100 K Ω PU |
| KEY_ROW4 | AD8 | — | NVCC_KEYPAD | UHVIO | ALT1 | gpio4_GPIO[15] | Input | 360 K Ω PD |
| LVDS_BG_RES | C18 | — | NVCC_LVDS_BG | ANALOG | — | LVDS_BG_RES | — | — |
| LVDS0_CLK_N | B19 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[25] | Input | Floating |
| LVDS0_CLK_P | A19 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[24] | Input | Floating |
| LVDS0_TX0_N | B22 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[31] | Input | Floating |
| LVDS0_TX0_P | A22 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[30] | Input | Floating |
| LVDS0_TX1_N | A21 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[29] | Input | Floating |
| LVDS0_TX1_P | B21 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[28] | Input | Floating |
| LVDS0_TX2_N | B20 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[27] | Input | Floating |
| LVDS0_TX2_P | A20 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[26] | Input | Floating |
| LVDS0_TX3_N | B18 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[23] | Input | Floating |
| LVDS0_TX3_P | A18 | — | NVCC_LVDS | LVDS | ALT0 | gpio7_GPI[22] | Input | Floating |
| LVDS1_CLK_N | A15 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[27] | Input | Floating |
| LVDS1_CLK_P | B15 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[26] | Input | Floating |
| LVDS1_TX0_N | B17 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[31] | Input | Floating |
| LVDS1_TX0_P | A17 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[30] | Input | Floating |
| LVDS1_TX1_N | A16 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[29] | Input | Floating |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|----------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|----------------|-----------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| LVDS1_TX1_P | B16 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[28] | Input | Floating |
| LVDS1_TX2_N | A14 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[25] | Input | Floating |
| LVDS1_TX2_P | B14 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[24] | Input | Floating |
| LVDS1_TX3_N | A13 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[23] | Input | Floating |
| LVDS1_TX3_P | B13 | — | NVCC_LVDS | LVDS | ALT0 | gpio6_GPI[22] | Input | Floating |
| NANDF_ALE | N3 | L2 | NVCC_NANDF | UHVIO | ALT1 | gpio6_GPIO[8] | Input | 100 KΩ PU |
| NANDF_CLE | G16 | — | NVCC_NANDF | UHVIO | ALT1 | gpio6_GPIO[7] | Input | 100 KΩ PU |
| NANDF_CS0 | P2 | M1 | NVCC_NANDF | UHVIO | ALT1 | gpio6_GPIO[11] | Input | 100 KΩ PU |
| NANDF_CS1 | A11 | — | NVCC_NANDF | UHVIO | ALT1 | gpio6_GPIO[14] | Input | 100 KΩ PU |
| NANDF_CS2 | C12 | — | NVCC_NANDF | UHVIO | ALT1 | gpio6_GPIO[15] | Input | 100 KΩ PU |
| NANDF_CS3 | A12 | — | NVCC_NANDF | UHVIO | ALT1 | gpio6_GPIO[16] | Input | 100 KΩ PU |
| NANDF_RB0 | C15 | — | NVCC_NANDF | UHVIO | ALT1 | gpio6_GPIO[10] | Input | 100 KΩ PU |
| NANDF_RE_B | M3 | K2 | NVCC_EIM_MAIN | UHVIO | ALT1 | gpio6_GPIO[13] | Input | 100 KΩ PU |
| NANDF_WE_B | M2 | K1 | NVCC_EIM_MAIN | UHVIO | ALT1 | gpio6_GPIO[12] | Input | 100 KΩ PU |
| NANDF_WP_B | T2 | N1 | NVCC_NANDF | UHVIO | ALT1 | gpio6_GPIO[9] | Input | 100 KΩ PU |
| PATA_BUFFER_EN | V6 | — | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[1] | Input | 100 KΩ PU |
| PATA_CS_0 | AA2 | — | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[9] | Input | 100 KΩ PU |
| PATA_CS_1 | AB1 | — | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[10] | Input | 100 KΩ PU |
| PATA_DA_0 | N2 | L1 | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[6] | Input | 100 KΩ PU |
| PATA_DA_1 | AB2 | — | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[7] | Input | 100 KΩ PU |
| PATA_DA_2 | Y3 | — | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[8] | Input | 100 KΩ PU |
| PATA_DATA0 | B9 | A7 | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[0] | Input | 100 KΩ PU |
| PATA_DATA1 | B8 | B6 | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[1] | Input | 100 KΩ PU |
| PATA_DATA10 | B10 | A8 | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[10] | Input | 100 KΩ PU |
| PATA_DATA11 | C9 | B7 | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[11] | Input | 100 KΩ PU |
| PATA_DATA12 | Y1 | — | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[12] | Input | 100 KΩ PU |
| PATA_DATA13 | AA1 | — | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[13] | Input | 100 KΩ PU |
| PATA_DATA14 | W1 | — | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[14] | Input | 100 KΩ PU |
| PATA_DATA15 | V1 | — | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[15] | Input | 100 KΩ PU |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|---------------|---------------------------------------|------------------------------------|---------------|-----------------|-------------------------------------|--------------------|-----------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| PATA_DATA2 | B6 | A5 | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[2] | Input | 100 KΩ PU |
| PATA_DATA3 | C5 | B4 | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[3] | Input | 100 KΩ PU |
| PATA_DATA4 | Y2 | — | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[4] | Input | 100 KΩ PU |
| PATA_DATA5 | V3 | — | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[5] | Input | 100 KΩ PU |
| PATA_DATA6 | V2 | — | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[6] | Input | 100 KΩ PU |
| PATA_DATA7 | W2 | — | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[7] | Input | 100 KΩ PU |
| PATA_DATA8 | B12 | A10 | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[8] | Input | 100 KΩ PU |
| PATA_DATA9 | B11 | B9 | NVCC_PATA | UHVIO | ALT1 | gpio2_GPIO[9] | Input | 100 KΩ PU |
| PATA_DIOR | AB3 | — | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[3] | Input | 100 KΩ PU |
| PATA_DIOW | AA6 | — | NVCC_PATA | UHVIO | ALT1 | gpio6_GPIO[17] | Input | 100 KΩ PU |
| PATA_DMACK | Y6 | — | NVCC_PATA | UHVIO | ALT1 | gpio6_GPIO[18] | Input | 100 KΩ PU |
| PATA_DMARQ | W6 | — | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[0] | Input | 100 KΩ PU |
| PATA_INTRQ | V7 | — | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[2] | Input | 100 KΩ PU |
| PATA_IORDY | B5 | A4 | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[5] | Input | 100 KΩ PU |
| PATA_RESET_B | B4 | A3 | NVCC_PATA | UHVIO | ALT1 | gpio7_GPIO[4] | Input | 100 KΩ PU |
| PMIC_ON_REQ | F12 | — | NVCC_SRTC_POW | GPIO | ALT0 | src_SRTCALARM | Output | — |
| PMIC_STBY_REQ | G17 | — | NVCC_SRTC_POW | GPIO | ALT0 | ccm_PMIC_VSTBY_REQ | Output | — |
| POR_B | AC27 | — | NVCC_RESET | LVIO | ALT0 | src_POR_B | Input | 100 KΩ PU |
| RESET_IN_B | AB28 | — | NVCC_RESET | LVIO | ALT0 | src_RESET_B | Input | 100 KΩ PU |
| SATA_REFCLKM | AJ18 | — | VPH | ANALOG | — | SATA_REFCLKM | — | — |
| SATA_REFCLKP | AH18 | — | VPH | ANALOG | — | SATA_REFCLKP | — | — |
| SATA_REXT | AJ17 | — | VPH | ANALOG | — | SATA_REXT | — | — |
| SATA_RXM | AH16 | — | VPH | ANALOG | — | SATA_RXM | — | — |
| SATA_RXP | AJ16 | — | VPH | ANALOG | — | SATA_RXP | — | — |
| SATA_TXM | AH14 | — | VPH | ANALOG | — | SATA_TXM | — | — |
| SATA_TXP | AJ14 | — | VPH | ANALOG | — | SATA_TXP | — | — |
| SD1_CLK | AJ26 | — | NVCC_SD1 | UHVIO | ALT1 | gpio1_GPIO[20] | Input | 100 KΩ PU |
| SD1_CMD | AH26 | — | NVCC_SD1 | UHVIO | ALT1 | gpio1_GPIO[18] | Input | 100 KΩ PU |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|-----------------|---------------------------------------|------------------------------------|------------------------------|-----------------|-------------------------------------|----------------|-----------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| SD1_DATA0 | AH27 | — | NVCC_SD1 | UHVIO | ALT1 | gpio1_GPIO[16] | Input | 100 KΩ PU |
| SD1_DATA1 | AG25 | — | NVCC_SD1 | UHVIO | ALT1 | gpio1_GPIO[17] | Input | 100 KΩ PU |
| SD1_DATA2 | AH25 | — | NVCC_SD1 | UHVIO | ALT1 | gpio1_GPIO[19] | Input | 100 KΩ PU |
| SD1_DATA3 | AJ25 | — | NVCC_SD1 | UHVIO | ALT1 | gpio1_GPIO[21] | Input | 100 KΩ PU |
| SD2_CLK | AG19 | — | NVCC_SD2 | UHVIO | ALT1 | gpio1_GPIO[10] | Input | 100 KΩ PU |
| SD2_CMD | AD21 | — | NVCC_SD2 | UHVIO | ALT1 | gpio1_GPIO[11] | Input | 100 KΩ PU |
| SD2_DATA0 | AH17 | — | NVCC_SD2 | UHVIO | ALT1 | gpio1_GPIO[15] | Input | 100 KΩ PU |
| SD2_DATA1 | AG17 | — | NVCC_SD2 | UHVIO | ALT1 | gpio1_GPIO[14] | Input | 100 KΩ PU |
| SD2_DATA2 | AD17 | — | NVCC_SD2 | UHVIO | ALT1 | gpio1_GPIO[13] | Input | 100 KΩ PU |
| SD2_DATA3 | AG18 | — | NVCC_SD2 | UHVIO | ALT1 | gpio1_GPIO[12] | Input | 100 KΩ PU |
| TEST_MODE | AA27 | — | NVCC_RESET | LVIO | ALT0 | tcu_TEST_MODE | Input | 100 KΩ PD |
| TVDCD_I0B_B ACK | B23 | — | TVDAC_AHVDDRGB | ANALOG | — | TVDCD_I0B_BACK | — | — |
| TVDCD_I0G_B ACK | A24 | — | TVDAC_AHVDDRGB | ANALOG | — | TVDCD_I0G_BACK | — | — |
| TVDCD_I0R_B ACK | C28 | — | TVDAC_AHVDDRGB | ANALOG | — | TVDCD_I0R_BACK | — | — |
| TVDAC_COMP | A25 | — | TVDAC_AHVDDRGB | ANALOG | — | TVDAC_COMP | — | — |
| TVDAC_I0B | A23 | — | TVDAC_AHVDDRGB | ANALOG | — | TVDAC_I0B | — | — |
| TVDAC_I0G | B24 | — | TVDAC_AHVDDRGB | ANALOG | — | TVDAC_I0G | — | — |
| TVDAC_I0R | C29 | — | TVDAC_AHVDDRGB | ANALOG | — | TVDAC_I0R | — | — |
| USB_H1_DN | AH21 | — | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG50 | — | USB_H1_DN | — | — |
| USB_H1_DP | AJ21 | — | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG50 | — | USB_H1_DP | — | — |
| USB_H1_GPANAIO | AJ20 | — | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG25 | — | USB_H1_GPANAIO | — | — |
| USB_H1_RREFEXT | AH20 | — | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG25 | — | USB_H1_RREFEXT | — | — |

Table 118. PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O (continued)

| Contact Name | PoP Bottom Package Contact Assignment | PoP Top Package Contact Assignment | Power Rail | I/O Buffer Type | Out of Reset Condition ¹ | | | |
|---------------------|---------------------------------------|------------------------------------|-----------------------------------|-----------------|-------------------------------------|---------------------|-----------|----------------|
| | | | | | Alt. Mode | Function | Direction | Config./ Value |
| USB_H1_VBUS | AJ22 | — | USB_H1_VDDA25, USB_H1_VDDA33 | ANALOG5 0 | — | USB_H1_VBUS | — | — |
| USB_OTG_DN | AJ23 | — | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG5 0 | — | USB_OTG_DN | — | — |
| USB_OTG_DP | AH23 | — | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG5 0 | — | USB_OTG_DP | — | — |
| USB_OTG_GPA NAIO | AH24 | — | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG2 5 | — | USB_OTG_GPANAI O | — | — |
| USB_OTG_ID | AH22 | — | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG2 5 | — | USB_OTG_ID | — | — |
| USB_OTG_RRE FEXT | AJ24 | — | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG2 5 | — | USB_OTG_RREFE XT | — | — |
| USB_OTG_VBU S | AG21 | — | USB_OTG_VDDA25, USB_OTG_VDDA33 | ANALOG5 0 | — | USB_OTG_VBUS | — | — |
| XTAL | F15 | — | NVCC_XTAL | ANALOG | — | XTAL | — | — |

¹ The state immediately after reset and before ROM firmware or software has executed.

² During power-on reset this port acts as input for fuse override, ~33KΩ PU/PD recommended to set the value. See [Section 5.1](#), “[Boot Mode Configuration Pins](#)” for details.

³ During power-on reset this port acts as output for diagnostic signal INT_BOOT

⁴ During power-on reset this port acts as output for diagnostic signal ANY_PU_RST

6.3.3 12 x 12 mm PoP, 0.4 Pitch Ball Maps

[Table 119](#) shows the 12 × 12 mm, 0.4 pitch top ball map.

[Table 120](#) shows the 12 × 12 mm, 0.4 pitch bottom ball map.

Table 119. PoP 12 × 12 mm, 0.4 Pitch Top Ball Map

| | H | G | F | E | D | C | B | A |
|----|----------|----------|-------------|----------|----------|----------|-------------|--------------|
| 1 | EIM_DA15 | EIM_DA14 | POP_VCCQMM1 | EIM_DA13 | EIM_DA12 | GND | NC | NC |
| 2 | EIM_DA7 | EIM_DA6 | GND | EIM_DA5 | EIM_DA4 | POP_VDD2 | NC | NC |
| 3 | NC | NC | NC | NC | NC | NC | POP_VDD1 | PATA_RESET_B |
| 4 | NC | NC | NC | NC | NC | NC | PATA_DATA3 | PATA_IORDY |
| 5 | NC | NC | NC | NC | NC | NC | GND | PATA_DATA2 |
| 6 | NC | NC | NC | NC | NC | NC | PATA_DATA1 | POP_VCCMM |
| 7 | NC | NC | NC | NC | NC | NC | PATA_DATA11 | PATA_DATA0 |
| 8 | NC | NC | NC | NC | NC | NC | GND | PATA_DATA10 |
| 9 | NC | NC | NC | NC | NC | NC | PATA_DATA9 | POP_VCCQMM |
| 10 | NC | NC | NC | NC | NC | NC | GND | PATA_DATA8 |
| 11 | NC | NC | NC | NC | NC | NC | POP_VDD2 | POP_VDD1 |
| 12 | NC | NC | NC | NC | NC | NC | DRAM_D29 | GND |
| 13 | NC | NC | NC | NC | NC | NC | POP_VDDQ | DRAM_D27 |
| 14 | NC | NC | NC | NC | NC | NC | DRAM_D31 | DRAM_D25 |
| 15 | NC | NC | NC | NC | NC | NC | DRAM_D28 | GND |
| 16 | NC | NC | NC | NC | NC | NC | POP_VDDQ | DRAM_D30 |
| 17 | NC | NC | NC | NC | NC | NC | DRAM_D26 | DRAM_D24 |
| 18 | NC | NC | NC | NC | NC | NC | DRAM_SDQS3 | GND |
| 19 | NC | NC | NC | NC | NC | NC | POP_VDDQ | DRAM_SDQS3_B |
| 20 | NC | NC | NC | NC | NC | NC | DRAM_DQM3 | POP_VDD1 |
| 21 | NC | NC | NC | NC | NC | NC | POP_VDD2 | GND |
| 22 | DRAM_D21 | POP_VDDQ | DRAM_D20 | DRAM_D22 | POP_VDDQ | DRAM_D16 | NC | NC |
| 23 | DRAM_D23 | DRAM_D19 | GND | DRAM_D17 | DRAM_D18 | GND | NC | NC |
| | H | G | F | E | D | C | B | A |

Table 119. PoP 12 × 12 mm, 0.4 Pitch Top Ball Map (continued)

| | R | P | N | M | L | K | J |
|----|------------|--------------|------------|-----------|-----------|--------------|------------|
| 1 | GND | POP_ZQ | NANDF_WP_B | NANDF_CS0 | PATA_DA_0 | NANDF_WE_B | POP_VCCMM |
| 2 | POP_VDD2 | DDR_VREF | POP_VDD1 | GND | NANDF_ALE | NANDF_RE_B | GND |
| 3 | NC | NC | NC | NC | NC | NC | NC |
| 4 | NC | NC | NC | NC | NC | NC | NC |
| 5 | NC | NC | NC | NC | NC | NC | NC |
| 6 | NC | NC | NC | NC | NC | NC | NC |
| 7 | NC | NC | NC | NC | NC | NC | NC |
| 8 | NC | NC | NC | NC | NC | NC | NC |
| 9 | NC | NC | NC | NC | NC | NC | NC |
| 10 | NC | NC | NC | NC | NC | NC | NC |
| 11 | NC | NC | NC | NC | NC | NC | NC |
| 12 | NC | NC | NC | NC | NC | NC | NC |
| 13 | NC | NC | NC | NC | NC | NC | NC |
| 14 | NC | NC | NC | NC | NC | NC | NC |
| 15 | NC | NC | NC | NC | NC | NC | NC |
| 16 | NC | NC | NC | NC | NC | NC | NC |
| 17 | NC | NC | NC | NC | NC | NC | NC |
| 18 | NC | NC | NC | NC | NC | NC | NC |
| 19 | NC | NC | NC | NC | NC | NC | NC |
| 20 | NC | NC | NC | NC | NC | NC | NC |
| 21 | NC | NC | NC | NC | NC | NC | NC |
| 22 | POP_VDDQ | DRAM_SDQS0_B | POP_VDD1 | DDR_VREF | POP_VDD2 | POP_VDDQ | DRAM_SDQS2 |
| 23 | DRAM_SDQS0 | GND | DRAM_DQM0 | GND | DRAM_DQM2 | DRAM_SDQS2_B | GND |
| | R | P | N | M | L | K | J |

Table 119. PoP 12 × 12 mm, 0.4 Pitch Top Ball Map (continued)

| | AC | AB | AA | Y | W | V | U | T | |
|----|--------------|------------|----------|----------------|-----------|----------|-----------|---------|----|
| 1 | NC | NC | GND | DRAM_SDCLK_1_B | DRAM_A5 | GND | DRAM_A7 | DRAM_A9 | 1 |
| 2 | NC | NC | POP_VDD2 | DRAM_SDCLK_1 | POP_VDDCA | DRAM_A6 | POP_VDDCA | DRAM_A8 | 2 |
| 3 | DRAM_SDCKE0 | DRAM_CS0 | NC | NC | NC | NC | NC | NC | 3 |
| 4 | DRAM_SDCKE1 | DRAM_CS1 | NC | NC | NC | NC | NC | NC | 4 |
| 5 | GND | POP_VDD1 | NC | NC | NC | NC | NC | NC | 5 |
| 6 | DRAM_A0 | DRAM_A1 | NC | NC | NC | NC | NC | NC | 6 |
| 7 | DRAM_A2 | GND | NC | NC | NC | NC | NC | NC | 7 |
| 8 | POP_VDDCA | DRAM_A3 | NC | NC | NC | NC | NC | NC | 8 |
| 9 | GND | DRAM_A4 | NC | NC | NC | NC | NC | NC | 9 |
| 10 | POP_VDDMM | POP_VDD2 | NC | NC | NC | NC | NC | NC | 10 |
| 11 | POP_VACC | GND | NC | NC | NC | NC | NC | NC | 11 |
| 12 | GND | DRAM_D14 | NC | NC | NC | NC | NC | NC | 12 |
| 13 | DRAM_D10 | POP_VDDQ | NC | NC | NC | NC | NC | NC | 13 |
| 14 | DRAM_D8 | DRAM_D12 | NC | NC | NC | NC | NC | NC | 14 |
| 15 | GND | DRAM_D13 | NC | NC | NC | NC | NC | NC | 15 |
| 16 | DRAM_D15 | POP_VDDQ | NC | NC | NC | NC | NC | NC | 16 |
| 17 | DRAM_D11 | DRAM_D9 | NC | NC | NC | NC | NC | NC | 17 |
| 18 | GND | DRAM_SDQS1 | NC | NC | NC | NC | NC | NC | 18 |
| 19 | DRAM_SDQS1_B | POP_VDDQ | NC | NC | NC | NC | NC | NC | 19 |
| 20 | POP_VDD1 | DRAM_DQM1 | NC | NC | NC | NC | NC | NC | 20 |
| 21 | GND | POP_VDD2 | NC | NC | NC | NC | NC | NC | 21 |
| 22 | NC | NC | POP_VDDQ | DRAM_D3 | DRAM_D0 | POP_VDDQ | DRAM_D2 | DRAM_D6 | 22 |
| 23 | NC | NC | DRAM_D1 | GND | DRAM_D7 | DRAM_D5 | GND | DRAM_D4 | 23 |
| | AC | AB | AA | Y | W | V | U | T | |

Table 120. PoP 12 × 12 mm, 0.4 Pitch Bottom Ball Map

| | F | E | D | C | B | A |
|----|---------------|----------|----------|----------------|----------------|----------------|
| 1 | EIM_D23 | EIM_D25 | EIM_D26 | EIM_D30 | GND | GND |
| 2 | EIM_DA13 | EIM_DA12 | EIM_D28 | EIM_A22 | GND | GND |
| 3 | EIM_DA5 | EIM_DA4 | POP_VDD2 | POP_VDD1 | EIM_A23 | EIM_A25 |
| 4 | NC | NC | NC | EIM_CS1 | PATA_RESET_B | EIM_A24 |
| 5 | NC | NC | NC | PATA_DATA3 | PATA_IORDY | EIM_LBA |
| 6 | EIM_EB3 | NC | NC | EIM_A21 | PATA_DATA2 | EIM_A19 |
| 7 | EIM_D31 | NC | NC | EIM_D29 | EIM_A20 | EIM_A16 |
| 8 | EIM_A18 | NC | NC | POP_VCCMM | PATA_DATA1 | EIM_DA3 |
| 9 | EIM_D24 | NC | NC | PATA_DATA11 | PATA_DATA0 | EIM_OE |
| 10 | EIM_DA2 | NC | NC | EIM_D27 | PATA_DATA10 | EIM_DA8 |
| 11 | EIM_BCLK | NC | NC | POP_VCCQMM | PATA_DATA9 | NANDF_CS1 |
| 12 | PMIC_ON_REQ | NC | NC | NANDF_CS2 | PATA_DATA8 | NANDF_CS3 |
| 13 | NVCC_SRTC_POW | NC | NC | POP_VDD1 | LVDS1_TX3_P | LVDS1_TX3_N |
| 14 | NVCC_XTAL | NC | NC | POP_VDD2 | LVDS1_TX2_P | LVDS1_TX2_N |
| 15 | XTAL | NC | NC | NANDF_RB0 | LVDS1_CLK_P | LVDS1_CLK_N |
| 16 | VDDA | NC | NC | POP_VDDQ | LVDS1_TX1_P | LVDS1_TX1_N |
| 17 | DRAM_D29 | NC | NC | GND | LVDS1_TX0_N | LVDS1_TX0_P |
| 18 | NVCC_LVDS_BG | NC | NC | LVDS_BG_RES | LVDS0_TX3_N | LVDS0_TX3_P |
| 19 | NVCC_LVDS | NC | NC | DRAM_D25 | LVDS0_CLK_N | LVDS0_CLK_P |
| 20 | DRAM_D30 | NC | NC | POP_VDDQ | LVDS0_TX2_N | LVDS0_TX2_P |
| 21 | DRAM_D24 | NC | NC | DRAM_SDQS3_B | LVDS0_TX1_P | LVDS0_TX1_N |
| 22 | DRAM_SDCKE1 | NC | NC | DRAM_SDQS3 | LVDS0_TX0_N | LVDS0_TX0_P |
| 23 | TVDAC_DHVDD | NC | NC | DRAM_DQM3 | TVCDC_JOB_BACK | TVDAC_JOB |
| 24 | NVCC_EMI_DRAM | NC | NC | POP_VDDQ | TVDAC_IOP | TVCDC_IOP_BACK |
| 25 | NC | NC | NC | GPIO_13 | GPIO_10 | TVDAC_COMP |
| 26 | NC | NC | NC | POP_VDD1 | GPIO_11 | GPIO_12 |
| 27 | DRAM_D20 | POP_VDDQ | DRAM_A15 | POP_VDD2 | GPIO_14 | TVDAC_VREF |
| 28 | DRAM_D19 | DRAM_D22 | DRAM_D18 | TVCDC_IOR_BACK | GND | GND |
| 29 | DRAM_D23 | DRAM_D17 | DRAM_D16 | TVDAC_IOR | GND | GND |
| | F | E | D | C | B | A |

Table 120. PoP 12 × 12 mm, 0.4 Pitch Bottom Ball Map (continued)

| | M | L | K | J | H | G |
|----|------------|---------------|-------------------|----------------|---------------|----------------|
| 1 | CS10_DAT16 | CS10_DAT19 | EIM_DAO | EIM_EB0 | EIM_D16 | EIM_D22 |
| 2 | NANDF_WE_B | CS10_DAT18 | EIM_DA15 | EIM_DA14 | EIM_D18 | EIM_D19 |
| 3 | NANDF_RE_B | POP_VCCMM | EIM_DA7 | EIM_DA6 | POP_VCCQMM1 | EIM_D17 |
| 4 | NC | NC | NC | NC | NC | NC |
| 5 | NC | NC | NC | NC | NC | NC |
| 6 | VDDA | EIM_WAIT | EIM_DA9 | NVCC_CSI | EIM_D21 | NVCC_EIM_SEC |
| 7 | EIM_D20 | EIM_DA10 | EIM_DA11 | EIM_EB2 | EIM_RW | EIM_EB1 |
| 8 | NC | NC | NC | NC | NC | EIM_A17 |
| 9 | NC | NC | NC | NC | NC | NVCC_EIM_MAIN |
| 10 | NC | NC | NC | NC | NC | EIM_CS0 |
| 11 | VCC | VCC | NC | NC | NC | EIM_DA1 |
| 12 | VCC | VCC | NC | NC | NC | NVCC_NANDF |
| 13 | VCC | VCC | NC | NC | NC | GKIL |
| 14 | GND | GND | NC | NC | NC | ECKIL |
| 15 | GND | GND | NC | NC | NC | EXTAL |
| 16 | GND | GND | NC | NC | NC | NANDF_CLE |
| 17 | VCC | VCC | NC | NC | NC | PMIC_STBY_REQ |
| 18 | VCC | VCC | NC | NC | NC | DRAM_D27 |
| 19 | VCC | VCC | NC | NC | NC | DRAM_D31 |
| 20 | NC | NC | NC | NC | NC | DRAM_D28 |
| 21 | NC | NC | NC | NC | NC | DRAM_D26 |
| 22 | NC | NC | NC | NC | NC | TVDAC_AHVDDRGB |
| 23 | DRAM_A5 | DRAM_A3 | NVCC_EMI_DRAM_2P5 | DRAM_SDCLK_1_B | DRAM_SDCLK_1 | TVDAC_AHVDDRGB |
| 24 | DRAM_A8 | NVCC_EMI_DRAM | NVCC_EMI_DRAM | DRAM_CS1 | NVCC_EMI_DRAM | NVCC_EMI_DRAM |
| 25 | NC | NC | NC | NC | NC | NC |
| 26 | NC | NC | NC | NC | NC | NC |
| 27 | DRAM_A13 | DRAM_A14 | DRAM_SDBA1 | POP_VDDQ | DRAM_SDBA0 | DRAM_D21 |
| 28 | DRAM_A10 | DRAM_A12 | DRAM_SDBA2 | DRAM_RESET | DRAM_SDODT1 | DRAM_SDQS2 |
| 29 | DRAM_RAS | DRAM_SDODT0 | DRAM_SDWE | DRAM_A11 | DRAM_DQM2 | DRAM_SDQS2_B |
| | M | L | K | J | H | G |

Table 120. PoP 12 × 12 mm, 0.4 Pitch Bottom Ball Map (continued)

| | V | U | T | R | P | N |
|----|----------------|---------------|------------|------------------|---------------|---------------|
| 1 | PATA_DATA15 | CSIO_DAT12 | CSIO_DAT14 | CSIO_DAT13 | CSIO_DAT15 | CSIO_DAT17 |
| 2 | PATA_DATA6 | CSIO_DAT8 | NANDF_WP_B | CSIO_DAT10 | NANDF_CS0 | PATA_DA_0 |
| 3 | PATA_DATA5 | POP_ZQ | POP_VDD1 | CSIO_DAT5 | CSIO_DAT9 | NANDF_ALE |
| 4 | NC | NC | NC | NC | NC | NC |
| 5 | NC | NC | NC | NC | NC | NC |
| 6 | PATA_BUFFER_EN | CSIO_PIXCLK | CSIO_MCLK | VDDA | CSIO_DATA_EN | NVCC_PATA |
| 7 | PATA_INTRQ | CSIO_VSYNC | CSIO_DAT4 | CSIO_DAT11 | CSIO_DAT6 | CSIO_DAT7 |
| 8 | NC | NC | NC | NC | NC | NC |
| 9 | NC | NC | NC | NC | NC | NC |
| 10 | NC | NC | NC | NC | NC | NC |
| 11 | VDDGP | VDDGP | GND | GND | GND | VCC |
| 12 | VDDGP | VDDGP | GND | GND | GND | VCC |
| 13 | VDDGP | VDDGP | GND | GND | GND | VCC |
| 14 | GND | GND | NC | NC | NC | GND |
| 15 | GND | GND | NC | NC | NC | GND |
| 16 | GND | GND | NC | NC | NC | GND |
| 17 | VCC | VCC | GND | GND | GND | VCC |
| 18 | VCC | VCC | GND | GND | GND | VCC |
| 19 | VCC | VCC | GND | GND | GND | VCC |
| 20 | NC | NC | NC | NC | NC | NC |
| 21 | NC | NC | NC | NC | NC | NC |
| 22 | NC | NC | NC | NC | NC | NC |
| 23 | DRAM_A2 | DDR_VREF | DRAM_A9 | DRAM_CALIBRATION | DRAM_A6 | DRAM_A7 |
| 24 | NVCC_EMI_DRAM | NVCC_EMI_DRAM | VDDA | NVCC_EMI_DRAM | NVCC_EMI_DRAM | NVCC_EMI_DRAM |
| 25 | NC | NC | NC | NC | NC | NC |
| 26 | NC | NC | NC | NC | NC | NC |
| 27 | DRAM_D1 | DRAM_D3 | POP_VDD1 | DRAM_D4 | POP_VDD2 | POP_VDDQ |
| 28 | FEC_TXD1 | FEC_MDC | DRAM_D7 | DRAM_D5 | DRAM_SDQS0_B | DRAM_DQM0 |
| 29 | FEC_TX_EN | FEC_TXD0 | DRAM_D0 | DRAM_D2 | DRAM_D6 | DRAM_SDQS0 |
| | V | U | T | R | P | N |

Table 120. PoP 12 × 12 mm, 0.4 Pitch Bottom Ball Map (continued)

| | AD | AC | AB | AA | Y | W |
|----|----------------|----------------|-------------|-------------|-------------------|---------------|
| 1 | DISP0_DATA0 | DISP0_DAT12 | PATA_CS_1 | PATA_DATA13 | PATA_DATA12 | PATA_DATA14 |
| 2 | DISP0_DATA6 | DISP0_DAT2 | PATA_DA_1 | PATA_CS_0 | PATA_DATA4 | PATA_DATA7 |
| 3 | POP_VDDCA | DISP0_DAT1 | PATA_DIOR | POP_VDDCA | PATA_DA_2 | POP_VDD2 |
| 4 | NC | NC | NC | NC | NC | NC |
| 5 | NC | NC | NC | NC | NC | NC |
| 6 | NVCC_KEYPAD | DIO_PIN4 | DISP0_DAT17 | PATA_DIOW | PATA_DMACK | PATA_DMARQ |
| 7 | DIO_PIN2 | DIO_PIN3 | DISP0_DAT21 | DISP0_DAT19 | NVCC_LCD | NVCC_LCD |
| 8 | KEY_ROW4 | VDDAL1 | NC | NC | NC | NC |
| 9 | NVCC_GPIO | GPIO_18 | NC | NC | NC | NC |
| 10 | GPIO_8 | GPIO_17 | NC | NC | NC | NC |
| 11 | NVCC_JTAG | GPIO_7 | NC | NC | NC | VDDGP |
| 12 | GPIO_0 | GPIO_3 | NC | NC | NC | VDDGP |
| 13 | JTAG_TCK | GPIO_9 | NC | NC | NC | VDDGP |
| 14 | VDDA | NVCC_FEC | NC | NC | NC | GND |
| 15 | JTAG_MOD | JTAG_TDI | NC | NC | NC | GND |
| 16 | JTAG_TMS | NVCC_SD2 | NC | NC | NC | GND |
| 17 | SD2_DATA2 | JTAG_TRSTB | NC | NC | NC | VCC |
| 18 | NVCC_RESET | USB_H1_VDDA33 | NC | NC | NC | VCC |
| 19 | USB_H1_VDDA25 | USB_OTG_VDDA25 | NC | NC | NC | VCC |
| 20 | USB_OTG_VDDA33 | NVCC_SD1 | NC | NC | NC | NC |
| 21 | SD2_CMD | VDD_FUSE | NC | NC | NC | NC |
| 22 | NVCC_CKIH | VDD_ANA_PLL | NC | NC | NC | NC |
| 23 | VDD_REG | VDD_DIG_PLL | DRAM_CS0 | DRAM_CAS | DRAM_A1 | DRAM_A0 |
| 24 | NVCC_EMI_DRAM | NVCC_EMI_DRAM | DRAM_SDCKE0 | DRAM_A4 | NVCC_EMI_DRAM_2P5 | NVCC_EMI_DRAM |
| 25 | NC | NC | NC | NC | NC | NC |
| 26 | NC | NC | NC | NC | NC | NC |
| 27 | DRAM_DQM1 | POR_B | POP_VDDQ | TEST_MODE | FEC_CRS_DV | POP_VDDQ |
| 28 | FASTR_DIG | CKIH2 | RESET_IN_B | BOOT_MODE0 | FEC_RX_ER | FEC_RXD0 |
| 29 | FASTR_ANA | CKIH1 | BOOT_MODE1 | FEC_MDIO | FEC_REF_CLK | FEC_RXD1 |
| | AD | AC | AB | AA | Y | W |

Table 120. PoP 12 × 12 mm, 0.4 Pitch Bottom Ball Map (continued)

| | AJ | AH | AG | AF | AE |
|----|-----------------|-----------------|--------------|--------------|--------------|
| 1 | GND | GND | DISP0_DAT7 | DISP0_DAT4 | DISP0_DAT5 |
| 2 | GND | SVDDGP | DISP0_DAT10 | DIO_DISP_CLK | DISP0_DAT3 |
| 3 | DISP0_DAT9 | DISP0_DAT13 | DISP0_DAT14 | POP_VDD2 | DISP0_DAT11 |
| 4 | DISP0_DAT18 | DISP0_DAT15 | DISP0_DAT8 | NC | NC |
| 5 | DISP0_DAT20 | DISP0_DAT22 | DISP0_DAT16 | NC | NC |
| 6 | DISP0_DAT23 | DIO_PIN15 | POP_VDD1 | NC | NC |
| 7 | KEY_ROW2 | KEY_COL4 | KEY_ROW3 | NC | NC |
| 8 | KEY_COL3 | KEY_ROW1 | KEY_COL2 | NC | NC |
| 9 | KEY_COL1 | KEY_ROW0 | KEY_COL0 | NC | NC |
| 10 | GPIO_19 | GPIO_16 | POP_VDDCA | NC | NC |
| 11 | GPIO_5 | GPIO_4 | GPIO_2 | NC | NC |
| 12 | GPIO_6 | GPIO_1 | POP_VDD2 | NC | NC |
| 13 | VPH | VPH | POP_VDDMM | NC | NC |
| 14 | SATA_TXP | SATA_TXM | POP_VACC | NC | NC |
| 15 | GND | GND | JTAG_TDO | NC | NC |
| 16 | SATA_RXP | SATA_RXM | POP_VDDQ | NC | NC |
| 17 | SATA_REXT | SD2_DATA0 | SD2_DATA1 | NC | NC |
| 18 | SATA_REFCLKM | SATA_REFCLKP | SD2_DATA3 | NC | NC |
| 19 | VP | VP | SD2_CLK | NC | NC |
| 20 | USB_H1_GPANAIO | USB_H1_RREFEXT | POP_VDDQ | NC | NC |
| 21 | USB_H1_DP | USB_H1_DN | USB_OTG_VBUS | NC | NC |
| 22 | USB_H1_VBUS | USB_OTG_ID | DRAM_D10 | NC | NC |
| 23 | USB_OTG_DN | USB_OTG_DP | DRAM_D12 | NC | NC |
| 24 | USB_OTG_RREFEXT | USB_OTG_GPANAIO | POP_VDDQ | NC | NC |
| 25 | SD1_DATA3 | SD1_DATA2 | SD1_DATA1 | NC | NC |
| 26 | SD1_CLK | SD1_CMD | POP_VDD1 | NC | NC |
| 27 | DRAM_D15 | SD1_DATA0 | POP_VDD2 | POP_VDDQ | DRAM_SDQS1_B |
| 28 | GND | SVCC | DRAM_D14 | DRAM_D8 | DRAM_SDQS1 |
| 29 | GND | GND | DRAM_D11 | DRAM_D13 | DRAM_D9 |
| | AJ | AH | AG | AF | AE |

7 Revision History

Table 121 provides a revision history for this data sheet.

Table 121. i.MX53xD Data Sheet Document Revision History

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| Rev 4.1 | 02/2012 | <ul style="list-style-type: none"><li data-bbox="396 436 1406 493">• In Table 1, "Ordering Information," on page 3, changed the part number PCIMX538DZK1C to SCIMX538DZK1C. |

Table 121. i.MX53xD Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| Rev 4 | 11/2011 | <ul style="list-style-type: none"> • In Section 1, "Introduction," changed 1 GHz to 1.2 GHz in the second paragraph and updated the bulleted list after the second paragraph. • In Table 1, "Ordering Information," on page 3: <ul style="list-style-type: none"> —Removed part numbers "PCIMX535DVV1C" and "MCIMX538DZK1C" —Added a new part number "MCIMX535DVV2C" —Updated package information for part number "PCIMX538DZK1C" —Updated the second footnote • In Section 1.2, "Features," changed "Target frequency" to "Maximum frequency" and 1 GHz to 1–1.2 GHz in the third bullet item of the first bulleted list. • In Table 2, "i.MX53xD Digital and Analog Blocks," on page 8, removed "Sorenson H.263 decode, 4CIF resolution, 8 Mbps bit rate" from VPU brief description. • In Table 4, "Absolute Maximum Ratings," on page 17, changed the maximum voltage for VDDGP from 1.35V to 1.4V. • In Table 7, "i.MX53xD Operating Ranges," on page 20: <ul style="list-style-type: none"> —Added a row and a footnote for "ARM core supply voltage $f_{ARM} \leq 1200$ MHz" parameter of VDDGP —Added a new footnote for "Peripheral supply voltage" parameter of VCC —Updated the footnote for "Junction temperature" parameter • In Table 9, "Maximal Supply Currents," on page 23, made the following two changes for VDDGP: <ul style="list-style-type: none"> —Changed the test condition "1000 MHz ARM clock" to "1000 MHz ARM Clock at 1.27V, 105 °C" —Added a new row for VDDGP corresponding to 1200 MHz (1.2 GHz) • Added a note after Section 4.2.1, "Power-Up Sequence," cross-referencing i.MX53 System Development User's Guide. • In Table 11, "GPIO I/O DC Electrical Characteristics," on page 29: <ul style="list-style-type: none"> —Changed test condition "Iout = -1 mA" to "Iout = -0.8 mA" in the first row —Removed test condition "Iout= specified Ioh Drive" from the first row —Removed "0.8 x OVDD" from the Min column of the first row —Changed test condition "Iout = 1 mA" to "Iout = 0.8 mA" in the second row —Removed test condition "Iout= specified Iol Drive" from the second row —Removed "0.2 x OVDD" from the Max column of the second row —Removed rows 3–6 —Changed the max value for Iin at condition "Vin = OVDD or 0" in row 12 from 2 μA to 10 μA —Changed the max value for Iin at condition "Vin = OVDD" in rows 13–15 from 2 μA to 10 μA —Changed the max value for Iin at condition "Vin = 0 V" in row 15 from 36 μA to 40 μA —Changed the max value for Iin at condition "Vin = 0 V" in row 16 from 2 μA to 10 μA —Changed the max value for Iin at condition "Vin = OVDD" in row 16 from 36 μA to 40 μA • In Table 12, "DDR2 I/O DC Electrical Parameters," on page 30: <ul style="list-style-type: none"> —Added test condition "Ioh = -0.1 mA" in the first row —Added test condition "Iol = 0.1 mA" in the second row —Removed rows 3–4 • In Section 4, "Electrical Characteristics," removed the note appearing after the first paragraph. • In Section 4.2.1, "Power-Up Sequence," updated the fifth bullet item. • In Section 4.3.2.2, "LPDDR2 Mode I/O DC Parameters," added the sentence "The parameters in Table 13 are guaranteed per the operating ranges in Table 7, unless otherwise noted." before Table 13. • In Table 13, "LPDDR2 I/O DC Electrical Parameters," on page 31: <ul style="list-style-type: none"> —Added test condition "Ioh = -0.1 mA" in the first row —Added test condition "Iol = 0.1 mA" in the second row |

Revision History

Table 121. i.MX53xD Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|----------------------|---------|--|
| Rev 4 (continued) | 11/2011 | <ul style="list-style-type: none"> • In Table 14, "DDR3 I/O DC Electrical Parameters," on page 31: <ul style="list-style-type: none"> —Added test condition "Ioh = -0.1 mA" in the first row —Added test condition "Iol = 0.1 mA" in the second row • In Table 15, "LVIO DC Electrical Characteristics," on page 32: <ul style="list-style-type: none"> —Added test condition "Ioh = -0.8 mA" in the first row —Added test condition "Iol = 0.8 mA" in the second row • In Table 16, "UHVIO DC Electrical Characteristics," on page 33: <ul style="list-style-type: none"> —Changed test condition "Iout = -1 mA" to "Iout = -0.8 mA" in the first row —Removed test condition "Iout= specified Ioh Drive" from the first row —Removed "0.8 x OVDD" from the Min column of the first row —Changed test condition "Iout = 1 mA" to "Iout = 0.8 mA" in the second row —Removed test condition "Iout= specified Iol Drive" from the second row —Removed "0.2 x OVDD" from the Max column of the second row —Removed rows 3–6 • In Section 4.3.5, "LVDS I/O DC Parameters," added the sentence "The parameters in Table 17 are guaranteed per the operating ranges in Table 7, unless otherwise noted." before Table 17. • In Table 17, "LVDS DC Electrical Characteristics," on page 34, changed test condition "Rload=100Ω padP, -padN" to "Rload = 100Ω between padP and padN". • In Table 36, "NFC—Timing Characteristics," on page 51, corrected footnote number for Tdl. • In Table 50, "SD/eMMC4.3 Interface Timing Specification," on page 74, updated eSDHC output delay. • In Table 51, "eMMC4.4 Interface Timing Specification," on page 75, updated eSDHC output delay. • In Table 63, "TV Encoder Video Performance Specifications," on page 96, changed test condition "Fout = 9.28 MHz" for SFDR to "Fout = 8.3 MHz". • In Table 118, "PoP 12 x 12 mm Signal Assignments, Power Rails, and I/O," on page 176, removed the DRAM_SDCLK_0 and DRAM_SDCLK_0_B rows. |
| Rev 3 | 06/2011 | <ul style="list-style-type: none"> • In Section 4.1.1, "Absolute Maximum Ratings," updated the caution note on page 17. • In Table 116, "Additional PCB connections for PoP NAND Flash," on page 175, updated the second and third column headings. |

Table 121. i.MX53xD Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| Rev 2 | 05/2011 | <ul style="list-style-type: none"> • In Table 1, "Ordering Information," on page 3, deleted the row for part number PCIMX535DVV1B, added a row for MCIMX538DZK1C and updated the PCIMX538DZK1C row. • Updated the note on page 6 in Section 1.2, "Features." • Added 167 MHz ARM specification to Table 7, "i.MX53xD Operating Ranges," on page 20. • Modified VDD_FUSE design best practice footnote on Table 7, "i.MX53xD Operating Ranges," on page 20. • Changed VDD_FUSE max current to 120 mA in Table 9, "Maximal Supply Currents," on page 23. • Deleted the last row of Table 10, "USB Interface Current Consumption," on page 25. • Added Section 4.1.2.2, "PoP Package Thermal Resistance," according to package design report. • Made changes related to text, tables, and figures in Section 4.6.7, "DDR SDRAM Specific Parameters (DDR2/LVDDR2, LPDDR2, and DDR3). Changes include adding LPDDR2 waves, updating timings by ACCZ test results, and changing note about DDR load model. • Removed the Standard Serial Interfaces section. • In Table 11, "GPIO I/O DC Electrical Characteristics," on page 29, changed input current with no pull-up/down from 250/120 nA to 2 μA, all input currents with pull-up from 0.12 μA to 2 μA when $V_{in} = OVDD$, and input current with pull-down from 0.25 μA to 2 μA when $V_{in} = 0$. • In Table 12, Table 13, and Table 14, changed input current from the nA range to 1 μA. • In Table 15, "LVIO DC Electrical Characteristics," on page 32, changed input current with no pull-up/down from 250/120 nA to 1 μA, all input currents with pull-up from 0.12 μA to 1 μA when $V_{in} = OVDD$, and input current with pull-down from 0.25 μA to 1 μA when $V_{in} = 0$. • In Table 16, "UHVIO DC Electrical Characteristics," on page 33, changed input current with no pull-up/down from 300/63 nA to 1 μA, all input currents with pull-up from 0.06 μA to 1 μA when $V_{in} = OVDD$, and input current with pull-down from 0.3 μA to 1 μA when $V_{in} = 0$. • Updated keeper values in Table 11 through Table 16. • Fixed titles of Figure 18 through Figure 26, to fit original EIM AC spec. • Updated Figure 2, "Power-Up Detailed Sequence," on page 27. • Added Figure 27, "DTACK Write Access (DAP=0)," on page 61. • Added Table 19, "DDR Output Driver Average Impedance," on page 37. • Deleted the second footnote of Table 33, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 46. • Deleted the Revision 1.0 EIM Internal Module Multiplexing table. • Deleted the CKIL Electrical Specifications table. • Deleted the CSPI Slave Mode Timing Parameters table . • Updated the last paragraph of Section 4.7.8.6.1, "IPU Display Operating Signals." • Changed the title of the Section 4.4.2, "DDR Output Driver Average Impedance," from "LPDDR2 I/O Output Buffer Impedance." • Added Section 6.3.2.2, "PoP Memory Support and Signal Cross Reference." • Updated Table 36, "NFC—Timing Characteristics," on page 51. • Removed the "Differential pulse skew" row from Table 30, "AC Electrical Characteristics of LVDS Pad," on page 44. • Updated Table 64, "Asynchronous Display Interface Timing Parameters (Pixel Level)," on page 103. • Updated Table 65, "Asynchronous Parallel Interface Timing Parameters (Access Level)," on page 104. • Updated Table 101, "USB Timing Specification for Normal ULPI Mode," on page 141. • Updated the second footnote on Table 112, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 151. |

Revision History

Table 121. i.MX53xD Data Sheet Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|--|
| Rev 1 | 03/2011 | <ul style="list-style-type: none"> • Updated the first sentence of Section 3.1, “Special Signal Considerations.” • Deleted two tables, “Special Signal Considerations” and “JTAG Controller Interface Summary,” in Section 3.1, “Special Signal Considerations.” • Updated Table 7, “i.MX53xD Operating Ranges,” on page 20. <ul style="list-style-type: none"> • Changed VDDGP voltages as follows: <ul style="list-style-type: none"> — 400 MHz from 1.35 to 1.05 V maximum. — 800 MHz from 1.0/1.05/1.1 to 1.05/1.1/1.15 V minimum/nominal/maximum. — Stop mode from 0.9/0.95/1.1 to 0.8/0.85/1.3 V minimum/nominal/maximum. • Added statements to footnotes 5 and 6. • Added footnote on voltage ramping. • In Section 1, “Introduction,” the second bullet item changed from “Smartbooks” to “Smart mobile devices.” • In Table 1, “Ordering Information,” on page 3, added two new rows for part numbers PCIMX535DVV1C and MCIMX535DVV1C. |
| Rev 0 | 02/2011 | Initial release. |

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