Freescale Semiconductor
Technical Data

Document Number: MD7IC2050N
Rev. 1, 5/2010

√RoHS

RF LDMOS Wideband Integrated Power Amplifiers

MD7IC2050NR1
MD7IC2050GNR1
MD7IC2050NBR1

1880-2100 MHz, 10 W AVG., 28 V
SINGLE W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

The MD7IC2050N wideband integrated circuit is designed with on-chip matching that makes it usable from 1750-2050 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulation formats.

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1A} = I_{DQ1B} = 30 mA, I_{DQ2A} = 230 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 10 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
2025 MHz	30.5	34.7	8.7	-37.4

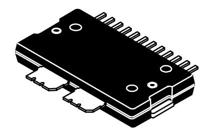
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 2017.5 MHz, 79 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 20 Watts to 80 Watts CW P_{out}
- Typical P_{out} @ 3 dB Compression Point ≃ 74 Watts CW

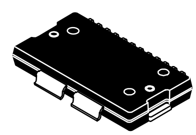
1880 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1A} = I_{DQ1B} = 30 mA, I_{DQ2A} = 230 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 10 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
1880 MHz	30.3	35.2	8.6	-34.9
1900 MHz	30.2	34.9	8.6	-36.3
1920 MHz	30.1	34.8	8.7	-36.9

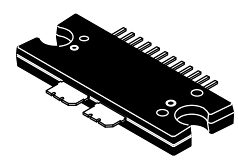
CASE 1618-02
TO-270 WB-14
PLASTIC
MD7IC2050NR1





CASE 1621-02
TO-270 WB-14 GULL
PLASTIC
MD7IC2050GNR1

CASE 1617-02
TO-272 WB-14
PLASTIC
MD7IC2050NBR1



Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Production Tested in a Symmetrical Doherty Configuration
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function [(1)]
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

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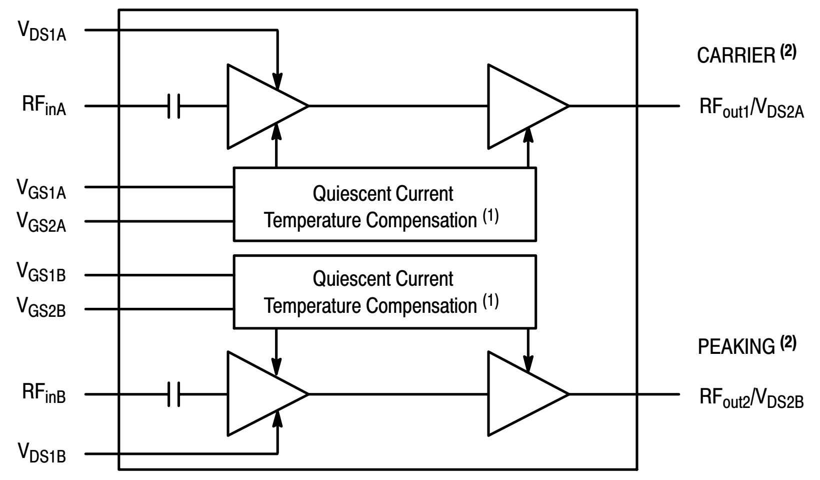
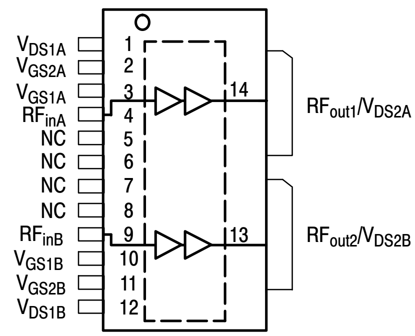


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.
2. Peaking and Carrier orientation is determined by the test fixture design.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
Input Power	P_{in}	28	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Final Doherty Application			
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 81°C, P_{out} = 50 W CW			
Stage 1A, 28 Vdc, I_{DQ1A} = 30 mA		8.2	
Stage 1B, 28 Vdc, I_{DQ1B} = 30 mA		8.2	
Stage 2A, 28 Vdc, I_{DQ2A} = 230 mA		1.8	
Stage 2B, 28 Vdc, V_{GS2B} = 1.4 Vdc		1.8	
Case Temperature 73°C, P_{out} = 10 W CW			
Stage 1A, 28 Vdc, I_{DQ1A} = 30 mA		8.3	
Stage 1B, 28 Vdc, I_{DQ1B} = 30 mA		8.3	
Stage 2A, 28 Vdc, I_{DQ2A} = 230 mA		1.9	
Stage 2B, 28 Vdc, V_{GS2B} = 1.4 Vdc		1.9	

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	0 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	II (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 - Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 - On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 23 μAdc)	$V_{GS(th)}$	1.2	1.9	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 30 mAdc)	$V_{GS(Q)}$	—	3	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 30 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.1	5.5	7.1	Vdc
Stage 2 - Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 - On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = 230 mAdc)	$V_{GS(Q)}$	—	3	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = 230 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.1	5.5	7.1	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	0.1	0.3	1.2	Vdc

Functional Tests (2,3,4) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 30 mA, I_{DQ2A} = 230 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 10 W Avg., f = 2025 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	28.5	30.5	33.0	dB
Power Added Efficiency	PAE	32.0	34.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	8.0	8.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37.4	-34.0	dBc

1. Each side of device measured separately.
2. Part internally matched both on input and output.
3. Measurement made with device in a Symmetrical Doherty configuration.
4. Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances [1] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 30 mA, I_{DQ2A} = 230 mA, V_{GS2B} = 1.4 Vdc, 2010-2025 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	60	—	W
P_{out} @ 3 dB Compression Point, CW	P3dB	—	74	—	W
IMD Symmetry @ 30 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	55	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Quiescent Current Accuracy over Temperature with 4.7 kΩ Gate Feed Resistors (-30 to 85°C) [2]	ΔI_{QT}	—	2.64	—	%
Gain Flatness in 15 MHz Bandwidth @ P_{out} = 10 W Avg.	G_F	—	0.1	—	dB
Gain Variation over Temperature (-30 °C to +85°C)	ΔG	—	0.033	—	dB/°C
Output Power Variation over Temperature (-30 °C to +85°C)	ΔP1dB	—	0.008	—	dBm/°C

Typical W-CDMA Broadband Performance — 1880 MHz (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQ1B} = 30 mA, I_{DQ2A} = 230 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 10 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1880 MHz	30.3	35.2	8.6	-34.9	-21
1900 MHz	30.2	34.9	8.6	-36.3	-21
1920 MHz	30.1	34.8	8.7	-36.9	-22

1. Measurement made with device in a Symmetrical Doherty configuration.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf.Select Documentation/Application Notes - AN1977 or AN1987.

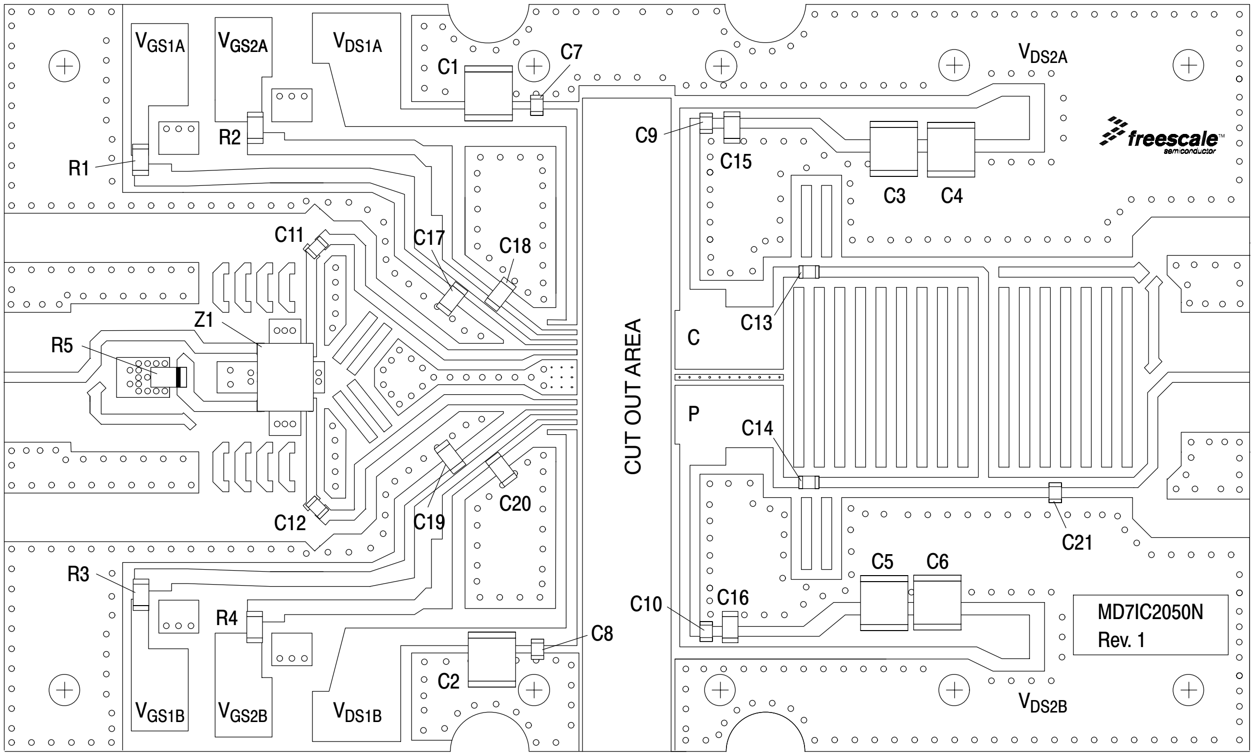


Figure 3. MD7IC2050NR1(GNR1)(NBR1) Test Circuit Component Layout

Table 6. MD7IC2050NR1(GNR1)(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C7, C8	4.7 pF Chip Capacitors	ATC600F4R7BT250XT	ATC
C9, C10	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C11, C12, C13, C14	39 pF Chip Capacitors	ATC600F390JT250XT	ATC
C15, C16, C17, C18, C19, C20	4.7 μF, 50 V Chip Capacitors	GRM31CR71H475KA12L	Murata
C21	1.0 pF Chip Capacitor	ATC600F1R0BT250XT	ATC
R1, R2, R3, R4	4.7 kΩ, 1/4 W Chip Resistors	CRCW12064701KEA	Vishay
R5	50 Ω, 1/4 W Thick Film Chip Resistor	RK73B2BTTD510J	KOA Speer
Z1	1900 MHz Band 90°, 3 dB Hybrid Coupler	GSC351-HYB1900	Soshin
PCB	0.020″, ε_r = 3.5	RF-35	Taconic

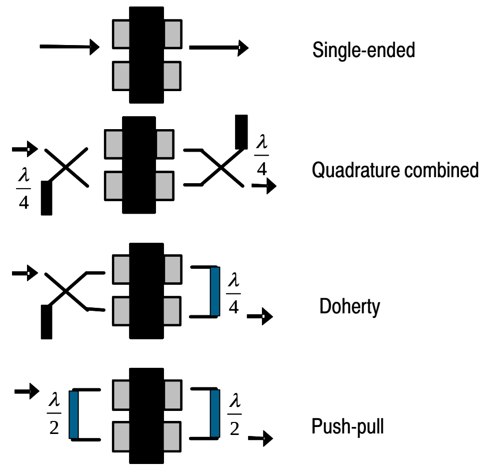


Figure 4. Possible Circuit Topologies

TYPICAL CHARACTERISTICS

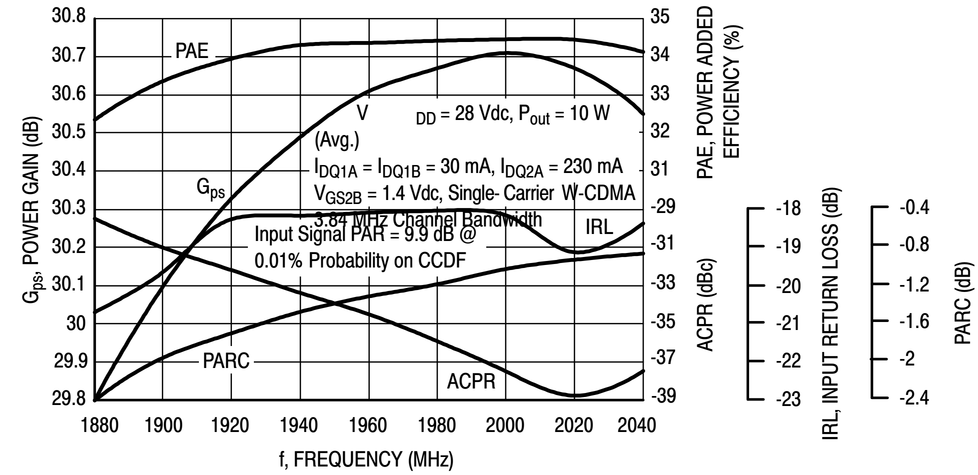


Figure 5. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 10 Watts Avg.

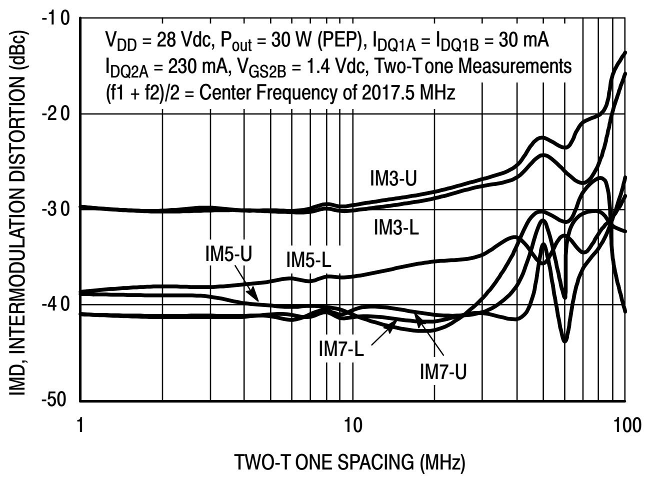


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

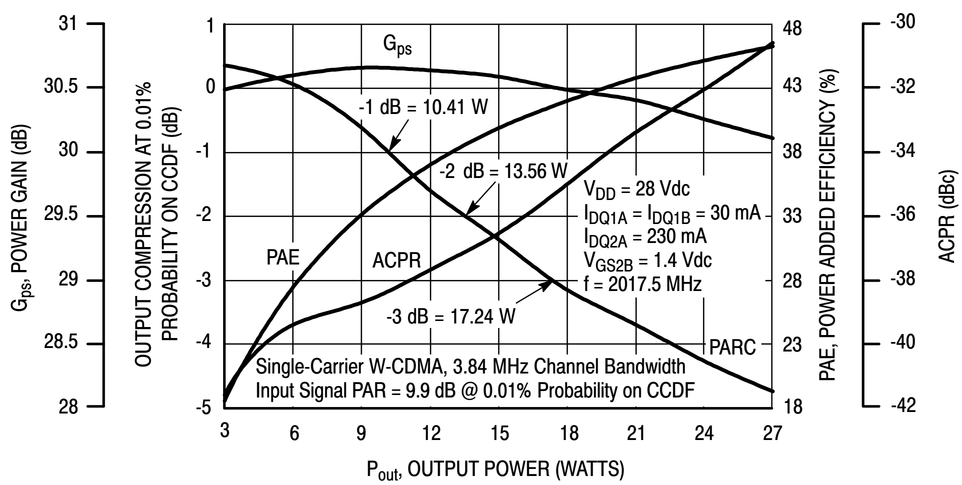


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

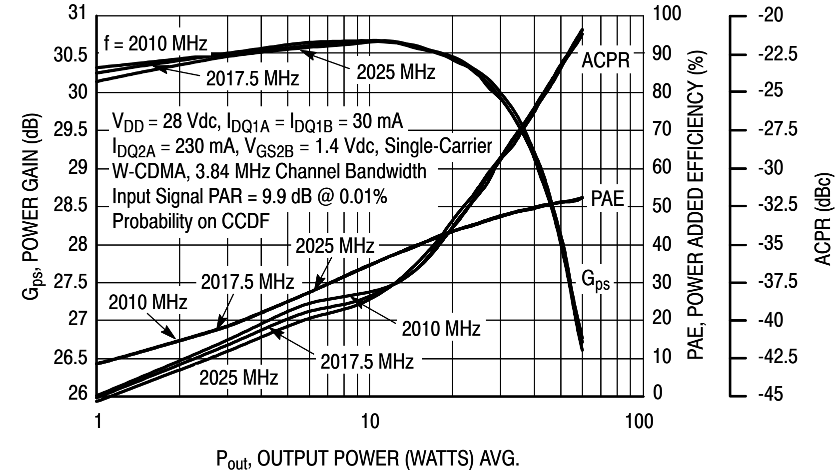


Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

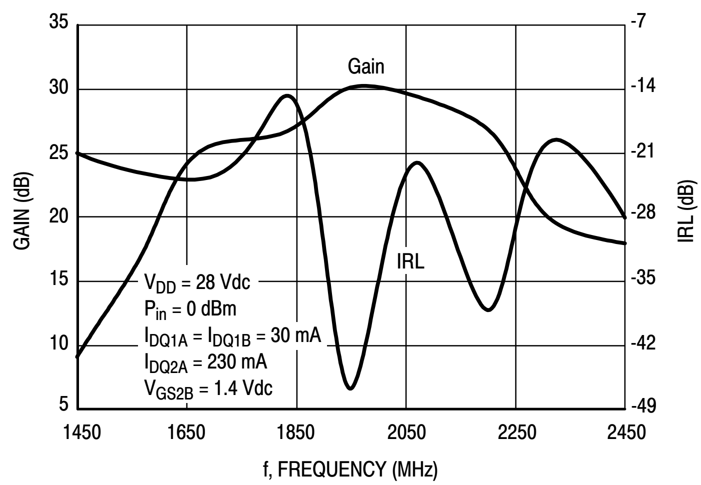


Figure 9. Broadband Frequency Response

W-CDMA TEST SIGNAL

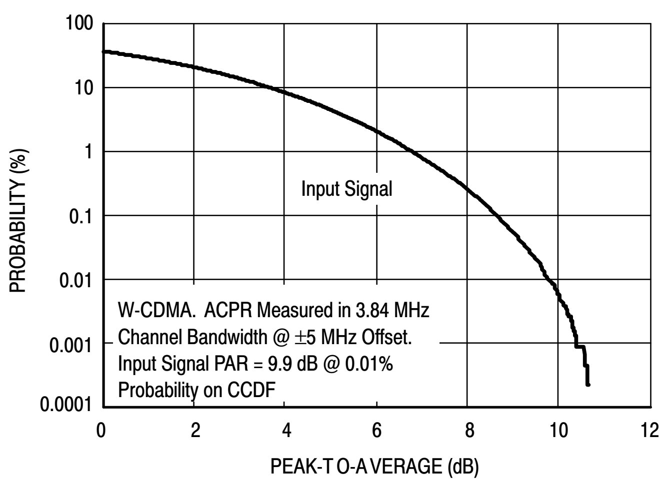


Figure 10. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

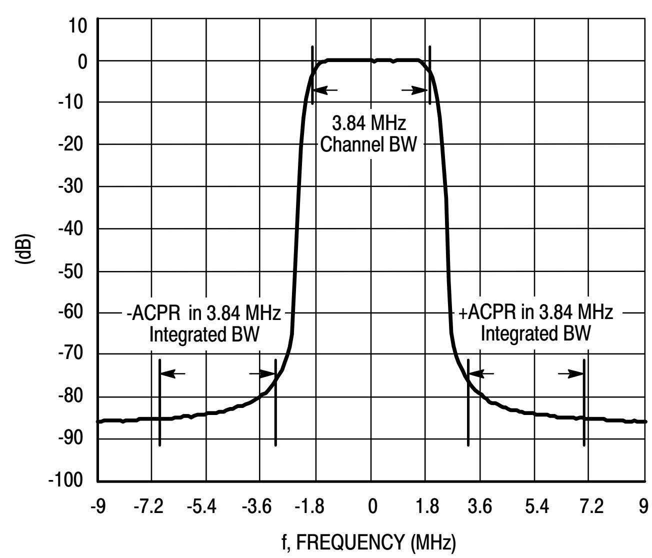


Figure 11. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQB} = 30 mA, I_{DQ2A} = 230 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 10 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
1995	60.12 - j33.28	11.79 - j6.72
2000	59.30 - j32.57	11.78 - j6.78
2005	58.41 - j32.06	11.78 - j6.85
2010	57.41 - j31.31	11.78 - j6.92
2015	56.31 - j30.27	11.79 - j7.00
2020	55.94 - j29.62	11.81 - j7.08
2025	55.28 - j28.90	11.81 - j7.16
2030	54.75 - j28.12	11.84 - j7.24
2035	54.39 - j27.55	11.80 - j7.33

Note: Measured with Peaking side open.

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

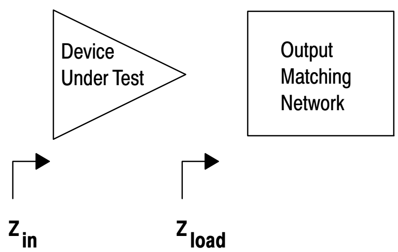


Figure 12. Series Equivalent Input and Load Impedance — Carrier Side

V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQB} = 30 mA, I_{DQ2A} = 230 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 10 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
1995	60.12 - j33.28	1.86 - j11.38
2000	59.30 - j32.57	1.80 - j11.24
2005	58.41 - j32.06	1.71 - j11.12
2010	57.41 - j31.31	1.64 - j11.00
2015	56.31 - j30.27	1.58 - j10.91
2020	55.94 - j29.62	1.51 - j10.78
2025	55.28 - j28.90	1.45 - j10.66
2030	54.75 - j28.12	1.38 - j10.56
2035	54.39 - j27.55	1.33 - j10.40

Note: Measured with Carrier side open.

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

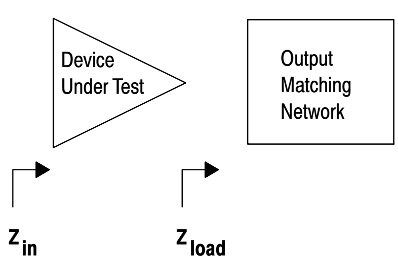
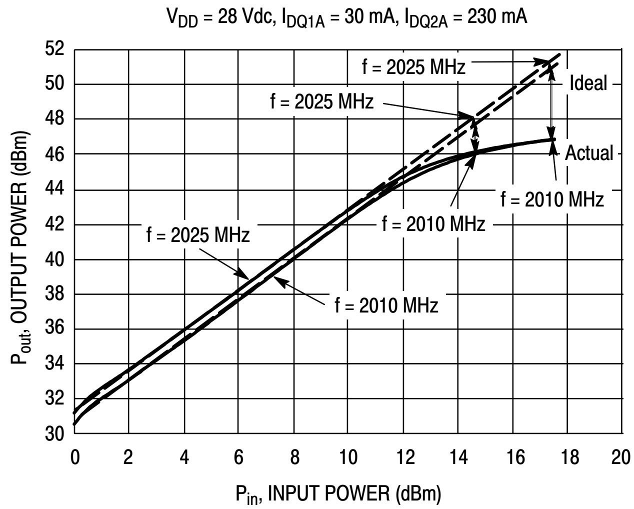


Figure 13. Series Equivalent Input and Load Impedance — Peaking Side

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	**dBm**	**Watts**	**dBm**
2010	40	46	49	46.9
2025	38.9	45.9	47.9	46.8

Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
2010	P1dB	73.6 + j31.1	6.8 - j13.7
2025	P1dB	68.9 + j26.7	8.3 - j14.3

Figure 14. CW Output Power versus Input Power @ 28 V

NOTE: Measurement made on the Class AB, carrier side of the device.

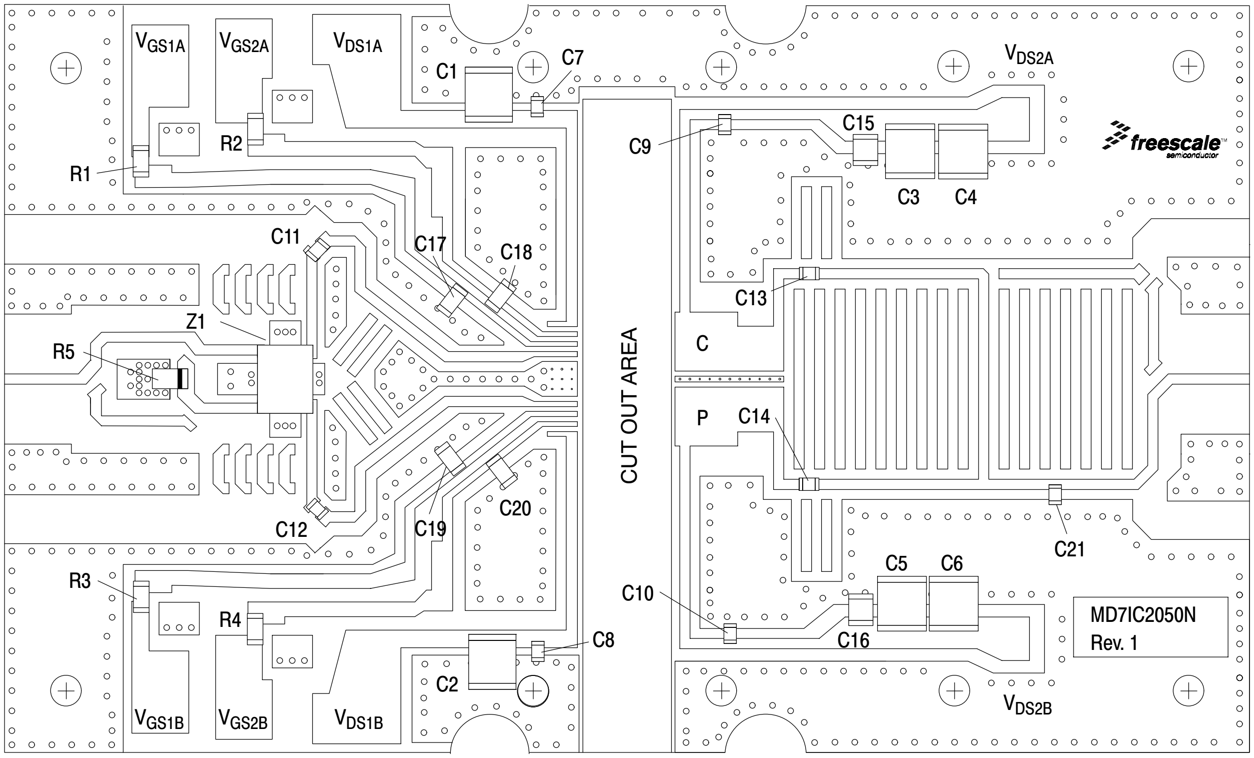


Figure 15. MD7IC2050NR1(GNR1)(NBR1) Test Circuit Component Layout — 1880 MHz

Table 7. MD7IC2050NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 1880 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C7, C8	6.8 pF Chip Capacitors	ATC600F6R8BT250XT	ATC
C9, C10	15 pF Chip Capacitors	ATC600F150JT250XT	ATC
C11, C12, C13, C14	33 pF Chip Capacitors	ATC600F330JT250XT	ATC
C15, C16	6.8 μF, 50 V Chip Capacitors	GRM32CF51H685ZA01L	Murata
C17, C18, C19, C20	2.2 μF, Chip Capacitors	GRM31CR61H225KA88L	Murata
C21	0.9 pF Chip Capacitor	ATC600F0R9BT250XT	ATC
R1, R2, R3, R4	4.7 kΩ, 1/4 W Chip Resistors	CRCW12064701FKEA	Vishay
R5	50 Ω, 1/4 W Thick Film Chip Resistor	RK73B2BTTD510J	KOA Speer
Z1	1900 MHz Band 90°, 3 dB Hybrid Coupler	GSC351-HYB1900	Soshin
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS

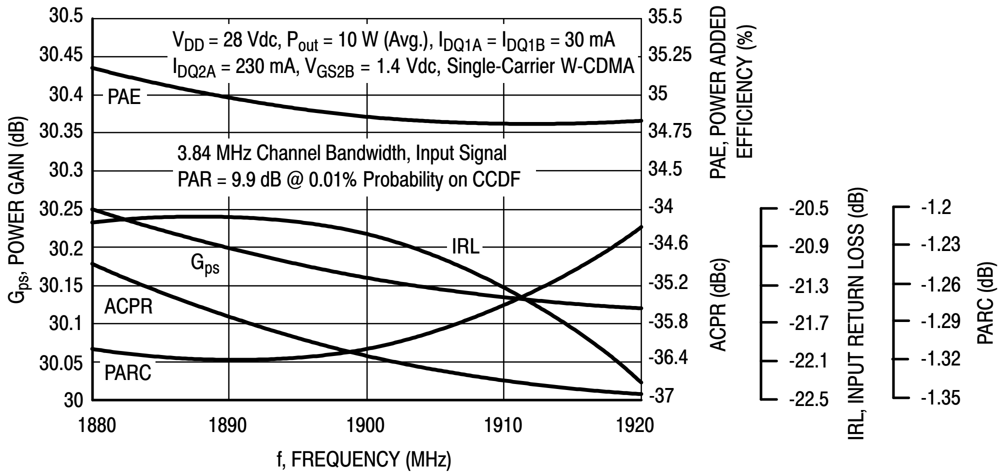


Figure 16. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 10 Watts Avg. — 1880 MHz

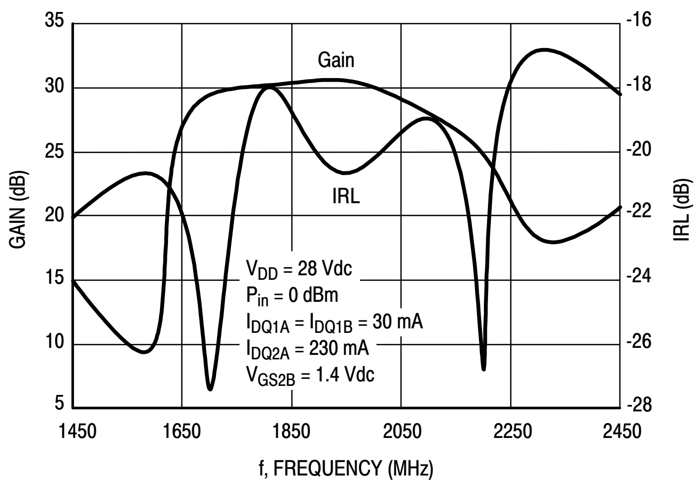


Figure 17. Broadband Frequency Response — 1880 MHz

V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQB} = 30 mA, I_{DQ2A} = 230 mA,
V_{GS2B} = 1.4 Vdc, P_{out} = 10 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
1725	24.58 + j28.09	13.68 - j7.83
1750	30.62 + j35.84	14.09 - j7.95
1775	39.80 + j43.59	14.42 - j8.13
1800	53.16 + j51.72	14.72 - j8.33
1825	75.48 + j54.32	15.02 - j8.57
1850	101.49 + j44.03	15.26 - j8.91
1875	127.43 + j11.39	15.47 - j9.29
1900	113.52 - j23.46	15.59 - j9.67
1925	92.03 - j36.95	15.66 - j10.15
1950	74.95 - j38.10	15.64 - j10.65
1975	64.95 - j35.67	15.59 - j11.22
2000	59.30 - j32.57	15.41 - j11.76
2025	55.28 - j28.90	15.20 - j12.36
2050	52.85 - j26.07	14.84 - j12.97
2075	51.34 - j23.91	14.42 - j13.56

Note: Measured with Peaking side open.

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

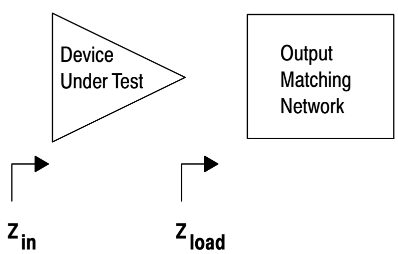


Figure 18. Series Equivalent Input and Load Impedance — Carrier Side — 1880 MHz

V_{DD} = 28 Vdc, I_{DQ1A} = I_{DQB} = 30 mA, I_{DQ2A} = 230 mA,
V_{GS2B} = 1.4 Vdc, P_{out} = 10 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
1725	24.58 + j28.09	4.10 - j18.22
1750	30.62 + j35.84	3.61 - j17.55
1775	39.80 + j43.59	3.09 - j16.79
1800	53.16 + j51.72	2.61 - j16.00
1825	75.48 + j54.32	2.31 - j15.22
1850	101.49 + j44.03	1.99 - j14.46
1875	127.43 + j11.39	1.71 - j13.71
1900	113.52 - j23.46	1.47 - j12.96
1925	92.03 - j36.95	1.27 - j12.19
1950	74.95 - j38.10	1.15 - j11.44
1975	64.95 - j35.67	1.04 - j10.70
2000	59.30 - j32.57	1.00 - j9.97
2025	55.28 - j28.90	0.98 - j9.28
2050	52.85 - j26.07	1.05 - j8.57
2075	51.34 - j23.91	1.16 - j7.91

Note: Measured with Carrier side open.

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

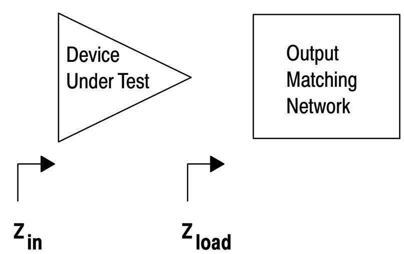
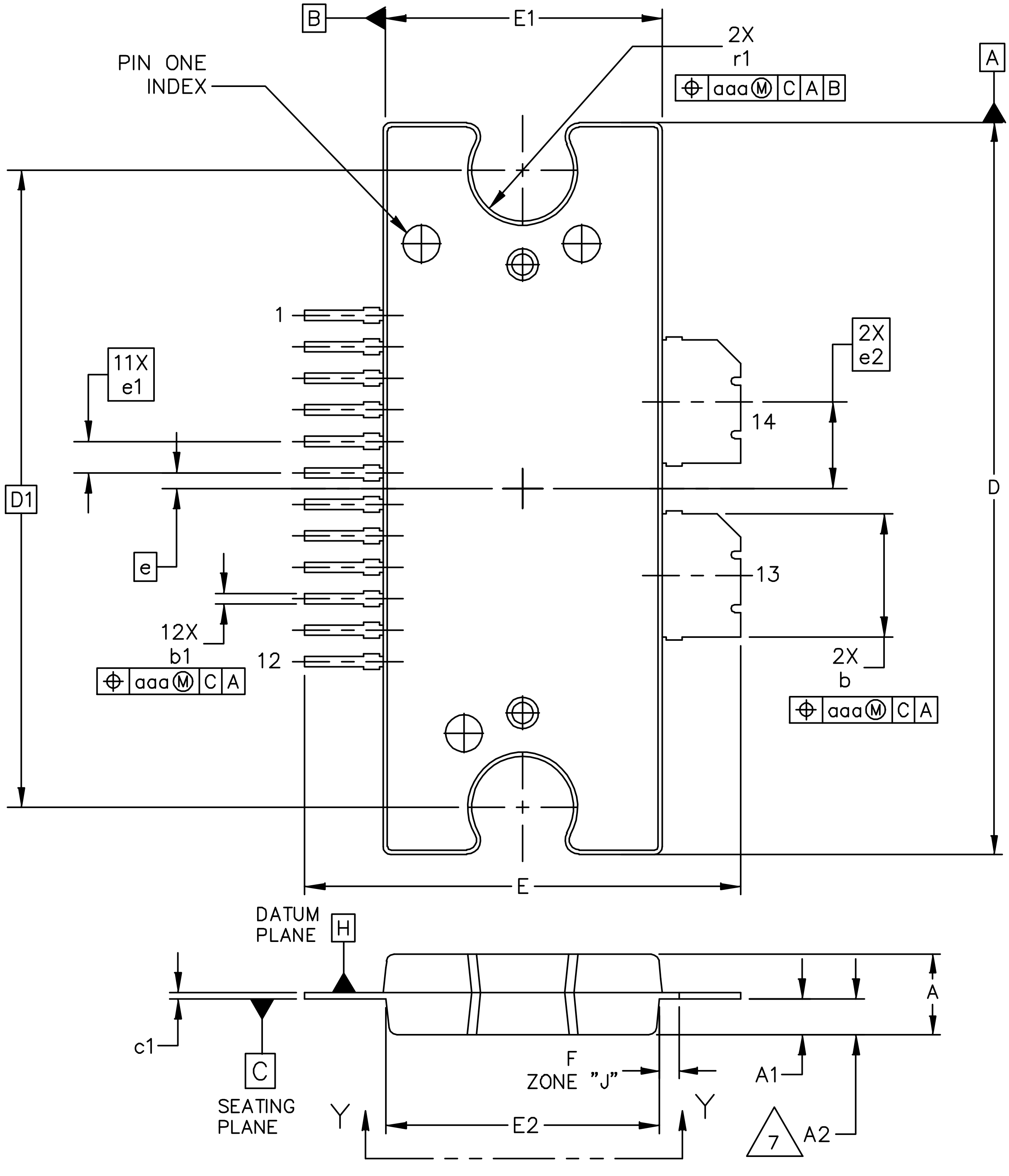


Figure 19. Series Equivalent Input and Load Impedance — Peaking Side — 1880 MHz

PACKAGE DIMENSIONS



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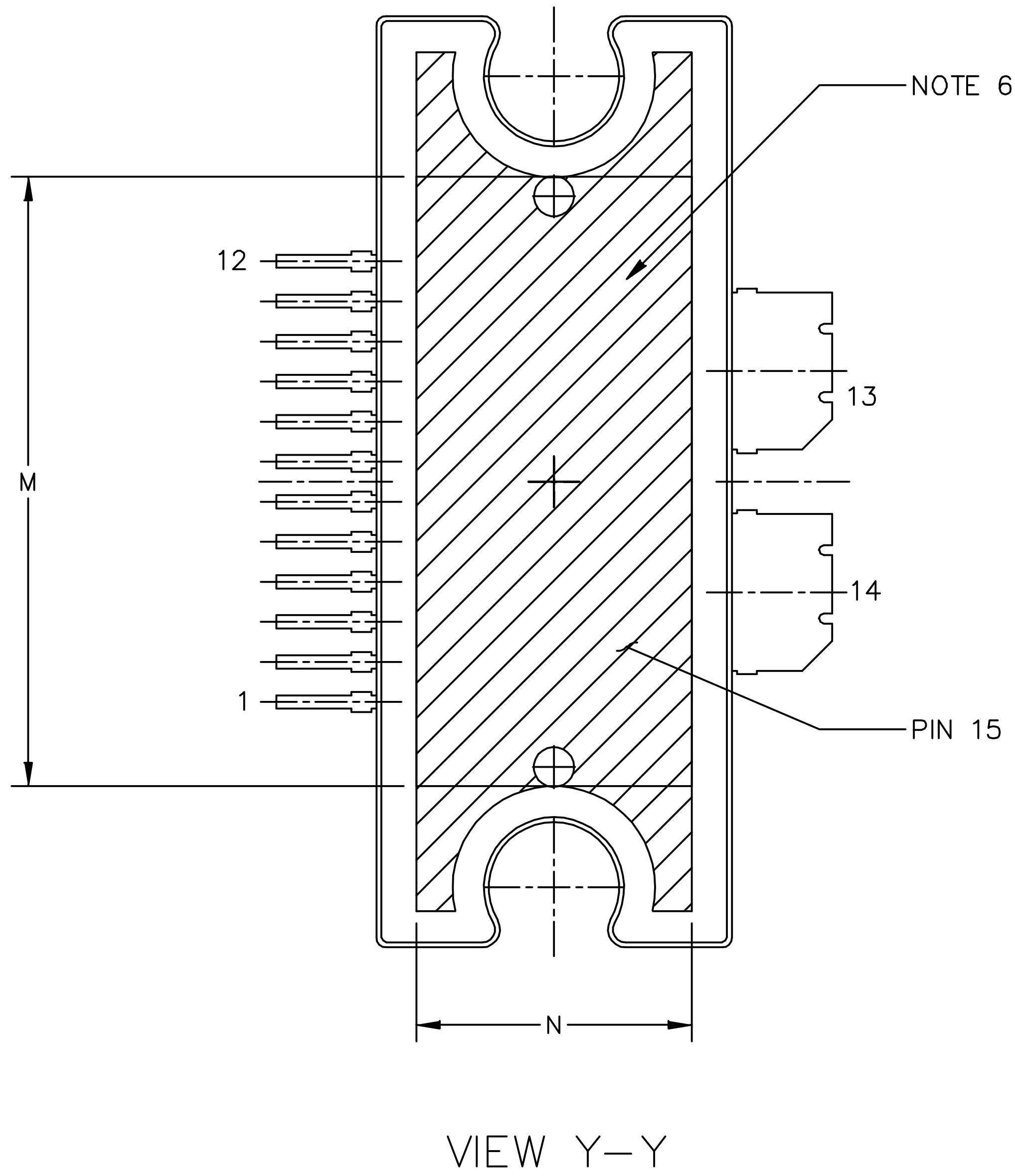
	CASE NUMBER: 1617–02		27 JUN 2007
	STANDARD: NON–JEDEC		



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	CASE NUMBER: 1617–02	27 JUN 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b	.154	.160	3.91	4.06
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.810 BSC		20.57 BSC		e1	.040 BSC		1.02 BSC	
E	.551	.559	14.00	14.20	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	r1	.063	.068	1.6	1.73
E2	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----					
N	.270	----	6.86	----					

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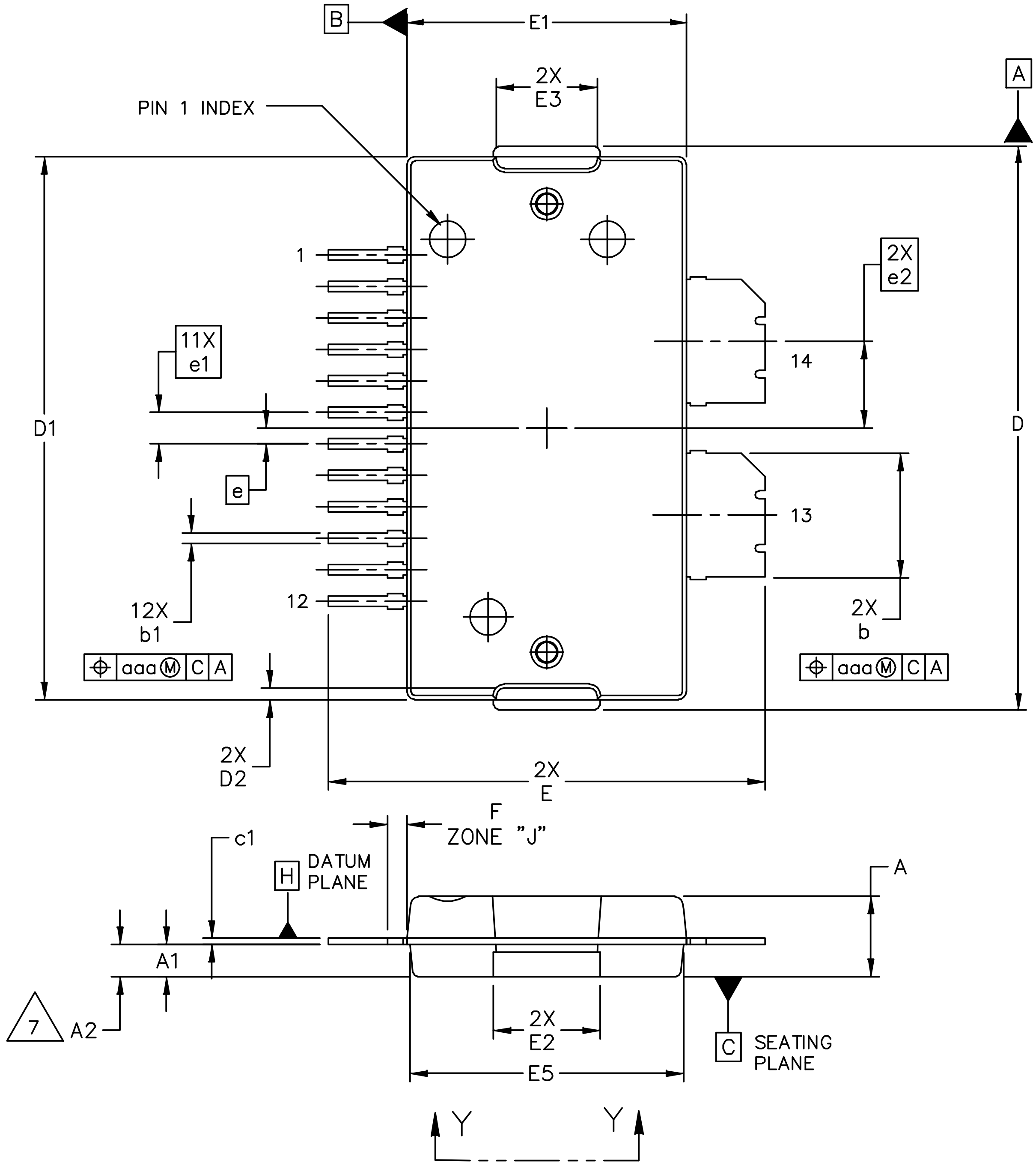

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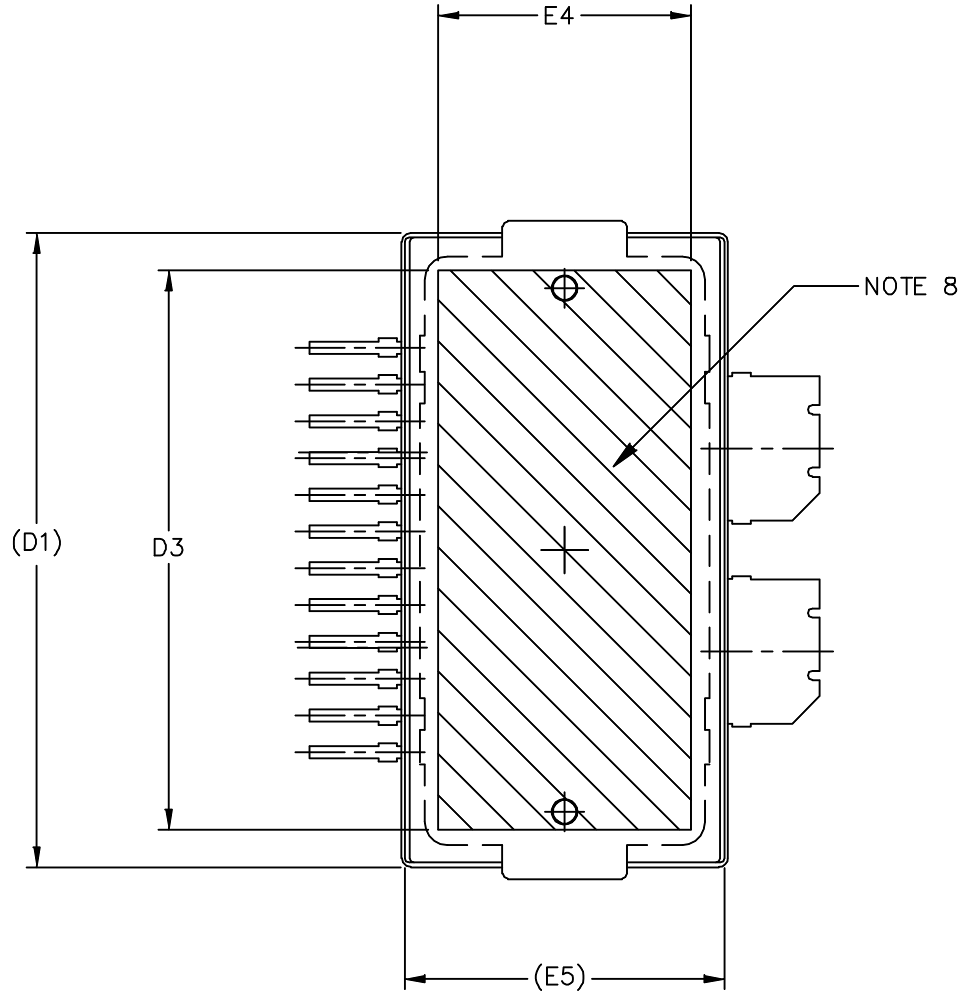

VIEW Y–Y

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	CASE NUMBER: 1618–02		19 JUN 2007
	STANDARD: NON–JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. DATUM PLANE —H— IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE —H—.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS —A— AND —B— TO BE DETERMINED AT DATUM PLANE —H—.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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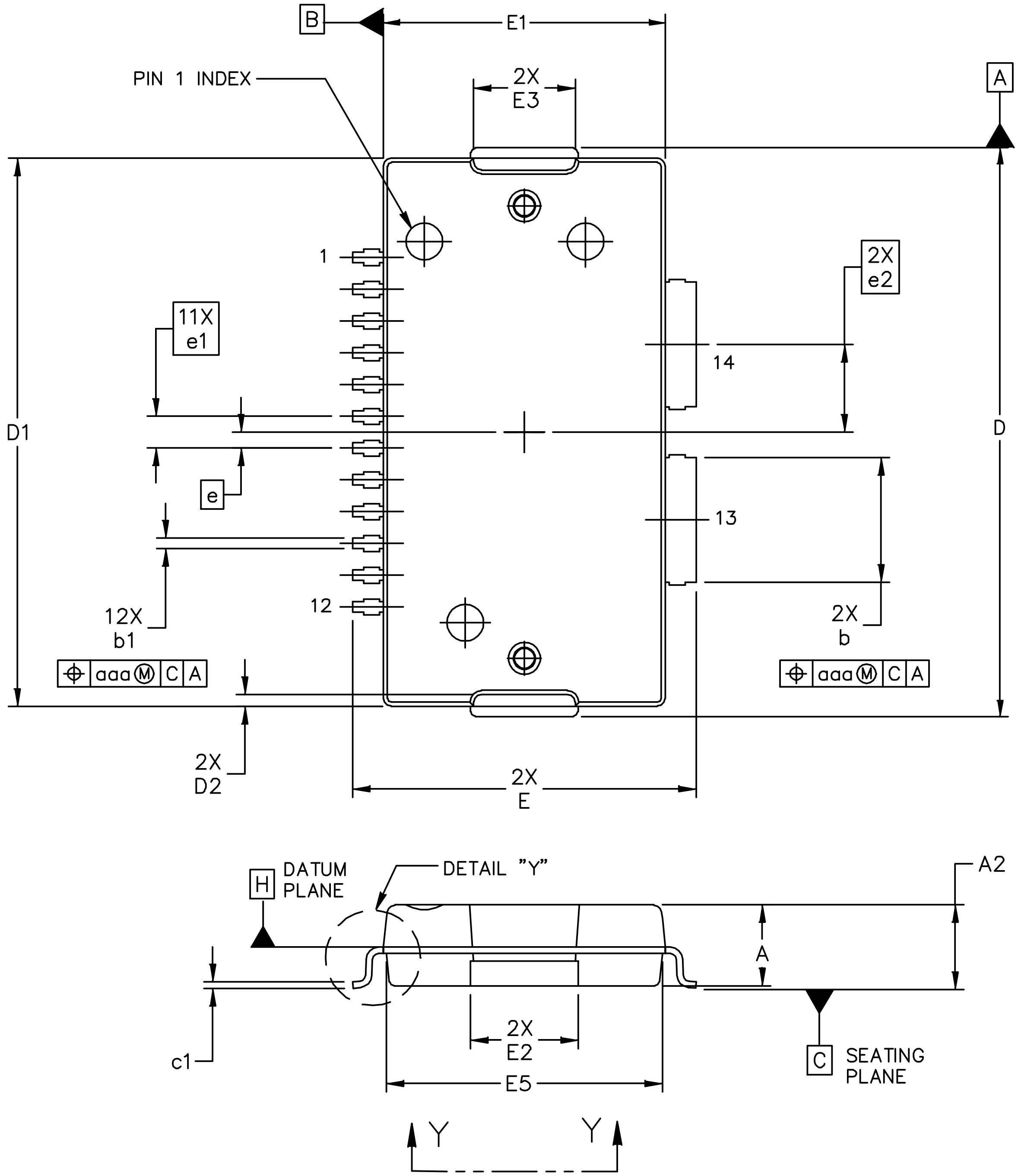
	STANDARD: NON—JEDEC	



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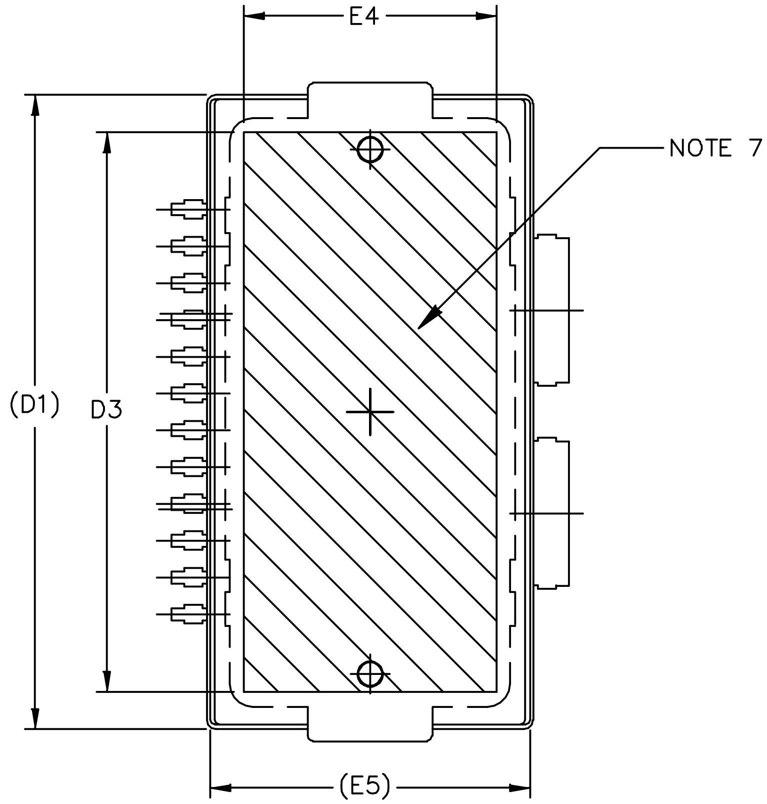
	CASE NUMBER: 1621−02	19 JUN 2007
	STANDARD: NON−JEDEC	



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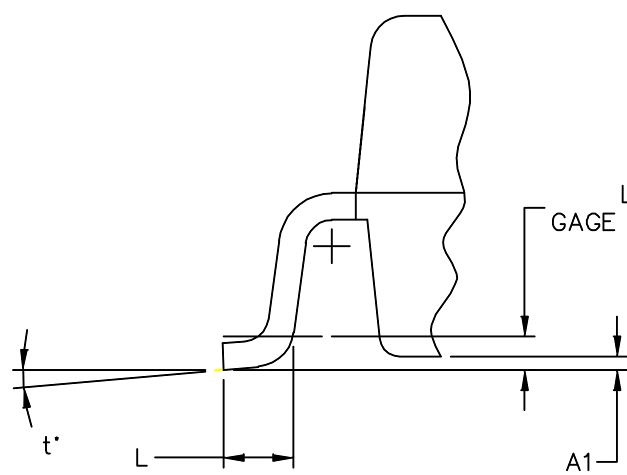

DETAIL "Y"

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	CASE NUMBER: 1621–02	19 JUN 2007
	STANDARD: NON–JEDEC	

NOTES:
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5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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	CASE NUMBER: 1621–02	19 JUN 2007
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PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2009	• Initial Release of Data Sheet
1	May 2010	• Corrected Thermal Characteristics table values for thermal resistance as follows: 50 W CW I_{DQ1B} changed from 6.1 to 8.2 °C/W and V_{GS2B} changed from 1.4 to 1.8 °C/W; 10 W CW I_{DQ1B} changed from 3.6 to 8.3 °C/W and V_{GS2B} changed from *Stage 2B is turned off to 1.9 °C/W. Thermal values now reflect the symmetrical Doherty nature of the device, p. 2 • Changed ESD Human Body Model rating from Class 1B to Class 0 to reflect recent ESD test results of the device, p. 3 • Added RF High Power Model availability to Product Software, p. 23

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