Freescale Semiconductor
Technical Data

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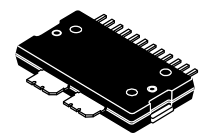
RoHS

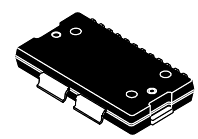
RF LDMOS Wideband Integrated Power Amplifiers

MD8IC925NR1
MD8IC925GNR1

728–960 MHz, 2.5 W AVG., 28 V SINGLE W–CDMA RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS



TO–270WB–14 PLASTIC MD8IC925NR1



TO–270WBG–14 PLASTIC MD8IC925GNR1

The MD8IC925N wideband integrated circuit is designed with on–chip matching that makes it usable from 728 to 960 MHz. This multi–stage structure is rated for 24 to 32 volt operation and covers all typical cellular base station modulation formats.

Driver Application — 900 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, $I_{DQ1(A+B)}$ = 58 mA, $I_{DQ2(A+B)}$ = 222 mA, P_{out} = 2.5 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
920 MHz	36.2	17.5	−48.9
940 MHz	36.2	17.4	−49.5
960 MHz	36.1	17.3	−49.1

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 940 MHz, 25 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 1 dB Compression Point ≃ 26 Watts CW

Driver Application — 700 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, $I_{DQ1(A+B)}$ = 58 mA, $I_{DQ2(A+B)}$ = 222 mA, P_{out} = 2.5 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
728 MHz	36.4	17.2	−48.9
748 MHz	36.4	17.6	−49.7
768 MHz	36.4	17.9	−50.5

Features

- Characterized with Series Equivalent Large–Signal Impedance Parameters and Common Source S–Parameters
- On–Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function [(1)]
- Integrated ESD Protection
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- 225°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13–inch Reel.

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1977 or AN1987.

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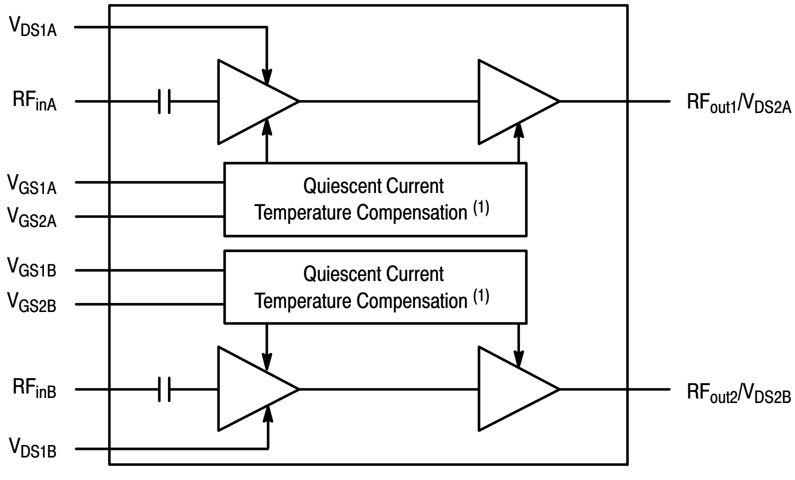
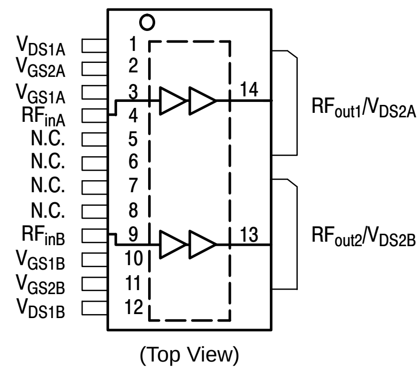


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	−0.5, +65	Vdc
Gate−Source Voltage	V_{GS}	−0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (2,3)	T_J	225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (3,4)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 2.5 W CW, 940 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA, 940 MHz Stage 2, 28 Vdc, $I_{DQ2(A+B)}$ = 222 mA, 940 MHz	$R_{\theta JC}$	 5.4 1.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22−A114)	1A
Machine Model (per EIA/JESD22−A115)	A
Charge Device Model (per JESD22−C101)	I

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22−A113, IPC/JEDEC J−STD−020	3	260	°C

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1977 or AN1987.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
4. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 − Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate−Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 − On Characteristics [1]					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 4 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA)	$V_{GS(Q)}$	—	2.4	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA, Measured in Functional Test)	$V_{GG(Q)}$	4.1	4.8	5.6	Vdc
Stage 2 − Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate−Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 − On Characteristics [1]					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 19 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ2(A+B)}$ = 222 mA)	$V_{GS(Q)}$	—	2.15	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ2(A+B)}$ = 222 mA, Measured in Functional Test)	$V_{GG(Q)}$	3.5	4.3	5.0	Vdc
Drain−Source On−Voltage (V_{GS} = 10 Vdc, I_D = 190 Adc)	$V_{DS(on)}$	0.1	0.21	1.2	Vdc

Functional Tests [2,3] (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA, $I_{DQ2(A+B)}$ = 222 mA, P_{out} = 2.5 W Avg., f = 940 MHz, Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	34.5	36.2	39.5	dB
Power Added Efficiency	PAE	15.5	17.4	—	%
Adjacent Channel Power Ratio	ACPR	—	−49.5	−47.0	dBc
Input Return Loss	IRL	—	−27	−10	dB

Typical Performance over Frequency (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA, $I_{DQ2(A+B)}$ = 222 mA, P_{out} = 2.5 W Avg, Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)	IRL (dB)
920 MHz	36.2	17.5	−48.9	−27
940 MHz	36.2	17.4	−49.5	−27
960 MHz	36.1	17.3	−49.1	−28

1. Each side of device measured separately.
2. Part internally matched both on input and output.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.

(continued)

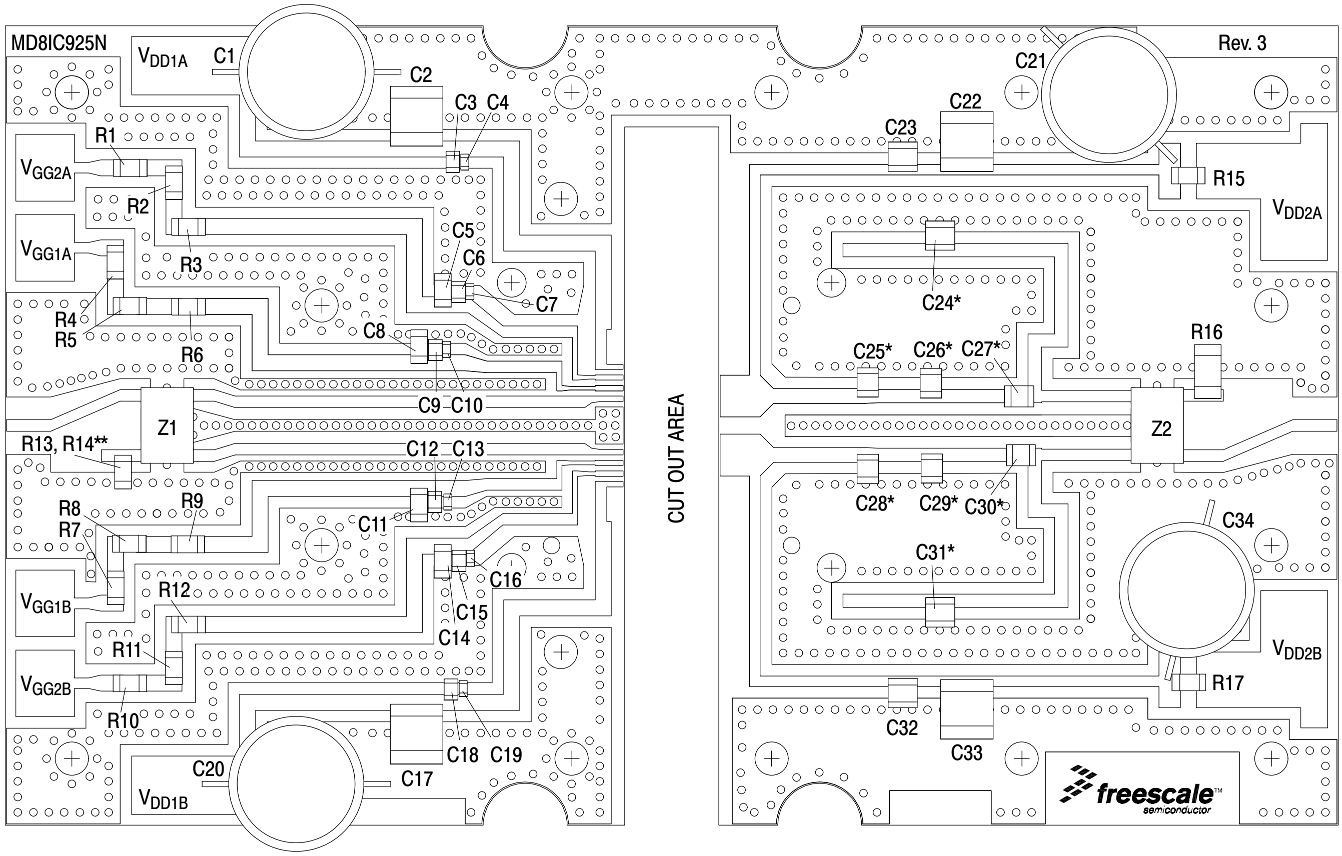
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA, $I_{DQ2(A+B)}$ = 222 mA, 920−960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	26	—	W
P_{out} @ 3 dB Compression Point, CW	P3dB	—	31	—	W
IMD Symmetry @ 28 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	20	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	75	—	MHz
Quiescent Current Accuracy over Temperature [1,2]	ΔI_{QT}				%
with 18 kΩ Gate Feed Resistors (−30 to 85°C) Stage 1		—	1.1	—	
with 20 kΩ Gate Feed Resistors (−30 to 85°C) Stage 2		—	1.9	—	
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 2.5 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (−30°C to +85°C)	ΔG	—	0.043	—	dB/°C
Output Power Variation over Temperature (−30°C to +85°C)	ΔP1dB	—	0.004	—	dB/°C

Typical Performance over Frequency (In Freescale 700 MHz Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA, $I_{DQ2(A+B)}$ = 222 mA, P_{out} = 2.5 W Avg., Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)	IRL (dB)
728 MHz	36.4	17.2	−48.9	−17
748 MHz	36.4	17.6	−49.7	−17
768 MHz	36.4	17.9	−50.5	−18

1. Each side of device measured separately.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1977 or AN1987.



*C24, C25, C26, C27, C28, C29, C30 and C31 are mounted vertically.
**R13 and R14 are stacked.

Figure 3. MD8IC925NR1 Test Circuit Component Layout — 920−960 MHz

Table 6. MD8IC925NR1 Test Circuit Component Designations and Values — 920−960 MHz

Part	Description	Part Number	Manufacturer
C1, C20, C21, C34	220 μF, 100 V Electrolytic Capacitors	EEV−FK2A221M	Panasonic−ECG
C2, C17, C22, C33	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C3, C6, C9, C12, C15, C18	0.01 μF Chip Capacitors	C0805C103K5RAC	Kemet
C4, C7, C10, C13, C16, C19	47 pF Chip Capacitors	ATC600F470JT250XT	ATC
C5, C8, C11, C14	1 μF Chip Capacitors	C3225X7R2A105KT	TDK
C23, C24, C31, C32	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C25, C28	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C26, C29	2.2 pF Chip Capacitors	ATC100B2R2JT500XT	ATC
C27, C30	4.3 pF Chip Capacitors	ATC100B4R3CT500XT	ATC
R1, R4, R7, R10	0 Ω, 3 A Chip Jumpers	CRCW12060000Z0EA	Vishay
R2, R3, R5, R6, R8, R9, R11, R12	1 kΩ, 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
R13, R14	100 Ω, 1/4 W Chip Resistors	CRCW1206100RFKEA	Vishay
R15, R17	0 Ω, 2 A Chip Jumpers	WCR1206−R005J	Welwyn
R16	50 Ω, 10 W Chip Resistor	81A7031−50−5F	Florida RF Labs
Z1, Z2	815−960 MHz Band, 90°, 3 dB Chip Hybrid Couplers	GSC362−HYB0900	Soshin
PCB	0.020″, ε_r = 3.55	RF35	Taconic

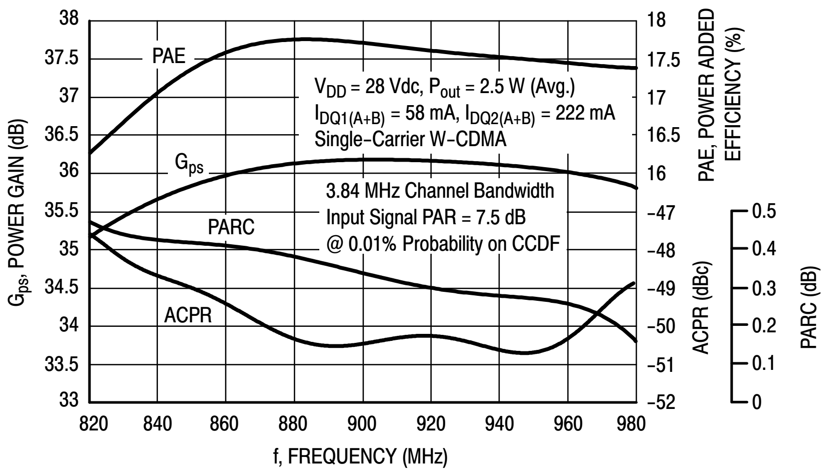


Figure 4. Output Peak−to−Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 2.5 Watts Avg.

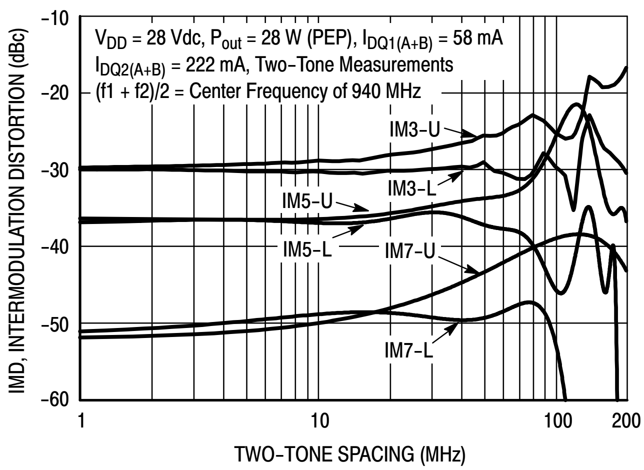


Figure 5. Intermodulation Distortion Products versus Two−Tone Spacing

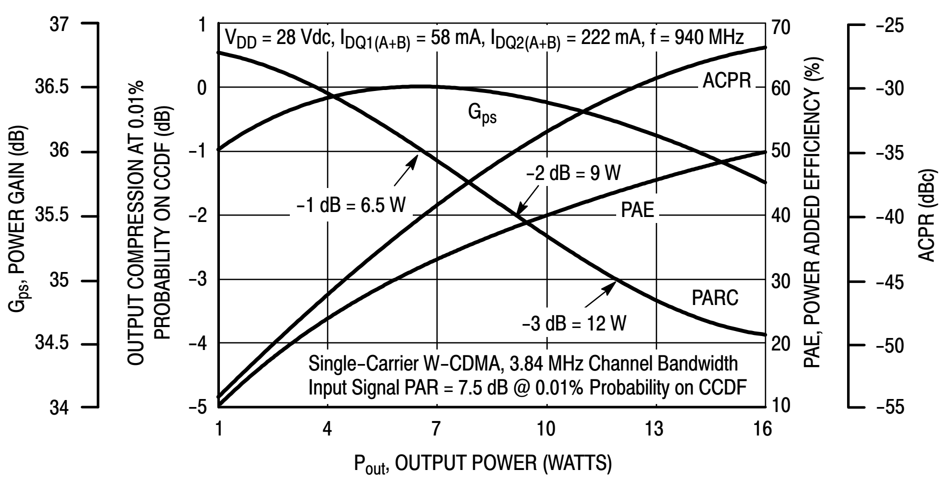


Figure 6. Output Peak−to−Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

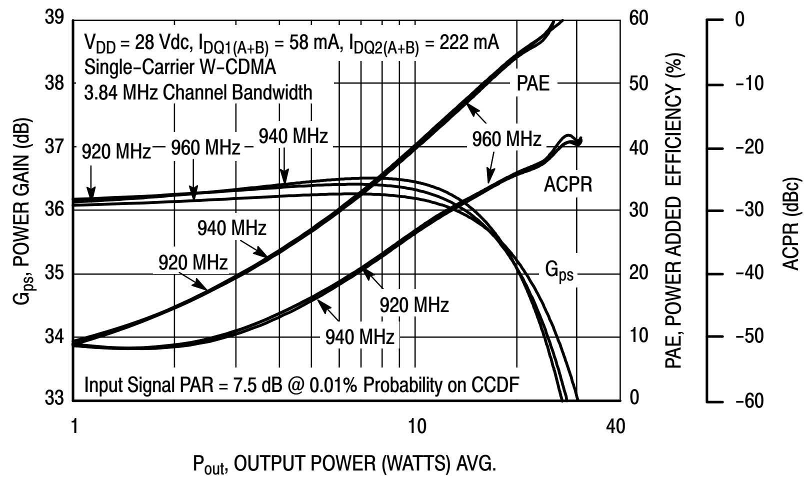


Figure 7. Single−Carrier W−CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

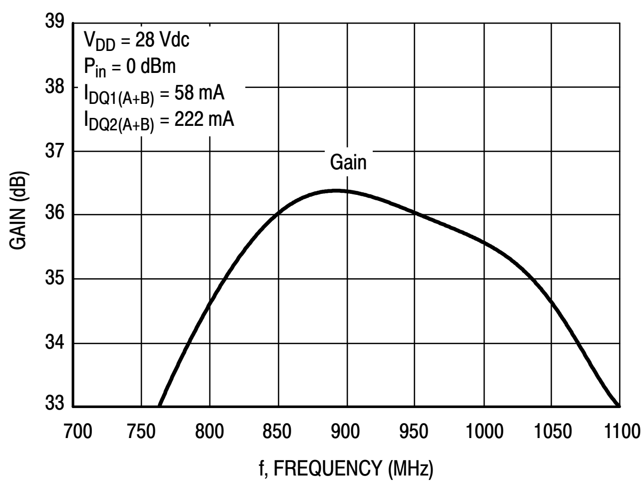


Figure 8. Broadband Frequency Response

W−CDMA TEST SIGNAL

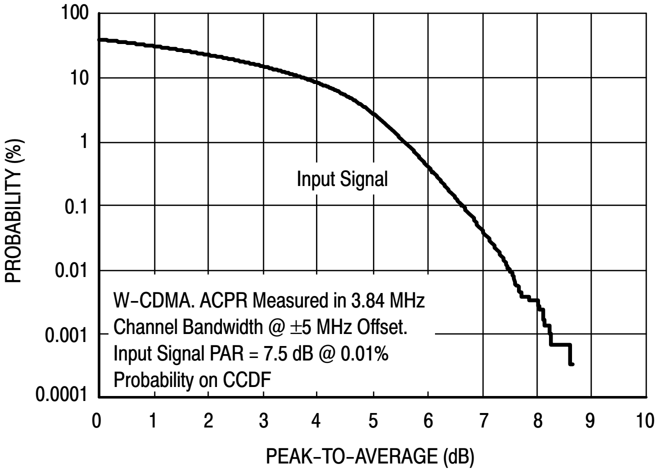


Figure 9. CCDF W−CDMA IQ Magnitude Clipping, Single−Carrier Test Signal

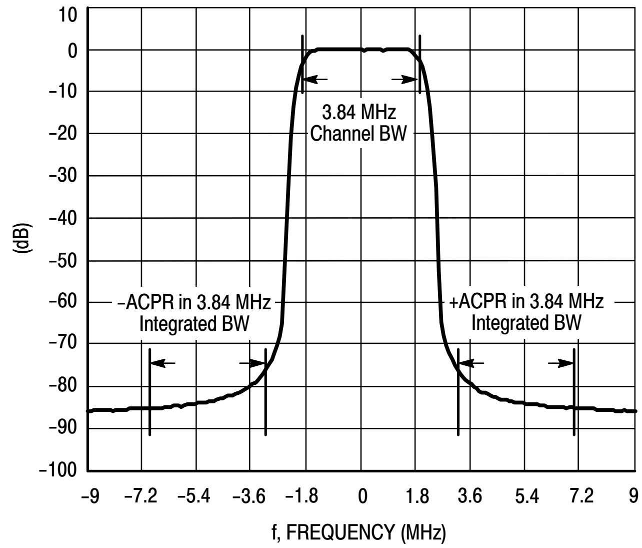


Figure 10. Single−Carrier W−CDMA Spectrum

V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA, $I_{DQ2(A+B)}$ = 222 mA, P_{out} = 2.5 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
820	47.9 + j2.34	7.51 + j5.45
840	47.9 + j2.47	7.62 + j5.42
860	47.8 + j2.61	7.60 + j5.41
880	47.8 + j2.75	7.48 + j5.44
900	47.7 + j2.89	7.27 + j5.55
920	47.7 + j3.04	7.00 + j5.74
940	47.7 + j3.19	6.71 + j6.01
960	47.6 + j3.34	6.40 + j6.37
980	47.6 + j3.49	6.10 + j6.79

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

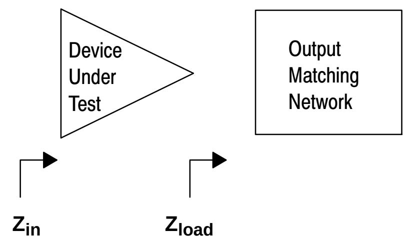


Figure 11. Series Equivalent Input and Load Impedance

V_{DD} = 28 Vdc, I_{DQ1A} = 21 mA, I_{DQ2A} = 101 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
920	59.9 − j18.3	56.8 + j19.1	10.9 + j2.37	32.4	43.0	20	57.8	−4.9
940	60.7 − j18.5	61.2 + j14.3	12.4 + j1.56	32.2	42.9	20	54.9	−5.2
960	62.9 − j10.5	64.5 + j8.82	14.8 + j0.656	31.9	42.9	20	55.1	−5.2

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
920	59.9 − j18.3	56.9 + j16.9	10.7 + j1.54	30.1	43.8	24	57.2	−5.4
940	60.7 − j18.5	60.8 + j12.3	11.7 + j1.11	30.0	43.7	24	55.6	−5.6
960	62.9 − j10.5	64.5 + j8.82	14.8 + j0.656	31.9	42.9	20	55.1	−5.2

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Figure 12. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 21 mA, I_{DQ2A} = 101 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

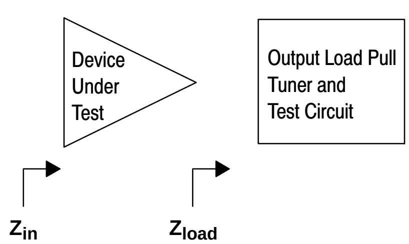
			Max Power Added Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
920	59.9 − j18.3	60.9 + j20.8	11.1 + j10.9	34.2	41.3	13	66.4	−6.7
940	60.7 − j18.5	66.5 + j16.0	10.0 + j11.8	34.4	40.7	12	63.5	−7.8
960	62.9 − j10.5	69.0 + j9.28	11.6 + j11.5	33.9	40.9	12	63.3	−6.8

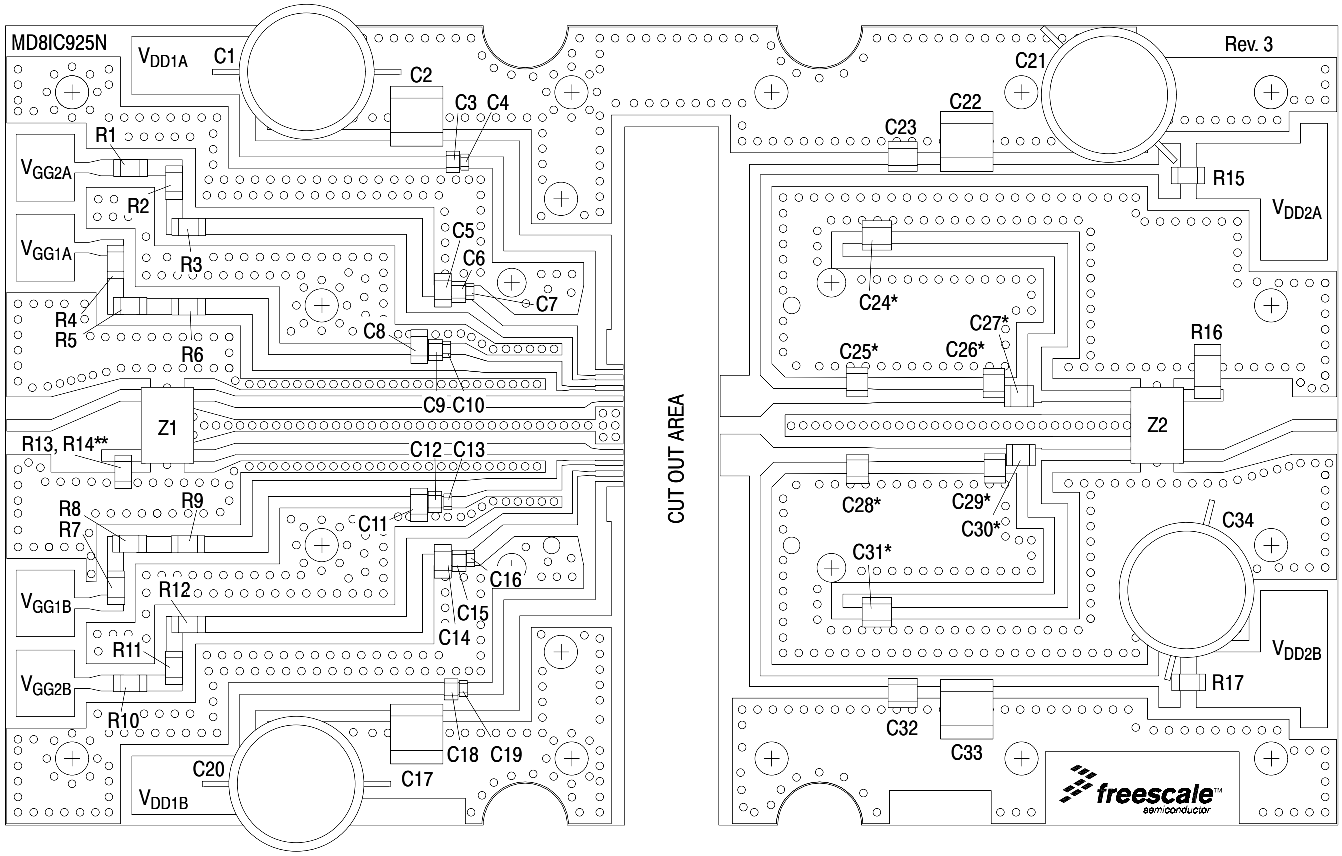
			Max Power Added Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
920	59.9 − j18.3	59.7 + j19.9	9.03 + j9.12	32.3	42.2	17	65.3	−9.9
940	60.7 − j18.5	64.3 + j14.2	10.5 + j9.80	32.1	42.0	16	62.3	−7.6
960	62.9 − j10.5	69.0 + j9.28	11.6 + j11.5	33.9	40.9	12	63.3	−6.8

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Figure 13. Load Pull Performance — Maximum Power Added Efficiency Tuning





*C24, C25, C26, C27, C28, C29, C30 and C31 are mounted vertically.
**R13 and R14 are stacked.

Figure 14. MD8IC925NR1 Test Circuit Component Layout — 728−768 MHz

Table 7. MD8IC925NR1 Test Circuit Component Designations and Values — 728−768 MHz

Part	Description	Part Number	Manufacturer
C1, C20, C21, C34	220 μF, 100 V Electrolytic Capacitors	EEV−FK2A221M	Panasonic−ECG
C2, C17, C22, C33	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C3, C6, C9, C12, C15, C18	0.01 μF Chip Capacitors	C0805C103K5RAC	Kemet
C4, C7, C10, C13, C16, C19	47 pF Chip Capacitors	ATC600F470JT250XT	ATC
C5, C8, C11, C14	1 μF Chip Capacitors	C3225X7R2A105KT	TDK
C23, C24, C31, C32	68 pF Chip Capacitors	ATC100B680JT500XT	ATC
C25, C28	2.2 pF Chip Capacitors	ATC100B2R2JT500XT	ATC
C26, C27, C29, C30	5.6 pF Chip Capacitors	ATC100B5R6CT500XT	ATC
R1, R4, R7, R10	0 Ω, 3 A Chip Jumpers	CRCW12060000Z0EA	Vishay
R2, R3, R5, R6, R8, R9, R11, R12	1 kΩ, 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
R13, R14	100 Ω, 1/4 W Chip Resistors	CRCW1206100RFKEA	Vishay
R15, R17	0 Ω, 2 A Chip Jumpers	WCR1206−R005J	Welwyn
R16	50 Ω, 10 W Chip Resistor	81A7031−50−5F	Florida RF Labs
Z1, Z2	815−960 MHz Band, 90°, 3 dB Chip Hybrid Couplers	GSC362−HYB0900	Soshin
PCB	0.020″, ε_r = 3.55	RF35	Taconic

ALTERNATIVE CHARACTERIZATION — 728−768 MHz

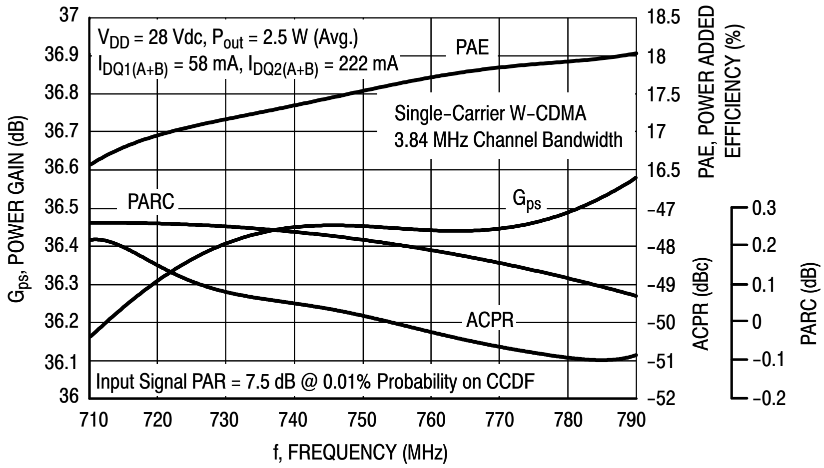


Figure 15. Output Peak−to−Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 2.5 Watts Avg.

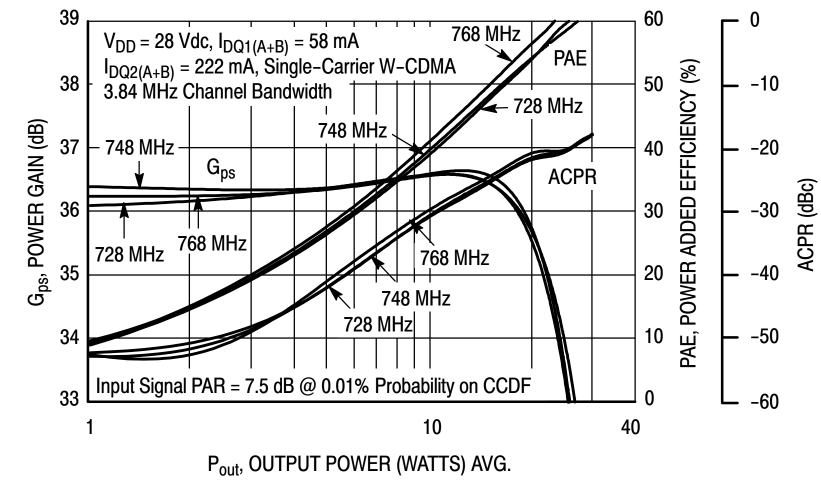


Figure 16. Single−Carrier W−CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

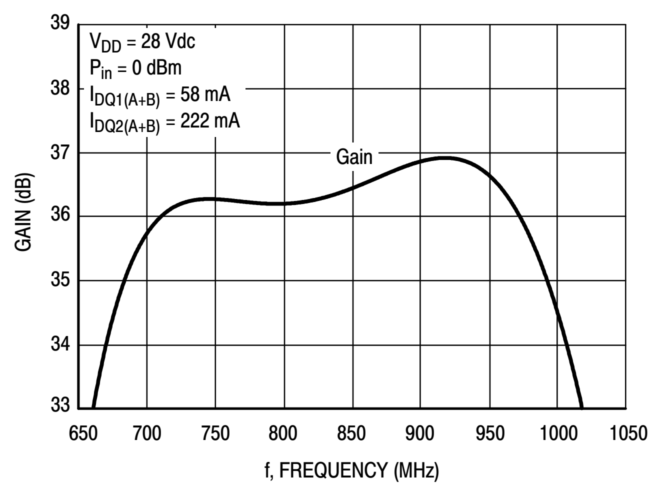


Figure 17. Broadband Frequency Response

V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 58 mA, $I_{DQ2(A+B)}$ = 222 mA, P_{out} = 2.5 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
710	48.2 + j1.65	8.02 + j6.72
720	48.2 + j1.71	8.43 + j6.89
730	48.2 + j1.77	8.64 + j7.04
740	48.1 + j1.83	8.84 + j7.17
750	48.0 + j1.89	9.01 + j7.29
760	48.1 + j1.95	9.16 + j7.39
770	48.0 + j2.01	9.28 + j7.49
780	48.0 + j2.08	9.38 + j7.59
790	48.0 + j2.14	9.45 + j7.68

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

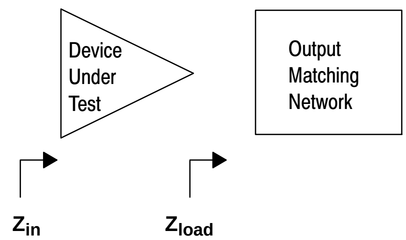


Figure 18. Series Equivalent Input and Load Impedance — 728−768 MHz

V_{DD} = 28 Vdc, I_{DQ1A} = 21 mA, I_{DQ2A} = 101 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power						
			P1dB						
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
730	25.7 − j5.86	24.7 + j3.12	8.35 + j5.97	34.0	42.7	19	58.9	−3.6
750	24.8 − j8.46	24.8 + j6.48	8.50 + j5.61	33.9	42.8	19	57.8	−2.6
770	27.5 − j12.2	26.5 + j10.4	10.0 + j4.28	33.7	43.1	20	60.0	−3.0

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
730	25.7 − j5.86	25.7 + j3.64	8.59 + j4.89	31.6	43.5	23	60.0	−6.0
750	24.8 − j8.46	26.0 + j6.61	8.40 + j4.59	31.5	43.6	23	58.2	−4.4
770	27.5 − j12.2	26.5 + j10.4	10.0 + j4.28	33.7	43.1	20	60.0	−3.0

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Figure 19. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 21 mA, I_{DQ2A} = 101 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

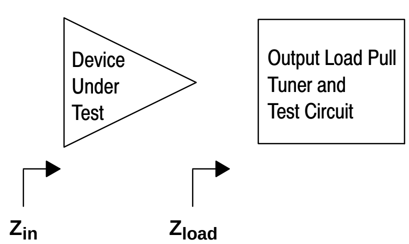
			Max Power Added Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
730	25.7 − j5.86	23.9 + j6.61	14.0 + j13.4	36.2	40.7	12	68.0	−6.4
750	24.8 − j8.46	24.2 + j10.2	12.4 + j13.8	36.5	40.5	11	66.0	−6.1
770	27.5 − j12.2	25.7 + j14.3	11.4 + j13.5	36.3	41.0	13	70.5	−8.2

			Max Power Added Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	PAE (%)	AM/PM (°)
730	25.7 − j5.86	24.1 + j6.09	11.2 + j12.4	34.4	41.6	14	69.4	−11
750	24.8 − j8.46	25.3 + j9.02	12.0 + j11.3	34.0	42.0	16	67.8	−6.3
770	27.5 − j12.2	25.7 + j14.3	11.4 + j13.5	36.3	41.0	13	70.5	−8.2

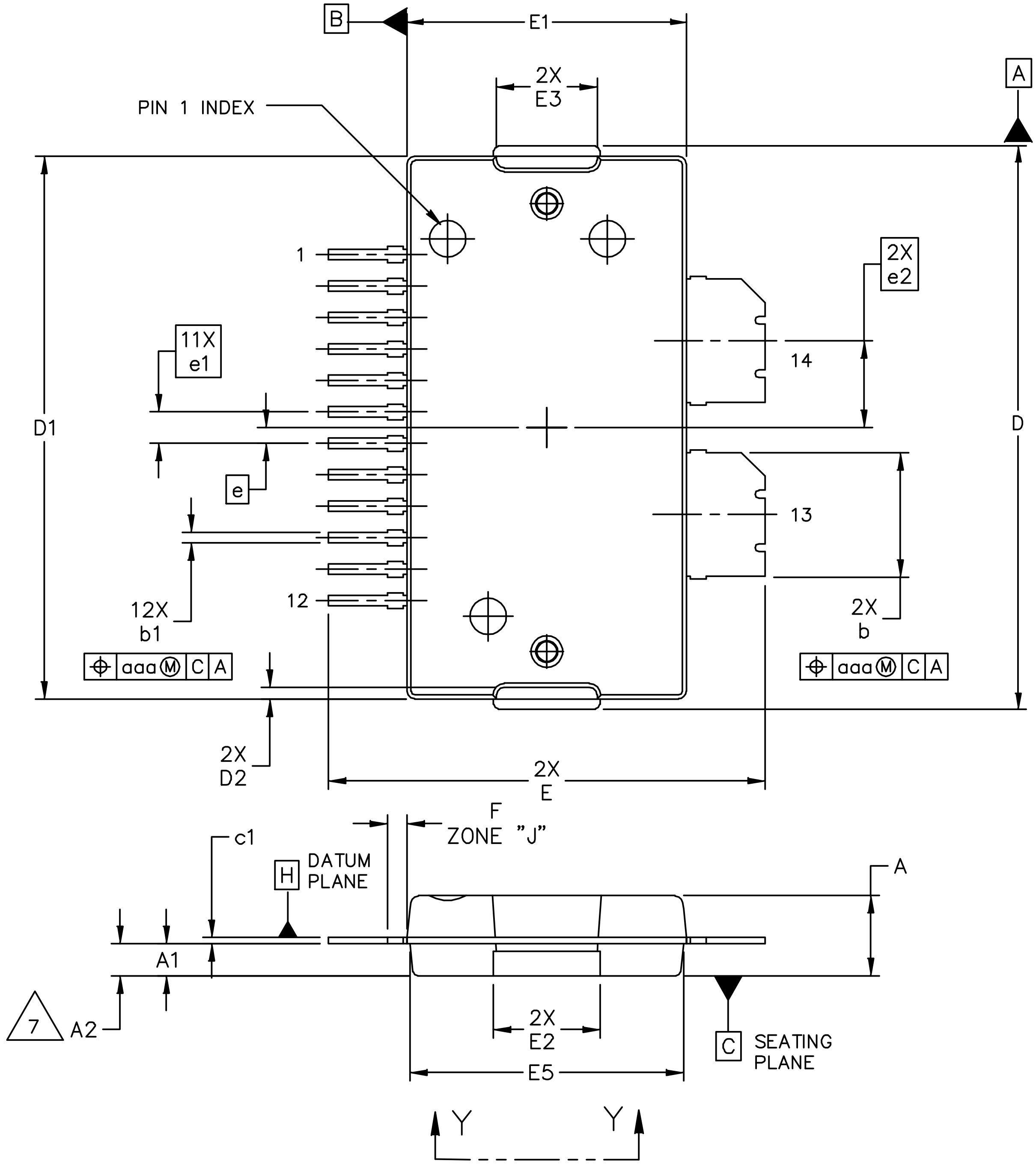
(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Figure 20. Load Pull Performance — Maximum Power Added Efficiency Tuning



PACKAGE DIMENSIONS



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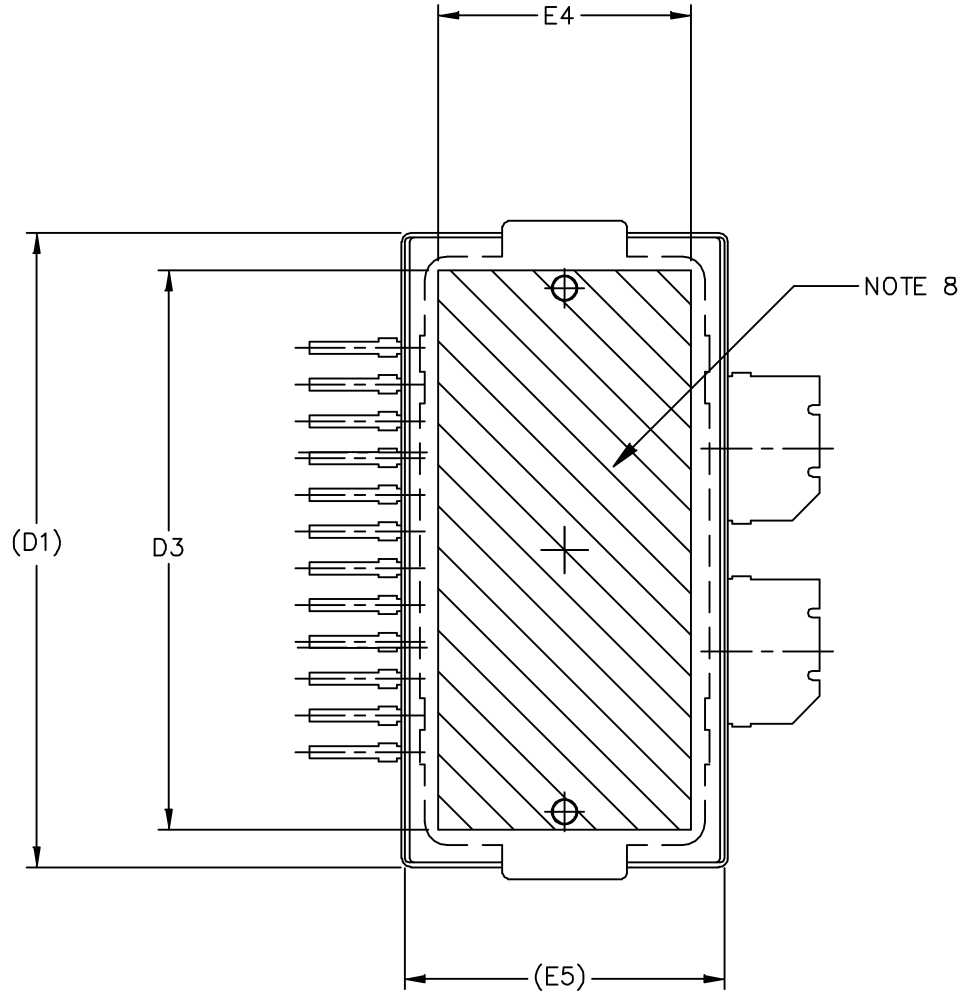
TITLE: TO–270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: A
	CASE NUMBER: 1618–02	19 JUN 2007
	STANDARD: NON–JEDEC	



VIEW Y–Y

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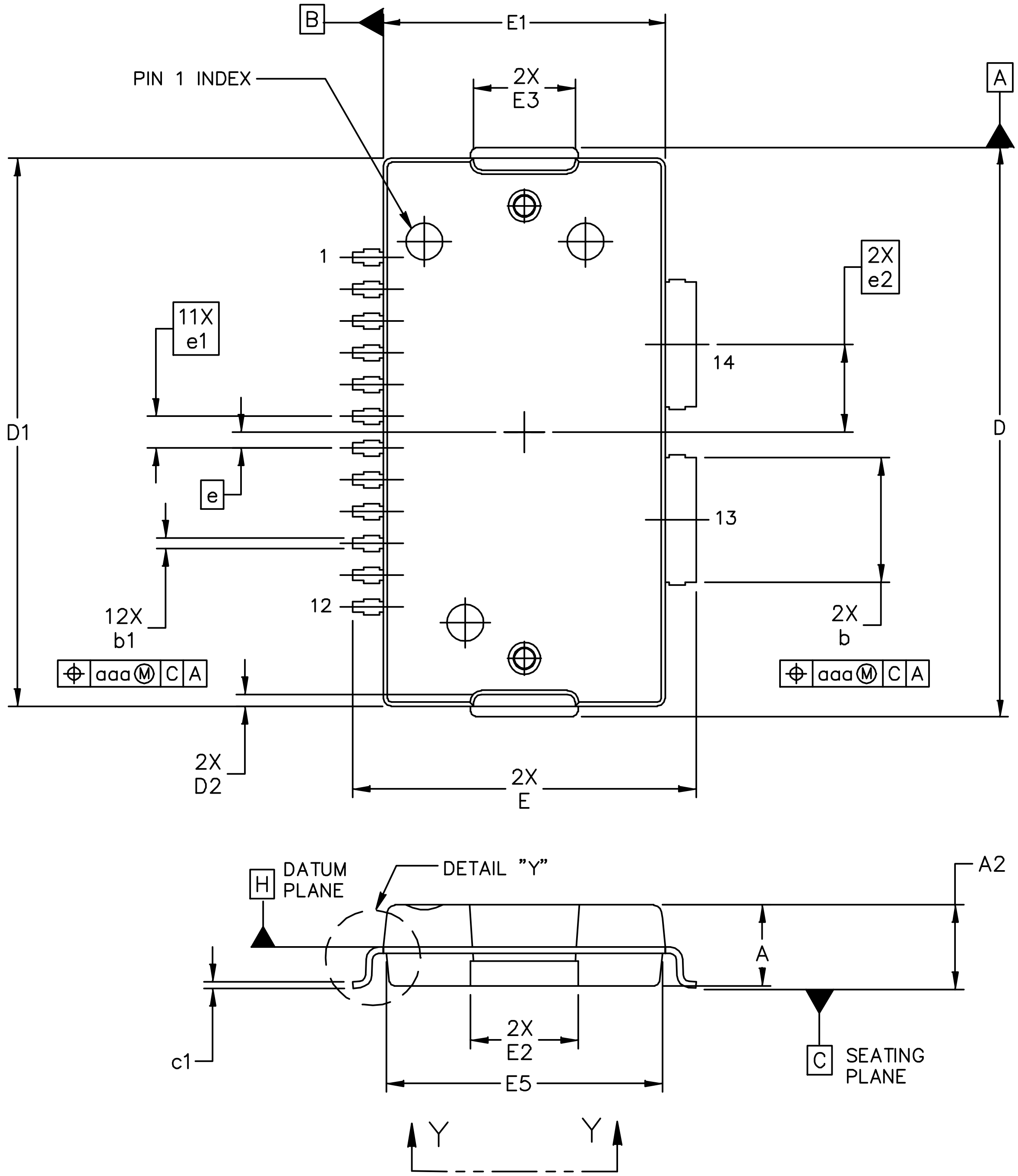
	CASE NUMBER: 1618–02	19 JUN 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DATUM PLANE −H− IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	−−−	15.24	−−−	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	−−−	6.86	−−−					
E5	.346	.350	8.79	8.89					

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO−270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: A
	CASE NUMBER: 1618−02	19 JUN 2007
	STANDARD: NON−JEDEC	



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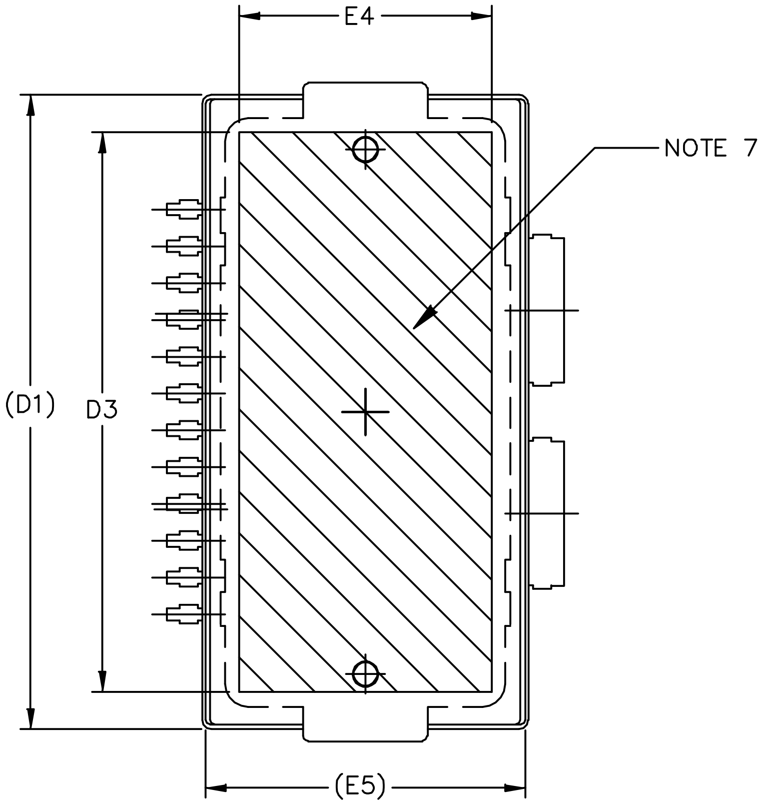
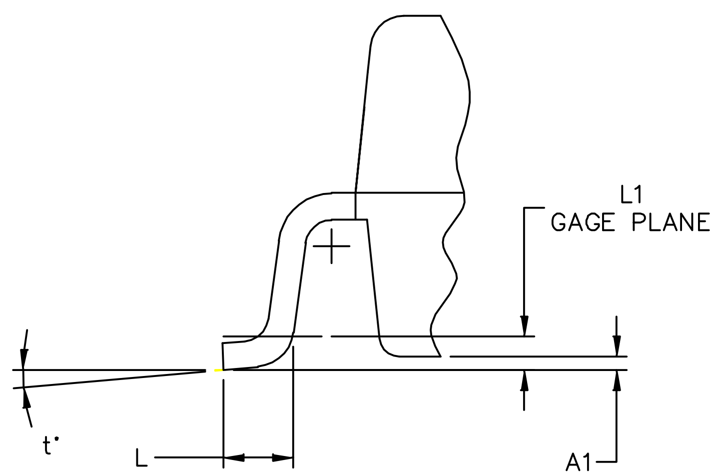
	CASE NUMBER: 1621–02		19 JUN 2007
	STANDARD: NON–JEDEC		



VIEW Y–Y



DETAIL "Y"

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
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	CASE NUMBER: 1621–02	19 JUN 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3789: Clamping of High Power RF Transistors and RFICs in Over−Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2013	• Initial Release of Data Sheet

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