

RF LDMOS Wideband 2-Stage Power Amplifiers

Designed for broadband commercial and industrial applications with frequencies from 132 MHz to 960 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment. These devices have a 2-stage design with off-chip matching for the input, interstage and output networks to cover the desired frequency band.

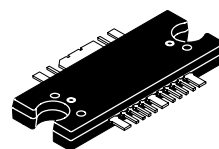
- Typical Performance: 800 MHz, 28 Volts, $I_{DQ1} = 80$ mA, $I_{DQ2} = 650$ mA, $P_{out} = 70$ Watts PEP
Power Gain — 30 dB
Drain Efficiency — 48%
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 850 MHz, 70 Watts CW Output Power

Features

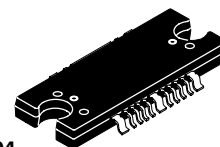
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MW5IC970NBR1
MW5IC970GNBR1

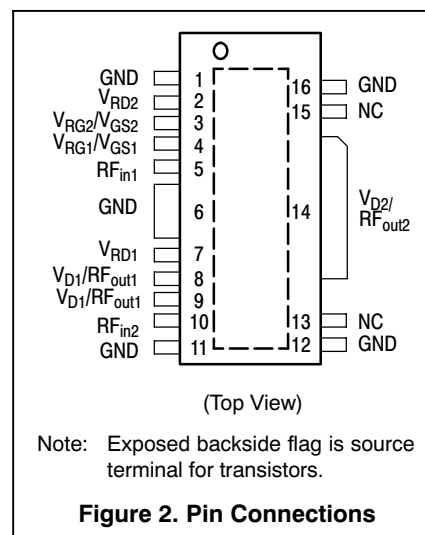
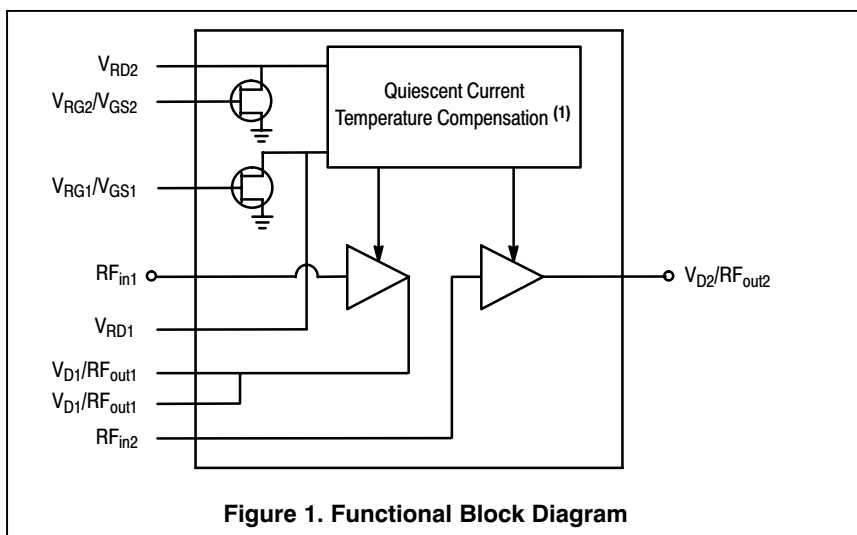
800-900 MHz, 70 W, 28 V
RF LDMOS WIDEBAND
2-STAGE POWER AMPLIFIERS



CASE 1329-09
TO-272 WB-16
PLASTIC
MW5IC970NBR1



CASE 1329A-04
TO-272 WB-16 GULL
PLASTIC
MW5IC970GNBR1



1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value ⁽¹⁾	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Final Application ($P_{out} = 70$ W CW)	Stage 1, 28 Vdc, $I_{DQ} = 80$ mA Stage 2, 28 Vdc, $I_{DQ} = 650$ mA	5.2 0.8	
EDGE Application ($P_{out} = 35$ W CW)	Stage 1, 28 Vdc, $I_{DQ} = 80$ mA Stage 2, 28 Vdc, $I_{DQ} = 650$ mA	5.3 0.8	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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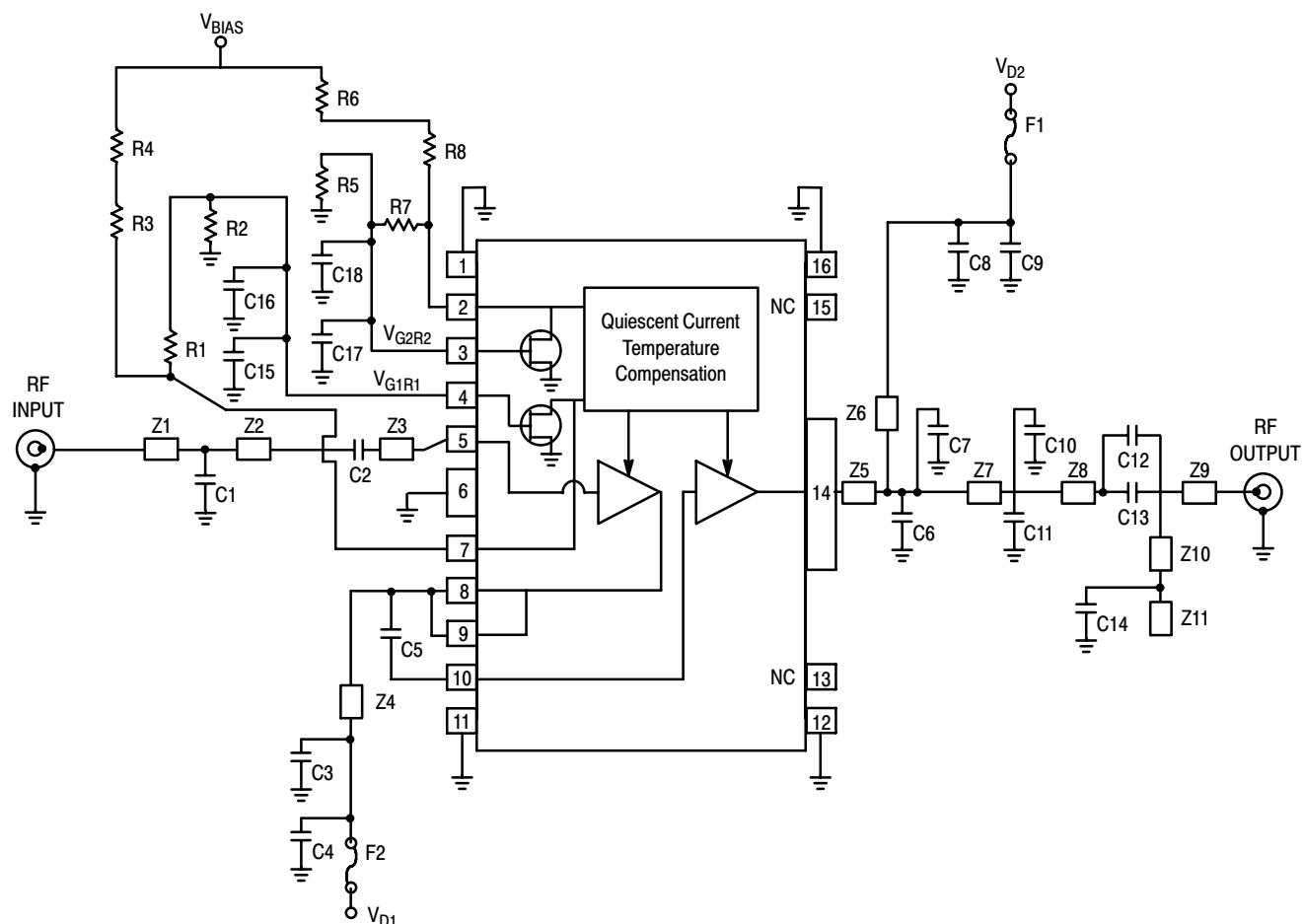
Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28.5$ Vdc, $I_{DQ1} = 80$ mA, $I_{DQ2} = 650$ mA, $P_{out} = 70$ W PEP, $f_1 = 870.0$ MHz, $f_2 = 870.1$ MHz

Power Gain	G_{ps}	26.5	30	34.5	dB
Drain Efficiency	η_D	40	48	—	%
Input Return Loss	IRL	—	-12	-10	dB
Intermodulation Distortion	IMD	—	-33	-28	dBc

Typical 800/900 MHz Performances (In Freescale 800/900 MHz Reference Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQ1} = 80$ mA, $I_{DQ2} = 650$ mA, 740-870 MHz, 870-960 MHz

Gain Flatness in 30 MHz Bandwidth @ $P_{out} = 70$ W CW	G_F	—	2	—	dB
Gain Flatness in 30 MHz Instantaneous Bandwidth @ $P_{out} = 70$ W CW	G_F	—	0.2	—	dB
Delay @ $P_{out} = 70$ W CW Including Output Matching	Delay	—	4.5	—	ns
Part-to-Part Phase Variation @ $P_{out} = 70$ W CW	$\Delta\Phi$	—	± 15	—	°

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.



Z1	0.485" x 0.066" Microstrip	Z7	0.040" x 0.233" Microstrip
Z2	0.270" x 0.040" Microstrip	Z8	0.450" x 0.120" Microstrip
Z3	0.068" x 0.020" Microstrip	Z9	0.100" x 0.066" Microstrip
Z4	0.950" x 0.040" Microstrip	Z10	1.000" x 0.040" Microstrip
Z5	0.131" x 0.233" Microstrip	Z11	0.148" x 0.040" Microstrip
Z6	0.797" x 0.050" Microstrip	PCB	Rogers 4350B, 0.030", $\epsilon_r = 3.5$

Figure 3. MW5IC970NBR1 (GNBR1) Test Circuit Schematic

Table 6. MW5IC970NBR1 (GNBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C10, C11	3.9 pF Chip Capacitors	ATC600S3R9BT250T	ATC
C2	56 pF Chip Capacitor	ATC600S560JT250T	ATC
C3, C8, C14, C15, C17	39 pF Chip Capacitors	GRM40001C0G390J050BD	Murata
C4, C9	10 μ F Chip Capacitors	ECJ4YF1H106Z	Panasonic
C5	24 pF Chip Capacitor	ATC600F240JT250T	ATC
C6, C7	15 pF Chip Capacitors	ATC600F150JT250T	ATC
C12	4.7 pF Chip Capacitor	ATC600F4R7BT250T	ATC
C13	0.4 pF Chip Capacitor	ATC600F0R4BT250T	ATC
C16, C18, C19, C20	0.015 μ F Chip Capacitors	GRM400X7R153J050BD	Murata
F1	5A Surface Mount Fuse	1FT5A	Little Fuse
F2	1A Surface Mount Fuse	1FT1A	Little Fuse
R1, R7	681 Ω , 1/8 W Chip Resistors	CRCW08056810FKEA	Vishay
R2, R5	4.75 k Ω , 1/8 W Chip Resistors	CRCW08054751FKEA	Vishay
R3, R4, R8	1.21 k Ω , 1/8 W Chip Resistors	CRCW08051211FKEA	Vishay
R6	267 Ω , 1/8 W Chip Resistor	CRCW08052670FKEA	Vishay

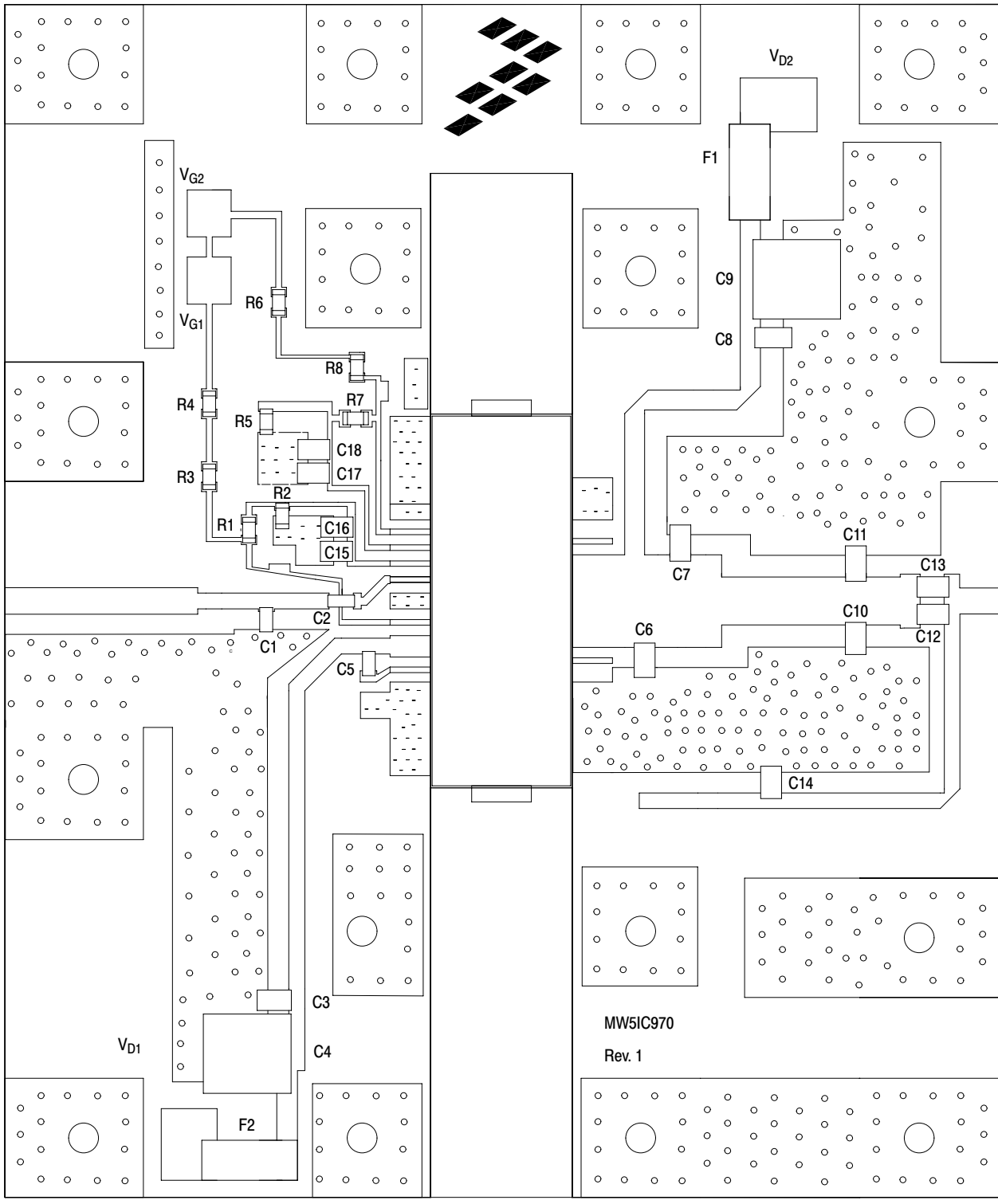


Figure 4. MW5IC970NBR1(GNBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

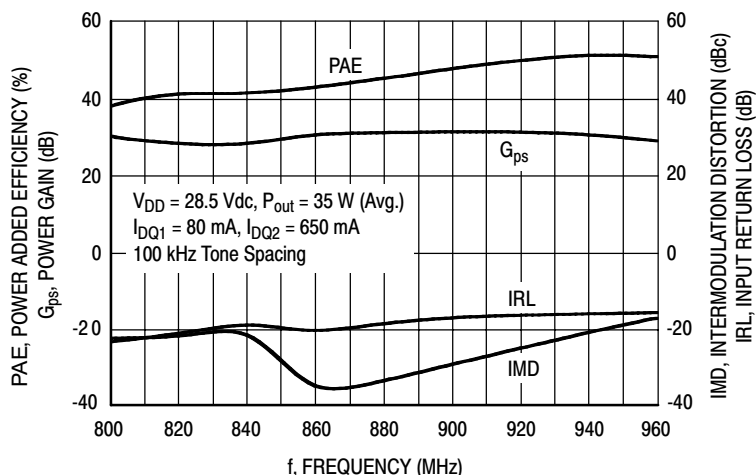


Figure 5. Two-Tone Wideband Performance @ $P_{out} = 35$ Watts (Avg.)

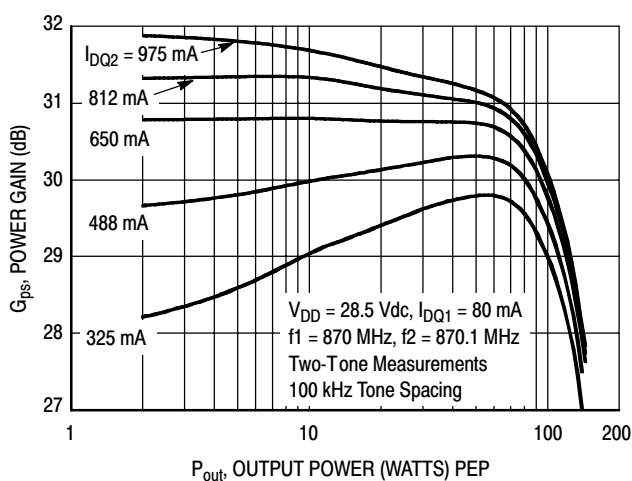


Figure 6. Two-Tone Power Gain versus Output Power

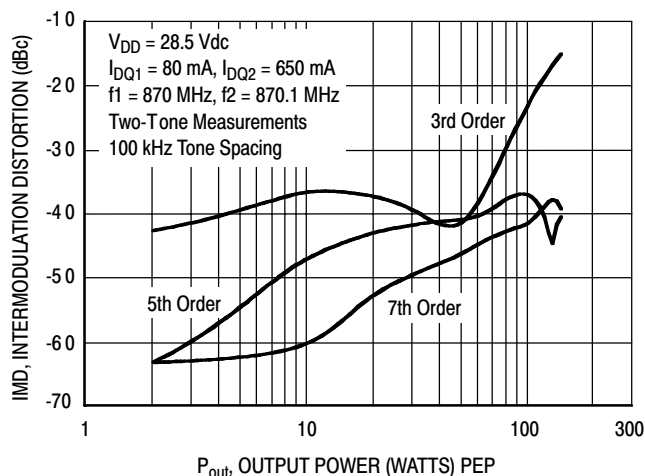


Figure 7. Intermodulation Distortion Products versus Output Power

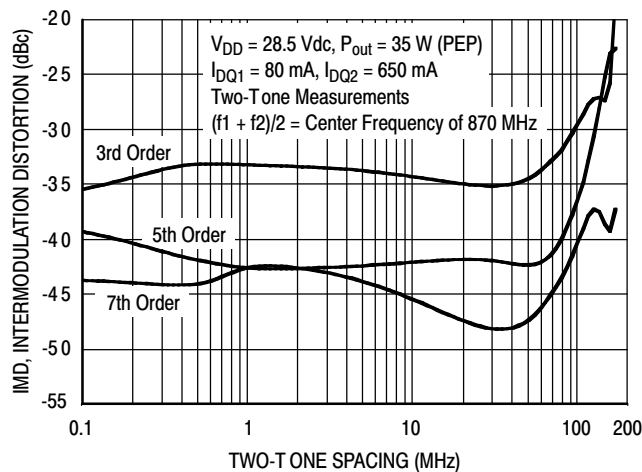


Figure 8. Intermodulation Distortion Products versus Tone Spacing

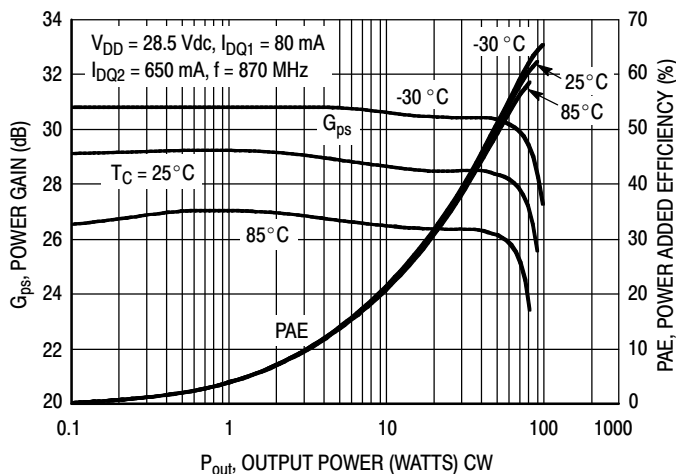


Figure 9. Power Gain and Power Added Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS

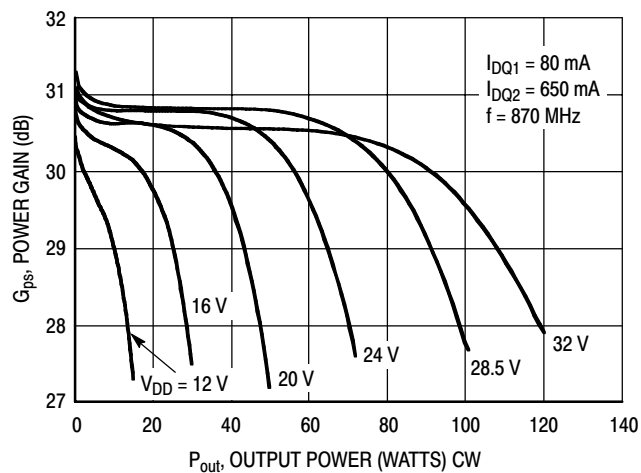
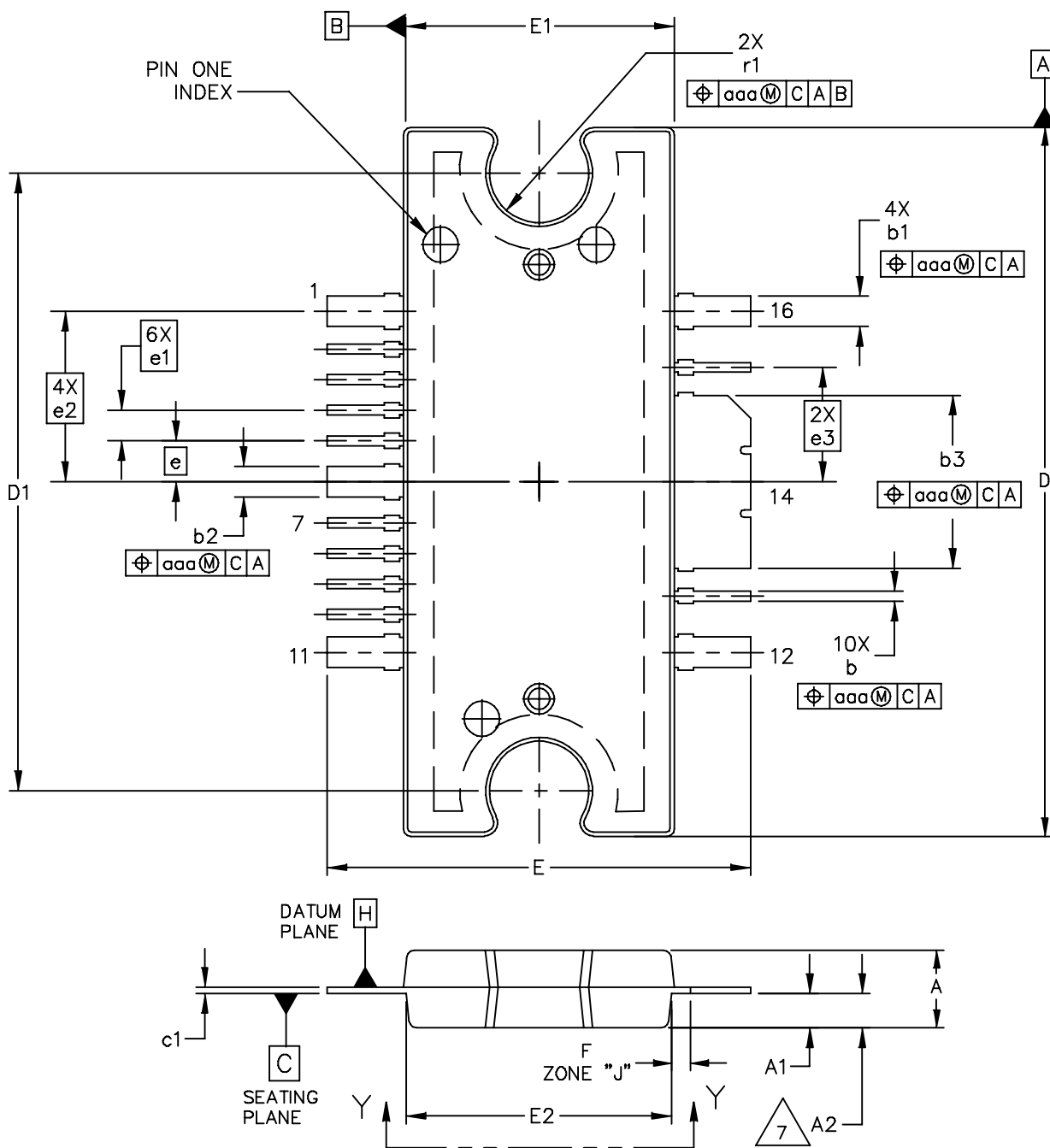
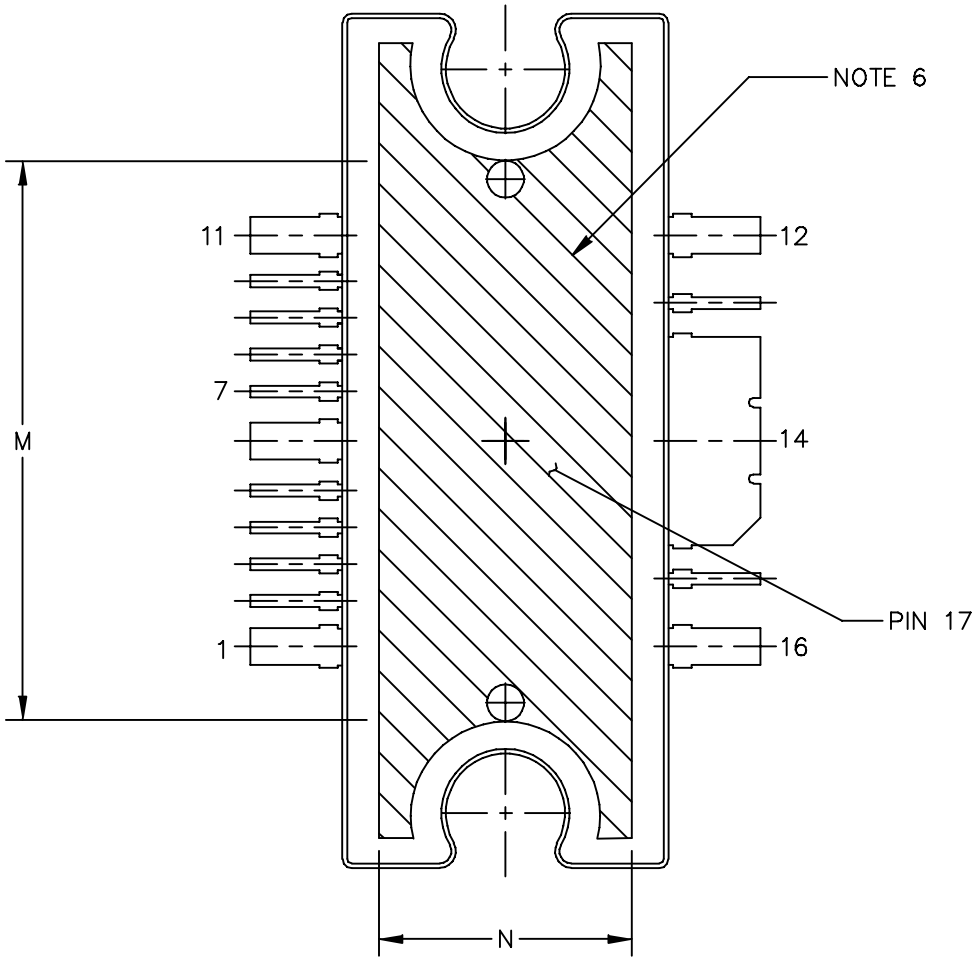


Figure 10. Power Gain versus Output Power

PACKAGE DIMENSIONS



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TITLE: TO-272 WIDE BODY MULTI-LEAD			DOCUMENT NO: 98ARH99164A		REV: M
			CASE NUMBER: 1329-09		23 AUG 2007
			STANDARD: NON-JEDEC		



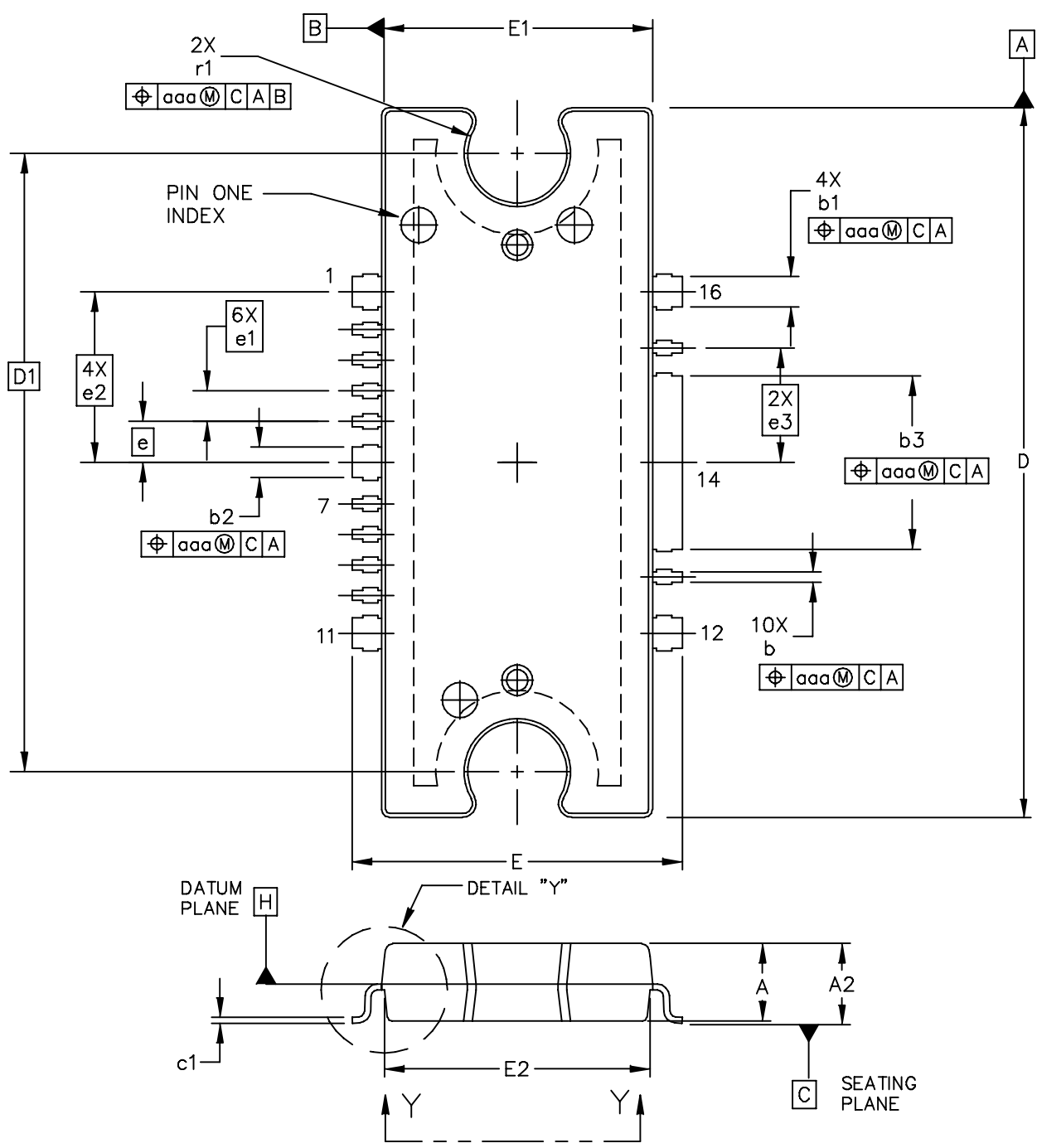
VIEW Y-Y

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	CASE NUMBER: 1329-09	23 AUG 2007	
	STANDARD: NON-JEDEC		

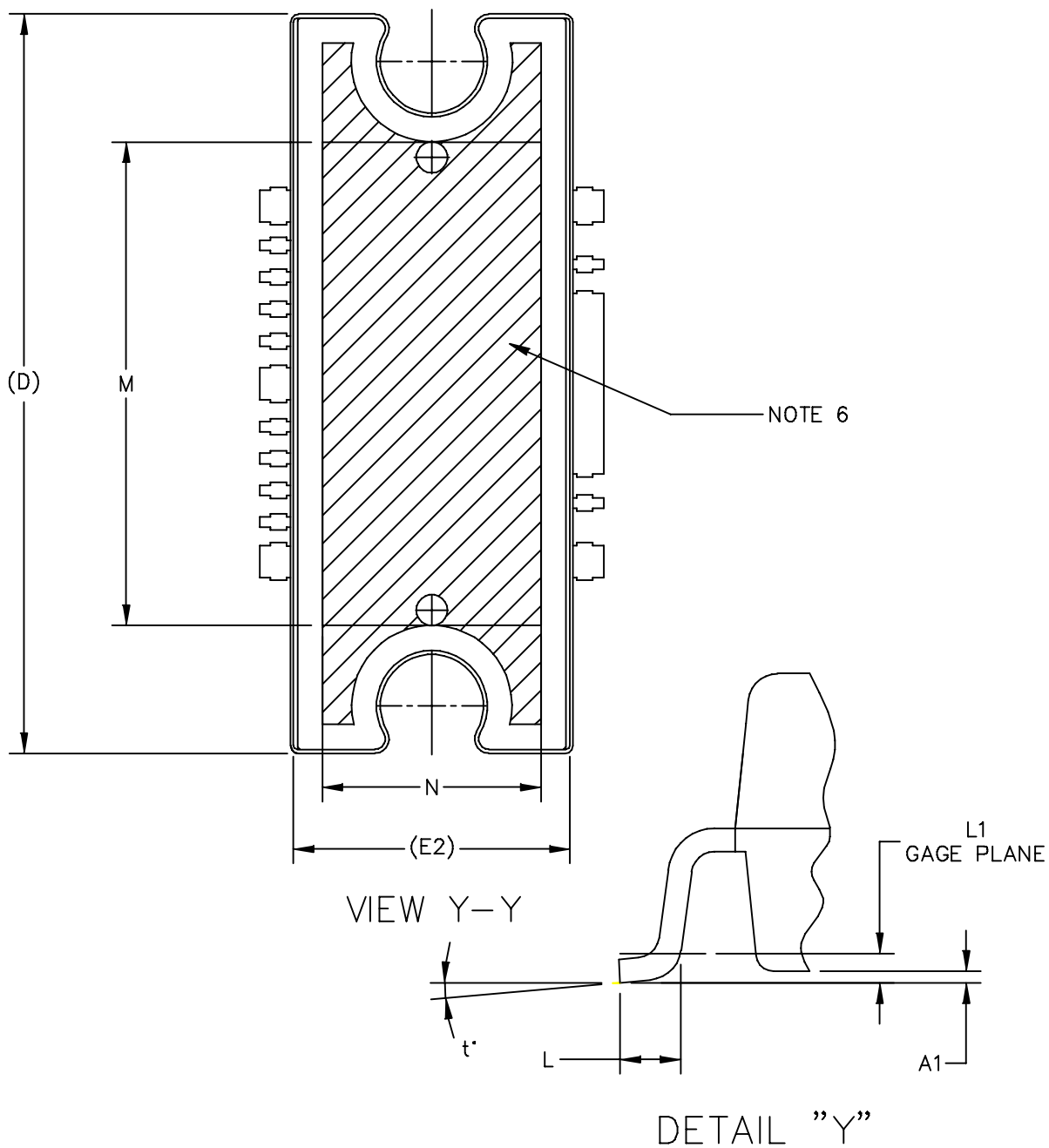
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----	aaa	.004		.10	
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		CASE NUMBER: 1329A-04	20 JUN 2007
		STANDARD: JEDEC MO-253 BA	



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	CASE NUMBER: 1329A-04	20 JUN 2007	
	STANDARD: JEDEC MO-253 BA		

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5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.001	.004	0.02	0.10	b1	.037	.043	0.94	1.09
A2	.099	.110	2.51	2.79	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
L	.018	.024	0.46	0.61	e3	.150 BSC		3.81 BSC	
L1	.01 BSC		0.25 BSC		r1	.063	.068	1.6	1.73
M	.600	----	15.24	----	t	2'	8'	2'	8'
N	.270	----	6.86	----	aaa	.004		.10	
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					STANDARD: JEDEC MO-253 BA				

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
2	Apr. 2008	<ul style="list-style-type: none"> • Document Number changed from MW5IC970NBR1 to MW5IC970N with the addition of the MW5IC970GNBR1 part number. Revision history sequencing maintained from first release of data sheet, p. 1 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 2 • Updated Part Numbers in Table 6, Component Designations and Values, to RoHS compliant part numbers, p. 3 • Replaced Case Outline 1329-09, Issue L, with 1329-09, Issue M, p. 1, 7-9. Added pin numbers 1 through 17. • Added Case Outline 1329A-04, Issue F, p. 1, 10-12 • Added Product Documentation and Revision History, p. 13
3	Jan. 2010	<ul style="list-style-type: none"> • Changed Storage Temperature Range in Max Ratings table from -65 to +200 to -65 to +150 for standardization across products, p. 2

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