Freescale Semiconductor
Application Note

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e300 (MPC603e) and e500 Register Model Comparison

The products described in this document are microprocessor cores built on Power Architecture™ technology. This application note outlines the differences between the registers implemented in the e300 core (MPC603e processor) and the e500 microprocessor core. It also discusses the differences between the register models defined by the Apple/IBM/Motorola (AIM) version and those defined by the Power instruction set architecture (Power ISA).

Registers defined by both the AIM version of the PowerPC architecture and Power ISA are identified by the level of the architecture at which the register is defined, as follows:

- Book I, user instruction set architecture (UISA)
- Book II, virtual environment architecture (VEA)
- Book III or III-E (Book III for AIM, Book III-E for Power ISA), operating environment architecture (OEA)
- Book IV, implementation definition

In addition, Power ISA also includes a fourth book, called Book VLE, which contains additional definitions. Neither the e300 or the e500 cores contain registers defined by Book VLE.

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For Power ISA, some registers defined in Book I and Book II may have slightly different definitions based on the category in which they are classified. Readers should generally use the definition given for the Embedded category if such a distinction exists.

Registers identified as EIS are defined as part of the Freescale extensions to Power ISA by the *EREF*. Although some of these registers may also be defined in Power ISA, if identified as EIS, these registers contain additional fields and or semantics that are not defined in Power ISA.

NOTE

This document does not attempt to identify specific differences between register fields implemented in a register. For example, although most machine state register (MSR) fields are the same in all processors, each device typically has implementation-specific fields that are not identified in this document. Consult the user's manuals for full descriptions of register fields.

1 Migrating from PowerPC AIM Architecture to Power ISA Register Model

Migrating from the PowerPC AIM register model implemented in the 603e to the Power ISA register model implemented in the e500 is relatively straightforward, keeping in mind the following points:

- Bit numbering in Power ISA registers has changed so that bits in 32-bit registers use a 64-bit numbering scheme in which the lower 32 bits are numbered 32–63, but correspond exactly to bits 0–31 in the 32-bit AIM definition of the PowerPC architecture as implemented in the e300.
- User-level software is binary upwardly compatible across both versions of the architecture, so most of the changes appear in registers that are defined by Book III-E and Book II, primarily associated with the memory-management unit (MMU), timer, and interrupt register models.
  - Note that e500v1 and e500v2 cores do not implement Power ISA category Floating Point, but do support the Embedded floating point subcategories defined under category SPE. This means that user-level software that employs floating point from e300 is not binary compatible with e500v1 and e500v2 cores and will generally require software to be recompiled. e500mc cores implement Power ISA category Floating Point and do not require user-level software to be recompiled.
- The MMU register model differences are as follows:
  - The Power ISA does not support the following 32-bit MMU-related registers:
    - Instruction and data block address translation registers (IBATs and DBATs).
    - Segment registers (SR0–SR15)
  - The Power ISA defines a new process identification register (PID)
  - The EIS defines the following additional MMU registers:
    - Process ID registers (PID1–PID2) for e500v1 and e500v2. Note that the EIS defines the Power ISA PID register as PID0.
    - MMU control and status register 0 (MMUCSR0)
    - MMU configuration register (MMUCFG)

  - TLB configuration registers (TLB*n*CFG)
  - MMU assist registers (MAS0–MAS8)
  - External process ID registers (EPLC and EPSC)
  - Logical partition ID register (LPIDR)
- The interrupt register model differences are as follows:
  - The DSISR has been replaced with a more generalized exception syndrome register (ESR)
  - The DAR has been replaced with the data effective address register (DEAR)
  - The Power ISA defines the following additional registers:
    - Critical save/restore registers 0 and 1 (CSRR0)
    - Critical save/restore register 1 (CSRR1)
    - Machine check save/restore register 0 (MCSRR0)
    - Machine check save/restore register 1 (MCSRR1)
    - Machine check syndrome register (MCSR)
    - Enhanced debug save/restore register 0 (DSRR0)
    - Enhanced debug save/restore register 1 (DSRR1)
    - Guest save/restore register 0 (GSRR0)
    - Guest save/restore register 1 (GSRR1)
    - Interrupt vector prefix register (IVPR)
    - Guest interrupt vector prefix register (GIVPR)
    - Exception syndrome register (ESR)
    - Guest exception syndrome register (GESR)
    - Guest data effective address register (GDEAR)
    - Interrupt vector offset registers (IVORs)
    - Guest interrupt vector offset registers (GIVORs)
  - The EIS defines the following additional registers:
    - External proxy register (EPR)
    - Guest external proxy register (GEPR)
- The Power ISA considers time base registers as SPRs (rather than time base registers, TBRs)
- The Power ISA defines additional timer resources, which use the following registers:
  - Decrementer auto-reload register (DECAR)
  - Timer status register (TSR)
  - Timer control register (TCR)
  - Alternate time base registers (ATBL and ATBU)

  In addition, timer-related interrupts (decrementer, watchdog timer, and fixed-interval timer) are each assigned IVOR registers.

- The EIS defines the following additional L1 cache registers:
  - L1 cache control and status register 0 (L1CSR0)
  - L1 cache control and status register 1 (L1CSR1)
  - L1 cache control and status register 2 (L1CSR2)
  - L1 cache configuration register 0 (L1CFG0)
  - L1 cache configuration register 1 (L1CFG1)
- The EIS defines several additional L2 cache registers identified as L2*xxxxxxxx*.
- The EIS defines the following additional debug registers:
  - Debug status register (DBSR0)
  - Debug control register 0 (DBCR0)
  - Debug control register 1 (DBCR1)
  - Debug control register 2 (DBCR2)
  - Debug control register 4 (DBCR4)
- The Power ISA defines the following additional debug registers:
  - Data address compare register 1 (DAC1)
  - Data address compare register 2 (DAC2)
  - Instruction address compare register 1 (IAC1)
  - Instruction address compare register 2 (IAC2)
  - The Power ISA defines the following additional registers used by the e500mc core to support virtualization from category Embedded.hypervisor:
- The EIS defines a set of register resources used exclusively by the performance monitor. PMRs are similar to SPRs except that they access performance monitor registers and are accessed through **mtpmr** and **mfpmr** instructions, which are also defined by the EIS.

2 Special-Purpose Registers by SPR Number

Table 1 lists the SPRs by number. Note that this decimal number is not a direct conversion of the binary value. For reasons of space, this table does not include the binary representation of the SPR field, which in the **mtspr** and **mfspr** instructions is encoded in two, 5-bit fields that are swapped, as shown in the **mtspr** encoding in Figure 1.

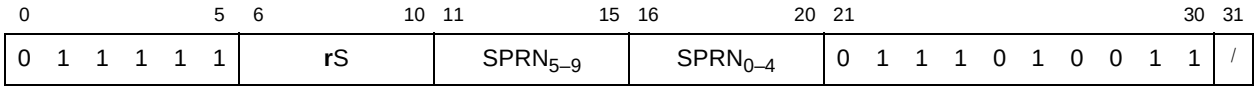

Figure 1. mtspr Instruction Encoding

For example, the decrementer register, DEC, is SPR 22. The binary conversion yields 10110. so SPR[0–4] = 10110 and SPR[5–9] = 00000. Likewise, the PVR is SPR 287, which is encoded as SPR[0–4] = 11111 and SPR[5–9] = 01000.

Access in Table 1 is given by the lowest level of privilege required to access the SPR. The following access methods appear in the table:

- User—denotes access is available for both **mfspr** and **mtspr** regardless of privilege level
- User RO—denotes access is available for only **mfspr** regardless of privilege level
- Sup—denotes access is available for both **mfspr** and **mtspr** when operating in supervisor mode (MSR[PR] = 1), regardless of the state of the MSR[GS] bit (i.e. it is available in hypervisor state as well).
- Sup RO—denotes access is available for only **mfspr** when operating in supervisor mode (MSR[PR] = 1), regardless of the state of the MSR[GS] bit (i.e. it is available in hypervisor state as well)
- Hypervisor—denotes access is available for both **mfspr** and **mtspr** when operating in hypervisor mode (MSR[GS,PR] = 00). For processors that do not implement the Power ISA category Embeded.Hypervisor, access is available when operating in supervisor state (MSR[PR] = 0).
- Hypervisor RO—denotes access is available for only **mfspr** when operating in hypervisor mode (MSR[GS,PR] = 00). For processors that do not implement the Power ISA category Embeded.Hypervisor, access is available when operating in supervisor state (MSR[PR] = 0).
- Hypervisor WO—denotes access is available for only **mtspr** when operating in hypervisor mode (MSR[GS,PR] = 00). For processors that do not implement the Power ISA category Embeded.Hypervisor, access is available when operating in supervisor state (MSR[PR] = 0).
- Hypervisor R/Clear—denotes access is available for both **mfspr** and **mtspr** when operating in hypervisor mode (MSR[GS,PR] = 00); however, an **mtspr** only clears bit positions in the SPR that correspond to the bits set in the source GPR. For processors that do not implement the Power ISA category Embeded.Hypervisor, access is available when operating in supervisor state (MSR[PR] = 0).

Table 1. Special-Purpose Registers (by SPR Number)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
1	XER	Integer exception register	User	Book I	Yes	Yes	Yes	Yes	Yes
8	LR	Link register	User	Book I	Yes	Yes	Yes	Yes	Yes
9	CTR	Count register	User	Book I	Yes	Yes	Yes	Yes	Yes
18	DAR	Data address register	Sup	Book III	Yes	—	Yes	—	—
22	DEC	Decrementer	Hyp	Book III	Yes	Yes	Yes	Yes	Yes
25	SDR1	SDR1 register	Sup	Book III	Yes	—	Yes	—	—
26	SRR0	Save/restore register 0	Sup[1]	Book III	Yes	Yes	Yes	Yes	Yes
27	SRR1	Save/restore register 1	Sup[1]	Book III	Yes	Yes	Yes	Yes	Yes
48	PID (PID0)	Process ID register	Sup	Book III	—	Yes	—	Yes	Yes
58	CSRR0	Critical save/restore register 0	Hyp	Book III	—	Yes	Yes	Yes	Yes
59	CSRR1	Critical save/restore register 1	Hyp	Book III	—	Yes	Yes	Yes	Yes

Table 1. Special-Purpose Registers (by SPR Number) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
61	DEAR	Data exception address register	Sup[1]	Book III	—	Yes	—	Yes	Yes
62	ESR	Exception syndrome register	Sup[1]	Book III	—	Yes	—	Yes	Yes
63	IVPR	Interrupt vector prefix	Hyp	Book III	—	Yes	—	Yes	Yes
256	USPRG0 (VRSAVE)	User SPR general 0[2]	User	Book III	—	Yes	—	Yes	Yes
259	SPRG3	SPR general 3	User RO	Book III	—	Yes	—	Yes	Yes
260	SPRG4	SPR general 4	User RO	Book III	—	Yes	—	Yes	Yes
261	SPRG5	SPR general 5	User RO	Book III	—	Yes	—	Yes	Yes
262	SPRG6	SPR general 6	User RO	Book III	—	Yes	—	Yes	Yes
263	SPRG7	SPR general 7	User RO	Book III	—	Yes	—	Yes	Yes
268	TBL(R)	Time base lower	User RO	Book II	Yes	Yes	Yes	Yes	Yes
269	TBU (R)	Time base upper	User RO	Book II	Yes	Yes	Yes	Yes	Yes
272	SPRG0	SPR general 0	Sup[1]	Book III	Yes	Yes	Yes	Yes	Yes
273	SPRG1	SPR general 1	Sup[1]	Book III	Yes	Yes	Yes	Yes	Yes
274	SPRG2	SPR general 2	Sup[1]	Book III	Yes	Yes	Yes	Yes	Yes
275	SPRG3	SPR general 3	Sup[1]	Book III	—	Yes	—	Yes	Yes
276	SPRG4	SPR general 4	Sup	Book III	—	Yes	Yes	Yes	Yes
277	SPRG5	SPR general 5	Sup	Book III	—	Yes	Yes	Yes	Yes
278	SPRG6	SPR general 6	Sup	Book III	—	Yes	Yes	Yes	Yes
279	SPRG7	SPR general 7	Sup	Book III	—	Yes	Yes	Yes	Yes
280	ASR	Address space register[3]	Sup	Book III	Yes	—	—	—	—
280	DSISR	Address space register	Sup	Book III	Yes	—	—	—	—
282	EAR	External access register[4]	Sup	Book III	Yes	—	—	—	—
286[5]	PIR	Processor ID register	Sup[1]	Book III	—	Yes	—	Yes	Yes
286[6]	SVR	System version register	Sup RO	Book IV	—	—	Yes	—	—
287	PVR	Processor version register	Sup RO	Book III	Yes	Yes	Yes	Yes	Yes
304	DBSR	Debug status register	Hyp R/Clear	Book III	—	Yes	—	Yes	Yes
306	DBSRWR	Debug status register write	Hyp	Book III	—	Yes	—	—	Yes
307	EPCR	Embedded processor control register	Hyp	Book III	—	Yes	—	—	Yes
308	DBCR0	Debug control register 0	Hyp	Book III	—	Yes	—	Yes	Yes
309	DBCR1	Debug control register 1	Hyp	Book III	—	Yes	—	Yes	Yes

Table 1. Special-Purpose Registers (by SPR Number) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
309	IBCR	Instruction address breakpoint control register	Sup	Book IV	—	—	Yes	—	—
310	DBCR	Data address breakpoint control register	Sup	Book IV	—	—	Yes	—	—
310	DBCR2	Debug control register 2	Hyp	Book III	—	Yes	—	Yes	Yes
311	MBAR	Memory base address register	Sup	Book IV	—	—	Yes	—	—
311	MSRP	MSR protect	Hyp	Book III	—	Yes	—	—	Yes
312	IAC1	Instruction address compare 1	Hyp	Book III	—	Yes	—	Yes	Yes
313	IAC2	Instruction address compare 2	Hyp	Book III	—	Yes	—	Yes	Yes
316	DAC1	Data address compare 1	Hyp	Book III	—	Yes	—	Yes	Yes
317	DABR2	Data address breakpoint register 2	Sup	Book IV	—	—	Yes	—	—
317	DAC2	Data address compare 2	Hyp	Book III	—	Yes	—	Yes	Yes
336	TSR	Timer status register	Hyp R/Clear	Book III	—	Yes	—	Yes	Yes
338	LPIDR	Logical PID register	Hyp	Book III	—	Yes	—	—	Yes
339	MAS5	MMU assist register 5	Hyp	Book III	—	Yes	—	—	Yes
340	TCR	Timer control register	Hyp	Book III	—	Yes	—	Yes	Yes
341	MAS8	MMU assist register 8	Hyp	Book III	—	Yes	—	—	Yes
368	GSPRG0	Guest SPR general 0	Sup	Book III	—	Yes	—	—	Yes
369	GSPRG1	Guest SPR general 1	Sup	Book III	—	Yes	—	—	Yes
370	GSPRG2	Guest SPR general 2	Sup	Book III	—	Yes	—	—	Yes
371	GSPRG3	Guest SPR general 3	Sup	Book III	—	Yes	—	—	Yes
378	GSRR0	Guest save/restore register 0	Sup	Book III	—	Yes	—	—	Yes
379	GSRR1	Guest save/restore register 1	Sup	Book III	—	Yes	—	—	Yes
380	GEPR	Guest external proxy register	Sup	EIS	—	Yes	—	—	Yes
381	GDEAR	Guest data exception address register	Sup	Book III	—	Yes	—	—	Yes
382	GPIR	Guest processor ID register	Sup[7]	Book III	—	Yes	—	—	Yes
383	GESR	Guest exception syndrome register	Sup	Book III	—	Yes	—	—	Yes
400	IVOR0	Critical input interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
401	IVOR1	Machine check interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
402	IVOR2	Data storage interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
403	IVOR3	Instruction storage interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
404	IVOR4	External input interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes

Table 1. Special-Purpose Registers (by SPR Number) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
405	IVOR5	Alignment interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
406	IVOR6	Program interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
407	IVOR7	Floating-point unavailable interrupt offset.	Hyp	Book III	—	Yes	—	Yes	Yes
408	IVOR8	System call interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
409	IVOR9	APU unavailable interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
410	IVOR10	Decrementer interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
411	IVOR11	Fixed-interval timer interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
412	IVOR12	Watchdog timer interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
413	IVOR13	Data TLB error interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
414	IVOR14	Instruction TLB error interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
415	IVOR15	Debug interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
432	IVOR38	Guest processor doorbell interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
433	IVOR39	Guest processor doorbell critical and machine check interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
434	IVOR40	Hypervisor system call interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
435	IVOR41	Hypervisor privilege interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
440	GIVOR2	Guest data storage interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
441	GIVOR3	Guest instruction storage interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
442	GIVOR4	Guest external input interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
443	GIVOR8	Guest system call interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
444	GIVOR13	Guest data TLB error interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
445	GIVOR14	Guest instruction TLB error interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
447	GIVPR	Guest interrupt vector prefix	Hyp	Book III	—	Yes	—	—	Yes
512	SPEFSCR	Address space register	User	Book I	—	Yes	—	Yes	—
513	BBEAR	Branch buffer entry address register	User	Book IV	—	—	—	Yes	—
514	BBTAR	Branch buffer target address register	User	Book IV	—	—	—	Yes	—
515	L1CFG0	L1 cache configuration register 0	User RO	EIS	—	Yes	—	Yes	Yes
516	L1CFG1	L1 cache configuration register 1	User RO	EIS	—	Yes	—	Yes	Yes
517	NPIDR	Nexus processor ID register	User	EIS	—	Yes	—	Yes	Yes

Table 1. Special-Purpose Registers (by SPR Number) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
519	L2CFG0	L2 cache configuration register 0	User RO	EIS	—	—	—	—	Yes
526	ATBL	Alternate time base register lower	User RO	Book II	—	Yes	—	Yes	Yes
527	ATBU	Alternate time base register upper	User RO	Book II	—	Yes	—	Yes	Yes
528	IBAT0U	Instruction BAT 0 upper	Sup	Book III	Yes	—	Yes	—	—
528	IVOR32	SPE unavailable interrupt offset	Hyp	Book III	—	Yes	—	Yes	—
529	IBAT0L	Instruction BAT 0 lower	Sup	Book III	Yes	—	Yes	—	—
529	IVOR33	Embedded floating point data exception interrupt offset	Hyp	Book III	—	Yes	—	Yes	—
530	IBAT1U	Instruction BAT 1 upper	Sup	Book III	Yes	—	Yes	—	—
530	IVOR34	Embedded floating point round interrupt offset	Hyp	Book III	—	Yes	—	Yes	—
531	IBAT1L	Instruction BAT 1 lower	Sup	Book III	Yes	—	Yes	—	—
531	IBAT2L	Instruction BAT 2 lower	Sup	Book III	Yes	—	Yes	—	—
531	IVOR35	Performance monitor interrupt offset	Hyp	EIS	—	Yes	—	Yes	Yes
532	IBAT2U	Instruction BAT 2 upper	Sup	Book III	Yes	—	Yes	—	—
532	IVOR36	Processor doorbell interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
533	IBAT3L	Instruction BAT 3 lower	Sup	Book III	Yes	—	Yes	—	—
533	IVOR37	Processor doorbell critical interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
534	IBAT3U	Instruction BAT 3 upper	Sup	Book III	Yes	—	Yes	—	—
536	DBAT0U	Data BAT 0 upper	Sup	Book III	Yes	—	Yes	—	—
537	DBAT0L	Data BAT 0 lower	Sup	Book III	Yes	—	Yes	—	—
538	DBAT1U	Data BAT 1 upper	Sup	Book III	Yes	—	Yes	—	—
539	DBAT1L	Data BAT 1 lower	Sup	Book III	Yes	—	Yes	—	—
540	DBAT2U	Data BAT 2 upper	Sup	Book III	Yes	—	Yes	—	—
541	DBAT2L	Data BAT 2 lower	Sup	Book III	Yes	—	Yes	—	—
542	DBAT3U	Data BAT 3 upper	Sup	Book III	Yes	—	Yes	—	—
543	DBAT3L	Data BAT 3 lower	Sup	Book III	Yes	—	Yes	—	—
560	IBAT4U	Instruction BAT 4 upper	Sup	Book III	—	—	Yes	—	—
561	IBAT4L	Instruction BAT 4 lower	Sup	Book III	—	—	Yes	—	—
562	IBAT5U	Instruction BAT 5 upper	Sup	Book III	—	—	Yes	—	—
563	DBCR4	Debug control register 4	Hyp	EIS	—	Yes	—	—	Yes
563	IBAT5L	Instruction BAT 5 lower	Sup	Book III	—	—	Yes	—	—
564	IBAT6U	Instruction BAT 6 upper	Sup	Book III	—	—	Yes	—	—

Table 1. Special-Purpose Registers (by SPR Number) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
565	IBAT6L	Instruction BAT 6 lower	Sup	Book III	—	—	Yes	—	—
566	IBAT7U	Instruction BAT 7 upper	Sup	Book III	—	—	Yes	—	—
567	IBAT7L	Instruction BAT 7 lower	Sup	Book III	—	—	Yes	—	—
568	DBAT4U	Data BAT 4 upper	Sup	Book III	—	—	Yes	—	—
569	DBAT4L	Data BAT 4 lower	Sup	Book III	—	—	Yes	—	—
569	MCARU	Machine check address register upper	Hyp RO	EIS	—	Yes	—	Yes	Yes
570	DBAT5U	Data BAT 5 upper	Sup	Book III	—	—	Yes	—	—
570	MCSRR0	Machine-check save/restore register 0	Hyp	Book III	—	Yes	—	Yes	Yes
571	DBAT5L	Data BAT 5 lower	Sup	Book III	—	—	Yes	—	—
571	MCSRR1	Machine-check save/restore register 1	Hyp	Book III	—	Yes	—	Yes	Yes
572	DBAT6U	Data BAT 6 upper	Sup	Book III	—	—	Yes	—	—
572	MCSR	Machine check syndrome register	Hyp	Book III	—	Yes		Yes	Yes
573	DBAT6L	Data BAT 6 lower	Sup	Book III	—	—	Yes	—	—
573	MCAR	Machine check address register	Hyp RO	EIS	—	Yes	—	Yes	Yes
574	DBAT7U	Data BAT 7 upper	Sup	Book III	—	—	Yes	—	—
574	DSRR0	Debug save/restore register 0	Hyp	Book III	—	Yes	—	—	Yes
575	DBAT7L	Data BAT 7 lower	Sup	Book III	—	—	Yes	—	—
575	DSRR1	Debug save/restore register 1	Hyp	Book III	—	Yes	—	—	Yes
576	DDAM	Debug data acquisition message.	User	EIS	—	Yes	—	—	Yes
604	SPRG8	SPRG8	Hyp	Book III	—	Yes	—	Yes	Yes
605	SPRG9	SPRG9	Sup	Book III	—	Yes	—	—	Yes
606	L1CSR2	L1 cache control and status register 2	Hyp	EIS	—	—	—	Yes	Yes
624	MAS0	MMU assist register 0	Sup	Book III	—	Yes	—	Yes	Yes
625	MAS1	MMU assist register 1	Sup	Book III	—	Yes	—	Yes	Yes
626	MAS2	MMU assist register 2	Sup	Book III	—	Yes	—	Yes	Yes
627	MAS3	MMU assist register 3	Sup	Book III	—	Yes	—	Yes	Yes
628	MAS4	MMU assist register 4	Sup	Book III	—	Yes	—	Yes	Yes
630	MAS6	MMU assist register 6	Sup	Book III	—	Yes	—	Yes	Yes
633	PID1	Process ID register 1	Sup	(EIS)[8]	—	Yes	—	Yes	—
634	PID2	Process ID register 2	Sup	(EIS)[8]	—	Yes	—	Yes	—

Table 1. Special-Purpose Registers (by SPR Number) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
688	TLB0CFG	TLB configuration register 0	Hyp RO	Book III	—	Yes	—	Yes	Yes
689	TLB1CFG	TLB configuration register 1	Hyp RO	Book III	—	Yes	—	Yes	Yes
696	CDCSR0	Core device control and status register	Hyp	EIS	—	Yes	—	—	Yes
702	EPR	External proxy register	Sup[1]	EIS	—	Yes	—	—	Yes
720	L2ERRINTEN	L2 cache error interrupt enable	Hyp	EIS	—	—	—	—	Yes
721	L2ERRATTR	L2 cache error attribute	Hyp	EIS	—	—	—	—	Yes
722	L2ERRADDR	L2 cache error address	Hyp	EIS	—	—	—	—	Yes
723	L2ERREADDR	L2 cache error extended address	Hyp	EIS	—	—	—	—	Yes
724	L2ERRCTL	L2 cache error control	Hyp	EIS	—	—	—	—	Yes
725	L2ERRDIS	L2 cache error disable	Hyp	EIS	—	—	—	—	Yes
944	MAS7	MMU assist register 7	Sup	Book III	—	Yes	—	Yes	Yes
947	EPLC	External PID load context	Sup[9]	Book III	—	Yes	—	—	Yes
948	EPSC	External PID store context	Sup[9]	Book III	—	Yes	—	—	Yes
975	DEVENT	Debug event	User	EIS	—	Yes	—	—	Yes
976	DMISS	Data TLB miss register	Sup	Book IV	—	—	Yes	—	—
977	DCMP	Data TLB compare register	Sup	Book IV	—	—	Yes	—	—
978	HASH1	Primary hash register	Sup	Book IV	—	—	Yes	—	—
979	HASH2	Secondary hash register	Sup	Book IV	—	—	Yes	—	—
980	IMISS	Instruction TLB miss register	Sup	Book IV	—	—	Yes	—	—
981	ICMP	Instruction TLB compare register	Sup	Book IV	—	—	Yes	—	—
982	RPA	Required physical address register	Sup	Book III	Yes	—	Yes	—	—
983	NSPD	Nexus SPR access data	Hyp	EIS	—	Yes	—	—	Yes
984	NSPC	Nexus SPR access configuration	Hyp	EIS	—	Yes	—	—	Yes
985	L2ERRINJHI	L2 cache error injection mask high	Hyp	EIS	—	—	—	—	Yes
986	L2ERRINJLO	L2 cache error injection mask low	Hyp	EIS	—	—	—	—	Yes
987	L2ERRINJCTL	L2 cache error injection control	Hyp	EIS	—	—	—	—	Yes
988	L2CAPTDATAHI	L2 cache error capture data high	Hyp	EIS	—	—	—	—	Yes
989	L2CAPTDATALO	L2 cache error capture data low	Hyp	EIS	—	—	—	—	Yes
990	L2CAPTECC	L2 cache error capture ECC syndrome	Hyp	EIS	—	—	—	—	Yes
991	L2ERRDET	L2 cache error detect	Hyp	EIS	—	—	—	—	Yes
1008	HID0	Hardware implementation dependent register 0	Hyp	EIS	—	—	Yes	Yes	Yes

Table 1. Special-Purpose Registers (by SPR Number) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
1009	HID1	Hardware implementation dependent register 1	Sup	Book IV	—	—	Yes	Yes	—
1010	IABR	Instruction address breakpoint register	Sup	Book III	Yes	—	Yes	—	—
1010	L1CSR0	L1 cache control and status register 0	Hyp	EIS	—	Yes	—	Yes	Yes
1011	HID2	Hardware implementation dependent register 2	Sup	Book IV	—	—	Yes	—	—
1011	L1CSR1	L1 cache control and status register 1	Hyp	EIS	—	Yes	—	Yes	Yes
1012	MMUCSR0	MMU control and status register 0	Hyp	EIS	—	Yes	—	Yes	Yes
1013	BUCSR	Branch unit control and status register	Hyp	EIS	—	Yes	—	Yes	Yes
1013	DABR	Data address breakpoint register	Sup	Book IV	—	—	Yes	—	—
1015	MMUCFG	MMU configuration register	Hyp RO	Book III	—	Yes	—	Yes	Yes
1017	L2CSR0	L2 cache control and status register 0	Hyp	EIS	—	—	—	—	Yes
1018	IABR2	Instruction address breakpoint register 2	Sup	Book III	—	—	Yes	—	—
1018	L2CSR1	L2 cache control and status register 1	Hyp	EIS	—	—	—	—	Yes
1023	SVR	System version register	Sup RO	EIS	—	—	Yes	Yes	Yes
1023[5]	PIR	Processor ID register	Sup RO	Book III	Yes	—	—	—	—

1 When these registers are accessed in Guest supervisor state, the access are mapped to their analogous guest SPRs (e.g. DEAR is mapped to GDEAR). See Power ISA.

2 USPRG0 is a separate physical register from SPRG0.

3 64-bit implementations only.

4 Optional facility in the PowerPC architecture.

5 The AIM version of the PowerPC architecture assigns SPR 1023 to PIR. Power ISA assigned it to SPR 286.

6 The 603e/e300 implementations assigns SPR 286 to SVR. EIS assigned it to 1023.

7 This register is only writeable in Hypervisor state, but can be read in Guest supervisor state

8 Earlier versions of EIS defined more than one PID register. PID registers other than PID (PID0) have been dropped from the latest version of EIS.

9 Certain fields in the register are only writeable when in Hypervisor state

3 Special-Purpose Registers by SPR Abbreviation

Table 2 lists SPRs by their abbreviated name.

Table 2. Special-Purpose Registers (by Abbreviated Name)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
280	ASR	Address space register[1]	Sup	Book III	Yes	—	—	—	—
526	ATBL	Alternate time base register lower	User RO	Book II	—	Yes	—	Yes	Yes
527	ATBU	Alternate time base register upper	User RO	Book II	—	Yes	—	Yes	Yes
513	BBEAR	Branch buffer entry address register	User	Book IV	—	—	—	Yes	—
514	BBTAR	Branch buffer target address register	User	Book IV	—	—	—	Yes	—
1013	BUCSR	Branch unit control and status register	Hyp	EIS	—	Yes	—	Yes	Yes
696	CDCSR0	Core device control and status register	Hyp	EIS	—	Yes	—	—	Yes
58	CSRR0	Critical save/restore register 0	Hyp	Book III	—	Yes	Yes	Yes	Yes
59	CSRR1	Critical save/restore register 1	Hyp	Book III	—	Yes	Yes	Yes	Yes
9	CTR	Count register	User	Book I	Yes	Yes	Yes	Yes	Yes
1013	DABR	Data address breakpoint register	Sup	Book IV	—	—	Yes	—	—
317	DABR2	Data address breakpoint register 2	Sup	Book IV	—	—	Yes	—	—
316	DAC1	Data address compare 1	Hyp	Book III	—	Yes	—	Yes	Yes
317	DAC2	Data address compare 2	Hyp	Book III	—	Yes	—	Yes	Yes
18	DAR	Data address register	Sup	Book III	Yes	—	Yes	—	—
537	DBAT0L	Data BAT 0 lower	Sup	Book III	Yes	—	Yes	—	—
536	DBAT0U	Data BAT 0 upper	Sup	Book III	Yes	—	Yes	—	—
539	DBAT1L	Data BAT 1 lower	Sup	Book III	Yes	—	Yes	—	—
538	DBAT1U	Data BAT 1 upper	Sup	Book III	Yes	—	Yes	—	—
541	DBAT2L	Data BAT 2 lower	Sup	Book III	Yes	—	Yes	—	—
540	DBAT2U	Data BAT 2 upper	Sup	Book III	Yes	—	Yes	—	—
543	DBAT3L	Data BAT 3 lower	Sup	Book III	Yes	—	Yes	—	—
542	DBAT3U	Data BAT 3 upper	Sup	Book III	Yes	—	Yes	—	—
569	DBAT4L	Data BAT 4 lower	Sup	Book III	—	—	Yes	—	—
568	DBAT4U	Data BAT 4 upper	Sup	Book III	—	—	Yes	—	—
571	DBAT5L	Data BAT 5 lower	Sup	Book III	—	—	Yes	—	—
570	DBAT5U	Data BAT 5 upper	Sup	Book III	—	—	Yes	—	—
573	DBAT6L	Data BAT 6 lower	Sup	Book III	—	—	Yes	—	—

Table 2. Special-Purpose Registers (by Abbreviated Name) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
572	DBAT6U	Data BAT 6 upper	Sup	Book III	—	—	Yes	—	—
575	DBAT7L	Data BAT 7 lower	Sup	Book III	—	—	Yes	—	—
574	DBAT7U	Data BAT 7 upper	Sup	Book III	—	—	Yes	—	—
310	DBCR	Data address breakpoint control register	Sup	Book IV	—	—	Yes	—	—
308	DBCR0	Debug control register 0	Hyp	Book III	—	Yes	—	Yes	Yes
309	DBCR1	Debug control register 1	Hyp	Book III	—	Yes	—	Yes	Yes
310	DBCR2	Debug control register 2	Hyp	Book III	—	Yes	—	Yes	Yes
563	DBCR4	Debug control register 4	Hyp	EIS	—	Yes	—	—	Yes
304	DBSR	Debug status register	Hyp R/Clear	Book III	—	Yes	—	Yes	Yes
306	DBSRWR	Debug status register write	Hyp	Book III	—	Yes	—	—	Yes
977	DCMP	Data TLB compare register	Sup	Book IV	—	—	Yes	—	—
576	DDAM	Debug data acquisition message.	User	EIS	—	Yes	—	—	Yes
61	DEAR	Data exception address register	Sup[2]	Book III	—	Yes	—	Yes	Yes
22	DEC	Decrementer	Hyp	Book III	Yes	Yes	Yes	Yes	Yes
975	DEVENT	Debug event	User	EIS	—	Yes	—	—	Yes
976	DMISS	Data TLB miss register	Sup	Book IV	—	—	Yes	—	—
280	DSISR	Address space register	Sup	Book III	Yes	—	—	—	—
574	DSRR0	Debug save/restore register 0	Hyp	Book III	—	Yes	—	—	Yes
575	DSRR1	Debug save/restore register 1	Hyp	Book III	—	Yes	—	—	Yes
282	EAR	External access register[3]	Sup	Book III	Yes	—	—	—	—
307	EPCR	Embedded processor control register	Hyp	Book III	—	Yes	—	—	Yes
947	EPLC	External PID load context	Sup[4]	Book III	—	Yes	—	—	Yes
702	EPR	External proxy register	Sup[2]	EIS	—	Yes	—	—	Yes
948	EPSC	External PID store context	Sup[4]	Book III	—	Yes	—	—	Yes
62	ESR	Exception syndrome register	Sup[2]	Book III	—	Yes	—	Yes	Yes
381	GDEAR	Guest data exception address register	Sup	Book III	—	Yes	—	—	Yes
380	GEPR	Guest external proxy register	Sup	EIS	—	Yes	—	—	Yes
383	GESR	Guest exception syndrome register	Sup	Book III	—	Yes	—	—	Yes
444	GIVOR13	Guest data TLB error interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
445	GIVOR14	Guest instruction TLB error interrupt offset	Hyp	Book III	—	Yes	—	—	Yes

Table 2. Special-Purpose Registers (by Abbreviated Name) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
440	GIVOR2	Guest data storage interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
441	GIVOR3	Guest instruction storage interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
442	GIVOR4	Guest external input interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
443	GIVOR8	Guest system call interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
447	GIVPR	Guest interrupt vector prefix	Hyp	Book III	—	Yes	—	—	Yes
382	GPIR	Guest processor ID register	Sup[5]	Book III	—	Yes	—	—	Yes
368	GSPRG0	Guest SPR general 0	Sup	Book III	—	Yes	—	—	Yes
369	GSPRG1	Guest SPR general 1	Sup	Book III	—	Yes	—	—	Yes
370	GSPRG2	Guest SPR general 2	Sup	Book III	—	Yes	—	—	Yes
371	GSPRG3	Guest SPR general 3	Sup	Book III	—	Yes	—	—	Yes
378	GSRR0	Guest save/restore register 0	Sup	Book III	—	Yes	—	—	Yes
379	GSRR1	Guest save/restore register 1	Sup	Book III	—	Yes	—	—	Yes
978	HASH1	Primary hash register	Sup	Book IV	—	—	Yes	—	—
979	HASH2	Secondary hash register	Sup	Book IV	—	—	Yes	—	—
1008	HID0	Hardware implementation dependent register 0	Hyp	EIS	—	—	Yes	Yes	Yes
1009	HID1	Hardware implementation dependent register 1	Sup	Book IV	—	—	Yes	Yes	—
1011	HID2	Hardware implementation dependent register 2	Sup	Book IV	—	—	Yes	—	—
1010	IABR	Instruction address breakpoint register	Sup	Book III	Yes	—	Yes	—	—
1018	IABR2	Instruction address breakpoint register 2	Sup	Book III	—	—	Yes	—	—
312	IAC1	Instruction address compare 1	Hyp	Book III	—	Yes	—	Yes	Yes
313	IAC2	Instruction address compare 2	Hyp	Book III	—	Yes	—	Yes	Yes
529	IBAT0L	Instruction BAT 0 lower	Sup	Book III	Yes	—	Yes	—	—
528	IBAT0U	Instruction BAT 0 upper	Sup	Book III	Yes	—	Yes	—	—
531	IBAT1L	Instruction BAT 1 lower	Sup	Book III	Yes	—	Yes	—	—
530	IBAT1U	Instruction BAT 1 upper	Sup	Book III	Yes	—	Yes	—	—
531	IBAT2L	Instruction BAT 2 lower	Sup	Book III	Yes	—	Yes	—	—
532	IBAT2U	Instruction BAT 2 upper	Sup	Book III	Yes	—	Yes	—	—
533	IBAT3L	Instruction BAT 3 lower	Sup	Book III	Yes	—	Yes	—	—
534	IBAT3U	Instruction BAT 3 upper	Sup	Book III	Yes	—	Yes	—	—

Table 2. Special-Purpose Registers (by Abbreviated Name) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
561	IBAT4L	Instruction BAT 4 lower	Sup	Book III	—	—	Yes	—	—
560	IBAT4U	Instruction BAT 4 upper	Sup	Book III	—	—	Yes	—	—
563	IBAT5L	Instruction BAT 5 lower	Sup	Book III	—	—	Yes	—	—
562	IBAT5U	Instruction BAT 5 upper	Sup	Book III	—	—	Yes	—	—
565	IBAT6L	Instruction BAT 6 lower	Sup	Book III	—	—	Yes	—	—
564	IBAT6U	Instruction BAT 6 upper	Sup	Book III	—	—	Yes	—	—
567	IBAT7L	Instruction BAT 7 lower	Sup	Book III	—	—	Yes	—	—
566	IBAT7U	Instruction BAT 7 upper	Sup	Book III	—	—	Yes	—	—
309	IBCR	Instruction address breakpoint control register	Sup	Book IV	—	—	Yes	—	—
981	ICMP	Instruction TLB compare register	Sup	Book IV	—	—	Yes	—	—
980	IMISS	Instruction TLB miss register	Sup	Book IV	—	—	Yes	—	—
400	IVOR0	Critical input interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
401	IVOR1	Machine check interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
410	IVOR10	Decrementer interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
411	IVOR11	Fixed-interval timer interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
412	IVOR12	Watchdog timer interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
413	IVOR13	Data TLB error interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
414	IVOR14	Instruction TLB error interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
415	IVOR15	Debug interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
402	IVOR2	Data storage interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
403	IVOR3	Instruction storage interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
528	IVOR32	SPE unavailable interrupt offset	Hyp	Book III	—	Yes	—	Yes	—
529	IVOR33	Embedded floating point data exception interrupt offset	Hyp	Book III	—	Yes	—	Yes	—
530	IVOR34	Embedded floating point round interrupt offset	Hyp	Book III	—	Yes	—	Yes	—
531	IVOR35	Performance monitor interrupt offset	Hyp	EIS	—	Yes	—	Yes	Yes
532	IVOR36	Processor doorbell interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
533	IVOR37	Processor doorbell critical interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
432	IVOR38	Guest processor doorbell interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
433	IVOR39	Guest processor doorbell critical and machine check interrupt offset	Hyp	Book III	—	Yes	—	—	Yes

Table 2. Special-Purpose Registers (by Abbreviated Name) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
404	IVOR4	External input interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
434	IVOR40	Hypervisor system call interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
435	IVOR41	Hypervisor privilege interrupt offset	Hyp	Book III	—	Yes	—	—	Yes
405	IVOR5	Alignment interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
406	IVOR6	Program interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
407	IVOR7	Floating-point unavailable interrupt offset.	Hyp	Book III	—	Yes	—	Yes	Yes
408	IVOR8	System call interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
409	IVOR9	APU unavailable interrupt offset	Hyp	Book III	—	Yes	—	Yes	Yes
63	IVPR	Interrupt vector prefix	Hyp	Book III	—	Yes	—	Yes	Yes
515	L1CFG0	L1 cache configuration register 0	User RO	EIS	—	Yes	—	Yes	Yes
516	L1CFG1	L1 cache configuration register 1	User RO	EIS	—	Yes	—	Yes	Yes
1010	L1CSR0	L1 cache control and status register 0	Hyp	EIS	—	Yes	—	Yes	Yes
1011	L1CSR1	L1 cache control and status register 1	Hyp	EIS	—	Yes	—	Yes	Yes
606	L1CSR2	L1 cache control and status register 2	Hyp	EIS	—	—	—	Yes	Yes
988	L2CAPTDATAHI	L2 cache error capture data high	Hyp	EIS	—	—	—	—	Yes
989	L2CAPTDATALO	L2 cache error capture data low	Hyp	EIS	—	—	—	—	Yes
990	L2CAPTECC	L2 cache error capture ECC syndrome	Hyp	EIS	—	—	—	—	Yes
519	L2CFG0	L2 cache configuration register 0	User RO	EIS	—	—	—	—	Yes
1017	L2CSR0	L2 cache control and status register 0	Hyp	EIS	—	—	—	—	Yes
1018	L2CSR1	L2 cache control and status register 1	Hyp	EIS	—	—	—	—	Yes
722	L2ERRADDR	L2 cache error address	Hyp	EIS	—	—	—	—	Yes
721	L2ERRATTR	L2 cache error attribute	Hyp	EIS	—	—	—	—	Yes
724	L2ERRCTL	L2 cache error control	Hyp	EIS	—	—	—	—	Yes
991	L2ERRDET	L2 cache error detect	Hyp	EIS	—	—	—	—	Yes
725	L2ERRDIS	L2 cache error disable	Hyp	EIS	—	—	—	—	Yes
723	L2ERREADDR	L2 cache error extended address	Hyp	EIS	—	—	—	—	Yes
987	L2ERRINJCTL	L2 cache error injection control	Hyp	EIS	—	—	—	—	Yes
985	L2ERRINJHI	L2 cache error injection mask high	Hyp	EIS	—	—	—	—	Yes

Table 2. Special-Purpose Registers (by Abbreviated Name) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
986	L2ERRINJLO	L2 cache error injection mask low	Hyp	EIS	—	—	—	—	Yes
720	L2ERRINTEN	L2 cache error interrupt enable	Hyp	EIS	—	—	—	—	Yes
338	LPIDR	Logical PID register	Hyp	Book III	—	Yes	—	—	Yes
8	LR	Link register	User	Book I	Yes	Yes	Yes	Yes	Yes
624	MAS0	MMU assist register 0	Sup	Book III	—	Yes	—	Yes	Yes
625	MAS1	MMU assist register 1	Sup	Book III	—	Yes	—	Yes	Yes
626	MAS2	MMU assist register 2	Sup	Book III	—	Yes	—	Yes	Yes
627	MAS3	MMU assist register 3	Sup	Book III	—	Yes	—	Yes	Yes
628	MAS4	MMU assist register 4	Sup	Book III	—	Yes	—	Yes	Yes
339	MAS5	MMU assist register 5	Hyp	Book III	—	Yes	—	—	Yes
630	MAS6	MMU assist register 6	Sup	Book III	—	Yes	—	Yes	Yes
944	MAS7	MMU assist register 7	Sup	Book III	—	Yes	—	Yes	Yes
341	MAS8	MMU assist register 8	Hyp	Book III	—	Yes	—	—	Yes
311	MBAR	Memory base address register	Sup	Book IV	—	—	Yes	—	—
573	MCAR	Machine check address register	Hyp RO	EIS	—	Yes	—	Yes	Yes
569	MCARU	Machine check address register upper	Hyp RO	EIS	—	Yes	—	Yes	Yes
572	MCSR	Machine check syndrome register	Hyp	Book III	—	Yes	—	Yes	Yes
570	MCSRR0	Machine-check save/restore register 0	Hyp	Book III	—	Yes	—	Yes	Yes
571	MCSRR1	Machine-check save/restore register 1	Hyp	Book III	—	Yes	—	Yes	Yes
1015	MMUCFG	MMU configuration register	Hyp RO	Book III	—	Yes	—	Yes	Yes
1012	MMUCSR0	MMU control and status register 0	Hyp	EIS	—	Yes	—	Yes	Yes
311	MSRP	MSR protect	Hyp	Book III	—	Yes	—	—	Yes
517	NPIDR	Nexus processor ID register	User	EIS	—	Yes	—	Yes	Yes
984	NSPC	Nexus SPR access configuration	Hyp	EIS	—	Yes	—	—	Yes
983	NSPD	Nexus SPR access data	Hyp	EIS	—	Yes	—	—	Yes
48	PID (PID0)	Process ID register	Sup	Book III	—	Yes	—	Yes	Yes
633	PID1	Process ID register 1	Sup	(EIS)[6]	—	Yes	—	Yes	—
634	PID2	Process ID register 2	Sup	(EIS)[6]	—	Yes	—	Yes	—
286[7]	PIR	Processor ID register	Sup[2]	Book III	—	Yes	—	Yes	Yes
1023[7]	PIR	Processor ID register	Sup RO	Book III	Yes	—	—	—	—

Table 2. Special-Purpose Registers (by Abbreviated Name) (continued)

Defined SPR Number	SPR Abbreviation	Name	Access	Source	Defined		Implemented		
					AIM	Power ISA	e300	e500 v2	e500 mc
287	PVR	Processor version register	Sup RO	Book III	Yes	Yes	Yes	Yes	Yes
982	RPA	Required physical address register	Sup	Book III	Yes	—	Yes	—	—
25	SDR1	SDR1 register	Sup	Book III	Yes	—	Yes	—	—
512	SPEFSCR	Address space register	User	Book I	—	Yes	—	Yes	—
272	SPRG0	SPR general 0	Sup[2]	Book III	Yes	Yes	Yes	Yes	Yes
273	SPRG1	SPR general 1	Sup[2]	Book III	Yes	Yes	Yes	Yes	Yes
274	SPRG2	SPR general 2	Sup[2]	Book III	Yes	Yes	Yes	Yes	Yes
259	SPRG3	SPR general 3	User RO[2]	Book III	—	Yes	—	Yes	Yes
275	SPRG3	SPR general 3	Sup[2]	Book III	—	Yes	—	Yes	Yes
260	SPRG4	SPR general 4	User RO	Book III	—	Yes	—	Yes	Yes
276	SPRG4	SPR general 4	Sup	Book III	—	Yes	Yes	Yes	Yes
261	SPRG5	SPR general 5	User RO	Book III	—	Yes	—	Yes	Yes
277	SPRG5	SPR general 5	Sup	Book III	—	Yes	Yes	Yes	Yes
262	SPRG6	SPR general 6	User RO	Book III	—	Yes	—	Yes	Yes
278	SPRG6	SPR general 6	Sup	Book III	—	Yes	Yes	Yes	Yes
263	SPRG7	SPR general 7	User RO	Book III	—	Yes	—	Yes	Yes
279	SPRG7	SPR general 7	Sup	Book III	—	Yes	Yes	Yes	Yes
604	SPRG8	SPRG8	Hyp	Book III	—	Yes	—	Yes	Yes
605	SPRG9	SPRG9	Sup	Book III	—	Yes	—	—	Yes
26	SRR0	Save/restore register 0	Sup[2]	Book III	Yes	Yes	Yes	Yes	Yes
27	SRR1	Save/restore register 1	Sup[2]	Book III	Yes	Yes	Yes	Yes	Yes
286[8]	SVR	System version register	Sup RO	Book IV	—	—	Yes	—	—
1023	SVR	System version register	Sup RO	EIS	—	—	Yes	Yes	Yes
268	TBL(R)	Time base lower	User RO	Book II	Yes	Yes	Yes	Yes	Yes
269	TBU (R)	Time base upper	User RO	Book II	Yes	Yes	Yes	Yes	Yes
340	TCR	Timer control register	Hyp	Book III	—	Yes	—	Yes	Yes
688	TLB0CFG	TLB configuration register 0	Hyp RO	Book III	—	Yes	—	Yes	Yes
689	TLB1CFG	TLB configuration register 1	Hyp RO	Book III	—	Yes	—	Yes	Yes
336	TSR	Timer status register	Hyp R/Clear	Book III	—	Yes	—	Yes	Yes
256	USPRG0 (VRSAVE)	User SPR general 0[9]	User	Book III	—	Yes	—	Yes	Yes
1	XER	Integer exception register	User	Book I	Yes	Yes	Yes	Yes	Yes

[1] 64-bit implementations only.

2 When these registers are accessed in Guest supervisor state, the access are mapped to their analogous guest SPRs (e.g. DEAR is mapped to GDEAR). See Power ISA.
3 Optional facility in the PowerPC architecture.
4 Certain fields in the register are only writeable when in Hypervisor state
5 This register is only writeable in Hypervisor state, but can be read in Guest supervisor state
6 Earlier versions of EIS defined more than one PID register. PID registers other than PID (PID0) have been dropped from the latest version of EIS.
7 The AIM version of the PowerPC architecture assigns SPR 1023 to PIR. Power ISA assigned it to SPR 286.
8 The 603e/e300 implementations assigns SPR 286 to SVR. EIS assigned it to 1023.
9 USPRG0 is a separate physical register from SPRG0.

4 Architecture-Defined Non-SPR Registers by Abbreviation

Table 3 lists the system registers that are not SPRs. They are listed alphabetically by abbreviation.

Table 3. Architecture-Defined Non-SPR Registers by Abbreviation

Abbreviation	Name	Access	Source	Defined		Implemented		
				AIM	Power ISA	e300	e500v2	e500mc
ACC[1]	Accumulator	User	Book I	—	Yes	—	Yes	—
CR	Condition register	User	Book I	Yes	Yes	Yes	Yes	Yes
FPR0–FPR31[2]	Floating-point registers 0–31	User	Book I	Yes	Yes	Yes	—	Yes
FPSCR[2]	Floating-point status and control register	User	Book I	Yes	Yes	Yes	—	Yes
GPR0–GPR31	General-purpose registers 0–31	User	Book I	Yes	Yes	Yes	Yes[3]	Yes
MSR	Machine state register	Sup	Book III	Yes	Yes	Yes	Yes	Yes

1 Processors that implement Power ISA category SPE only.
2 Processors that implement Power ISA category Floating point and processors that implement the AIM PowerPC architecture.
3 Note that GPRs are 64 bits each on processors that implement category SPE or category 64-bit. E500v2 implements category SPE.

5 Freescale EIS-Defined Performance Monitor Registers (PMRs)

The Freescale EIS defines a set of register resources used exclusively by the performance monitor. PMRs are similar to the SPRs defined in the embedded category in the Power ISA and are accessed through **mtpmr** and **mfpmr** instructions, which are also defined by the EIS. Table 4 lists PMRs by PMR number.

NOTE

User-level software that attempts to read or write supervisor-level PMRs causes a privilege exception.

Further note that **mtpmr** and **mfpmr** instructions use the same split-field encodings as the **mtspr** and **mfspr** instructions.

The e500 implements all of these PMRs.

Table 4. Performance Monitor Registers–(by PMR Number)

PMR Number	Abbreviation	Register Name	Access	Supervisor/User[1]
0	UPMC0	User performance monitor counter 0	R	User
1	UPMC1	User performance monitor counter 1	R	User
2	UPMC2	User performance monitor counter 2	R	User
3	UPMC3	User performance monitor counter 3	R	User
16	PMC0	Performance monitor counter 0	R/W	Supervisor
17	PMC1	Performance monitor counter 1	R/W	Supervisor
18	PMC2	Performance monitor counter 2	R/W	Supervisor
19	PMC3	Performance monitor counter 3	R/W	Supervisor
128	UPMLCa0	User performance monitor local control a0	R	User
129	UPMLCa1	User performance monitor local control a1	R	User
130	UPMLCa2	User performance monitor local control a2	R	User
131	UPMLCa3	User performance monitor local control a3	R	User
144	PMLCa0	Performance monitor local control a0	R/W	Supervisor
145	PMLCa1	Performance monitor local control a1	R/W	Supervisor
146	PMLCa2	Performance monitor local control a2	R/W	Supervisor
147	PMLCa3	Performance monitor local control a3	R/W	Supervisor
256	UPMLCb0	User performance monitor local control b0	R	User
257	UPMLCb1	User performance monitor local control b1	R	User
258	UPMLCb2	User performance monitor local control b2	R	User
259	UPMLCb3	User performance monitor local control b3	R	User
272	PMLCb0	Performance monitor local control b0	R/W	Supervisor
273	PMLCb1	Performance monitor local control b1	R/W	Supervisor
274	PMLCb2	Performance monitor local control b2	R/W	Supervisor
275	PMLCb3	Performance monitor local control b3	R/W	Supervisor
384	UPMGC0	User performance monitor global control register 0	R	User
400	PMGC0	Performance monitor global control register 0	R/W	Supervisor

[1] Note that user-accessible registers can also be accessed by supervisor-level software.

Table 5 lists PMRs by their abbreviated names.

Table 5. Performance Monitor Registers–(by PMR Abbreviation)

Abbreviation	Register Name	PMR Number	Access	Supervisor/User [1]
PMC0	Performance monitor counter 0	16	R/W	Supervisor
PMC1	Performance monitor counter 1	17	R/W	Supervisor
PMC2	Performance monitor counter 2	18	R/W	Supervisor
PMC3	Performance monitor counter 3	19	R/W	Supervisor
PMGC0	Performance monitor global control register 0	400	R/W	Supervisor
PMLCa0	Performance monitor local control a0	144	R/W	Supervisor
PMLCa1	Performance monitor local control a1	145	R/W	Supervisor
PMLCa2	Performance monitor local control a2	146	R/W	Supervisor
PMLCa3	Performance monitor local control a3	147	R/W	Supervisor
PMLCb0	Performance monitor local control b0	272	R/W	Supervisor
PMLCb1	Performance monitor local control b1	273	R/W	Supervisor
PMLCb2	Performance monitor local control b2	274	R/W	Supervisor
PMLCb3	Performance monitor local control b3	275	R/W	Supervisor
UPMC0	User performance monitor counter 0	0	R	User
UPMC1	User performance monitor counter 1	1	R	User
UPMC2	User performance monitor counter 2	2	R	User
UPMC3	User performance monitor counter 3	3	R	User
UPMGC0	User performance monitor global control register 0	384	R	User
UPMLCa0	User performance monitor local control a0	128	R	User
UPMLCa1	User performance monitor local control a1	129	R	User
UPMLCa2	User performance monitor local control a2	130	R	User
UPMLCa3	User performance monitor local control a3	131	R	User
UPMLCb0	User performance monitor local control b0	256	R	User
UPMLCb1	User performance monitor local control b1	257	R	User
UPMLCb2	User performance monitor local control b2	258	R	User
UPMLCb3	User performance monitor local control b3	259	R	User

[1] Note that user-accessible registers can also be accessed by supervisor-level software.

6 Revision History

Table 6 provides a revision history for this application note.

Table 6. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	09/2009	• Removed mention of IARR from document. • Changed document to reflect differences from e300 core to e500v2 and e500mc cores. • Added new registers. • Nomenclature about “Power ISA” updated to reflect the fact that the architecture is structured in “Books.” • Nomenclature updated to current Power Architecture language.
0	07/2003	Initial release.

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