Freescale Semiconductor
Data Sheet: Technical Data

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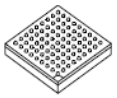
P3041

P3041 QorIQ Integrated Processor Hardware Specifications



FC-PBGA–1295
37.5 mm x 37.5 mm

The P3041 QorIQ integrated processor utilizes four processor cores built on Power Architecture® technology. The cores include high-performance data path acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, base station controllers, and general-purpose embedded computing. Its high level of integration offers significant performance benefits compared to multiple discrete devices while also greatly simplifying board design.

The chip includes the following functions and features:

- Four e500mc Power Architecture cores, each with a backside 128 KB L2 cache with ECC
  - Three levels of instructions: User, supervisor, and hypervisor
  - Independent boot and reset
  - Secure boot capability
- CoreNet fabric supporting coherent and non-coherent transactions amongst CoreNet end-points
- CoreNet platform cache with ECC
- CoreNet bridges between the CoreNet fabric the I/Os, datapath accelerators, and high and low speed peripheral interfaces
- One 10-Gigabit Ethernet (XAUI) controller
- Five 1-Gigabit Ethernet controllers
  - SGMII interfaces
    - 2.5 Gbps SGMII interfaces
  - RGMII interfaces
- One 64-bit DDR3 SDRAM memory controller with ECC
- Multicore programmable interrupt controller
- Four I^2C controllers
- Four 2-pin UARTs or two 4-pin UARTs
- Two 4-channel DMA engines
- Enhanced local bus controller (eLBC)
- Four PCI Express 2.0 controllers/ports
- Two serial RapidIO® controllers/ports (sRIO port) supporting version 1.3 with features from 2.1
- Two serial ATA (SATA 2.0) controllers
- Enhanced secure digital host controller (SD/MMC)
- Enhanced serial peripheral interfaces (eSPI)
- 2× high-speed USB 2.0 controllers with integrated PHYs

Table of Contents

This figure shows the major functional units within the chip.

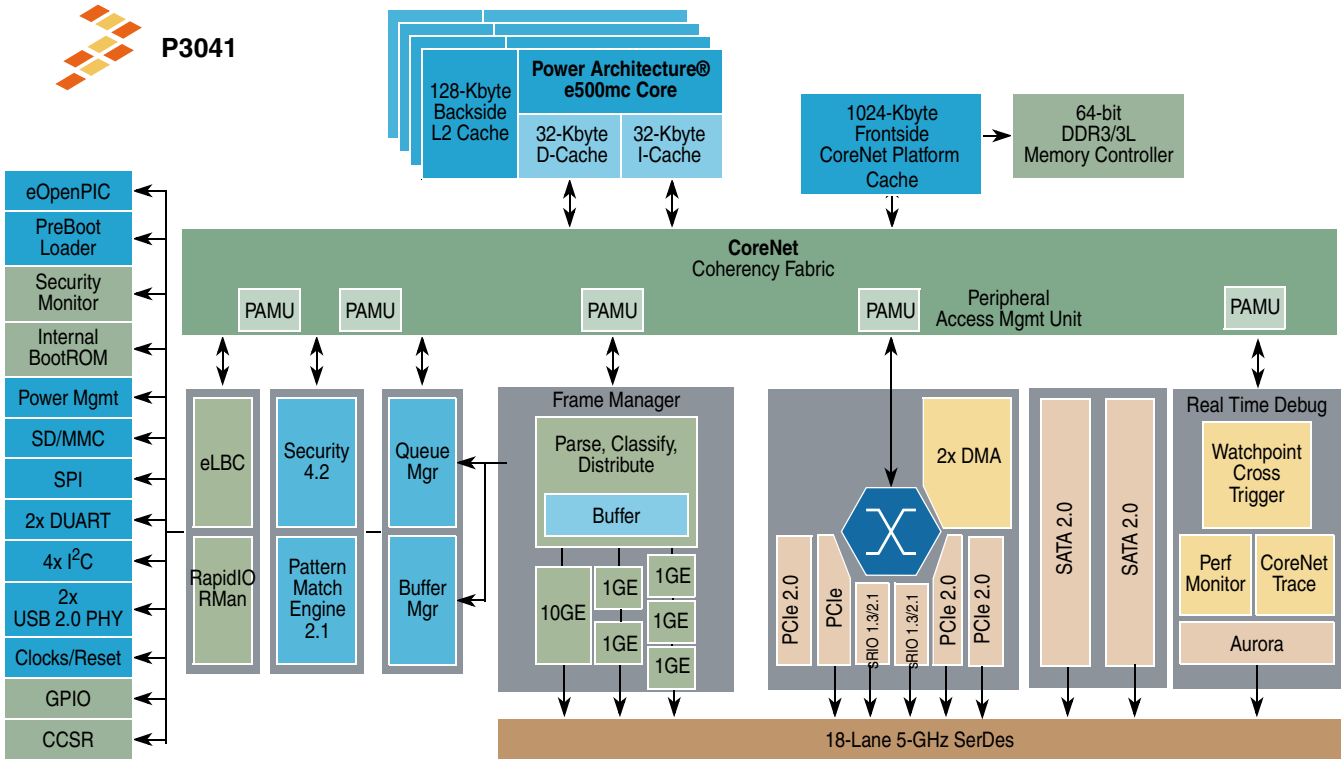


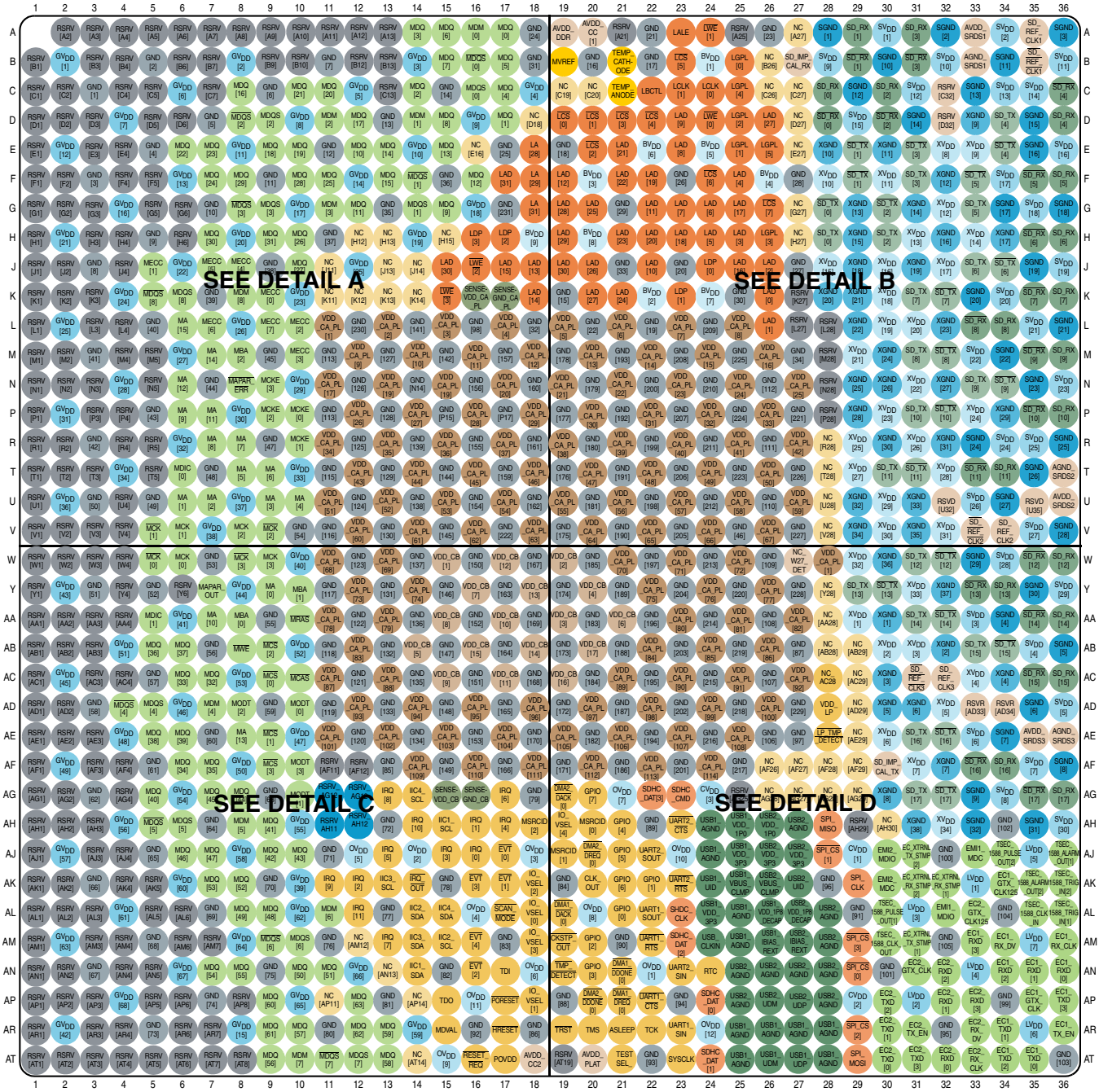
Figure 1. Block Diagram

1 Pin Assignments and Reset States

This section contains top view and detailed quadrant views of the FC-PBGA ball map diagram followed by a pinout list.

1.1 1295 FC-PBGA Ball Layout Diagrams

These figures show the FC-PBGA ball map diagrams.



Signal Groups

OV_{DD}	I/O Supply Voltage	SV_{DD}	SerDes Core Power Supply	$AVDD\_SRDS1$	SerDes 1 PLL Supply Voltage	SENSE-VDD	Core Group A Voltage Sense
LV_{DD}	I/O Supply Voltage	XV_{DD}	SerDes Transcvr Pad Supply	$AVDD\_SRDS2$	SerDes 2 PLL Supply Voltage	SENSE-VDD_CB	Core Group B Voltage Sense
GV_{DD}	DDR DRAM I/O Supply	$VDD\_CA\_CB\_PL$	Core A, B and Platform Supply Voltage	$AVDD\_PLAT$	Platform PLL Supply Voltage	SENSE-VDD_CA_CB_PL	Core A, B and Platform Voltage Sense
CV_{DD}	SPI Voltage Supply	VDD_CB	Core Group B Supply Voltage	$AVDD\_CC$	Core PLL Supply Voltage	RSRV	Reserved
BV_{DD}	Local Bus I/O Supply	POVDD	Fuse Programming Override Supply				

Figure 2. 1295 BGA Ball Map Diagram (Top View)

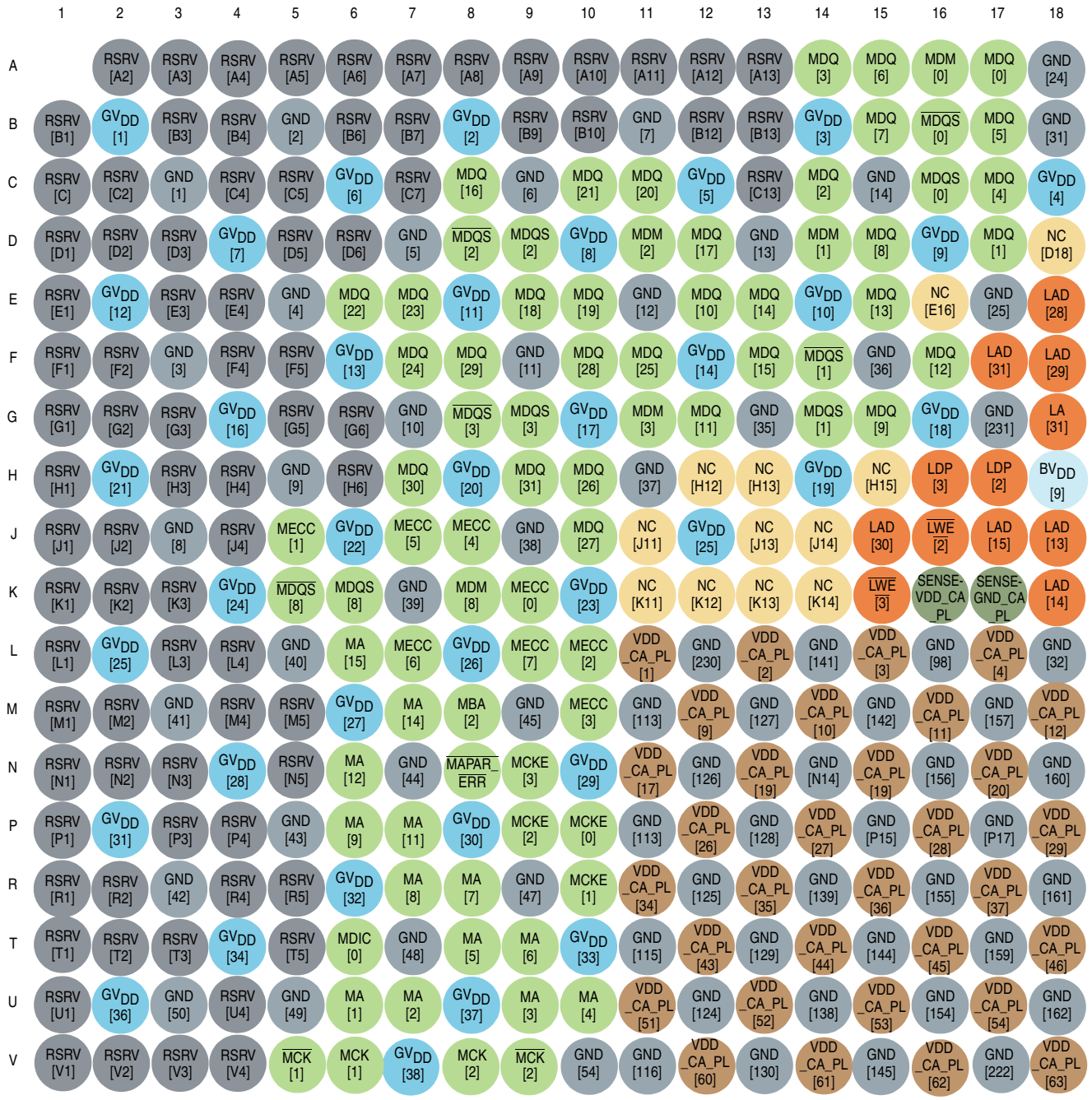


Figure 3. 1295 BGA Ball Map Diagram (Detail View A)

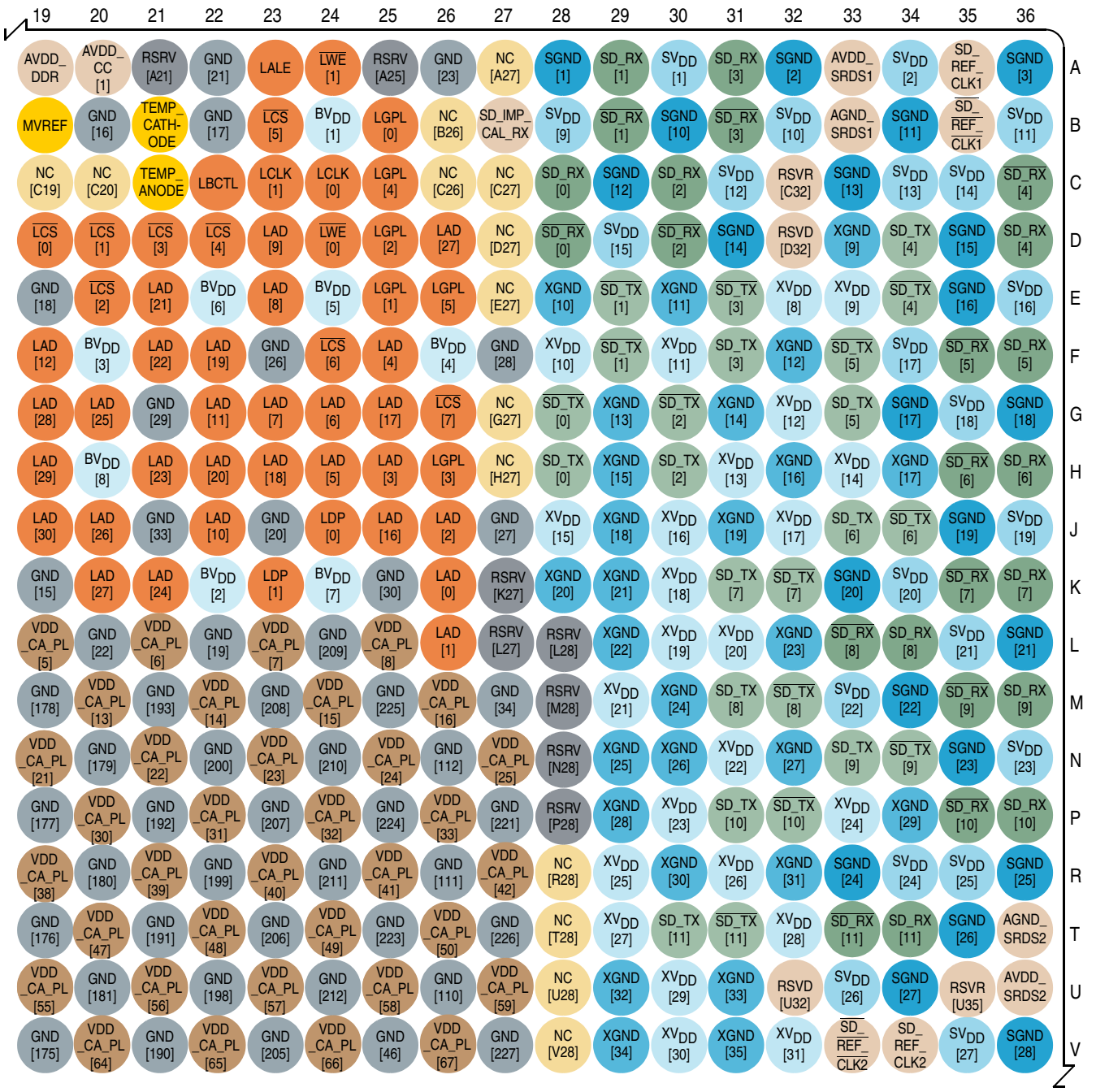


Figure 4. 1295 BGA Ball Map Diagram (Detail View B)

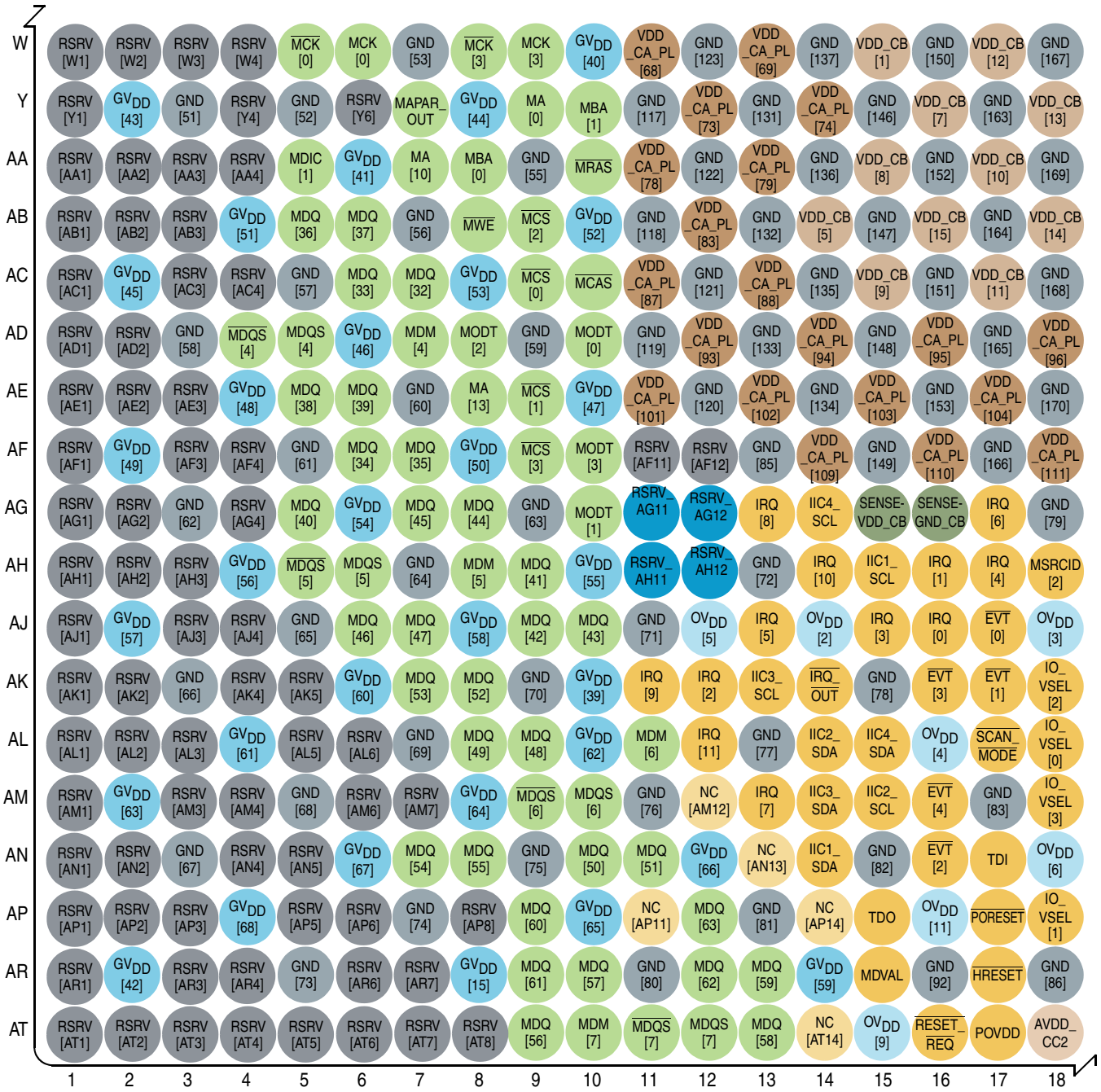


Figure 5. 1295 BGA Ball Map Diagram (Detail View C)

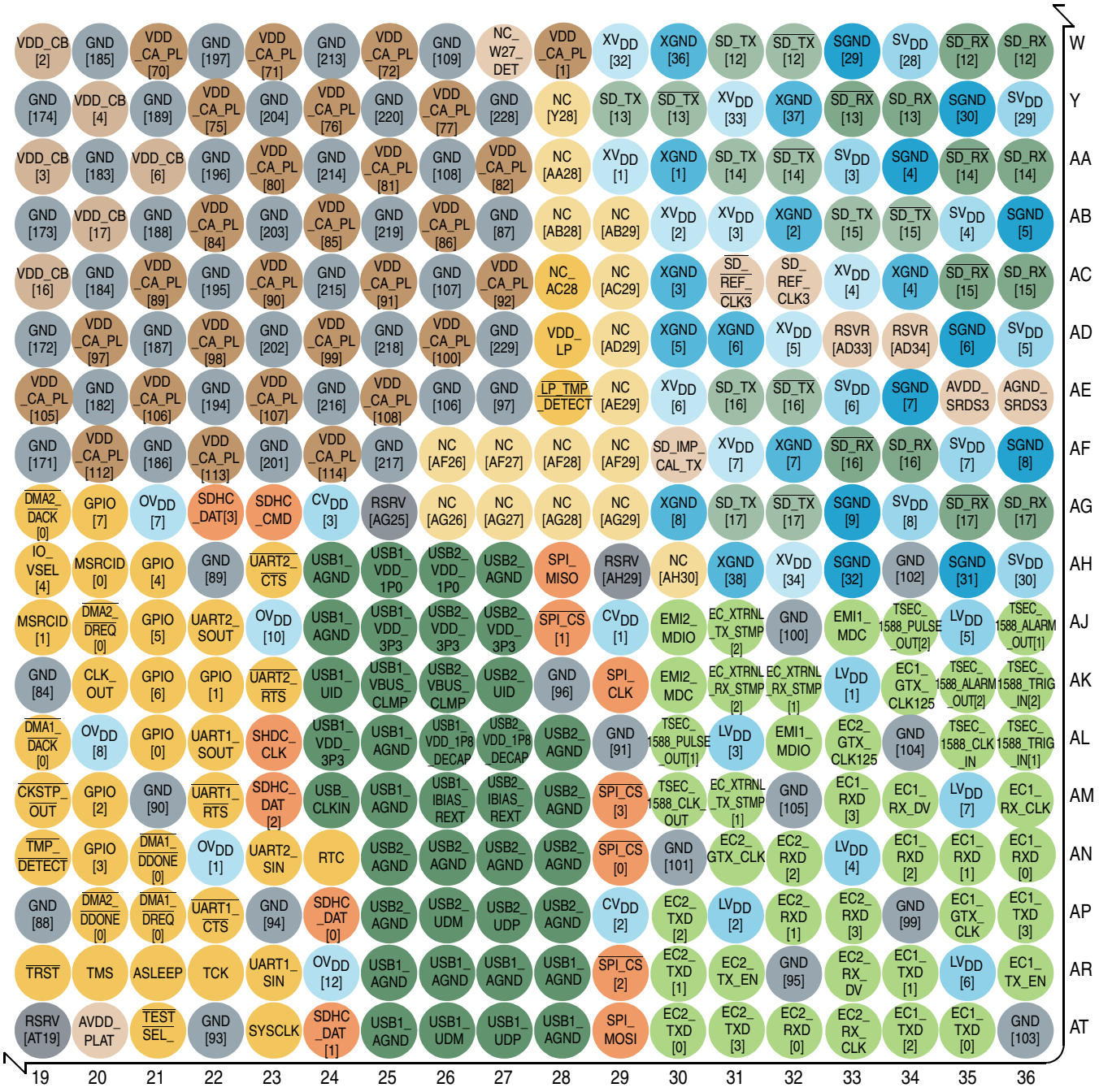


Figure 6. 1295 BGA Ball Map Diagram (Detail View D)

1.2 Pinout List

This table provides the pinout listing for the 1295 FC-PBGA package by bus.

Table 1. Pins List by Bus

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface					
MDQ00	Data	A17	I/O	GV_{DD}	—
MDQ01	Data	D17	I/O	GV_{DD}	—
MDQ02	Data	C14	I/O	GV_{DD}	—
MDQ03	Data	A14	I/O	GV_{DD}	—
MDQ04	Data	C17	I/O	GV_{DD}	—
MDQ05	Data	B17	I/O	GV_{DD}	—
MDQ06	Data	A15	I/O	GV_{DD}	—
MDQ07	Data	B15	I/O	GV_{DD}	—
MDQ08	Data	D15	I/O	GV_{DD}	—
MDQ09	Data	G15	I/O	GV_{DD}	—
MDQ10	Data	E12	I/O	GV_{DD}	—
MDQ11	Data	G12	I/O	GV_{DD}	—
MDQ12	Data	F16	I/O	GV_{DD}	—
MDQ13	Data	E15	I/O	GV_{DD}	—
MDQ14	Data	E13	I/O	GV_{DD}	—
MDQ15	Data	F13	I/O	GV_{DD}	—
MDQ16	Data	C8	I/O	GV_{DD}	—
MDQ17	Data	D12	I/O	GV_{DD}	—
MDQ18	Data	E9	I/O	GV_{DD}	—
MDQ19	Data	E10	I/O	GV_{DD}	—
MDQ20	Data	C11	I/O	GV_{DD}	—
MDQ21	Data	C10	I/O	GV_{DD}	—
MDQ22	Data	E6	I/O	GV_{DD}	—
MDQ23	Data	E7	I/O	GV_{DD}	—
MDQ24	Data	F7	I/O	GV_{DD}	—
MDQ25	Data	F11	I/O	GV_{DD}	—
MDQ26	Data	H10	I/O	GV_{DD}	—
MDQ27	Data	J10	I/O	GV_{DD}	—
MDQ28	Data	F10	I/O	GV_{DD}	—
MDQ29	Data	F8	I/O	GV_{DD}	—
MDQ30	Data	H7	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
MDQ31	Data	H9	I/O	GV_{DD}	—
MDQ32	Data	AC7	I/O	GV_{DD}	—
MDQ33	Data	AC6	I/O	GV_{DD}	—
MDQ34	Data	AF6	I/O	GV_{DD}	—
MDQ35	Data	AF7	I/O	GV_{DD}	—
MDQ36	Data	AB5	I/O	GV_{DD}	—
MDQ37	Data	AB6	I/O	GV_{DD}	—
MDQ38	Data	AE5	I/O	GV_{DD}	—
MDQ39	Data	AE6	I/O	GV_{DD}	—
MDQ40	Data	AG5	I/O	GV_{DD}	—
MDQ41	Data	AH9	I/O	GV_{DD}	—
MDQ42	Data	AJ9	I/O	GV_{DD}	—
MDQ43	Data	AJ10	I/O	GV_{DD}	—
MDQ44	Data	AG8	I/O	GV_{DD}	—
MDQ45	Data	AG7	I/O	GV_{DD}	—
MDQ46	Data	AJ6	I/O	GV_{DD}	—
MDQ47	Data	AJ7	I/O	GV_{DD}	—
MDQ48	Data	AL9	I/O	GV_{DD}	—
MDQ49	Data	AL8	I/O	GV_{DD}	—
MDQ50	Data	AN10	I/O	GV_{DD}	—
MDQ51	Data	AN11	I/O	GV_{DD}	—
MDQ52	Data	AK8	I/O	GV_{DD}	—
MDQ53	Data	AK7	I/O	GV_{DD}	—
MDQ54	Data	AN7	I/O	GV_{DD}	—
MDQ55	Data	AN8	I/O	GV_{DD}	—
MDQ56	Data	AT9	I/O	GV_{DD}	—
MDQ57	Data	AR10	I/O	GV_{DD}	—
MDQ58	Data	AT13	I/O	GV_{DD}	—
MDQ59	Data	AR13	I/O	GV_{DD}	—
MDQ60	Data	AP9	I/O	GV_{DD}	—
MDQ61	Data	AR9	I/O	GV_{DD}	—
MDQ62	Data	AR12	I/O	GV_{DD}	—
MDQ63	Data	AP12	I/O	GV_{DD}	—
MECC0	Error Correcting Code	K9	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
MECC1	Error Correcting Code	J5	I/O	GV_{DD}	—
MECC2	Error Correcting Code	L10	I/O	GV_{DD}	—
MECC3	Error Correcting Code	M10	I/O	GV_{DD}	—
MECC4	Error Correcting Code	J8	I/O	GV_{DD}	—
MECC5	Error Correcting Code	J7	I/O	GV_{DD}	—
MECC6	Error Correcting Code	L7	I/O	GV_{DD}	—
MECC7	Error Correcting Code	L9	I/O	GV_{DD}	—
$\overline{\text{MAPAR\_ERR}}$	Address Parity Error	N8	I	GV_{DD}	4
MAPAR_OUT	Address Parity Out	Y7	O	GV_{DD}	—
MDM0	Data Mask	A16	O	GV_{DD}	—
MDM1	Data Mask	D14	O	GV_{DD}	—
MDM2	Data Mask	D11	O	GV_{DD}	—
MDM3	Data Mask	G11	O	GV_{DD}	—
MDM4	Data Mask	AD7	O	GV_{DD}	—
MDM5	Data Mask	AH8	O	GV_{DD}	—
MDM6	Data Mask	AL11	O	GV_{DD}	—
MDM7	Data Mask	AT10	O	GV_{DD}	—
MDM8	Data Mask	K8	O	GV_{DD}	—
MDQS0	Data Strobe	C16	I/O	GV_{DD}	—
MDQS1	Data Strobe	G14	I/O	GV_{DD}	—
MDQS2	Data Strobe	D9	I/O	GV_{DD}	—
MDQS3	Data Strobe	G9	I/O	GV_{DD}	—
MDQS4	Data Strobe	AD5	I/O	GV_{DD}	—
MDQS5	Data Strobe	AH6	I/O	GV_{DD}	—
MDQS6	Data Strobe	AM10	I/O	GV_{DD}	—
MDQS7	Data Strobe	AT12	I/O	GV_{DD}	—
MDQS8	Data Strobe	K6	I/O	GV_{DD}	—
$\overline{\text{MDQS0}}$	Data Strobe	B16	I/O	GV_{DD}	—
$\overline{\text{MDQS1}}$	Data Strobe	F14	I/O	GV_{DD}	—
$\overline{\text{MDQS2}}$	Data Strobe	D8	I/O	GV_{DD}	—
$\overline{\text{MDQS3}}$	Data Strobe	G8	I/O	GV_{DD}	—
$\overline{\text{MDQS4}}$	Data Strobe	AD4	I/O	GV_{DD}	—
$\overline{\text{MDQS5}}$	Data Strobe	AH5	I/O	GV_{DD}	—
$\overline{\text{MDQS6}}$	Data Strobe	AM9	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MDQS7}}$	Data Strobe	AT11	I/O	GV_{DD}	—
$\overline{\text{MDQS8}}$	Data Strobe	K5	I/O	GV_{DD}	—
MBA0	Bank Select	AA8	O	GV_{DD}	—
MBA1	Bank Select	Y10	O	GV_{DD}	—
MBA2	Bank Select	M8	O	GV_{DD}	—
MA00	Address	Y9	O	GV_{DD}	—
MA01	Address	U6	O	GV_{DD}	—
MA02	Address	U7	O	GV_{DD}	—
MA03	Address	U9	O	GV_{DD}	—
MA04	Address	U10	O	GV_{DD}	—
MA05	Address	T8	O	GV_{DD}	—
MA06	Address	T9	O	GV_{DD}	—
MA07	Address	R8	O	GV_{DD}	—
MA08	Address	R7	O	GV_{DD}	—
MA09	Address	P6	O	GV_{DD}	—
MA10	Address	AA7	O	GV_{DD}	—
MA11	Address	P7	O	GV_{DD}	—
MA12	Address	N6	O	GV_{DD}	—
MA13	Address	AE8	O	GV_{DD}	—
MA14	Address	M7	O	GV_{DD}	—
MA15	Address	L6	O	GV_{DD}	—
$\overline{\text{MWE}}$	Write Enable	AB8	O	GV_{DD}	—
$\overline{\text{MRAS}}$	Row Address Strobe	AA10	O	GV_{DD}	—
$\overline{\text{MCAS}}$	Column Address Strobe	AC10	O	GV_{DD}	—
$\overline{\text{MCS0}}$	Chip Select	AC9	O	GV_{DD}	—
$\overline{\text{MCS1}}$	Chip Select	AE9	O	GV_{DD}	—
$\overline{\text{MCS2}}$	Chip Select	AB9	O	GV_{DD}	—
$\overline{\text{MCS3}}$	Chip Select	AF9	O	GV_{DD}	—
MCKE0	Clock Enable	P10	O	GV_{DD}	—
MCKE1	Clock Enable	R10	O	GV_{DD}	—
MCKE2	Clock Enable	P9	O	GV_{DD}	—
MCKE3	Clock Enable	N9	O	GV_{DD}	—
MCK0	Clock	W6	O	GV_{DD}	—
MCK1	Clock	V6	O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
MCK2	Clock	V8	O	GV_{DD}	—
MCK3	Clock	W9	O	GV_{DD}	—
$\overline{\text{MCK0}}$	Clock complements	W5	O	GV_{DD}	—
$\overline{\text{MCK1}}$	Clock complements	V5	O	GV_{DD}	—
$\overline{\text{MCK2}}$	Clock complements	V9	O	GV_{DD}	—
$\overline{\text{MCK3}}$	Clock complements	W8	O	GV_{DD}	—
MODT0	On-die termination	AD10	O	GV_{DD}	—
MODT1	On-die termination	AG10	O	GV_{DD}	—
MODT2	On-die termination	AD8	O	GV_{DD}	—
MODT3	On-die termination	AF10	O	GV_{DD}	—
MDIC0	Driver impedance calibration	T6	I/O	GV_{DD}	16
MDIC1	Driver impedance calibration	AA5	I/O	GV_{DD}	16
Local Bus Controller Interface					
LAD00	Muxed data/address	K26	I/O	BV_{DD}	3
LAD01	Muxed data/address	L26	I/O	BV_{DD}	3
LAD02	Muxed data/address	J26	I/O	BV_{DD}	3
LAD03	Muxed data/address	H25	I/O	BV_{DD}	3
LAD04	Muxed data/address	F25	I/O	BV_{DD}	3
LAD05	Muxed data/address	H24	I/O	BV_{DD}	3
LAD06	Muxed data/address	G24	I/O	BV_{DD}	3
LAD07	Muxed data/address	G23	I/O	BV_{DD}	3
LAD08	Muxed data/address	E23	I/O	BV_{DD}	3
LAD09	Muxed data/address	D23	I/O	BV_{DD}	3
LAD10	Muxed data/address	J22	I/O	BV_{DD}	3
LAD11	Muxed data/address	G22	I/O	BV_{DD}	3
LAD12	Muxed data/address	F19	I/O	BV_{DD}	3
LAD13	Muxed data/address	J18	I/O	BV_{DD}	3
LAD14	Muxed data/address	K18	I/O	BV_{DD}	3
LAD15	Muxed data/address	J17	I/O	BV_{DD}	3
LAD16	Muxed data/address	J25	I/O	BV_{DD}	35
LAD17	Muxed data/address	G25	I/O	BV_{DD}	35
LAD18	Muxed data/address	H23	I/O	BV_{DD}	35
LAD19	Muxed data/address	F22	I/O	BV_{DD}	35
LAD20	Muxed data/address	H22	I/O	BV_{DD}	35

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
LAD21	Muxed data/address	E21	I/O	BV_{DD}	35
LAD22	Muxed data/address	F21	I/O	BV_{DD}	35
LAD23	Muxed data/address	H21	I/O	BV_{DD}	3
LAD24	Muxed data/address	K21	I/O	BV_{DD}	3
LAD25	Muxed data/address	G20	I/O	BV_{DD}	35
LAD26	Muxed data/address	J20	I/O	BV_{DD}	3,32
LAD27	Muxed data/address	D26	I/O	BV_{DD}	—
LAD28	Muxed data/address	E18	I/O	BV_{DD}	—
LAD29	Muxed data/address	F18	I/O	BV_{DD}	—
LAD30	Muxed data/address	J15	I/O	BV_{DD}	—
LAD31	Muxed data/address	F17	I/O	BV_{DD}	—
LDP0	Data parity	J24	I/O	BV_{DD}	—
LDP1	Data parity	K23	I/O	BV_{DD}	—
LDP2	Data parity	H17	I/O	BV_{DD}	—
LDP3	Data parity	H16	I/O	BV_{DD}	—
LA27	Non-muxed address	K20	O	BV_{DD}	—
LA28	Non-muxed address	G19	O	BV_{DD}	35
LA29	Non-muxed Address	H19	O	BV_{DD}	35
LA30	Non-muxed Address	J19	O	BV_{DD}	35
LA31	Non-muxed Address	G18	O	BV_{DD}	35
$\overline{\text{LCS0}}$	Chip selects	D19	O	BV_{DD}	5
$\overline{\text{LCS1}}$	Chip selects	D20	O	BV_{DD}	5
$\overline{\text{LCS2}}$	Chip selects	E20	O	BV_{DD}	5
$\overline{\text{LCS3}}$	Chip selects	D21	O	BV_{DD}	5
$\overline{\text{LCS4}}$	Chip selects	D22	O	BV_{DD}	5
$\overline{\text{LCS5}}$	Chip selects	B23	O	BV_{DD}	5
$\overline{\text{LCS6}}$	Chip selects	F24	O	BV_{DD}	5
$\overline{\text{LCS7}}$	Chip selects	G26	O	BV_{DD}	5
$\overline{\text{LWE0}}$	Write enable	D24	O	BV_{DD}	—
$\overline{\text{LWE1}}$	Write enable	A24	O	BV_{DD}	—
$\overline{\text{LWE2}}$	Write enable	J16	O	BV_{DD}	—
$\overline{\text{LWE3}}$	Write enable	K15	O	BV_{DD}	—
LBCTL	Buffer control	C22	O	BV_{DD}	—
LALE	Address latch enable	A23	I/O	BV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
LGPL0/LFCLE	UPM general purpose line 0/ LFCLE—FCM	B25	O	BV_{DD}	3, 4
LGPL1/LFALE	UPM general purpose line 1/ LFALE—FCM	E25	O	BV_{DD}	3, 4
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM general purpose line 2/ LOE_B—Output Enable	D25	O	BV_{DD}	3, 4
LGPL3/$\overline{\text{LFWP}}$	UPM general purpose IIne 3/ LFWP_B—FCM	H26	O	BV_{DD}	3, 4
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	UPM general purpose line 4/ LGTA_B—FCM	C25	I/O	BV_{DD}	40
LGPL5	UPM general purpose line 5/Amux	E26	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	C24	O	BV_{DD}	—
LCLK1	Local Bus Clock	C23	O	BV_{DD}	—
DMA					
$\overline{\text{DMA1\_DREQ0}}$/GPIO18	DMA1 channel 0 request	AP21	I	OV_{DD}	26
$\overline{\text{DMA1\_DACK0}}$/GPIO19	DMA1 channel 0 acknowledge	AL19	O	OV_{DD}	26
$\overline{\text{DMA1\_DDONE0}}$	DMA1 channel 0 done	AN21	O	OV_{DD}	27
$\overline{\text{DMA2\_DREQ0}}$/GPIO20/ALT_MDVAL	DMA2 channel 0 request	AJ20	I	OV_{DD}	26
$\overline{\text{DMA2\_DACK0}}$/$\overline{\text{EVT7}}$/ALT_MDSRCID0	DMA2 channel 0 acknowledge	AG19	O	OV_{DD}	26
$\overline{\text{DMA2\_DDONE0}}$/$\overline{\text{EVT8}}$/ALT_MDSRCID1	DMA2 channel 0 done	AP20	O	OV_{DD}	26
USB Host Port 1					
USB1_UDP	USB1 PHY data plus	AT27	I/O	$USB\_V_{DD}\_3P3$	—
USB1_UDM	USB1 PHY data minus	AT26	I/O	$USB\_V_{DD}\_3P3$	—
USB1_VBUS_CLMP	USB1 PHY VBUS divided signals	AK25	I	$USB\_V_{DD}\_3P3$	38
USB1_UID	USB1 PHY ID detect	AK24	I	$USB1\_V_{DD}\_1P8\_DECAP$	—
USB_CLKIN	USB PHY clock input	AM24	I	OV_{DD}	—
USB1_DRVVBUS/GPIO4	USB1 5V supply enable	AH21	O	OV_{DD}	—
USB1_PWRFAULT/GPIO5	USB1 Power fault	AJ21	I	OV_{DD}	—
USB Host Port 2					
USB2_UDP	USB2 PHY data plus	AP27	I/O	$USB\_V_{DD}\_3P3$	—
USB2_UDM	USB2 PHY data minus	AP26	I/O	$USB\_V_{DD}\_3P3$	—
USB2_VBUS_CLMP	USB2 PHY VBUS divided signals	AK26	I	$USB\_V_{DD}\_3P3$	38
USB2_UID	USB2 PHY ID detect	AK27	I	$USB2\_V_{DD}\_1P8\_DECAP$	—
USB2_DRVVBUS/GPIO6	USB2 5V supply enable	AK21	O	OV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
USB2_PWRFAULT/GPIO7	USB2 Power Fault	AG20	I	OV_{DD}	—
Programmable Interrupt Controller					
IRQ00	External Interrupts	AJ16	I	OV_{DD}	—
IRQ01	External Interrupts	AH16	I	OV_{DD}	—
IRQ02	External Interrupts	AK12	I	OV_{DD}	—
IRQ03/GPIO21	External Interrupts	AJ15	I	OV_{DD}	26
IRQ04/GPIO22	External Interrupts	AH17	I	OV_{DD}	26
IRQ05/GPIO23	External Interrupts	AJ13	I	OV_{DD}	26
IRQ06/GPIO24	External Interrupts	AG17	I	OV_{DD}	26
IRQ07/GPIO25	External Interrupts	AM13	I	OV_{DD}	26
IRQ08/GPIO26	External Interrupts	AG13	I	OV_{DD}	26
IRQ09/GPIO27	External Interrupts	AK11	I	OV_{DD}	26
IRQ10/GPIO28	External Interrupts	AH14	I	OV_{DD}	26
IRQ11/GPIO29	External Interrupts	AL12	I	OV_{DD}	26
$\overline{\text{IRQ\_OUT}}$/$\overline{\text{EVT9}}$	Interrupt Output	AK14	O	OV_{DD}	1, 2, 26
Trust					
$\overline{\text{TMP\_DETECT}}$	Tamper detect	AN19	I	OV_{DD}	27
$\overline{\text{LP\_TMP\_DETECT}}$	Low power tamper detect	AE28	I	V_{DD_LP}	27
eSDHC					
SDHC_CMD	Command/response	AG23	I/O	CV_{DD}	—
SDHC_DAT0	Data	AP24	I/O	CV_{DD}	—
SDHC_DAT1	Data	AT24	I/O	CV_{DD}	—
SDHC_DAT2	Data	AM23	I/O	CV_{DD}	—
SDHC_DAT3	Data	AG22	I/O	OV_{DD}	—
SDHC_DAT4/$\overline{\text{SPI\_CS0}}$	Data	AN29	O	CV_{DD}	26, 31
SDHC_DAT5/$\overline{\text{SPI\_CS1}}$	Data	AJ28	O	CV_{DD}	26, 31
SDHC_DAT6/$\overline{\text{SPI\_CS2}}$	Data	AR29	O	CV_{DD}	26, 31
SDHC_DAT7/$\overline{\text{SPI\_CS3}}$	Data	AM29	O	CV_{DD}	26, 31
SDHC_CLK	Host to card clock	AL23	O	CV_{DD}	—
$\overline{\text{SDHC\_CD}}$/IIC3_SCL/GPIO16	Card detection	AK13	I	OV_{DD}	26, 27,31
SDHC_WP/IIC3_SDA/GPIO17	Card write protection	AM14	I	OV_{DD}	26, 27,31

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
eSPI					
SPI_MOSI	Master out slave in	AT29	I/O	CV_{DD}	—
SPI_MISO	Master in slave out	AH28	I	CV_{DD}	—
SPI_CLK	eSPI clock	AK29	O	CV_{DD}	—
$\overline{\text{SPI\_CS0}}$/SDHC_DAT4	eSPI chip select	AN29	O	CV_{DD}	26
$\overline{\text{SPI\_CS1}}$/SDHC_DAT5	eSPI chip select	AJ28	O	CV_{DD}	26
$\overline{\text{SPI\_CS2}}$/SDHC_DAT6	eSPI chip select	AR29	O	CV_{DD}	26
$\overline{\text{SPI\_CS3}}$/SDHC_DAT7	eSPI chip select	AM29	O	CV_{DD}	26
IEEE 1588					
TSEC_1588_CLK_IN	Clock in	AL35	I	LV_{DD}	—
TSEC_1588_TRIG_IN1	Trigger in 1	AL36	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RX_ER	Trigger in 2	AK36	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1	Alarm out 1	AJ36	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/EC1_COL/GPIO30	Alarm out 2	AK35	O	LV_{DD}	26
TSEC_1588_CLK_OUT	Clock out	AM30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1	Pulse out1	AL30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_CRS/GPIO31	Pulse out2	AJ34	O	LV_{DD}	26
Ethernet Management Interface 1					
EMI1_MDC	Management data clock	AJ33	O	LV_{DD}	—
EMI1_MDIO	Management data in/out	AL32	I/O	LV_{DD}	—
Ethernet Management Interface 2					
EMI2_MDC	Management data clock	AK30	O	1.2 V	2, 18, 22
EMI2_MDIO	Management data in/out	AJ30	I/O	1.2 V	2, 18, 22
Ethernet Reference Clock					
EC1_GTX_CLK125	Reference clock (RGMII)	AK34	I	LV_{DD}	27
EC2_GTX_CLK125	Reference clock (RGMII)	AL33	I	LV_{DD}	27
Ethernet External Timestamping					
EC_XTRNL_TX_STMP1	External timestamp transmit 1	AM31	I	LV_{DD}	—
EC_XTRNL_RX_STMP1	External timestamp receive 1	AK32	I	LV_{DD}	—
EC_XTRNL_TX_STMP2	External timestamp transmit 2	AJ31	I	LV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
EC_XTRNL_RX_STMP2	External timestamp receive 2	AK31	I	LV_{DD}	—
Three-Speed Ethernet Controller 1					
EC1_TXD3	Transmit data	AP36	O	LV_{DD}	—
EC1_TXD2	Transmit data	AT34	O	LV_{DD}	—
EC1_TXD1	Transmit data	AR34	O	LV_{DD}	—
EC1_TXD0	Transmit data	AT35	O	LV_{DD}	—
EC1_TX_EN	Transmit enable	AR36	O	LV_{DD}	15
EC1_GTX_CLK	Transmit clock out (RGMII)	AP35	O	LV_{DD}	26
EC1_RXD3	Receive data	AM33	I	LV_{DD}	27
EC1_RXD2	Receive data	AN34	I	LV_{DD}	27
EC1_RXD1	Receive data	AN35	I	LV_{DD}	27
EC1_RXD0	Receive data	AN36	I	LV_{DD}	27
EC1_RX_DV	Receive data valid	AM34	I	LV_{DD}	27
EC1_RX_CLK	Receive clock	AM36	I	LV_{DD}	27
TSEC_1588_TRIG_IN2	Trig In 1	AK36	I	LV_{DD}	—
TSEC_1588_ALARM_OUT2	1588 alarm out 2	AK35	O	LV_{DD}	26
GPIO31/TSEC_1588_PULSE_OUT2	Pulse out 2	AJ34	O	LV_{DD}	26
Three-Speed Ethernet Controller 2					
EC2_TXD3	Transmit data	AT31	O	LV_{DD}	—
EC2_TXD2	Transmit data	AP30	O	LV_{DD}	—
EC2_TXD1	Transmit data	AR30	O	LV_{DD}	—
EC2_TXD0	Transmit data	AT30	O	LV_{DD}	—
EC2_TX_EN	Transmit enable	AR31	O	LV_{DD}	15
EC2_GTX_CLK	Transmit clock out (RGMII)	AN31	O	LV_{DD}	26
EC2_RXD3	Receive data	AP33	I	LV_{DD}	27
EC2_RXD2	Receive data	AN32	I	LV_{DD}	27
EC2_RXD1	Receive data	AP32	I	LV_{DD}	26, 27
EC2_RXD0	Receive data	AT32	I	LV_{DD}	26, 27
EC2_RX_DV	Receive data valid	AR33	I	LV_{DD}	27
EC2_RX_CLK	Receive clock	AT33	I	LV_{DD}	27
UART					
UART1_SOUT/GPIO8	Transmit data	AL22	O	OV_{DD}	26
UART2_SOUT/GPIO9	Transmit data	AJ22	O	OV_{DD}	26

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
UART1_SIN/GPIO10	Receive data	AR23	I	OV_{DD}	26
UART2_SIN/GPIO11	Receive data	AN23	I	OV_{DD}	26
$\overline{\text{UART1\_RTS}}$/UART3_SOUT/GPIO12	Ready to send	AM22	O	OV_{DD}	26
$\overline{\text{UART2\_RTS}}$/UART4_SOUT/GPIO13	Ready to send	AK23	O	OV_{DD}	26
$\overline{\text{UART1\_CTS}}$/UART3_SIN/GPIO14	Clear to send	AP22	I	OV_{DD}	26
$\overline{\text{UART2\_CTS}}$/UART4_SIN/GPIO15	Clear to send	AH23	I	OV_{DD}	26
I^2C Interface					
IIC1_SCL	Serial clock	AH15	I/O	OV_{DD}	2, 14
IIC1_SDA	Serial data	AN14	I/O	OV_{DD}	2, 14
IIC2_SCL	Serial clock	AM15	I/O	OV_{DD}	2, 14
IIC2_SDA	Serial data	AL14	I/O	OV_{DD}	2, 14
IIC3_SCL/$\overline{\text{SDHC\_CD}}$/GPIO16	Serial clock	AK13	I/O	OV_{DD}	2, 14, 27
IIC3_SDA/SDHC_WP/GPIO17	Serial data	AM14	I/O	OV_{DD}	2, 14, 27
IIC4_SCL/$\overline{\text{EVT5}}$	Serial clock	AG14	I/O	OV_{DD}	2, 14
IIC4_SDA/$\overline{\text{EVT6}}$	Serial data	AL15	I/O	OV_{DD}	2, 14
SerDes (x18) PCIe, Serial RapidIO, Aurora, 10GE, 1GE					
SD_TX17	Transmit data (positive)	AG31	O	XV_{DD}	—
SD_TX16	Transmit data (positive)	AE31	O	XV_{DD}	—
SD_TX15	Transmit data (positive)	AB33	O	XV_{DD}	—
SD_TX14	Transmit data (positive)	AA31	O	XV_{DD}	—
SD_TX13	Transmit data (positive)	Y29	O	XV_{DD}	—
SD_TX12	Transmit data (positive)	W31	O	XV_{DD}	—
SD_TX11	Transmit data (positive)	T30	O	XV_{DD}	—
SD_TX10	Transmit data (positive)	P31	O	XV_{DD}	—
SD_TX09	Transmit data (positive)	N33	O	XV_{DD}	—
SD_TX08	Transmit data (positive)	M31	O	XV_{DD}	—
SD_TX07	Transmit data (positive)	K31	O	XV_{DD}	—
SD_TX06	Transmit data (positive)	J33	O	XV_{DD}	—
SD_TX05	Transmit data (positive)	G33	O	XV_{DD}	—
SD_TX04	Transmit data (positive)	D34	O	XV_{DD}	—
SD_TX03	Transmit data (positive)	F31	O	XV_{DD}	—
SD_TX02	Transmit data (positive)	H30	O	XV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
SD_TX01	Transmit data (positive)	F29	O	XV_{DD}	—
SD_TX00	Transmit data (positive)	H28	O	XV_{DD}	—
$\overline{\text{SD\_TX17}}$	Transmit data (negative)	AG32	O	XV_{DD}	—
$\overline{\text{SD\_TX16}}$	Transmit data (negative)	AE32	O	XV_{DD}	—
$\overline{\text{SD\_TX15}}$	Transmit data (negative)	AB34	O	XV_{DD}	—
$\overline{\text{SD\_TX14}}$	Transmit data (negative)	AA32	O	XV_{DD}	—
$\overline{\text{SD\_TX13}}$	Transmit data (negative)	Y30	O	XV_{DD}	—
$\overline{\text{SD\_TX12}}$	Transmit data (negative)	W32	O	XV_{DD}	—
$\overline{\text{SD\_TX11}}$	Transmit data (negative)	T31	O	XV_{DD}	—
$\overline{\text{SD\_TX10}}$	Transmit data (negative)	P32	O	XV_{DD}	—
$\overline{\text{SD\_TX09}}$	Transmit data (negative)	N34	O	XV_{DD}	—
$\overline{\text{SD\_TX08}}$	Transmit data (negative)	M32	O	XV_{DD}	—
$\overline{\text{SD\_TX07}}$	Transmit data (negative)	K32	O	XV_{DD}	—
$\overline{\text{SD\_TX06}}$	Transmit data (negative)	J34	O	XV_{DD}	—
$\overline{\text{SD\_TX05}}$	Transmit data (negative)	F33	O	XV_{DD}	—
$\overline{\text{SD\_TX04}}$	Transmit data (negative)	E34	O	XV_{DD}	—
$\overline{\text{SD\_TX03}}$	Transmit data (negative)	E31	O	XV_{DD}	—
$\overline{\text{SD\_TX02}}$	Transmit data (negative)	G30	O	XV_{DD}	—
$\overline{\text{SD\_TX01}}$	Transmit data (negative)	E29	O	XV_{DD}	—
$\overline{\text{SD\_TX00}}$	Transmit data (negative)	G28	O	XV_{DD}	—
SD_RX17	Receive data (positive)	AG36	I	XV_{DD}	—
SD_RX16	Receive data (positive)	AF34	I	XV_{DD}	—
SD_RX15	Receive data (positive)	AC36	I	XV_{DD}	—
SD_RX14	Receive data (positive)	AA36	I	XV_{DD}	—
SD_RX13	Receive data (positive)	Y34	I	XV_{DD}	—
SD_RX12	Receive data (positive)	W36	I	XV_{DD}	—
SD_RX11	Receive data (positive)	T34	I	XV_{DD}	—
SD_RX10	Receive data (positive)	P36	I	XV_{DD}	—
SD_RX09	Receive data (positive)	M36	I	XV_{DD}	—
SD_RX08	Receive data (positive)	L34	I	XV_{DD}	—
SD_RX07	Receive data (positive)	K36	I	XV_{DD}	—
SD_RX06	Receive data (positive)	H36	I	XV_{DD}	—
SD_RX05	Receive data (positive)	F36	I	XV_{DD}	—
SD_RX04	Receive data (positive)	D36	I	XV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
SD_RX03	Receive data (positive)	A31	I	XV_{DD}	—
SD_RX02	Receive data (positive)	C30	I	XV_{DD}	—
SD_RX01	Receive data (positive)	A29	I	XV_{DD}	—
SD_RX00	Receive data (positive)	C28	I	XV_{DD}	—
$\overline{\text{SD\_RX17}}$	Receive data (negative)	AG35	I	XV_{DD}	—
$\overline{\text{SD\_RX16}}$	Receive data (negative)	AF33	I	XV_{DD}	—
$\overline{\text{SD\_RX15}}$	Receive data (negative)	AC35	I	XV_{DD}	—
$\overline{\text{SD\_RX14}}$	Receive data (negative)	AA35	I	XV_{DD}	—
$\overline{\text{SD\_RX13}}$	Receive data (negative)	Y33	I	XV_{DD}	—
$\overline{\text{SD\_RX12}}$	Receive data (negative)	W35	I	XV_{DD}	—
$\overline{\text{SD\_RX11}}$	Receive data (negative)	T33	I	XV_{DD}	—
$\overline{\text{SD\_RX10}}$	Receive data (negative)	P35	I	XV_{DD}	—
$\overline{\text{SD\_RX09}}$	Receive data (negative)	M35	I	XV_{DD}	—
$\overline{\text{SD\_RX08}}$	Receive data (negative)	L33	I	XV_{DD}	—
$\overline{\text{SD\_RX07}}$	Receive data (negative)	K35	I	XV_{DD}	—
$\overline{\text{SD\_RX06}}$	Receive data (negative)	H35	I	XV_{DD}	—
$\overline{\text{SD\_RX05}}$	Receive data (negative)	F35	I	XV_{DD}	—
$\overline{\text{SD\_RX04}}$	Receive data (negative)	C36	I	XV_{DD}	—
$\overline{\text{SD\_RX03}}$	Receive data (negative)	B31	I	XV_{DD}	—
$\overline{\text{SD\_RX02}}$	Receive data (negative)	D30	I	XV_{DD}	—
$\overline{\text{SD\_RX01}}$	Receive data (negative)	B29	I	XV_{DD}	—
$\overline{\text{SD\_RX00}}$	Receive data (negative)	D28	I	XV_{DD}	—
SD_REF_CLK1	SerDes bank 1 PLL reference clock	A35	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK1}}$	SerDes bank 1 PLL reference clock complement	B35	I	XV_{DD}	—
SD_REF_CLK2	SerDes bank 2 PLL reference clock	V34	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK2}}$	SerDes bank 2 PLL reference clock complement	V33	I	XV_{DD}	—
SD_REF_CLK3	SerDes bank 3 PLL reference clock	AC32	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK3}}$	SerDes bank 3 PLL reference clock complement	AC31	I	XV_{DD}	—
General-Purpose Input/Output					
GPIO0	General purpose input/output	AL21	I/O	OV_{DD}	—
GPIO1	General purpose input/output	AK22	I/O	OV_{DD}	—
GPIO2	General purpose input/output	AM20	I/O	OV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GPIO3	General purpose input/output	AN20	I/O	OV_{DD}	—
GPIO4/USB1_DRVVBUS	General purpose input/output	AH21	I/O	OV_{DD}	—
GPIO5/USB1_PWRFAULT	General purpose input/output	AJ21	I/O	OV_{DD}	—
GPIO6/USB2_DRVVBUS	General purpose input/output	AK21	I/O	OV_{DD}	—
GPIO7/USB2_PWRFAULT	General purpose input/output	AG20	I/O	OV_{DD}	—
GPIO8/UART1_SOUT	General purpose input/output	AL22	I/O	OV_{DD}	—
GPIO9/UART2_SOUT	General purpose input/output	AJ22	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General purpose input/output	AR23	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General purpose input/output	AN23	I/O	OV_{DD}	—
GPIO12/$\overline{\text{UART1\_RTS}}$/UART3_SOUT	General purpose input/output	AM22	I/O	OV_{DD}	—
GPIO13/$\overline{\text{UART2\_RTS}}$/UART4_SOUT	General purpose input/output	AK23	I/O	OV_{DD}	—
GPIO14/$\overline{\text{UART1\_CTS}}$/UART3_SIN	General purpose input/output	AP22	I/O	OV_{DD}	—
GPIO15/$\overline{\text{UART2\_CTS}}$/UART4_SIN	General purpose input/output	AH23	I/O	OV_{DD}	—
GPIO16/IIC3_SCL/$\overline{\text{SDHC\_CD}}$	General purpose input/output	AK13	I/O	OV_{DD}	27
GPIO17/IIC3_SDA/SDHC_WP	General purpose input/output	AM14	I/O	OV_{DD}	27
GPIO18/$\overline{\text{DMA1\_DREQ0}}$	General purpose input/output	AP21	I/O	OV_{DD}	—
GPIO19/$\overline{\text{DMA1\_DACK0}}$	General purpose input/output	AL19	I/O	OV_{DD}	—
GPIO20/$\overline{\text{DMA2\_DREQ0}}$/ALT_MDVAL	General purpose input/output	AJ20	I/O	OV_{DD}	—
GPIO21/IRQ03	General purpose input/output	AJ15	I/O	OV_{DD}	—
GPIO22/IRQ04	General purpose input/output	AH17	I/O	OV_{DD}	—
GPIO23/IRQ05	General purpose input/output	AJ13	I/O	OV_{DD}	—
GPIO24/IRQ06	General purpose input/output	AG17	I/O	OV_{DD}	—
GPIO25/IRQ07	General purpose input/output	AM13	I/O	OV_{DD}	—
GPIO26/IRQ08	General purpose input/output	AG13	I/O	OV_{DD}	—
GPIO27/IRQ09	General purpose input/output	AK11	I/O	OV_{DD}	—
GPIO28/IRQ10	General purpose input/output	AH14	I/O	OV_{DD}	—
GPIO29/IRQ11	General purpose input/output	AL12	I/O	OV_{DD}	—
GPIO30/TSEC_1588_ALARM_OUT2	General purpose input/output	AK35	I/O	LV_{DD}	25
GPIO31/TSEC_1588_PULSE_OUT2	General purpose input/output	AJ34	I/O	LV_{DD}	25
System Control					
$\overline{\text{PORESET}}$	Power on reset	AP17	I	OV_{DD}	—
$\overline{\text{HRESET}}$	Hard reset	AR17	I/O	OV_{DD}	1, 2
$\overline{\text{RESET\_REQ}}$	Reset request	AT16	O	OV_{DD}	35
$\overline{\text{CKSTP\_OUT}}$	Checkstop out	AM19	O	OV_{DD}	1, 2

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
Debug					
$\overline{\text{EVT0}}$	Event 0	AJ17	I/O	OV_{DD}	20
$\overline{\text{EVT1}}$	Event 1	AK17	I/O	OV_{DD}	—
$\overline{\text{EVT2}}$	Event 2	AN16	I/O	OV_{DD}	—
$\overline{\text{EVT3}}$	Event 3	AK16	I/O	OV_{DD}	—
$\overline{\text{EVT4}}$	Event 4	AM16	I/O	OV_{DD}	—
$\overline{\text{EVT5}}$/IIC4_SCL	Event 5	AG14	I/O	OV_{DD}	—
$\overline{\text{EVT6}}$/IIC4_SDA	Event 6	AL15	I/O	OV_{DD}	—
$\overline{\text{EVT7}}$/$\overline{\text{DMA2\_DACK0}}$/ALT_MSRCID0	Event 7	AG19	I/O	OV_{DD}	—
$\overline{\text{EVT8}}$/$\overline{\text{DMA2\_DDONE0}}$/ALT_MSRCID1	Event 8	AP20	I/O	OV_{DD}	—
$\overline{\text{EVT9}}$/$\overline{\text{IRQ\_OUT}}$	Event 9	AK14	I/O	OV_{DD}	—
MDVAL	Debug data valid	AR15	O	OV_{DD}	—
MSRCID0	Debug source ID 0	AH20	O	OV_{DD}	4, 35
MSRCID1	Debug source ID 1	AJ19	O	OV_{DD}	—
MSRCID2	Debug source ID 2	AH18	O	OV_{DD}	—
ALT_MDVAL/$\overline{\text{DMA2\_DREQ0}}$/GPIO20	Alternate debug data valid	AJ20	O	OV_{DD}	26
ALT_MSRCID0/$\overline{\text{DMA2\_DACK0}}$/$\overline{\text{EVT7}}$	Alternate debug source ID 0	AG19	O	OV_{DD}	26
ALT_MSRCID1/$\overline{\text{DMA2\_DDONE0}}$/$\overline{\text{EVT8}}$	Alternate debug source ID 1	AP20	O	OV_{DD}	26
CLK_OUT	Clock out	AK20	O	OV_{DD}	6
Clock					
RTC	Real time clock	AN24	I	OV_{DD}	—
SYSCLK	System clock	AT23	I	OV_{DD}	—
JTAG					
TCK	Test clock	AR22	I	OV_{DD}	—
TDI	Test data in	AN17	I	OV_{DD}	7
TDO	Test data out	AP15	O	OV_{DD}	6
TMS	Test mode select	AR20	I	OV_{DD}	7
$\overline{\text{TRST}}$	Test reset	AR19	I	OV_{DD}	7
DFT					
$\overline{\text{SCAN\_MODE}}$	Scan mode	AL17	I	OV_{DD}	39
TEST_SEL	Test mode select	AT21	I	OV_{DD}	12, 28
Power Management					
ASLEEP	Asleep	AR21	O	OV_{DD}	35

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
Input /Output Voltage Select					
IO_VSEL0	I/O Voltage select	AL18	I	OV_{DD}	30
IO_VSEL1	I/O Voltage select	AP18	I	OV_{DD}	30
IO_VSEL2	I/O Voltage select	AK18	I	OV_{DD}	30
IO_VSEL3	I/O Voltage select	AM18	I	OV_{DD}	30
IO_VSEL4	I/O Voltage select	AH19	I	OV_{DD}	30
Power and Ground Signals					
GND	Ground	A18	—	—	—
GND	Ground	A22	—	—	—
GND	Ground	A26	—	—	—
GND	Ground	B5	—	—	—
GND	Ground	B11	—	—	—
GND	Ground	B18	—	—	—
GND	Ground	B20	—	—	—
GND	Ground	B22	—	—	—
GND	Ground	C3	—	—	—
GND	Ground	C9	—	—	—
GND	Ground	C15	—	—	—
GND	Ground	D7	—	—	—
GND	Ground	D13	—	—	—
GND	Ground	E5	—	—	—
GND	Ground	E11	—	—	—
GND	Ground	E17	—	—	—
GND	Ground	E19	—	—	—
GND	Ground	F3	—	—	—
GND	Ground	F9	—	—	—
GND	Ground	F15	—	—	—
GND	Ground	F23	—	—	—
GND	Ground	F27	—	—	—
GND	Ground	G7	—	—	—
GND	Ground	G13	—	—	—
GND	Ground	G17	—	—	—
GND	Ground	G21	—	—	—
GND	Ground	H5	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GND	Ground	H11	—	—	—
GND	Ground	J3	—	—	—
GND	Ground	J9	—	—	—
GND	Ground	J21	—	—	—
GND	Ground	J23	—	—	—
GND	Ground	J27	—	—	—
GND	Ground	K7	—	—	—
GND	Ground	K19	—	—	—
GND	Ground	K25	—	—	—
GND	Ground	L5	—	—	—
GND	Ground	L12	—	—	—
GND	Ground	L14	—	—	—
GND	Ground	L16	—	—	—
GND	Ground	L18	—	—	—
GND	Ground	L20	—	—	—
GND	Ground	L22	—	—	—
GND	Ground	L24	—	—	—
GND	Ground	M3	—	—	—
GND	Ground	M9	—	—	—
GND	Ground	M11	—	—	—
GND	Ground	M13	—	—	—
GND	Ground	M15	—	—	—
GND	Ground	M17	—	—	—
GND	Ground	M19	—	—	—
GND	Ground	M21	—	—	—
GND	Ground	M23	—	—	—
GND	Ground	M25	—	—	—
GND	Ground	M27	—	—	—
GND	Ground	N7	—	—	—
GND	Ground	N12	—	—	—
GND	Ground	N14	—	—	—
GND	Ground	N16	—	—	—
GND	Ground	N18	—	—	—
GND	Ground	N20	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GND	Ground	N22	—	—	—
GND	Ground	N24	—	—	—
GND	Ground	N26	—	—	—
GND	Ground	P5	—	—	—
GND	Ground	P11	—	—	—
GND	Ground	P13	—	—	—
GND	Ground	P15	—	—	—
GND	Ground	P17	—	—	—
GND	Ground	P19	—	—	—
GND	Ground	P21	—	—	—
GND	Ground	P23	—	—	—
GND	Ground	P25	—	—	—
GND	Ground	P27	—	—	—
GND	Ground	R3	—	—	—
GND	Ground	R9	—	—	—
GND	Ground	R12	—	—	—
GND	Ground	R14	—	—	—
GND	Ground	R16	—	—	—
GND	Ground	R18	—	—	—
GND	Ground	R20	—	—	—
GND	Ground	R22	—	—	—
GND	Ground	R24	—	—	—
GND	Ground	R26	—	—	—
GND	Ground	T7	—	—	—
GND	Ground	T11	—	—	—
GND	Ground	T13	—	—	—
GND	Ground	T15	—	—	—
GND	Ground	T17	—	—	—
GND	Ground	T19	—	—	—
GND	Ground	T21	—	—	—
GND	Ground	T23	—	—	—
GND	Ground	T25	—	—	—
GND	Ground	T27	—	—	—
GND	Ground	U3	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GND	Ground	U5	—	—	—
GND	Ground	U12	—	—	—
GND	Ground	U14	—	—	—
GND	Ground	U16	—	—	—
GND	Ground	U18	—	—	—
GND	Ground	U20	—	—	—
GND	Ground	U22	—	—	—
GND	Ground	U24	—	—	—
GND	Ground	U26	—	—	—
GND	Ground	V10	—	—	—
GND	Ground	V11	—	—	—
GND	Ground	V13	—	—	—
GND	Ground	V15	—	—	—
GND	Ground	V17	—	—	—
GND	Ground	V19	—	—	—
GND	Ground	V21	—	—	—
GND	Ground	V23	—	—	—
GND	Ground	V25	—	—	—
GND	Ground	V27	—	—	—
GND	Ground	W7	—	—	—
GND	Ground	W12	—	—	—
GND	Ground	W14	—	—	—
GND	Ground	W16	—	—	—
GND	Ground	W18	—	—	—
GND	Ground	W20	—	—	—
GND	Ground	W22	—	—	—
GND	Ground	W24	—	—	—
GND	Ground	W26	—	—	—
GND	Ground	Y3	—	—	—
GND	Ground	Y5	—	—	—
GND	Ground	Y11	—	—	—
GND	Ground	Y13	—	—	—
GND	Ground	Y15	—	—	—
GND	Ground	Y17	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GND	Ground	Y19	—	—	—
GND	Ground	Y21	—	—	—
GND	Ground	Y23	—	—	—
GND	Ground	Y25	—	—	—
GND	Ground	Y27	—	—	—
GND	Ground	AA9	—	—	—
GND	Ground	AA12	—	—	—
GND	Ground	AA14	—	—	—
GND	Ground	AA16	—	—	—
GND	Ground	AA18	—	—	—
GND	Ground	AA20	—	—	—
GND	Ground	AA22	—	—	—
GND	Ground	AA24	—	—	—
GND	Ground	AA26	—	—	—
GND	Ground	AB7	—	—	—
GND	Ground	AB11	—	—	—
GND	Ground	AB13	—	—	—
GND	Ground	AB15	—	—	—
GND	Ground	AB17	—	—	—
GND	Ground	AB19	—	—	—
GND	Ground	AB21	—	—	—
GND	Ground	AB23	—	—	—
GND	Ground	AB25	—	—	—
GND	Ground	AB27	—	—	—
GND	Ground	AC5	—	—	—
GND	Ground	AC12	—	—	—
GND	Ground	AC14	—	—	—
GND	Ground	AC16	—	—	—
GND	Ground	AC18	—	—	—
GND	Ground	AC20	—	—	—
GND	Ground	AC22	—	—	—
GND	Ground	AC24	—	—	—
GND	Ground	AC26	—	—	—
GND	Ground	AD3	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GND	Ground	AD9	—	—	—
GND	Ground	AD11	—	—	—
GND	Ground	AD13	—	—	—
GND	Ground	AD15	—	—	—
GND	Ground	AD17	—	—	—
GND	Ground	AD19	—	—	—
GND	Ground	AD21	—	—	—
GND	Ground	AD23	—	—	—
GND	Ground	AD25	—	—	—
GND	Ground	AD27	—	—	—
GND	Ground	AE7	—	—	—
GND	Ground	AE12	—	—	—
GND	Ground	AE14	—	—	—
GND	Ground	AE16	—	—	—
GND	Ground	AE18	—	—	—
GND	Ground	AE20	—	—	—
GND	Ground	AE22	—	—	—
GND	Ground	AE24	—	—	—
GND	Ground	AE26	—	—	—
GND	Ground	AE27	—	—	—
GND	Ground	AF5	—	—	—
GND	Ground	AF13	—	—	—
GND	Ground	AF15	—	—	—
GND	Ground	AF17	—	—	—
GND	Ground	AF19	—	—	—
GND	Ground	AF21	—	—	—
GND	Ground	AF23	—	—	—
GND	Ground	AF25	—	—	—
GND	Ground	AG3	—	—	—
GND	Ground	AG9	—	—	—
GND	Ground	AG18	—	—	—
GND	Ground	AH7	—	—	—
GND	Ground	AH13	—	—	—
GND	Ground	AH22	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GND	Ground	AH34	—	—	—
GND	Ground	AJ5	—	—	—
GND	Ground	AJ11	—	—	—
GND	Ground	AJ32	—	—	—
GND	Ground	AK3	—	—	—
GND	Ground	AK9	—	—	—
GND	Ground	AK15	—	—	—
GND	Ground	AK19	—	—	—
GND	Ground	AK28	—	—	—
GND	Ground	AL7	—	—	—
GND	Ground	AL13	—	—	—
GND	Ground	AL29	—	—	—
GND	Ground	AL34	—	—	—
GND	Ground	AM5	—	—	—
GND	Ground	AM11	—	—	—
GND	Ground	AM17	—	—	—
GND	Ground	AM21	—	—	—
GND	Ground	AM32	—	—	—
GND	Ground	AN3	—	—	—
GND	Ground	AN9	—	—	—
GND	Ground	AN15	—	—	—
GND	Ground	AN30	—	—	—
GND	Ground	AP7	—	—	—
GND	Ground	AP13	—	—	—
GND	Ground	AP19	—	—	—
GND	Ground	AP23	—	—	—
GND	Ground	AP34	—	—	—
GND	Ground	AR5	—	—	—
GND	Ground	AR11	—	—	—
GND	Ground	AR16	—	—	—
GND	Ground	AR18	—	—	—
GND	Ground	AR32	—	—	—
GND	Ground	AT22	—	—	—
GND	Ground	AT36	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
XGND	SerDes transceiver GND	D33	—	—	—
XGND	SerDes transceiver GND	E28	—	—	—
XGND	SerDes transceiver GND	E30	—	—	—
XGND	SerDes transceiver GND	G29	—	—	—
XGND	SerDes transceiver GND	G31	—	—	—
XGND	SerDes transceiver GND	F32	—	—	—
XGND	SerDes transceiver GND	H29	—	—	—
XGND	SerDes transceiver GND	H32	—	—	—
XGND	SerDes transceiver GND	H34	—	—	—
XGND	SerDes transceiver GND	J29	—	—	—
XGND	SerDes transceiver GND	J31	—	—	—
XGND	SerDes transceiver GND	K28	—	—	—
XGND	SerDes transceiver GND	K29	—	—	—
XGND	SerDes transceiver GND	L29	—	—	—
XGND	SerDes transceiver GND	L32	—	—	—
XGND	SerDes transceiver GND	M30	—	—	—
XGND	SerDes transceiver GND	N29	—	—	—
XGND	SerDes transceiver GND	N30	—	—	—
XGND	SerDes transceiver GND	N32	—	—	—
XGND	SerDes transceiver GND	P29	—	—	—
XGND	SerDes transceiver GND	P34	—	—	—
XGND	SerDes transceiver GND	R30	—	—	—
XGND	SerDes transceiver GND	R32	—	—	—
XGND	SerDes transceiver GND	U29	—	—	—
XGND	SerDes transceiver GND	U31	—	—	—
XGND	SerDes transceiver GND	V29	—	—	—
XGND	SerDes transceiver GND	V31	—	—	—
XGND	SerDes transceiver GND	W30	—	—	—
XGND	SerDes transceiver GND	Y32	—	—	—
XGND	SerDes transceiver GND	AA30	—	—	—
XGND	SerDes transceiver GND	AB32	—	—	—
XGND	SerDes transceiver GND	AC30	—	—	—
XGND	SerDes transceiver GND	AC34	—	—	—
XGND	SerDes transceiver GND	AD30	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
XGND	SerDes transceiver GND	AD31	—	—	—
XGND	SerDes transceiver GND	AF32	—	—	—
XGND	SerDes transceiver GND	AH31	—	—	—
XGND	SerDes transceiver GND	AG30	—	—	—
SGND	SerDes core logic GND	A28	—	—	—
SGND	SerDes core logic GND	A32	—	—	—
SGND	SerDes core logic GND	A36	—	—	—
SGND	SerDes core logic GND	B30	—	—	—
SGND	SerDes core logic GND	B34	—	—	—
SGND	SerDes core logic GND	C29	—	—	—
SGND	SerDes core logic GND	C33	—	—	—
SGND	SerDes core logic GND	D31	—	—	—
SGND	SerDes core logic GND	D35	—	—	—
SGND	SerDes core logic GND	E35	—	—	—
SGND	SerDes core logic GND	G34	—	—	—
SGND	SerDes core logic GND	G36	—	—	—
SGND	SerDes core logic GND	J35	—	—	—
SGND	SerDes core logic GND	K33	—	—	—
SGND	SerDes core logic GND	L36	—	—	—
SGND	SerDes core logic GND	M34	—	—	—
SGND	SerDes core logic GND	N35	—	—	—
SGND	SerDes core logic GND	R33	—	—	—
SGND	SerDes core logic GND	R36	—	—	—
SGND	SerDes core logic GND	T35	—	—	—
SGND	SerDes core logic GND	U34	—	—	—
SGND	SerDes core logic GND	V36	—	—	—
SGND	SerDes core logic GND	W33	—	—	—
SGND	SerDes core logic GND	Y35	—	—	—
SGND	SerDes core logic GND	AA34	—	—	—
SGND	SerDes core logic GND	AB36	—	—	—
SGND	SerDes core logic GND	AD35	—	—	—
SGND	SerDes core logic GND	AE34	—	—	—
SGND	SerDes core logic GND	AF36	—	—	—
SGND	SerDes core logic GND	AG33	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
SGND	SerDes core logic GND	AH33	—	—	—
SGND	SerDes core logic GND	AH35	—	—	—
AGND_SRDS1	SerDes PLL1 GND	B33	—	—	—
AGND_SRDS2	SerDes PLL2 GND	T36	—	—	—
AGND_SRDS3	SerDes PLL3 GND	AE36	—	—	—
SENSEGND_CA_PL	Core group A and Platform GND sense	K17	—	—	8
SENSEGND_CB	Core group B GND sense	AG16	—	—	8
OVDD	General I/O supply	AG21	—	OV_{DD}	—
OVDD	General I/O supply	AJ12	—	OV_{DD}	—
OVDD	General I/O supply	AJ14	—	OV_{DD}	—
OVDD	General I/O supply	AJ18	—	OV_{DD}	—
OVDD	General I/O supply	AJ23	—	OV_{DD}	—
OVDD	General I/O supply	AL16	—	OV_{DD}	—
OVDD	General I/O supply	AL20	—	OV_{DD}	—
OVDD	General I/O supply	AN18	—	OV_{DD}	—
OVDD	General I/O supply	AN22	—	OV_{DD}	—
OVDD	General I/O supply	AP16	—	OV_{DD}	—
OVDD	General I/O supply	AR24	—	OV_{DD}	—
OVDD	General I/O supply	AT15	—	OV_{DD}	—
CVDD	eSPI and eSDHC supply	AG24	—	CV_{DD}	—
CVDD	eSPI and& eSDHC supply	AJ29	—	CV_{DD}	—
CVDD	eSPI and& eSDHC supply	AP29	—	CV_{DD}	—
GVDD	DDR supply	B2	—	GV_{DD}	—
GVDD	DDR supply	B8	—	GV_{DD}	—
GVDD	DDR supply	B14	—	GV_{DD}	—
GVDD	DDR supply	C18	—	GV_{DD}	—
GVDD	DDR supply	C12	—	GV_{DD}	—
GVDD	DDR supply	C6	—	GV_{DD}	—
GVDD	DDR supply	D4	—	GV_{DD}	—
GVDD	DDR supply	D10	—	GV_{DD}	—
GVDD	DDR supply	D16	—	GV_{DD}	—
GVDD	DDR supply	E14	—	GV_{DD}	—
GVDD	DDR supply	E8	—	GV_{DD}	—
GVDD	DDR supply	E2	—	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GVDD	DDR supply	F6	—	GV_{DD}	—
GVDD	DDR supply	F12	—	GV_{DD}	—
GVDD	DDR supply	G4	—	GV_{DD}	—
GVDD	DDR supply	G10	—	GV_{DD}	—
GVDD	DDR supply	G16	—	GV_{DD}	—
GVDD	DDR supply	H14	—	GV_{DD}	—
GVDD	DDR supply	H8	—	GV_{DD}	—
GVDD	DDR supply	H2	—	GV_{DD}	—
GVDD	DDR supply	J6	—	GV_{DD}	—
GVDD	DDR supply	J12	—	GV_{DD}	—
GVDD	DDR supply	K10	—	GV_{DD}	—
GVDD	DDR supply	K4	—	GV_{DD}	—
GVDD	DDR supply	L2	—	GV_{DD}	—
GVDD	DDR supply	L8	—	GV_{DD}	—
GVDD	DDR supply	M6	—	GV_{DD}	—
GVDD	DDR supply	N4	—	GV_{DD}	—
GVDD	DDR supply	N10	—	GV_{DD}	—
GVDD	DDR supply	P8	—	GV_{DD}	—
GVDD	DDR supply	P2	—	GV_{DD}	—
GVDD	DDR supply	R6	—	GV_{DD}	—
GVDD	DDR supply	T10	—	GV_{DD}	—
GVDD	DDR supply	T4	—	GV_{DD}	—
GVDD	DDR supply	U2	—	GV_{DD}	—
GVDD	DDR supply	U8	—	GV_{DD}	—
GVDD	DDR supply	V7	—	GV_{DD}	—
GVDD	DDR supply	W10	—	GV_{DD}	—
GVDD	DDR supply	Y2	—	GV_{DD}	—
GVDD	DDR supply	Y8	—	GV_{DD}	—
GVDD	DDR supply	AA6	—	GV_{DD}	—
GVDD	DDR supply	AB4	—	GV_{DD}	—
GVDD	DDR supply	AB10	—	GV_{DD}	—
GVDD	DDR supply	AC2	—	GV_{DD}	—
GVDD	DDR supply	AC8	—	GV_{DD}	—
GVDD	DDR supply	AD6	—	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
GVDD	DDR supply	AE10	—	GV_{DD}	—
GVDD	DDR supply	AE4	—	GV_{DD}	—
GVDD	DDR supply	AF2	—	GV_{DD}	—
GVDD	DDR supply	AF8	—	GV_{DD}	—
GVDD	DDR supply	AG6	—	GV_{DD}	—
GVDD	DDR supply	AH10	—	GV_{DD}	—
GVDD	DDR supply	AH4	—	GV_{DD}	—
GVDD	DDR supply	AJ2	—	GV_{DD}	—
GVDD	DDR supply	AJ8	—	GV_{DD}	—
GVDD	DDR supply	AK10	—	GV_{DD}	—
GVDD	DDR supply	AK6	—	GV_{DD}	—
GVDD	DDR supply	AL4	—	GV_{DD}	—
GVDD	DDR supply	AL10	—	GV_{DD}	—
GVDD	DDR supply	AM2	—	GV_{DD}	—
GVDD	DDR supply	AM8	—	GV_{DD}	—
GVDD	DDR supply	AN12	—	GV_{DD}	—
GVDD	DDR supply	AN6	—	GV_{DD}	—
GVDD	DDR supply	AP10	—	GV_{DD}	—
GVDD	DDR supply	AP4	—	GV_{DD}	—
GVDD	DDR supply	AR2	—	GV_{DD}	—
GVDD	DDR supply	AR8	—	GV_{DD}	—
GVDD	DDR supply	AR14	—	GV_{DD}	—
BVDD	Local bus supply	B24	—	BV_{DD}	—
BVDD	Local bus supply	E24	—	BV_{DD}	—
BVDD	Local bus supply	E22	—	BV_{DD}	—
BVDD	Local bus supply	F20	—	BV_{DD}	—
BVDD	Local bus supply	F26	—	BV_{DD}	—
BVDD	Local bus supply	H20	—	BV_{DD}	—
BVDD	Local bus supply	H18	—	BV_{DD}	—
BVDD	Local bus supply	K22	—	BV_{DD}	—
BVDD	Local bus supply	K24	—	BV_{DD}	—
SVDD	SerDes core logic supply	A30	—	SV_{DD}	—
SVDD	SerDes core logic supply	A34	—	SV_{DD}	—
SVDD	SerDes core logic supply	B28	—	SV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
SVDD	SerDes core logic supply	B32	—	SV_{DD}	—
SVDD	SerDes core logic supply	B36	—	SV_{DD}	—
SVDD	SerDes core logic supply	C31	—	SV_{DD}	—
SVDD	SerDes core logic supply	C34	—	SV_{DD}	—
SVDD	SerDes core logic supply	C35	—	SV_{DD}	—
SVDD	SerDes core logic supply	D29	—	SV_{DD}	—
SVDD	SerDes core logic supply	E36	—	SV_{DD}	—
SVDD	SerDes core logic supply	F34	—	SV_{DD}	—
SVDD	SerDes core logic supply	G35	—	SV_{DD}	—
SVDD	SerDes core logic supply	J36	—	SV_{DD}	—
SVDD	SerDes core logic supply	K34	—	SV_{DD}	—
SVDD	SerDes core logic supply	L35	—	SV_{DD}	—
SVDD	SerDes core logic supply	M33	—	SV_{DD}	—
SVDD	SerDes core logic supply	N36	—	SV_{DD}	—
SVDD	SerDes core logic supply	R34	—	SV_{DD}	—
SVDD	SerDes core logic supply	R35	—	SV_{DD}	—
SVDD	SerDes core logic supply	U33	—	SV_{DD}	—
SVDD	SerDes core logic supply	V35	—	SV_{DD}	—
SVDD	SerDes core logic supply	W34	—	SV_{DD}	—
SVDD	SerDes core logic supply	Y36	—	SV_{DD}	—
SVDD	SerDes core logic supply	AA33	—	SV_{DD}	—
SVDD	SerDes core logic supply	AB35	—	SV_{DD}	—
SVDD	SerDes core logic supply	AD36	—	SV_{DD}	—
SVDD	SerDes core logic supply	AE33	—	SV_{DD}	—
SVDD	SerDes core logic supply	AF35	—	SV_{DD}	—
SVDD	SerDes core logic supply	AG34	—	SV_{DD}	—
SVDD	SerDes core logic supply	AH36	—	SV_{DD}	—
XVDD	SerDes transceiver supply	E32	—	XV_{DD}	—
XVDD	SerDes transceiver supply	E33	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F28	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	G32	—	XV_{DD}	—
XVDD	SerDes transceiver supply	H31	—	XV_{DD}	—
XVDD	SerDes transceiver supply	H33	—	XV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
XVDD	SerDes transceiver supply	J28	—	XV_{DD}	—
XVDD	SerDes transceiver supply	J30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	J32	—	XV_{DD}	—
XVDD	SerDes transceiver supply	K30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	L30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	L31	—	XV_{DD}	—
XVDD	SerDes transceiver supply	M29	—	XV_{DD}	—
XVDD	SerDes transceiver supply	N31	—	XV_{DD}	—
XVDD	SerDes transceiver supply	P30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	P33	—	XV_{DD}	—
XVDD	SerDes transceiver supply	R29	—	XV_{DD}	—
XVDD	SerDes transceiver supply	R31	—	XV_{DD}	—
XVDD	SerDes transceiver supply	T29	—	XV_{DD}	—
XVDD	SerDes transceiver supply	T32	—	XV_{DD}	—
XVDD	SerDes transceiver supply	U30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	V30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	V32	—	XV_{DD}	—
XVDD	SerDes transceiver supply	W29	—	XV_{DD}	—
XVDD	SerDes transceiver supply	Y31	—	XV_{DD}	—
XVDD	SerDes transceiver supply	AA29	—	XV_{DD}	—
XVDD	SerDes transceiver supply	AB30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	AB31	—	XV_{DD}	—
XVDD	SerDes transceiver supply	AC33	—	XV_{DD}	—
XVDD	SerDes transceiver supply	AD32	—	XV_{DD}	—
XVDD	SerDes transceiver supply	AE30	—	XV_{DD}	—
XVDD	SerDes transceiver supply	AF31	—	XV_{DD}	—
XVDD	SerDes transceiver supply	AH32	—	XV_{DD}	—
LVDD	Ethernet controller 1 and 2 supply	AK33	—	LV_{DD}	—
LVDD	Ethernet controller 1 and 2 supply	AP31	—	LV_{DD}	—
LVDD	Ethernet controller 1 and 2 supply	AL31	—	LV_{DD}	—
LVDD	Ethernet controller 1 and 2 supply	AN33	—	LV_{DD}	—
LVDD	Ethernet controller 1 and 2 supply	AJ35	—	LV_{DD}	—
LVDD	Ethernet controller 1 and 2 supply	AR35	—	LV_{DD}	—
LVDD	Ethernet controller 1 and 2 supply	AM35	—	LV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
POVDD	Fuse programming override supply	AT17	—	POV_{DD}	33
VDD_CA_PL	Core Group A and Platform supply	L11	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	L13	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	L15	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	L17	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	L19	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	L21	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	L23	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	L25	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	M12	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	M14	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	M16	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	M18	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	M20	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	M22	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	M24	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	M26	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N11	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N13	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N15	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N17	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N19	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N21	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N23	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N25	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	N27	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	P12	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	P14	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	P16	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	P18	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	P20	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	P22	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	P24	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	P26	—	VDD_CA_PL	42

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
VDD_CA_PL	Core Group A and Platform supply	R11	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	R13	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	R15	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	R17	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	R19	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	R21	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	R23	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	R25	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	R27	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	T12	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	T14	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	T16	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	T18	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	T20	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	T22	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	T24	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	T26	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U11	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U13	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U15	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U17	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U19	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U21	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U23	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U25	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	U27	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	V12	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	V14	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	V16	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	V18	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	V20	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	V22	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	V24	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	V26	—	VDD_CA_PL	42

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
VDD_CA_PL	Core Group A and Platform supply	W11	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	W13	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	W21	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	W23	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	W25	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	W28	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	Y12	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	Y14	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	Y22	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	Y24	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	Y26	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AA11	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AA13	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AA23	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AA25	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AA27	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AB12	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AB22	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AB24	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AB26	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AC11	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AC13	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AC21	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AC23	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AC25	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AC27	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AD12	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AD14	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AD16	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AD18	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AD20	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AD22	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AD24	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AD26	—	VDD_CA_PL	42

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
VDD_CA_PL	Core Group A and Platform supply	AE11	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AE13	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AE15	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AE17	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AE19	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AE21	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AE23	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AE25	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AF14	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AF16	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AF18	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AF20	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AF22	—	VDD_CA_PL	42
VDD_CA_PL	Core Group A and Platform supply	AF24	—	VDD_CA_PL	42
VDD_CB	Core Group B supply	W15	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	W17	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	W19	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	Y16	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	Y18	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	Y20	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AA15	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AA17	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AA19	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AA21	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AB14	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AB16	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AB18	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AB20	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AC15	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AC17	—	V_{DD_CB}	42
VDD_CB	Core Group B supply	AC19	—	V_{DD_CB}	42
VDD_LP	Low power security monitor supply	AD28	—	V_{DD_LP}	27
AVDD_CC1	Core cluster PLL1 supply	A20	—	—	13
AVDD_CC2	Core cluster PLL2 supply	AT18	—	—	13

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
AVDD_PLAT	Platform PLL supply	AT20	—	—	13
AVDD_DDR	DDR PLL Supply	A19	—	—	13
AVDD_SRDS1	SerDes PLL1 supply	A33	—	—	13
AVDD_SRDS2	SerDes PLL2 supply	U36	—	—	13
AVDD_SRDS3	SerDes PLL3 supply	AE35	—	—	13
SENSEVDD_CA_PL	Core group A Vdd sense	K16	—	—	8
SENSEVDD_CB	Core group B Vdd sense	AG15	—	—	8
USB1_AGND	USB1 PHY Transceiver GND	AH24	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AJ24	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AL25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AM25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR26	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR27	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR28	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AT25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AT28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AH27	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AL28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AM28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN25	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN26	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN27	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AP25	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AP28	—	—	—
USB1_VDD_3P3	USB1 PHY Transceiver 3.3V Supply	AL24	—	—	—
USB1_VDD_3P3	USB1 PHY Transceiver 3.3V Supply	AJ25	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3V Supply	AJ26	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3V Supply	AJ27	—	—	—
USB1_VDD_1P0	USB1 PHY PLL 1.0V Supply	AH25	—	—	—
USB2_VDD_1P0	USB2 PHY PLL 1.0V Supply	AH26	—	—	—
Analog Signals					
MVREF	SSTL_1.5/1.35 Reference Voltage	B19	I	$GV_{DD}/2$	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	AF30	I	200Ω (±1%) to XV_{DD}	23
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	B27	I	200Ω (±1%) to SV_{DD}	24
TEMP_ANODE	Temperature Diode Anode	C21	—	internal diode	9
TEMP_CATHODE	Temperature Diode Cathode	B21	—	internal diode	9
USB1_IBIAS_REXT	USB PHY1 Reference Bias Current Generation	AM26	—	—	36
USB2_IBIAS_REXT	USB PHY2 Reference Bias Current Generation	AM27	—	—	36
USB1_VDD_1P8_DECAP	USB1 PHY 1.8V Output to External Decap	AL26	—	—	37
USB2_VDD_1P8_DECAP	USB2 PHY 1.8V Output to External Decap	AL27	—	—	37
No Connection Pins					
NC_A27	No Connection	A27	—	—	11
NC_B26	No Connection	B26	—	—	11
NC_C19	No Connection	C19	—	—	11
NC_C20	No Connection	C20	—	—	11
NC_C26	No Connection	C26	—	—	11
NC_C27	No Connection	C27	—	—	11
NC_D18	No Connection	D18	—	—	11
NC_D27	No Connection	D27	—	—	11
NC_E16	No Connection	E16	—	—	11
NC_E27	No Connection	E27	—	—	11
NC_G27	No Connection	G27	—	—	11
NC_H12	No Connection	H12	—	—	11
NC_H13	No Connection	H13	—	—	11
NC_H15	No Connection	H15	—	—	11
NC_H27	No Connection	H27	—	—	11
NC_J11	No Connection	J11	—	—	11
NC_J13	No Connection	J13	—	—	11
NC_J14	No Connection	J14	—	—	11
NC_K11	No Connection	K11	—	—	11
NC_K12	No Connection	K12	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
NC_K13	No Connection	K13	—	—	11
NC_K14	No Connection	K14	—	—	11
NC_R28	No Connection	R28	—	—	11
NC_T28	No Connection	T28	—	—	11
NC_U28	No Connection	U28	—	—	11
NC_V28	No Connection	V28	—	—	11
NC_W27_DET	No Connection	W27	—	—	11
NC_Y28	No Connection	Y28	—	—	11
NC_AA28	No Connection	AA28	—	—	11
NC_AB28	No Connection	AB28	—	—	11
NC_AB29	No Connection	AB29	—	—	11
NC_AC28	No Connection	AC28	—	—	11
NC_AC29	No Connection	AC29	—	—	11
NC_AD29	No Connection	AD29	—	—	11
NC_AE29	No Connection	AE29	—	—	11
NC_AF26	No Connection	AF26	—	—	11
NC_AF27	No Connection	AF27	—	—	11
NC_AF28	No Connection	AF28	—	—	11
NC_AF29	No Connection	AF29	—	—	11
NC_AG26	No Connection	AG26	—	—	11
NC_AG27	No Connection	AG27	—	—	11
NC_AG28	No Connection	AG28	—	—	11
NC_AG29	No Connection	AG29	—	—	11
NC_AH30	No Connection	AH30	—	—	11
NC_AM12	No Connection	AM12	—	—	11
NC_AN13	No Connection	AN13	—	—	11
NC_AP11	No Connection	AP11	—	—	11
NC_AP14	No Connection	AP14	—	—	11
NC_AT14	No Connection	AT14	—	—	11
Reserved Pins					
Reserve_C32	—	C32	—	—	11
Reserve_D32	—	D32	—	—	11
Reserve_U32	—	U32	—	—	11
Reserve_U35	—	U35	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
Reserve_AD33	—	AD33	—	—	11
Reserve_AD34	—	AD34	—	—	11
Reserve_AG11	—	AG11	—	GND	21
Reserve_AG12	—	AG12	—	GND	21
Reserve_AH11	—	AH11	—	GND	21
Reserve_AH12	—	AH12	—	GND	21
Reserve_A2	—	A2	—	—	11
Reserve_A3	—	A3	—	—	11
Reserve_A4	—	A4	—	—	11
Reserve_A5	—	A5	—	—	11
Reserve_A6	—	A6	—	—	11
Reserve_A7	—	A7	—	—	11
Reserve_A8	—	A8	—	—	11
Reserve_A9	—	A9	—	—	11
Reserve_A10	—	A10	—	—	11
Reserve_A11	—	A11	—	—	11
Reserve_A12	—	A12	—	—	11
Reserve_A13	—	A13	—	—	11
Reserve_A21	—	A21	—	—	11
Reserve_A25	—	A25	—	—	11
Reserve_B1	—	B1	—	—	11
Reserve_B3	—	B3	—	—	11
Reserve_B4	—	B4	—	—	11
Reserve_B6	—	B6	—	—	11
Reserve_B7	—	B7	—	—	11
Reserve_B9	—	B9	—	—	11
Reserve_B10	—	B10	—	—	11
Reserve_B12	—	B12	—	—	11
Reserve_B13	—	B13	—	—	11
Reserve_C1	—	C1	—	—	11
Reserve_C2	—	C2	—	—	11
Reserve_C4	—	C4	—	—	11
Reserve_C5	—	C5	—	—	11
Reserve_C7	—	C7	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
Reserve_C13	—	C13	—	—	11
Reserve_D1	—	D1	—	—	11
Reserve_D2	—	D2	—	—	11
Reserve_D3	—	D3	—	—	11
Reserve_D5	—	D5	—	—	11
Reserve_D6	—	D6	—	—	11
Reserve_E1	—	E1	—	—	11
Reserve_E3	—	E3	—	—	11
Reserve_E4	—	E4	—	—	11
Reserve_F1	—	F1	—	—	11
Reserve_F2	—	F2	—	—	11
Reserve_F4	—	F4	—	—	11
Reserve_F5	—	F5	—	—	11
Reserve_G1	—	G1	—	—	11
Reserve_G2	—	G2	—	—	11
Reserve_G3	—	G3	—	—	11
Reserve_G5	—	G5	—	—	11
Reserve_G6	—	G6	—	—	11
Reserve_H1	—	H1	—	—	11
Reserve_H3	—	H3	—	—	11
Reserve_H4	—	H4	—	—	11
Reserve_H6	—	H6	—	—	11
Reserve_J1	—	J1	—	—	11
Reserve_J2	—	J2	—	—	11
Reserve_J4	—	J4	—	—	11
Reserve_K1	—	K1	—	—	11
Reserve_K2	—	K2	—	—	11
Reserve_K3	—	K3	—	—	11
Reserve_K27	—	K27	—	—	11
Reserve_L1	—	L1	—	—	11
Reserve_L3	—	L3	—	—	11
Reserve_L4	—	L4	—	—	11
Reserve_L27	—	L27	—	—	11
Reserve_L28	—	L28	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
Reserve_M1	—	M1	—	—	11
Reserve_M2	—	M2	—	—	11
Reserve_M4	—	M4	—	—	11
Reserve_M5	—	M5	—	—	11
Reserve_M28	—	M28	—	—	11
Reserve_N1	—	N1	—	—	11
Reserve_N2	—	N2	—	—	11
Reserve_N3	—	N3	—	—	11
Reserve_N5	—	N5	—	—	11
Reserve_N28	—	N28	—	—	11
Reserve_P1	—	P1	—	—	11
Reserve_P3	—	P3	—	—	11
Reserve_P4	—	P4	—	—	11
Reserve_P28	—	P28	—	—	11
Reserve_R1	—	R1	—	—	11
Reserve_R2	—	R2	—	—	11
Reserve_R4	—	R4	—	—	11
Reserve_R5	—	R5	—	—	11
Reserve_T1	—	T1	—	—	11
Reserve_T2	—	T2	—	—	11
Reserve_T3	—	T3	—	—	11
Reserve_T5	—	T5	—	—	11
Reserve_U1	—	U1	—	—	11
Reserve_U4	—	U4	—	—	11
Reserve_V1	—	V1	—	—	11
Reserve_V2	—	V2	—	—	11
Reserve_V3	—	V3	—	—	11
Reserve_V4	—	V4	—	—	11
Reserve_W1	—	W1	—	—	11
Reserve_W2	—	W2	—	—	11
Reserve_W3	—	W3	—	—	11
Reserve_W4	—	W4	—	—	11
Reserve_Y1	—	Y1	—	—	11
Reserve_Y4	—	Y4	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
Reserve_Y6	—	Y6	—	—	11
Reserve_AA1	—	AA1	—	—	11
Reserve_AA2	—	AA2	—	—	11
Reserve_AA3	—	AA3	—	—	11
Reserve_AA4	—	AA4	—	—	11
Reserve_AB1	—	AB1	—	—	11
Reserve_AB2	—	AB2	—	—	11
Reserve_AB3	—	AB3	—	—	11
Reserve_AC1	—	AC1	—	—	11
Reserve_AC3	—	AC3	—	—	11
Reserve_AC4	—	AC4	—	—	11
Reserve_AD1	—	AD1	—	—	11
Reserve_AD2	—	AD2	—	—	11
Reserve_AE1	—	AE1	—	—	11
Reserve_AE2	—	AE2	—	—	11
Reserve_AE3	—	AE3	—	—	11
Reserve_AF1	—	AF1	—	—	11
Reserve_AF3	—	AF3	—	—	11
Reserve_AF4	—	AF4	—	—	11
Reserve_AF11	—	AF11	—	—	11
Reserve_AF12	—	AF12	—	—	11
Reserve_AG1	—	AG1	—	—	11
Reserve_AG2	—	AG2	—	—	11
Reserve_AG4	—	AG4	—	—	11
Reserve_AG25	—	AG25	—	—	11
Reserve_AH1	—	AH1	—	—	11
Reserve_AH2	—	AH2	—	—	11
Reserve_AH3	—	AH3	—	—	11
Reserve_AH29	—	AH29	—	—	11
Reserve_AJ1	—	AJ1	—	—	11
Reserve_AJ3	—	AJ3	—	—	11
Reserve_AJ4	—	AJ4	—	—	11
Reserve_AK1	—	AK1	—	—	11
Reserve_AK2	—	AK2	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
Reserve_AK4	—	AK4	—	—	11
Reserve_AK5	—	AK5	—	—	11
Reserve_AL1	—	AL1	—	—	11
Reserve_AL2	—	AL2	—	—	11
Reserve_AL3	—	AL3	—	—	11
Reserve_AL5	—	AL5	—	—	11
Reserve_AL6	—	AL6	—	—	11
Reserve_AM1	—	AM1	—	—	11
Reserve_AM3	—	AM3	—	—	11
Reserve_AM4	—	AM4	—	—	11
Reserve_AM6	—	AM6	—	—	11
Reserve_AM7	—	AM7	—	—	11
Reserve_AN1	—	AN1	—	—	11
Reserve_AN2	—	AN2	—	—	11
Reserve_AN4	—	AN4	—	—	11
Reserve_AN5	—	AN5	—	—	11
Reserve_AP1	—	AP1	—	—	11
Reserve_AP2	—	AP2	—	—	11
Reserve_AP3	—	AP3	—	—	11
Reserve_AP5	—	AP5	—	—	11
Reserve_AP6	—	AP6	—	—	11
Reserve_AP8	—	AP8	—	—	11
Reserve_AR1	—	AR1	—	—	11
Reserve_AR3	—	AR3	—	—	11
Reserve_AR4	—	AR4	—	—	11
Reserve_AR6	—	AR6	—	—	11
Reserve_AR7	—	AR7	—	—	11
Reserve_AT1	—	AT1	—	—	11
Reserve_AT2	—	AT2	—	—	11
Reserve_AT3	—	AT3	—	—	11
Reserve_AT4	—	AT4	—	—	11
Reserve_AT5	—	AT5	—	—	11
Reserve_AT6	—	AT6	—	—	11
Reserve_AT7	—	AT7	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes
Reserve_AT8	—	AT8	—	—	11
Reserve_AT19	—	AT19	—	—	11

Notes:

1. Recommend that a weak pull-up resistor (2–10 KΩ) be placed on this pin to OVDD.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ resistor. However, if the signal is intended to be high after reset and if there is any device on the net that may pull down the value of the net at reset, a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to BV_{DD} to ensure no random chip select assertion due to possible noise, etc.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the correspondent power and ground nets internally and may be connected as a differential pair to be used by the voltage regulators with remote sense function. For Rev1.1, the better solution is to use the far sense pins relative to the power supply location, the other pair can be left as no connected. The DC power simulation should be done during the board layout process to approve the selected solution.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A. If a thermal diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
11. Do not connect.
12. These are test signals for factory use only and must be pulled down (1 kΩ–2 kΩ) to GND for normal machine operation.
13. Independent supplies derived from board $V_{DD\_CA\_CB\_PL}$ (core clusters, platform, DDR) or SV_{DD} (SerDes).
14. Recommend that a pull-up resistor (1 kΩ) be placed on this pin to OV_{DD} if I^2C interface is used.
15. This pin requires an external 1 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, D*n*_MDIC[0] is grounded through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and D*n*_MDIC[1] is connected to GV_{DD} through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
18. These pins must be pulled up to 1.2V through a 180 Ω ± 1% resistor for EM2_MDC and a 330 Ω ± 1% resistor for EM2_MDIO.
20. Pin has a weak internal pull-up.
21. These pins must be pulled to ground (GND).
22. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
23. This pin requires a 200-Ω pull-up to XV_{DD}.
24. This pin requires a 200-Ω pull-up to SV_{DD}.
25. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
26. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW (Reset Configuration Word).
27. See Section 3.6, "Connection Recommendations," for additional details on this signal.

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Notes

28. For reduced core (core 2 and 3 disabled) mode, this signal must be pulled high (100 Ω–1 kΩ) to OVDD.
30. Warning, incorrect voltage select settings can lead to irreversible device damage. This pin has an internal 2 kΩ pull-down resistor, to pull it high, a pull-up resistor of less than 1 kΩ to OVDD should be used. See Section 3.2, "Supply Power Default Setting."
31. SDHC_DAT[4:7] require CV_{DD} = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.
32. The *cfg_xvdd_sel* (LAD[26]) reset configuration pin must select the correct voltage that is being supplied on the XV_{DD} pin. Incorrect voltage select settings can lead to irreversible damage to the device.
33. See Section 2.2, "Power-Up Sequencing and Section 5, "Security Fuse Processor," for additional details on this signal.
35. Pin must NOT be pulled down during power-on reset.
36. This pin must be connected to GND through a 10 kΩ ± 0.1% resistor with a low temperature coefficient of ≤ 25 ppm/°C for bias generation.
37. A 1μF to 1.5 μF capacitor connected to GND is required on this signal. A list of recommended capacitors are shown in Section 3.6.4.2, "USBn_V_{DD}_1P8_DECAP Capacitor Options."
38. A divider network is required on this signal. See Section 3.6.4, "USB Controller Connections."
39. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OVDD for normal machine operation.
40. For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.
41. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section describes the ratings, conditions, and other electrical characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Operating Conditions[1]

Parameter	Symbol	Max Value	Unit	Notes
Cores Group A (core 0–1) and Platform supply voltage (Silicon Rev 1.0)	$V_{DD\_CA\_PL}$	–0.3 to 1.1	V	9, 10
Cores Group B (core 2–3) supply voltage (Silicon Rev 1.0)	V_{DD_CB}	–0.3 to 1.1	V	9, 10
Cores Group A (core 0–1), Core Group B (core 2–3) and Platform supply voltage (Silicon Rev 1.1)	$V_{DD\_CA\_CB\_PL}$	–0.3 to 1.1	V	9, 10
PLL supply voltage (core, platform, DDR)	AV_{DD}	–0.3 to 1.1	V	—
PLL supply voltage (SerDes, filtered from SV_{DD})	AV_{DD_SRDS}	–0.3 to 1.1	V	—
Fuse programming override supply	POV_{DD}	–0.3 to 1.65	V	1

Table 2. Absolute Operating Conditions[1] (continued)

Parameter		Symbol	Max Value	Unit	Notes
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
eSPI, eSHDC		CV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
DDR3 and DDR3L DRAM I/O voltage		GV_{DD}	–0.3 to 1.65	V	—
Enhanced Local Bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Core power supply for SerDes transceivers		SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers		XV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	—
Ethernet I/O, Ethernet Management Interface 1 (EMI1), 1588, GPIO		LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3
Ethernet Management Interface 2 (EMI2)		LV_{DD}	–0.3 to 1.32	V	8
USB PHY Transceiver supply voltage		$USB\_V_{DD}\_3P3$	–0.3 to 3.63	V	—
USB PHY PLL supply voltage		$USB\_V_{DD}\_1P0$	–0.3 to 1.1	V	—
Low Power Security Monitor Supply		V_{DD_LP}	–0.3 to 1.1	V	—
Input voltage[7]	DDR3 and DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 7
	DDR3 and DDR3L DRAM reference	$MV_{REF}n$	–0.3 to (GV_{DD}/2+ 0.3)	V	2, 7
	Ethernet signals (except EMI2)	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 7
	eSPI, eSHDC	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 7
	Enhanced Local Bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	5, 7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6, 7
	SerDes signals	XV_{IN}	–0.4 to (XV_{DD} + 0.3)	V	7
	USB PHY Transceiver signals	$USB\_V_{IN}\_3P3$	–0.3 to ($USB\_V_{DD}\_3P3$ + 0.3)	V	7
	Ethernet Management Interface 2 (EMI2) signals	—	–0.3 to (1.2 + 0.3)	V	7

Table 2. Absolute Operating Conditions[1] (continued)

Parameter	Symbol	Max Value	Unit	Notes
Storage junction temperature range	T_{stg}	–55 to 150	°C	—

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. (C,X,B,G,L,O)V_{IN} may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 7.
8. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
9. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
10. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Parameter	Symbol	Recommended Value	Unit	Notes
Cores Group A (core 0–1) and Platform supply voltage (Silicon Rev 1.0)	$V_{DD\_CA\_PL}$	1.0 ± 40 mV (CPU speed > 1333 MHz) 1.0 ± 50 mV (CPU speed ≤ 1333 MHz)	V	5, 6
Cores Group B (core 2–3) supply voltage (Silicon Rev 1.0)	V_{DD_CB}	1.0 ± 40 mV (CPU speed > 1333 MHz) 1.0 ± 50 mV (CPU speed ≤ 1333 MHz)	V	5, 6
Cores Group A (core 0–1), Core Group B (core 2–3) and Platform supply voltage (Silicon Rev 1.1)	$V_{DD\_CA\_CB\_PL}$	1.0 ± 40 mV (CPU speed > 1333 MHz) 1.0 ± 50 mV (CPU speed ≤ 1333 MHz)	V	5, 6
PLL supply voltage (core, platform, DDR)	AV_{DD}	1.0 ± 40 mV (CPU speed > 1333 MHz) 1.0 ± 50 mV (CPU speed ≤ 1333 MHz)	V	—
PLL supply voltage (SerDes)	AV_{DD_SRDS}	1.0 ± 50 mV	V	—
Fuse programming override supply	POV_{DD}	1.5 ± 75 mV	V	1

Table 3. Recommended Operating Conditions (continued)

Parameter		Symbol	Recommended Value	Unit	Notes
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage		OV_{DD}	3.3 ± 165 mV	V	—
eSPI, eSDHC		CV_{DD}	3.3 ± 165 mV 2.5 ± 125 mV 1.8 ± 90 mV	V	—
DDR DRAM I/O voltage	DDR3 DDR3L	GV_{DD}	 1.5 ± 75 mV 1.35 ± 67 mV	V	—
Enhanced Local Bus I/O voltage		BV_{DD}	3.3 ± 165 mV 2.5 ± 125 mV 1.8 ± 90 mV	V	—
Core power supply for SerDes transceivers		SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers		XV_{DD}	1.8 ± 90 mV 1.5 ± 75 mV	V	—
Ethernet I/O, Ethernet Management Interface 1 (EMI1),1588, GPIO		LV_{DD}	3.3 ± 165 mV 2.5 ± 125 mV	V	2
USB PHY transceiver supply voltage		$USB\_V_{DD}\_3P3$	3.3 ± 165 mV	V	—
USB PHY PLL supply voltage		$USB\_V_{DD}\_1P0$	1.0 ± 50 mV	V	—
Low Power Security Monitor Supply		V_{DD_LP}	1.0 ± 50 mV	V	—
Input voltage	DDR3 and DDR3L DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR3 and DDR3L DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	—
	Ethernet signals (except EMI2)	LV_{IN}	GND to LV_{DD}	V	—
	eSPI, eSHDC	CV_{IN}	GND to CV_{DD}	V	—
	Enhanced Local Bus signals	BV_{IN}	GND to BV_{DD}	V	—
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	GND to OV_{DD}	V	—
	SerDes signals	XV_{IN}	GND to XV_{DD}	V	—
	USB PHY transceiver signals	$USB\_V_{IN}\_3P3$	GND to $USB\_V_{DD}\_3P3$	V	—
	Ethernet Management Interface 2 (EMI2) signals	—	GND to 1.2 V	V	4

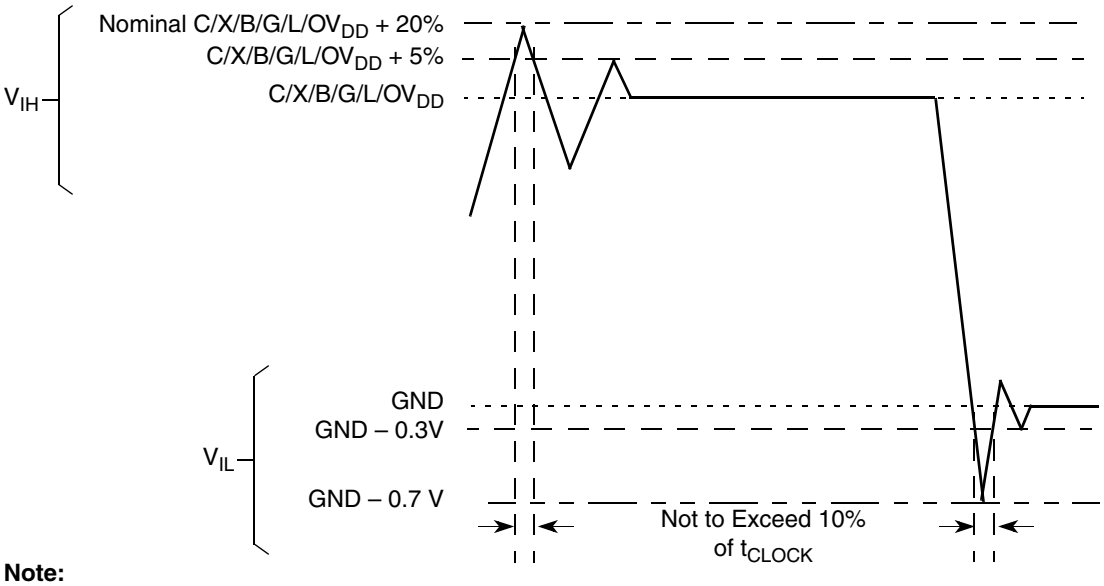
Table 3. Recommended Operating Conditions (continued)

Parameter		Symbol	Recommended Value	Unit	Notes
Operating Temperature range	Normal Operation	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—
	Extended Operation	T_A, T_J	T_A = –40 (min) to T_J = 105 (max)	°C	—
	Secure Boot Fuse Programming	T_A, T_J	T_A = 0(min) to T_J = 70 (max)	°C	1

Note:

1. POV_{DD} must be supplied 1.5 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power-Up Sequencing."
2. Selecting RGMII limits LV_{DD} to 2.5 V.
3. Unless otherwise stated in an interface's DC specifications, the maximum allowed input capacitance in this table is a general recommendation for signals.
4. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
5. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
6. Core Group A and Platform supply ($V_{DD\_CA\_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:

t_{CLOCK} refers to the clock period associated with the respective interface:
For I2C, t_{CLOCK} refers to SYSCLK.
For DDR GV_{DD}, t_{CLOCK} refers to D*n*_MCK.
For eSPI CV_{DD}, t_{CLOCK} refers to SPI_CLK.
For eLBC BV_{DD}, t_{CLOCK} refers to LCLK.
For SerDes XV_{DD}, t_{CLOCK} refers to SD_REF_CLK.
For dTSEC LV_{DD}, t_{CLOCK} refers to EC_GTX_CLK125.
For JTAG OV_{DD}, t_{CLOCK} refers to TCK.

Figure 7. Overshoot/Undershoot Voltage for BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}

The core and platform voltages must always be provided at nominal 1.0 V. See Table 3 for the actual recommended core voltage conditions. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. CV_{DD}, BV_{DD}, OV_{DD}, and LV_{DD}-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied $MV_{REF}n$ signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.5/SSTL_1.35 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

This table provides information about the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	(Nominal) Supply Voltage	Notes
Local Bus interface utilities signals	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR3 signal	20 (full-strength mode) 40 (half-strength mode)	GV_{DD} = 1.5 V	1
DDR3L signal	20 (full-strength mode) 40 (half-strength mode)	GV_{DD} = 1.35 V	1
eTSEC/10/100 signals	45 45	LV_{DD} = 3.3 V LV_{DD} = 2.5 V	—
DUART, system control, JTAG	45	OV_{DD} = 3.3 V	—
I^2C	45	OV_{DD} = 3.3 V	—
eSPI	45 45 45	CV_{DD} = 3.3 V CV_{DD} = 2.5 V CV_{DD} = 1.8 V	—

Note:

1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at T_j = 105 °C and at GV_{DD} (min).

2.2 Power-Up Sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

1. Bring up OV_{DD}, LV_{DD}, BV_{DD}, CV_{DD}, and USB_VDD_3P3. Drive POV_{DD} = GND.
   - — $\overline{\text{PORESET}}$ input must be driven asserted and held during this step.
   - — IO_VSEL inputs must be driven during this step and held stable during normal operation.
   - — USB_V_{DD}_3P3 rise time (10% to 90%) has a minimum of 350 µs.
2. Bring up $V_{DD\_CA\_CB\_PL}$, SV_{DD}, AV_{DD} (cores, platform, DDR, SerDes), and USB_V_{DD}_1P0. $V_{DD\_CA\_CB\_PL}$ and USB_VDD_1P0 must be ramped up simultaneously.
3. Bring up GV_{DD} (DDR), XV_{DD}.
4. Negate $\overline{\text{PORESET}}$ input as long as the required assertion/hold time has been met per Table 17.
5. For secure boot fuse programming, use the following steps:
   a) After negation of $\overline{\text{PORESET}}$, drive POV_{DD} = 1.5 V after a required minimum delay per Table 5.

b) After fuse programming is completed, it is required to return POV_{DD} = GND before the system is power cycled ($\overline{PORESET}$ assertion) or powered down ($V_{DD\_CA\_CB\_PL}$ ramp down) per the required timing specified in Table 5. See Section 5, "Security Fuse Processor," for additional details.

WARNING

Only two secure boot fuse programming events are permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND.

While VDD is ramping, current may be supplied from VDD through the P3041 to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

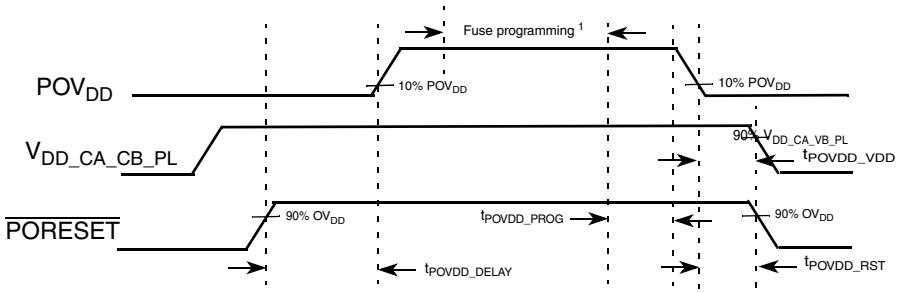
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} Timing [5]

Driver Type	Min	Max	Unit	Notes
t_{POVDD_DELAY}	100	—	SYSCLKs	1

Table 5. POV_{DD} Timing [5]

Driver Type	Min	Max	Unit	Notes
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the negation of $\overline{\text{PORESET}}$ to driving POV_{DD} ramp up. Delay measured from $\overline{\text{PORESET}}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to $V_{DD\_CA\_CB\_PL}$ ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before $V_{DD\_CA\_CB\_PL}$ is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to $\overline{\text{PORESET}}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{\text{PORESET}}$ assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

WARNING

Incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply Power Default Setting."

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the $V_{DD\_CA\_CB\_PL}$ supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power-Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Section 2.2, "Power-Up Sequencing," it is required that POV_{DD} = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down ($V_{DD\_CA\_CB\_PL}$ ramp down) per the required timing specified in Table 5.

$V_{DD\_CA\_CB\_PL}$ and USB_VDD_1P0 must be ramped down simultaneously. USB_V_{DD}_1P8_DECAP should start ramping down only after USB_V_{DD}_3P3 is below 1.65 V.

2.4 Power Characteristics

This table shows the power dissipations of the $V_{DD\_CA\_CB\_PL}$ and SV_{DD} supply for various operating platform clock frequencies versus the core and DDR clock frequencies. Note that these numbers are based on design estimates only and are preliminary. More accurate power numbers are available after the measurement on the silicon is complete.

Table 6. Power Dissipation

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	FM Freq (MHz)	$V_{DD\_CA\_CB\_PL}$ (V)	Junction Temp (°C)	Core and Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	Core and Platform Power[1] (W)	$V_{DD\_CA\_CB\_PL}$ Power (W)	SV_{DD} Power (W)	Notes
							Quad cores		Dual cores			
Typical	1500	750	1333	583	1.0	65	13.8	—	13.1	—	—	2, 3
Thermal						105	19.2	—	18.7	—	—	5,7
Maximum							19.9	18.1	19.0	17.1	2.0	4, 6, 7
Typical	1333	666	1333	541	1.0	65	12.2	—	11.7	—	—	2, 3
Thermal						105	16.9	—	16.4	—	—	5, 7
Maximum							17.5	15.7	16.7	14.8	2.0	4, 6, 7
Typical	1200	600	1200	500	1.0	65	10.9	—	10.4	—	—	2, 3
Thermal						105	14.8	—	14.4	—	—	5, 7
Maximum							15.4	13.5	14.6	12.8	2.0	4, 6, 7

Note:

1. Combined power of $V_{DD\_CA\_CB\_PL}$, SVDD with one DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% on all cores and executing DMA on the platform with 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform. with 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 7. P3041 I/O Power Supply Estimated Values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 Bits Per Controller	667 MT/s data rate	GVdd (1.5V)	0.705	1.764	W	1,2,5,6
	800 MT/s data rate		0.714	1.785		
	1066 MT/s data rate		0.731	1.827		
	1200 MT/s data rate		0.739	1.848		
	1333 MT/s data rate		0.747	1.869		

Table 7. P3041 I/O Power Supply Estimated Values (continued)

HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5V)	0.078	0.087	W	1, 7
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
	x1, 2.5/3.0/3.125/5.0 G-baud		0.088	0.099		
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC (per controller)	RGMII	LVdd (2.5V)	0.075	0.100	W	1,3,6
IEEE 1588	—	LVdd (2.5V)	0.004	0.005	W	1,3,6
eLBC	32-bit, 100Mhz	BVdd (1.8V)	0.048	0.120	W	1,3,6
		BVdd (2.5V)	0.072	0.193		
		BVdd (3.3V)	0.120	0.277		
	16-bit, 100Mhz	BVdd (1.8V)	0.021	0.030	W	1,3,6
		BVdd (2.5V)	0.036	0.046		
		BVdd (3.3V)	0.057	0.076		
eSDHC	—	Ovdd (3.3V)	0.014	0.150	W	1,3,6
eSPI	—	CVdd (1.8V)	0.004	0.005	W	1,3,6
		CVdd (2.5V)	0.006	0.008		
		CVdd (3.3V)	0.010	0.013		
USB	—	USB_Vdd_3P3	0.012	0.015	W	1,3,6
I2C	—	OVdd (3.3V)	0.002	0.003	W	1,3,6
DUART	—	OVdd (3.3V)	0.006	0.008	W	1,3,6
GPIO	x8	OVdd (1.8V)	0.005	0.006	W	1,3,4,6
		OVdd (2.5V)	0.007	0.009		
		OVdd (3.3V)	0.009	0.011		

Table 7. P3041 I/O Power Supply Estimated Values (continued)

Others (Reset, System Clock, JTAG & Misc.)	—	OVdd (3.3V)	0.003	0.015	W	1,3,4,6

Note:

1. The typical values are estimates and based on simulations at 65 °C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load
4. GPIO's are supported on 1.8V, 2.5V and 3.3V rails, as specified in the hardware specification.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105 °C. The values are not intended to be used as the maximum guranteed current.
7. The total power numbers of XVDD is dependent on customer application use case. This table lists all the SerDes configuration combination possible for the device. To get the XVDD power numbers, the user should add the combined lanes to match to the total SerDes lanes used, not simply multiply the power numbers by the number of lanes.

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the PLLs at allowable voltage levels.

Table 8. AV_{DD} Power Dissipation

AV_{DD}s	Typical	Maximum	Unit	Notes
AV_{DD_DDR}	5	15	mW	1
AV_{DD_CC1}				
AV_{DD_CC2}				
AV_{DD_PLAT}				
AV_{DD_SRDS1}	—	36	mW	2
AV_{DD_SRDS2}				
AV_{DD_SRDS3}				
USB_V_{DD}_1P0	—	10	mW	3

Note:

1. $V_{DD\_CA\_CB\_PL}$ = 1.0 V, T_A = 80°C, T_J = 105°C
2. SV_{DD} = 1.0 V, T_A = 80°C, T_J = 105°C
3. USB_V_{DD}_1P0 = 1.0V, T_A = 80°C, T_J = 105°C

This table shows the estimated power dissipation on the POV_{DD} supply for the P3041, at allowable voltage levels.

Table 9. POV_{DD} Power Dissipation

Supply	Maximum	Unit	Notes
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the P3041, at allowable voltage levels.

Table 10. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Notes
V_{DD_LP} (P3041 on, 105C)	1.5	mW	1
V_{DD_LP} (P3041 off, 70C)	195	uW	2
V_{DD_LP} (P3041 off, 40C)	132	uW	2

Note:

1. V_{DD_LP} = 1.0 V, T_J = 105°C.
2. When P3041 is off, V_{DD_LP} may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC which switches V_{DD_LP} to battery when SOC powered down. See P3041 Reference Manual Trust Architecture chapter for more information.

This table shows the thermal characteristics for the chip.

Table 11. Package Thermal Characteristics [6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	14	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	11	°C/W	1, 3
Junction to ambient (at 200 ft/min)	Single-layer board (1s)	$R_{\Theta JMA}$	9	°C/W	1, 2
Junction to ambient (at 200 ft/min)	Four-layer board (2s2p)	$R_{\Theta JMA}$	7	°C/W	1, 2
Junction to board	—	$R_{\Theta JB}$	3	°C/W	3
Junction to case top	—	$R_{\Theta JCtop}$	.53	°C/W	4
Junction to lid top	—	$R_{\Theta JClid}$	.16	°C/W	5

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51–3 and JESD51-6 with the board (JESD51–9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51–8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Junction-to-lid-top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.
6. Reference Section 3.8, “Thermal Management Information,” for additional details.

2.5 Input Clocks

This section describes the system clock timing specifications, spread spectrum sources, real-time clock timing, dTSEC Gigabit Ethernet reference clock timing, and other clock sources.

2.5.1 System Clock (SYSCLK) Timing Specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 12. SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	—	**15**	pf	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the system clock (SYSCLK) AC timing specifications.

Table 13. SYSCLK AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	67	—	133	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	±150	ps	—
SYSCLK jitter phase noise at – 56dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ± 0.3 ΔV_{AC} at center of peak-to-peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.5.2 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output

jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread spectrum sources if the recommendations listed in this table are observed.

Table 14. Spread Spectrum Clock Source Recommendations

For recommended operating conditions, see Table 3.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:
1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 13.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

2.5.3 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the e500mc; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 16× the period of the platform clock. That is, minimum clock high time is 8× (platform clock), and minimum clock low time is 8× (platform clock). There is no minimum RTC frequency; RTC may be grounded if not needed.

2.5.4 dTSEC Gigabit Ethernet Reference Clock Timing

This table provides the dTSEC gigabit reference clocks DC electrical characteristics.

Table 15. EC_GTX_CLK125 DC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 3.

This table provides the dTSEC gigabit reference clocks AC timing specifications.

Table 16. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	± 150	ps	2

Notes:
1. Rise and fall times for EC_GTX_CLK125 are measured from 20% to 80% (rise time) and 80% to 20% (fall time) of LV_{DD}.
2. EC_GTX_CLK125 is used to generate the GTX clock for the dTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the dTSEC GTX_CLK. See Section 2.11.2.2, "RGMII AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.5.5 Other Input Clocks

A description of the overall clocking of this device is available in the *P3041 QorIQ Integrated Multicore Communication Processor Family Reference Manual* in the form of a clock subsystem block diagram. For information on the input clock requirements of functional blocks of the device—such as SerDes, Ethernet Management, eSDHC, local bus—see the specific interface section.

2.6 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

Table 17. RESET Initialization AC Timing Specifications

Parameter	Min	Max	Unit[1]	Notes
Required assertion time of $\overline{\text{PORESET}}$	1	—	ms	3
Required input assertion time of $\overline{\text{HRESET}}$	32	—	SYSCLKs	1, 2

Table 17. RESET Initialization AC Timing Specifications (continued)

Parameter	Min	Max	Unit[1]	Notes
Input setup time for POR configurations with respect to the negation of $\overline{\text{PORESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configurations with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the chip.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1 “Power-On Reset Sequence,” of the *P3041 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up. See Section 2.2, “Power-Up Sequencing.”

This table provides the PLL lock times.

Table 18. PLL Lock Times

Parameter	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—

2.7 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 19. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.8 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.8.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 20. DDR3 SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.5 V)[1]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed the $MV_{REF}n$ DC level by more than ±1% of the DC value (that is, ±15 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to $MV_{REF}n$ with a min value of $MV_{REF}n$ – 0.04 and a max value of $MV_{REF}n$ + 0.04. V_{TT} should track variations in the DC level of $MV_{REF}n$.
4. The voltage regulator for $MV_{REF}n$ must meet the specifications stated in Table 23.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.35 V)[1]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$MV_{REF}n$	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	$MV_{REF}n$ + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF}n$ – 0.090	V	5

Table 21. DDR3L SDRAM Interface DC Electrical Characteristics (GV_{DD} = 1.35 V)[1] (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.3	mA	7, 8
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.3	—	mA	7, 8

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. $MV_{REF}n$ is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}n$ may not exceed the $MV_{REF}n$ DC level by more than ±1% of the DC value (that is, ±13.5mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF}n with a min value of MV_{REF}n – 0.04 and a max value of MV_{REF}n + 0.04. V_{TT} should track variations in the DC level of $MV_{REF}n$.
4. The voltage regulator for $MV_{REF}n$ must meet the specifications stated in Table 23.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. I_{OH} and I_{OL} are measured at GV_{DD} = 1.283 V.

This table provides the DDR controller interface capacitance for DDR3 and DDR3L.

Table 22. DDR3 and DDR3L SDRAM Capacitance

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:
1. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.150 V.
2. This parameter is sampled. GV_{DD} = 1.35 V – 0.067 V / + 0.100 V (for DDR3L), f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.167 V.

This table provides the current draw characteristics for MVREF*n*.

Table 23. Current Draw Characteristics for MVREF*n*

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3 SDRAM for MVREF*n*	MVREF*n*	—	500	μA	—
Current draw for DDR3L SDRAM for MVREF*n*	MVREF*n*	—	500	μA	—

2.8.2 DDR3 and DDR3L SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the required GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.8.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 24. DDR3 SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 1200 MT/s data rate	V_{ILAC}	—	MVREFn – 0.150	V	—
	≤ 1200 MT/s data rate			MVREFn – 0.175		
AC input high voltage	> 1200 MT/s data rate	V_{IHAC}	MVREFn + 0.150	—	V	—
	≤ 1200 MT/s data rate		MVREFn + 0.175			

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 25. DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 1200 MT/s data rate	V_{ILAC}	—	MVREF*n* – 0.135	V	—
	≤ 1200 MT/s data rate			MVREF*n* – 0.160		
AC input high voltage	> 1200 MT/s data rate	V_{IHAC}	MVREF*n* + 0.135	—	V	—
	≤ 1200 MT/s data rate		MVREF*n* + 0.160			

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 26. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}			ps	1
1333 MT/s data rate		–125	125		
1200 MT/s data rate		–142	142		
1066 MT/s data rate		–170	170		
800 MT/s data rate		–200	200		

Table 26. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}			ps	2
1333 MT/s data rate		–250	250		
1200 MT/s data rate		–275	275		
1066 MT/s data rate		–300	300		
800 MT/s data rate		–425	425		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

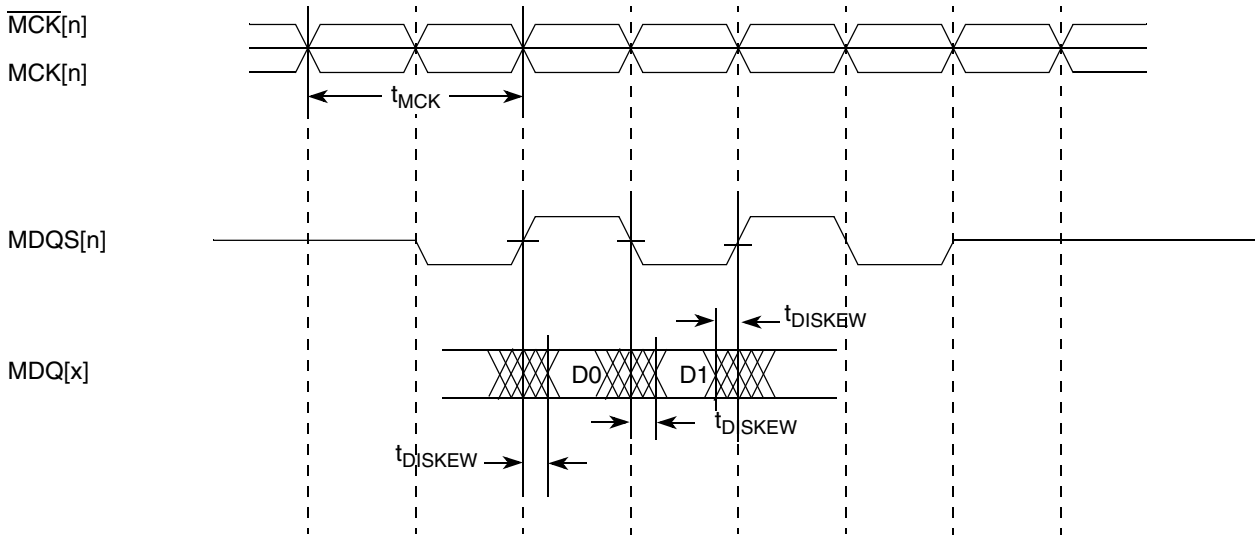


Figure 9. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

2.8.2.2 DDR3 and DDDR3L SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR3 SDRAM interface.

Table 27. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1.5	2.5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
800 MT/s data rate		0.917	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
800 MT/s data rate		0.917	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
800 MT/s data rate		0.917	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
800 MT/s data rate		0.917	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
≥ 1066 MT/s data rate		–0.245	0.245		4, 6
800 MT/s data rate		–0.375	0.375		4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		

Table 27. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ and MDQS/$\overline{\text{MDQS}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *P3041 QorIQ Integrated Multicore Communication Processor Family* for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
6. Note that for 1200/1333/1600 frequencies it is required to program the start value of the DQS adjust for write leveling.

NOTE

For the ADDR/CMD setup and hold specifications in Table 27, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

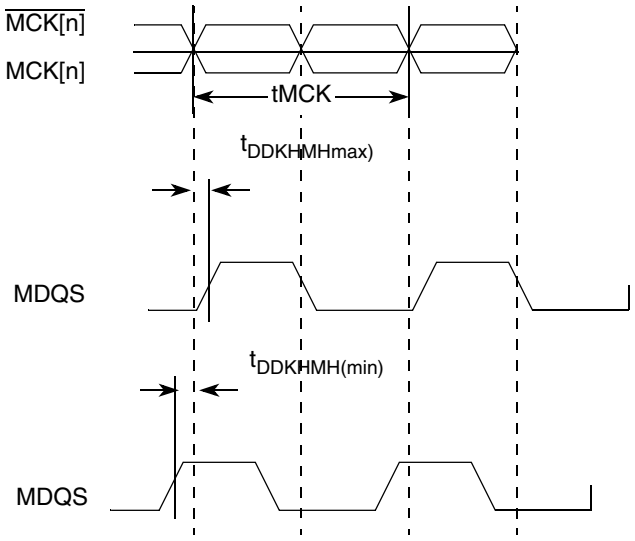


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

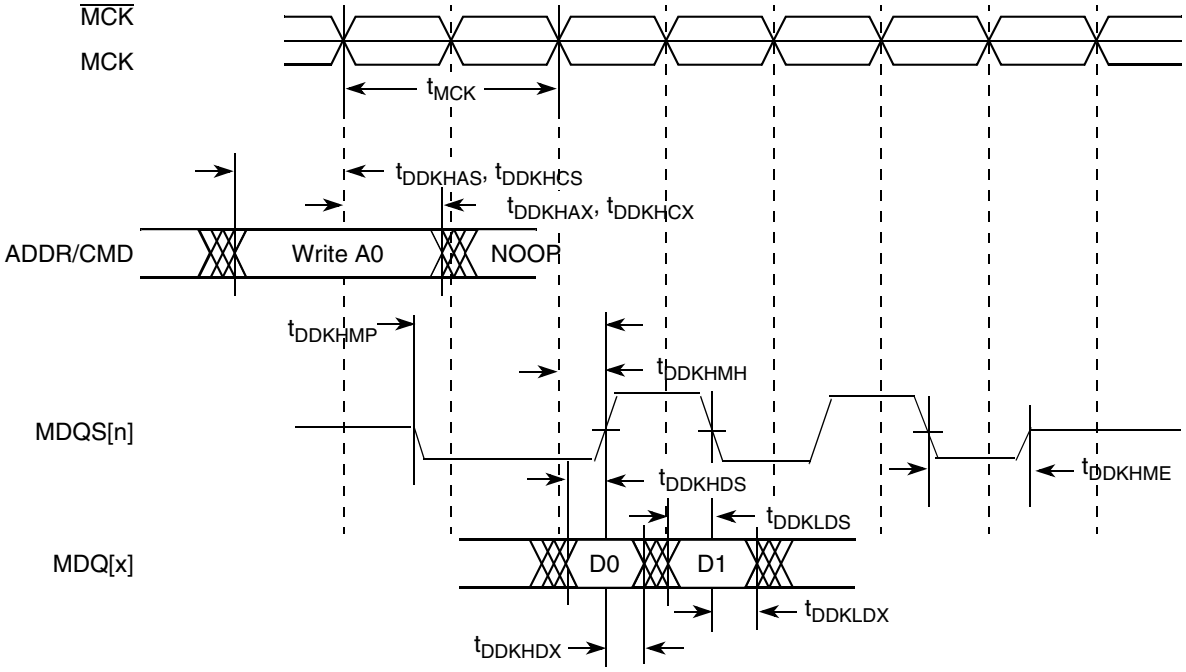


Figure 11. DDR3 and DDR3L Output Timing Diagram

This figure provides the AC test load for the DDR3 controller bus.

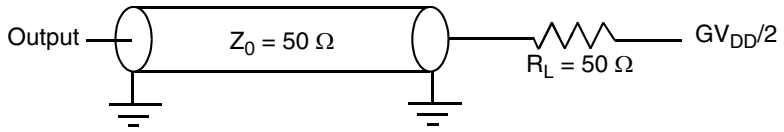


Figure 12. DDR3 Controller Bus AC Test Load

2.8.2.3 DDR3 and DDR3L SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 and DDR3L SDRAM controller interface. This figure shows the differential timing specification.

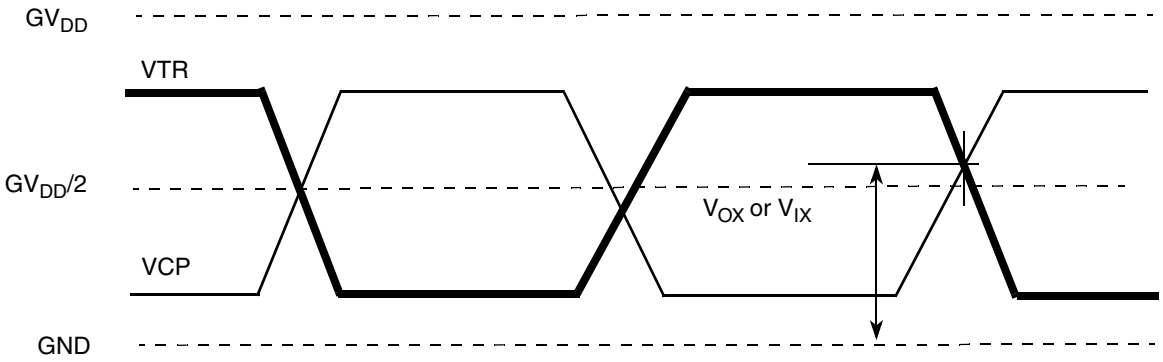


Figure 13. DDR3 and DDR3L SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

This table provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 28. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.150$	$0.5 \times GV_{DD} + 0.150$	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.115$	$0.5 \times GV_{DD} + 0.115$	V	1

Note:

1. I/O drivers are calibrated before making measurements.

This table provides the DDR3L differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 29. DDR3L SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.135$	$0.5 \times GV_{DD} + 0.135$	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.105$	$0.5 \times GV_{DD} + 0.105$	V	1

Note:

1. I/O drivers are calibrated before making measurements.

2.9 eSPI

This section describes the DC and AC electrical specifications for the eSPI interface.

2.9.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 3.3 V.

Table 30. eSPI DC Electrical Characteristics (CV_{DD} = 3.3 V)[1,2]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.8	V
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA
Output high voltage (CV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Output low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 2.5 V.

Table 31. eSPI DC Electrical Characteristics (CV_{DD} = 2.5 V)[1,2]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	1.7	—	V
Input low voltage	V_{IL}	—	0.7	V
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA
Output high voltage (CV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V
Output low voltage (CV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 32. eSPI DC Electrical Characteristics (CV_{DD} = 1.8 V)[1,2]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	1.25	—	V
Input low voltage	V_{IL}	—	0.6	V
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA
Output high voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V
Output low voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.9.2 eSPI AC Timing Specifications

This table provides the eSPI input and output AC timing specifications.

Table 33. eSPI AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX}	2 + ($t_{PLATFORM\_CLK}$ *SPMODE[HO_ADJ])	—	ns	2, 3
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV}	—	5.24 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
eSPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	7	—	ns	—
eSPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. The greater of the two output timings for t_{NIKHOX} and t_{NIKHOV} are used when SPCOM[RxDelay] of the eSPI command register is set. For example, the t_{NIKHOX} is 4.0 and t_{NIKHOV} is 7.0 if SPCOM[RxDelay] is set to be 1.

This figure provides the AC test load for the eSPI.

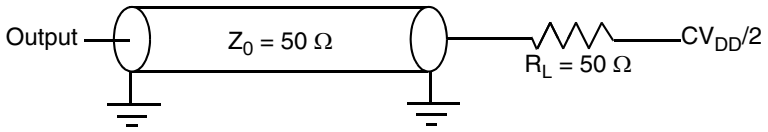


Figure 14. eSPI AC Test Load

This table represents the AC timing from Table 33 in master mode (internal clock). Note that although timing specifications generally refer to the rising edge of the clock, Figure 15 also applies when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

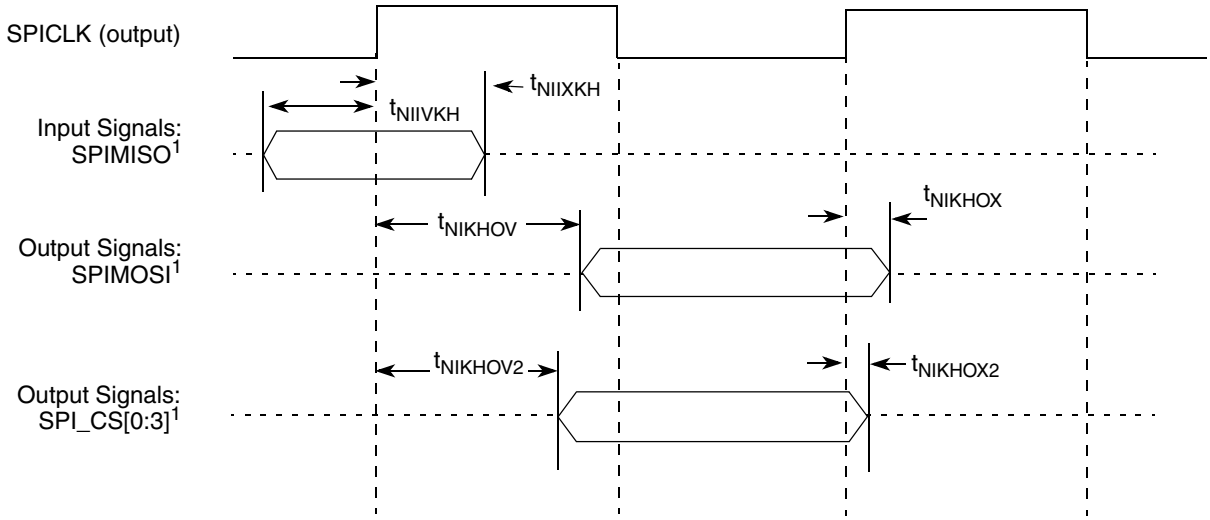


Figure 15. eSPI AC Timing in Master Mode (Internal Clock) Diagram

2.10 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

2.10.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 34. DUART DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1

Table 34. DUART DC Electrical Characteristics (OV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:
1. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
2. Note that the symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.10.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 35. DUART AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2*1,048,576)	baud	1
Maximum baud rate	f_{PLAT}/(2*16)	baud	1, 2
Oversample rate	16	—	3

Notes:
1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.11 Ethernet: Datapath Three-Speed Ethernet (dTSEC), Management Interface, IEEE Std 1588

This section provides the AC and DC electrical characteristics for the datapath three-speed Ethernet controller, the Ethernet Management Interface, and the IEEE Std 1588 interface.

2.11.1 SGMII Timing Specifications

See Section 2.19.9, "SGMII Interface."

2.11.2 RGMII Timing Specifications

This section discusses the electrical characteristics for the RGMII interfaces.

2.11.2.1 RGMII DC Electrical Characteristics

This table shows the RGMII DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 36. RGMII DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.11.2.2 RGMII AC Timing Specifications

This table presents the RGMII AC timing specifications.

Table 37. RGMII AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.8	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of GTX_CLK125 by more than 300 ppm.

This figure shows the RGMII AC timing and multiplexing diagrams.

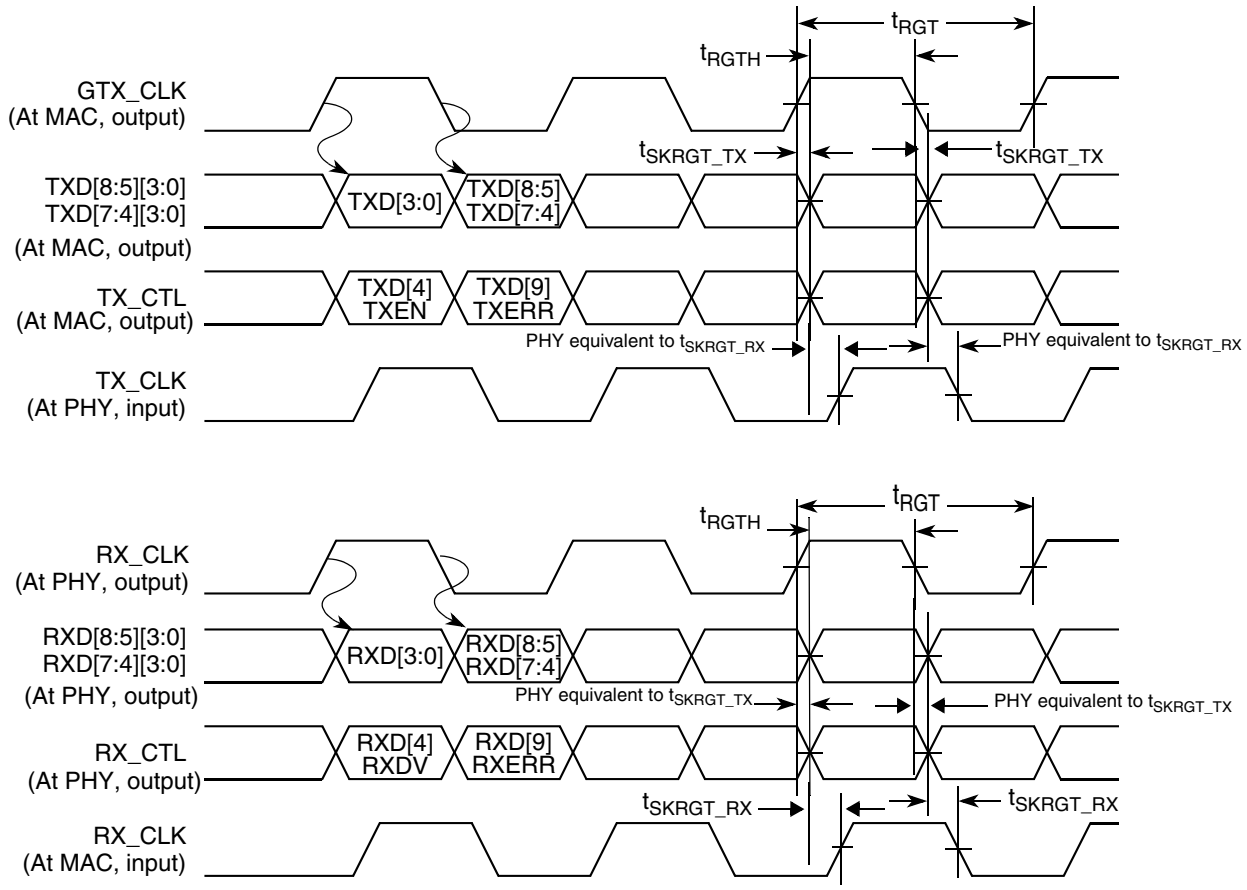


Figure 16. RGMII AC Timing and Multiplexing Diagrams

2.11.3 Ethernet Management Interface

This section discusses the electrical characteristics for the EMI1 and EMI2 interfaces. EMI1 is the PHY management interface controlled by the MDIO controller associated with Frame Manager 1 1GMAC-1. EMI2 is the XAUI PHY management interface controlled by the MDIO controller associated with Frame Manager 1 10GMAC-0.

2.11.3.1 Ethernet Management Interface 1 DC Electrical Characteristics

The Ethernet management interface is defined to operate at a supply voltage of 3.3 V. This table provides the DC electrical characteristics for the Ethernet management interface.

Table 38. Ethernet Management Interface 1 DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

The Ethernet management interface is defined to operate at a supply voltage of 2.5 V. The DC electrical characteristics for the Ethernet management interface is provided in this table.

Table 39. Ethernet Management Interface 1 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. Note that the symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

2.11.3.2 Ethernet Management Interface 2 DC Electrical Characteristics

Ethernet Management Interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface. The DC electrical characteristics for EMI2_MDIO and EMI2_MDC are provided in this section.

Table 40. Ethernet Management Interface 2 DC Electrical Characteristics (1.2 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.84	—	V	—
Input low voltage	V_{IL}	—	0.36	V	—
Output high voltage (I_{OH}= −100 μA)	V_{OH}	1.0	—	V	—
Output low voltage (I_{OL} = 100 μA)	V_{OL}	—	0.2	V	—
Output low current (V_{OL} = 0.2 V)	I_{OL}	4	—	mA	—
Input capacitance	C_{IN}	—	10	pF	—

2.11.3.3 Ethernet Management Interface 1 AC Timing Specifications

This table provides the Ethernet management interface AC timing specifications.

Table 41. Ethernet Management Interface 1 AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 6$	—	$(16 \times t_{plb\_clk}) + 6$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the frame manager clock period.

2.11.3.4 Ethernet Management Interface 2 AC Electrical Characteristics

Table 42. Ethernet Management Interface 2 AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(0.5 \times (1/f_{MDC})) - 6$	—	$(0.5 \times (1/f_{MDC})) + 6$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the frame manager clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the management data clock frequency, f_{MDC}. The delay is equal to 0.5 management data clock period ±6 ns. For example, with a management data clock of 2.5 MHz, the min/max delay is 200 ns ± 6 ns.

This figure shows the Ethernet management interface timing diagram.

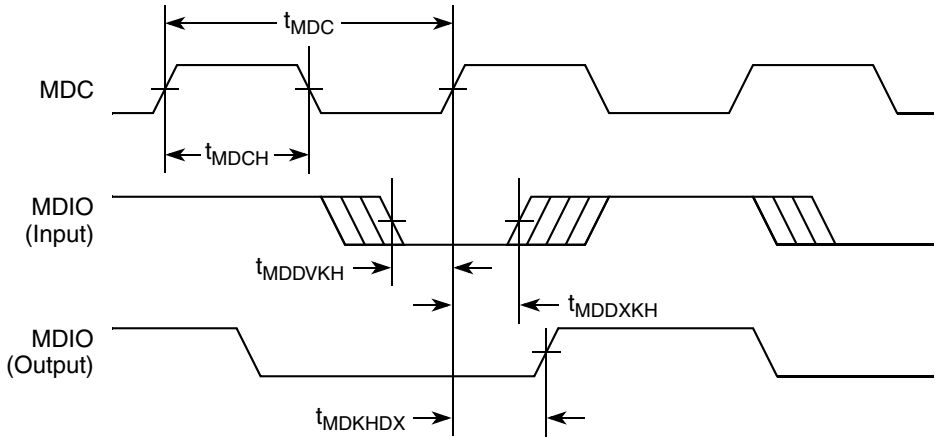


Figure 17. Ethernet Management Interface Timing Diagram

2.11.4 eTSEC IEEE Std 1588 Timing Specifications

This section discusses the electrical characteristics for the eTSEC IEEE Std 1588 interfaces.

2.11.4.1 eTSEC IEEE Std 1588 DC Electrical Characteristics

This table shows eTSEC IEEE Std 1588 DC electrical characteristics when operating at LV_{DD} = 3.3 V supply.

Table 43. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

This table shows the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 44. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.11.4.2 eTSEC IEEE Std 1588 AC Electrical Characteristics

This table provides the IEEE 1588 AC timing specifications.

Table 45. eTSEC IEEE 1588 AC Timing Specifications

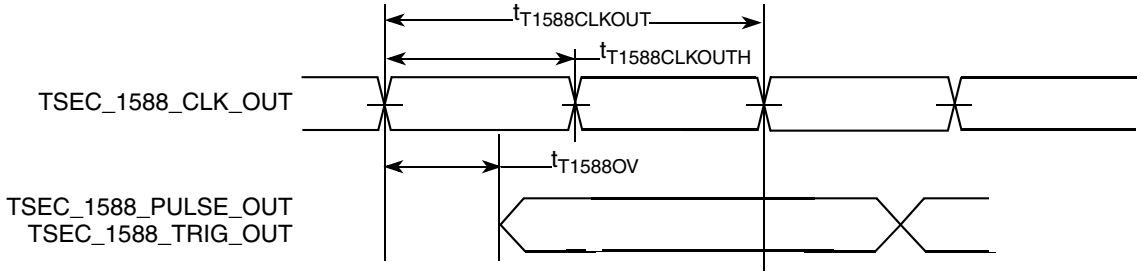
For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK clock period	$t_{T1588CLK}$	6.4	—	$T_{RX\_CLK} \times 7$	ns	1, 2
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	3
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.5	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Notes:

1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the P3041P2041 *QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns, respectively.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is noninverting. Otherwise, it is counted starting at the falling edge.

Figure 18. eTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

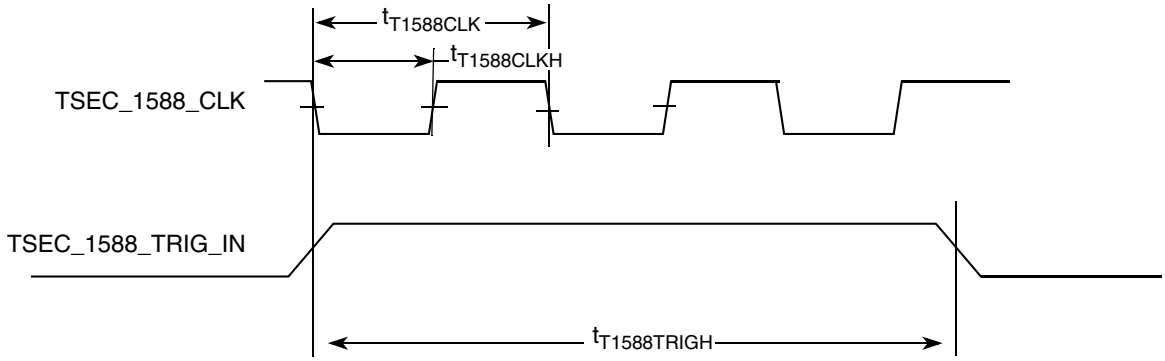


Figure 19. eTSEC IEEE 1588 Input AC Timing

2.12 USB

This section provides the AC and DC electrical specifications for the USB interface.

2.12.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface at USB_VDD_3P3 = 3.3 V.

Table 46. USB DC Electrical Characteristics (USB_V_{DD}_3P3 = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage[1]	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (USB_V_{IN}_3P3 = 0 V or USB_V_{IN}_3P3 = USB_V_{DD}_3P3)	I_{IN}	—	±40	μA	2
Output high voltage (USB_V_{DD}_3P3 = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (USB_V_{DD}_3P3 = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_V_{IN}_3P3 values found in Table 3.
2. The symbol USB_V_{IN}_3P3, in this case, represents the USB_V_{IN}_3P3 symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.12.2 USB AC Electrical Specifications

This table provides the USB clock input (USB*n*_CLKIN) AC timing specifications.

Table 47. USB_CLK_IN AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	—	MHz	—
Rise/Fall time	Measured between 10% and 90%	t_{USRF}	—	—	6	ns	1
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%	—
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%	—
Total input jitter/time interval error	RMS value measured with a second-order, high-pass filter of 500-kHz bandwidth	t_{CLK_PJ}	—	—	5	ps	—

Note:

1. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.13 Enhanced Local Bus Interface (eLBC)

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.13.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V.

Table 48. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended Operating Conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V.

Table 49. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 1.8 V.

Table 50. Enhanced Local Bus DC Electrical Characteristics (BV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.13.2 Enhanced Local Bus AC Timing Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.13.2.1 Test Condition

This figure provides the AC test load for the enhanced local bus.

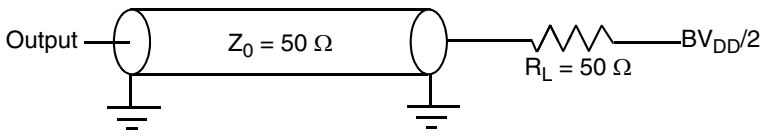


Figure 20. Enhanced Local Bus AC Test Load

2.13.2.2 Local Bus AC Timing Specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table describes the AC timing specifications of the local bus interface.

Table 51. Enhanced Local Bus AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	2.0	ns	—
Output hold (Except LALE)	t_{LBKLOX}	–3.5	—	ns	5
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	2 platform clock cycles - 1ns (LBCR[AHD] = 1)	—	ns	4
		4 platform clock cycles - 1ns (LBCR[AHD] = 0)			

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLKs at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. After power on reset, LBCR[AHD] defaults to 0.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

This figure shows the AC timing diagram of the local bus interface.

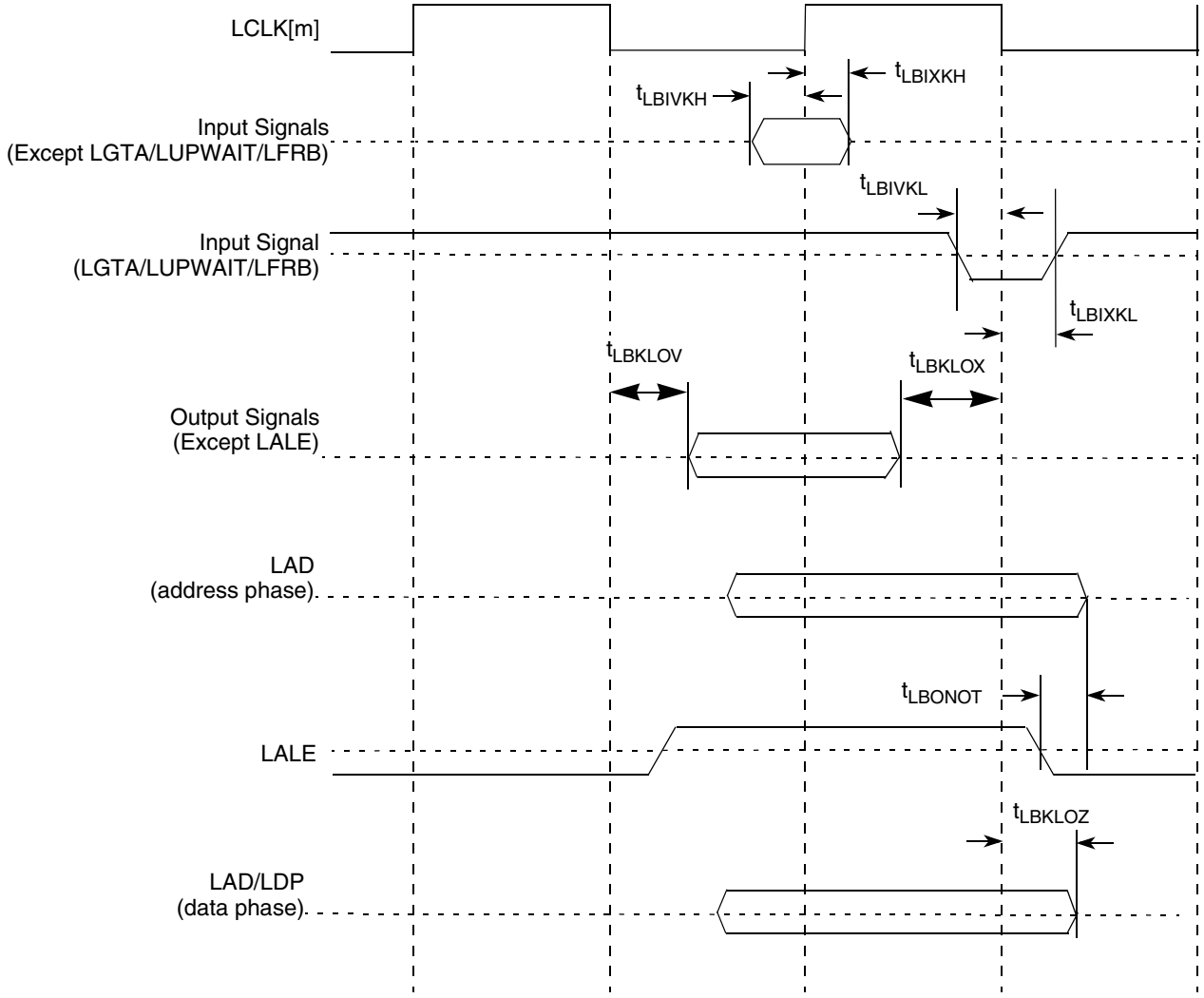


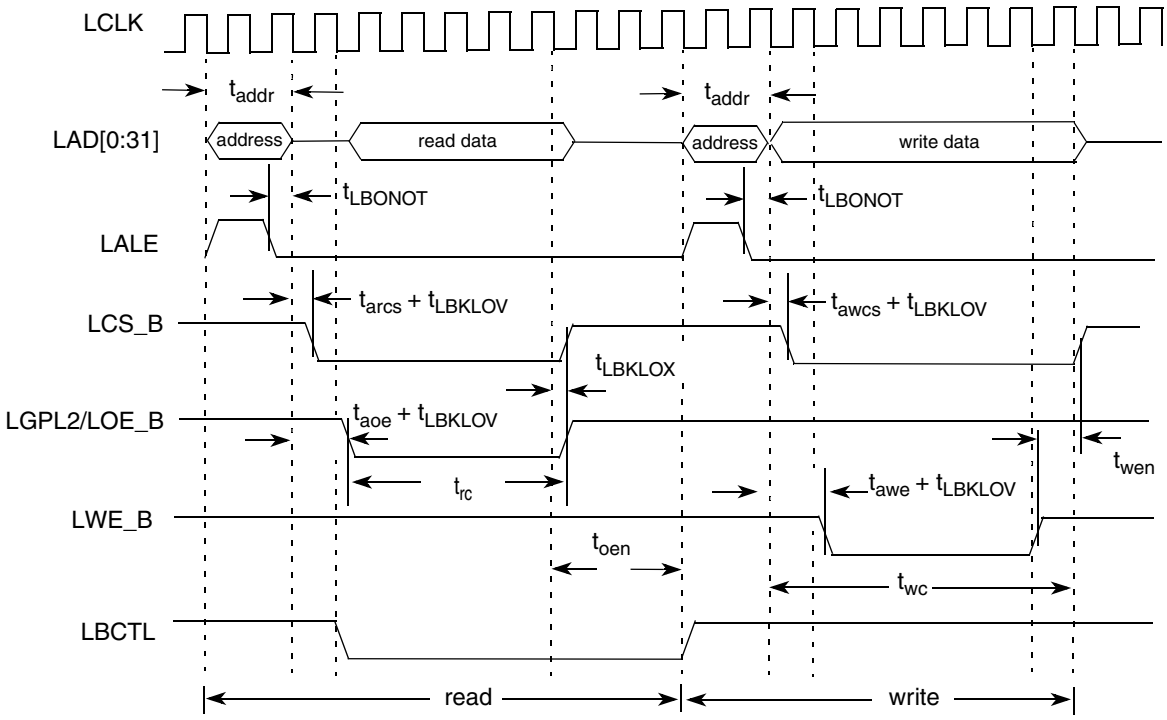
Figure 21. Enhanced Local Bus Signals

Figure 22 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

This figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the *P3041 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.

Figure 22. GPCM Output Timing Diagram

2.14 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.14.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 52. eSDHC Interface DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 × CV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × CV_{DD}	V	1
Input/Output leakage current	I_{IN}/I_{OZ}	—	–50	50	μA	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at CV_{DD} min	0.75 × CV_{DD}	—	V	—

Table 52. eSDHC Interface DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output low voltage	V_{OL}	I_{OL} = 100μA at CV_{DD} min	—	0.125 × CV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at CV_{DD} min	CV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA at CV_{DD} min	—	0.3	V	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. Open drain mode for MMC cards only.

2.14.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in Figure 23 and Figure 24.

Table 53. eSDHC AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/high-speed mode MMC Full-speed/high-speed mode	f_{SHSCK}	 0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/high-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/high-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	2.5	—	ns	4
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD/SDIO card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–50 MHz for an SD/SDIO card and 0–52 MHz for an MMC card.
3. To satisfy setup timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

This figure provides the eSDHC clock input timing diagram.

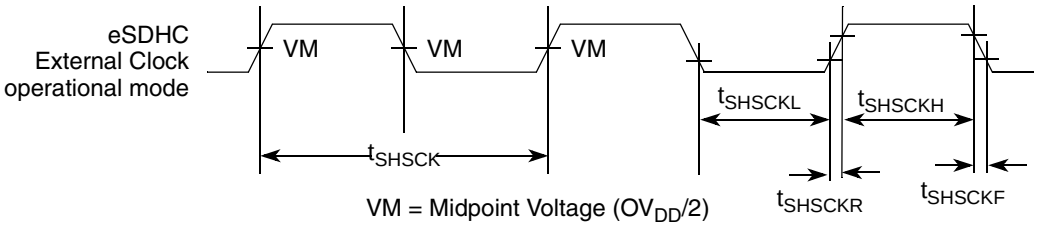


Figure 23. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

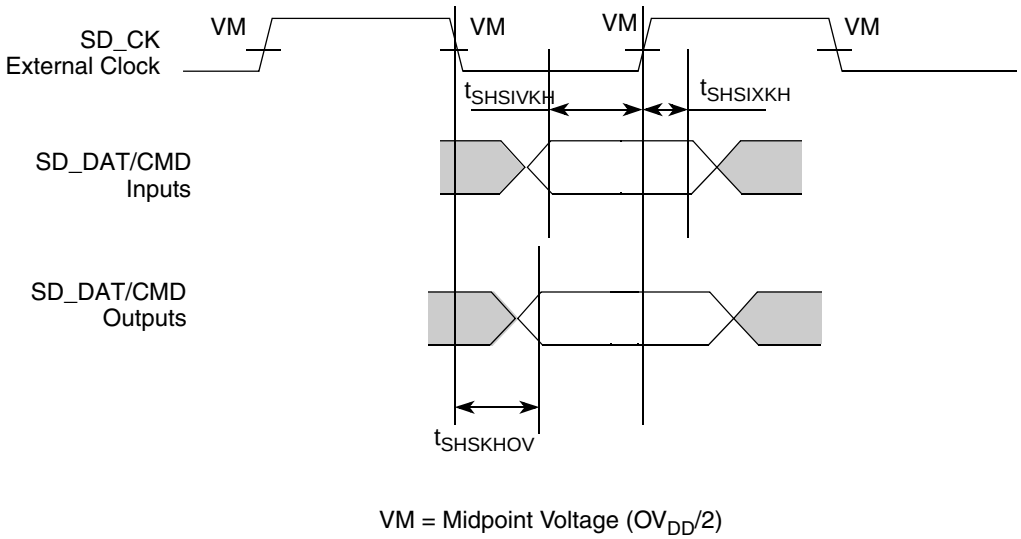


Figure 24. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.15 Multicore Programmable Interrupt Controller (MPIC) and Trust Specifications

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

2.15.1 MPIC and Trust DC specifications

This figure provides the DC electrical characteristics for the MPIC interface.

Table 54. MPIC DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1

Table 54. MPIC DC Electrical Characteristics (OV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3

2.15.2 MPIC and Trust AC Timing Specifications

This table provides the MPIC input and output AC timing specifications.

Table 55. MPIC Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Notes
MPIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLKs	1
Trust inputs—minimum pulse width	t_{TIWID}	3	—	SYSCLKs	2

Note:

1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs must be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode
2. Trust inputs are asynchronous to any visible clock. Trust inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation when working in edge triggered mode. For low power trust input pin LP_TMP_DETECT, the voltage is V_{DD_LP} and see Table 3 for the voltage requirment.

2.16 JTAG Controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.16.1 JTAG DC Electrical Characteristics

This table provides the JTAG DC electrical characteristics.

Table 56. JTAG DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1

Table 56. JTAG DC Electrical Characteristics (OV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Table 3.

2.16.2 JTAG AC Timing Specifications

This table provides the JTAG AC timing specifications as defined in Figure 25 through Figure 28.

Table 57. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at OVDD/2 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	2
Input setup times Boundary-scan USB only Boundary (except USB) TDI, TMS	t_{JTDVKH}	 14 4 4	—	 ns	—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times Boundary-scan data TDO	t_{JTKLDV}	—	 15 10	ns	3
Output hold times	t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

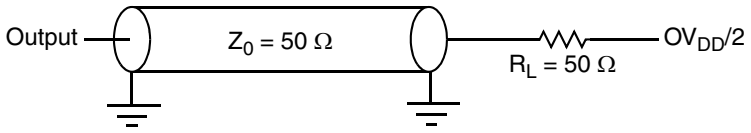


Figure 25. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

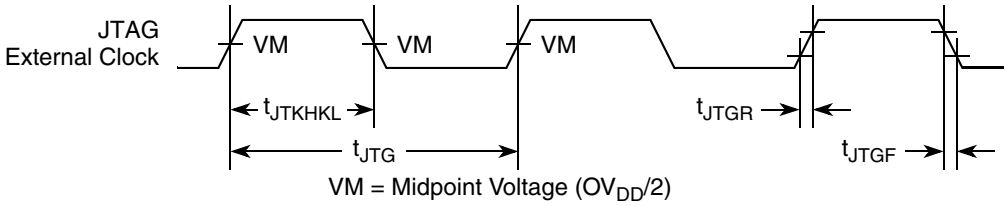


Figure 26. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

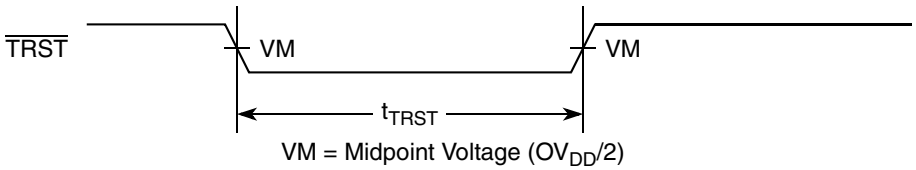


Figure 27. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

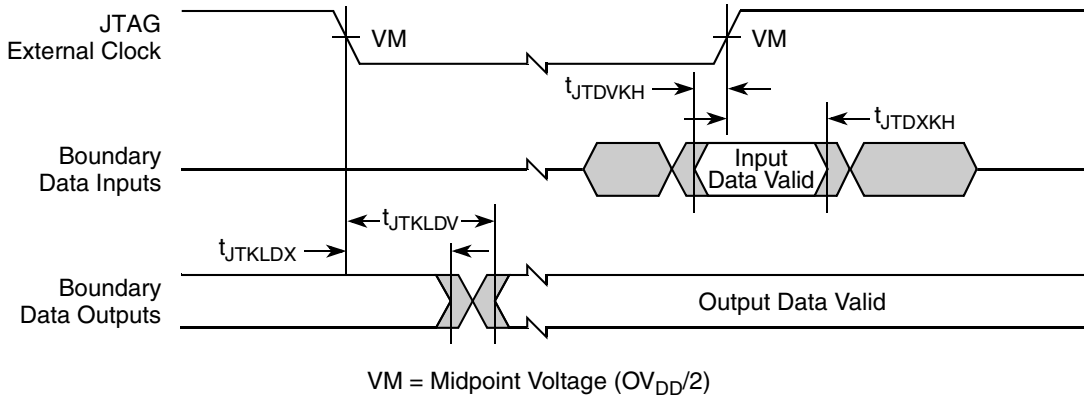


Figure 28. Boundary-Scan Timing Diagram

2.17 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface.

2.17.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 58. I²C DC Electrical Characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current for each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–40	40	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. Refer to the *P3041QorIQ Integrated Multicore Communication Processor Family Reference Manual* for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.17.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 59. I²C AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

Table 59. I²C AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, application note AN2919 referred to in note 2 above is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

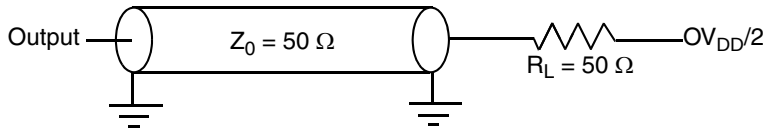


Figure 29. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

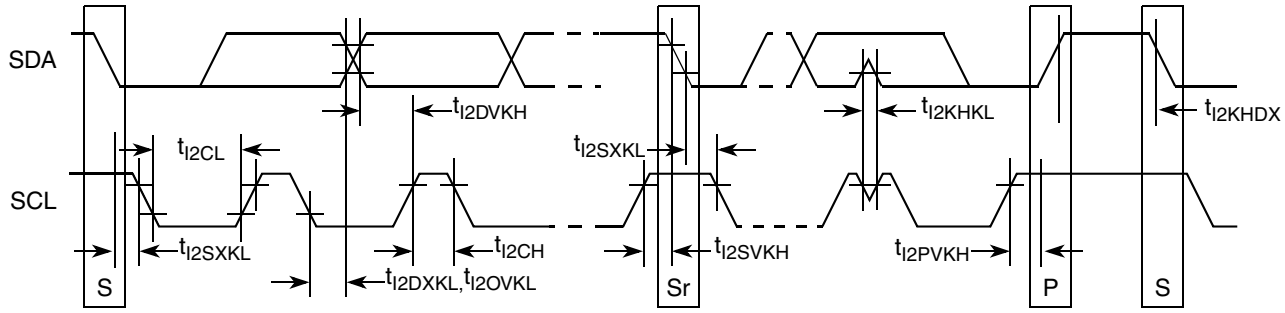


Figure 30. I²C Bus AC Timing Diagram

2.18 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for GPIO pins operating at 3.3 V.

Table 60. GPIO DC Electrical Characteristics (LV_{DD} or OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max L/OV_{IN} respective values found in Table 3.
2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} = 2.5 V.

Table 61. GPIO DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 62. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

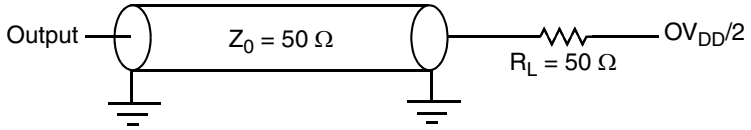


Figure 31. GPIO AC Test Load

2.19 High-Speed Serial Interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, Serial RapidIO, XAUI, Aurora and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.19.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 32 shows the waveform for either a transmitter output (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or a receiver input (SD_RX*n* and $\overline{\text{SD\_RX}n}$). Each signal swings between A volts and B volts where A > B.

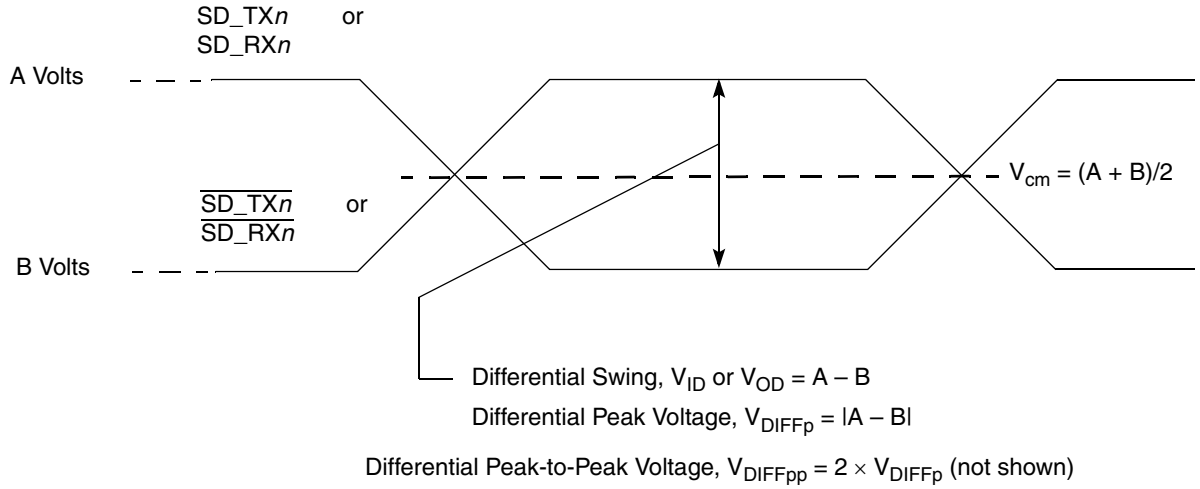


Figure 32. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing
The transmitter output signals and the receiver input signals SD_TX*n*, $\overline{\text{SD\_TX}n}$, SD_RX*n* and $\overline{\text{SD\_RX}n}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**)
The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TXn} - V_{\overline{SD\_TXn}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**)
The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RXn} - V_{\overline{SD\_RXn}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}
The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$
Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform
The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_TX}n}$, for example) from the non-inverting signal ($\overline{\text{SD\_TX}n}$, for example) within a differential pair. There is

only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 37 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn} + V_{\overline{SD\_TXn}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{TD}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.19.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK1 and $\overline{SD\_REF\_CLK1}$ for SerDes bank1, SD_REF_CLK2 and $\overline{SD\_REF\_CLK2}$ for SerDes bank2, and SD_REF_CLK3 and $\overline{SD\_REF\_CLK3}$ for SerDes bank3.

SerDes banks 1–3 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCL:

- SerDes bank 1: PEX1/2/3/4, sRIO1/2, SGMII (1.25 Gbps only) or Aurora.
- SerDes bank 2: PEX3, SGMII (1.25 or 3.125 GBaud) or XAUI.
- SerDes bank 3: sRIO1, SATA, SGMII (1.25 or 3.125 GBaud) or XAUI.

The following sections describe the SerDes reference clock requirements and provide application information.

2.19.2.1 SerDes Reference Clock Receiver Characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

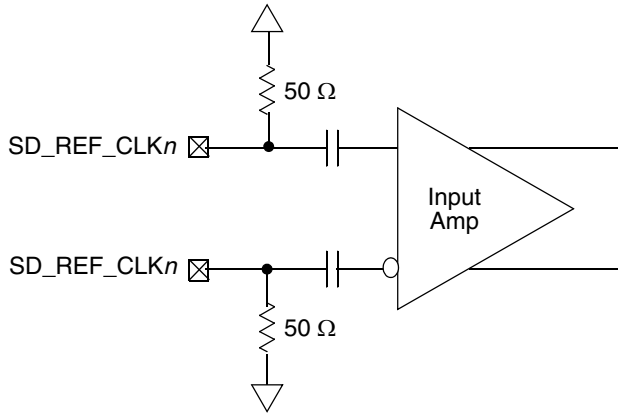


Figure 33. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (SV_{DD}) are as specified in Section 2.1.2, "Recommended Operating Conditions."
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ are internally AC-coupled differential inputs as shown in Figure 33. Each differential clock input (SD_REF_CLK*n* or $\overline{\text{SD\_REF\_CLK}n}$) has on-chip 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.19.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Section 2.19.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 34 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

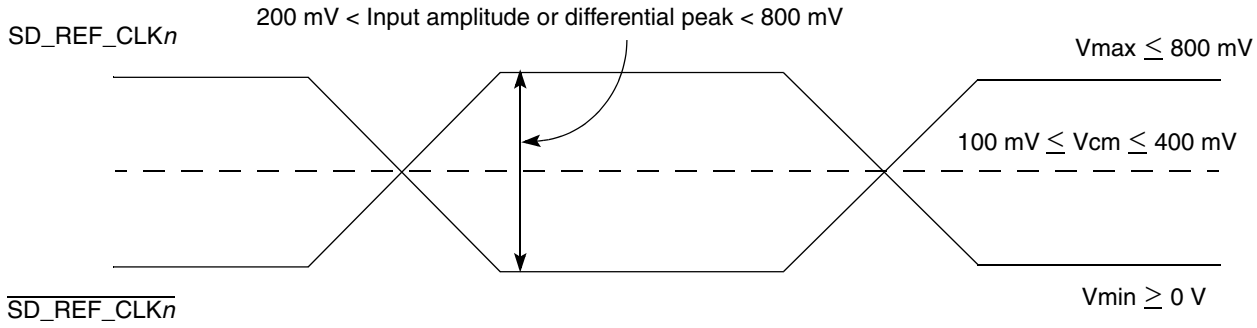


Figure 34. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). Figure 35 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

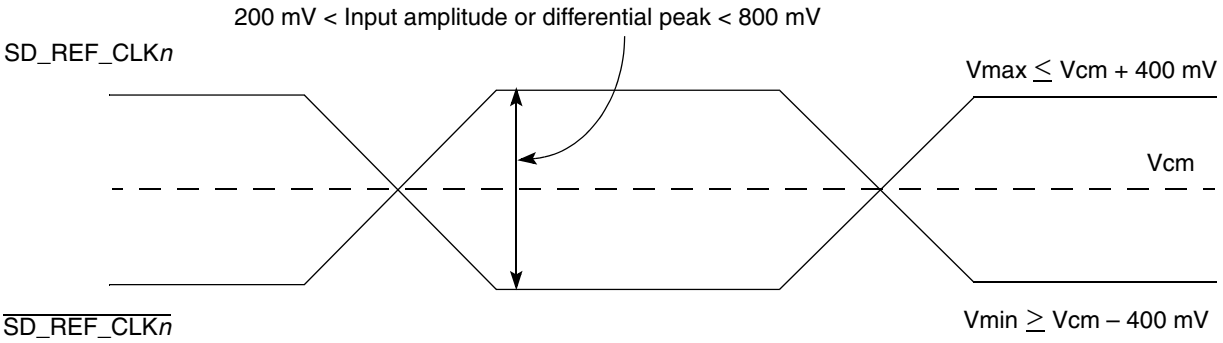


Figure 35. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The SD_REF_CLK*n* input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}n}$ either left unconnected or tied to ground.
  - The SD_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 36 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}n}$) through the same source impedance as the clock input (SD_REF_CLK*n*) in use.

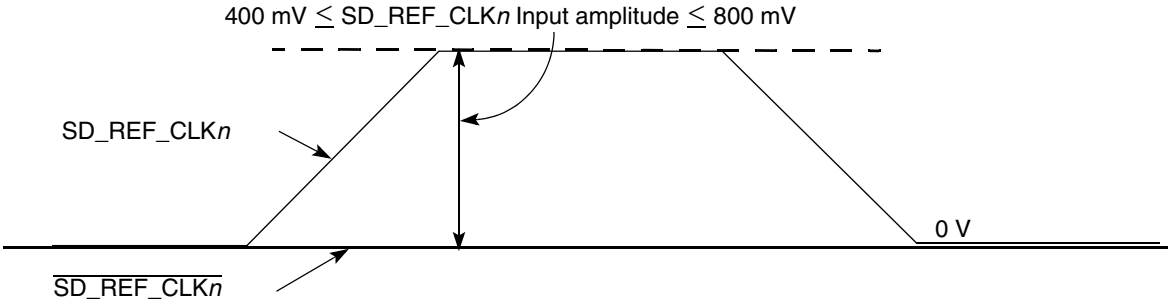


Figure 36. Single-Ended Reference Clock Input DC Requirements

2.19.2.3 AC Requirements for SerDes Reference Clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

Table 63. SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ Input Clock Requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125/156.25	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching	Rise-Fall Matching	—	—	20	%	5, 6

Notes:
1. **Caution:** Only 100, 125 and 156.25 have been tested. In-between values do not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus $\overline{\text{SD\_REF\_CLK}n}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 37.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD\_REF\_CLK}n}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD\_REF\_CLK}n}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* must be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}n}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38.

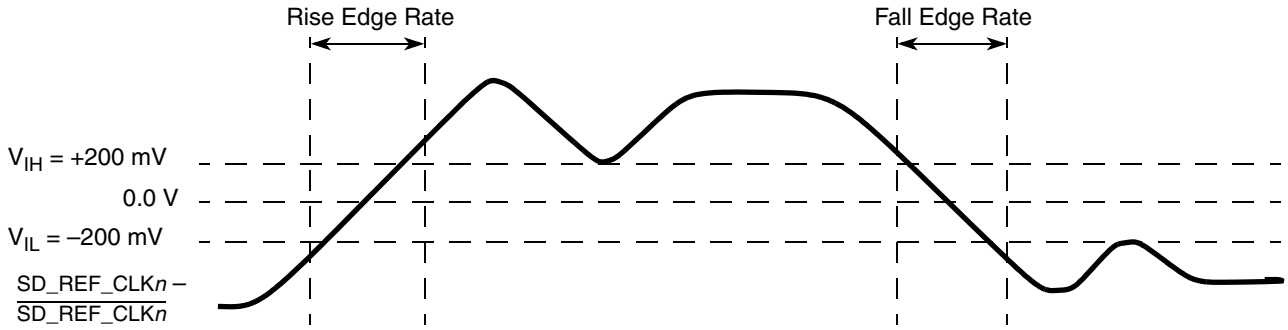


Figure 37. Differential Measurement Points for Rise and Fall Time

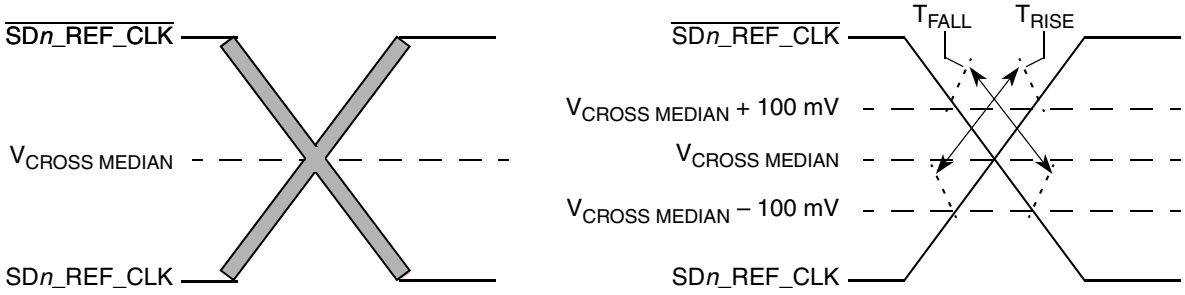


Figure 38. Single-Ended Measurement Points for Rise and Fall Time Matching

2.19.2.4 Spread Spectrum Clock

SD_REF_CLK1/$\overline{\text{SD\_REF\_CLK1}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

SD_REF_CLK2/$\overline{\text{SD\_REF\_CLK2}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.

SD_REF_CLK3/$\overline{\text{SD\_REF\_CLK3}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

2.19.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

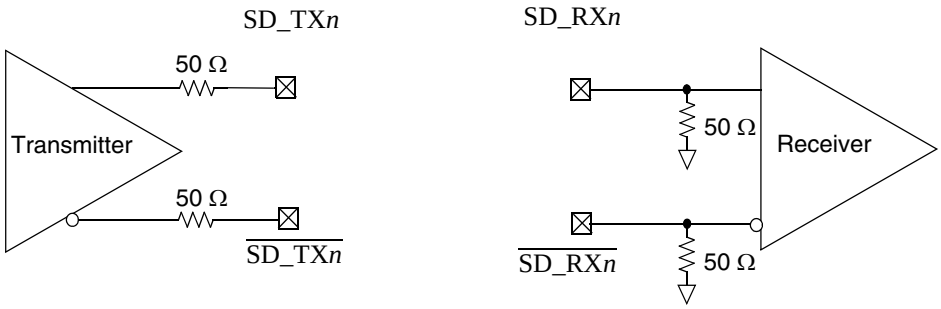


Figure 39. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- Section 2.19.4, "PCI Express"
- Section 2.19.5, "Serial RapidIO (sRIO)"
- Section 2.19.6, "XAUI"
- Section 2.19.7, "Aurora"
- Section 2.19.8, "Serial ATA (SATA)
- Section 2.19.9, "SGMII Interface"

Note that external AC-coupling capacitor is required for the above serial transmission protocols per the protocol's standard requirements.

2.19.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

2.19.4.1 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

2.19.4.2 PCI Express Clocking Requirements for SD_REF_CLK*n* and SD_REF_CLK*n*

SerDes banks 1–2 (SD_REF_CLK[1:2] and $\overline{\text{SD\_REF\_CLK[1:2]}}$) may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is not supported on SerDes bank 3.

For more information on these specifications, see Section 2.19.2, "SerDes Reference Clocks."

2.19.4.3 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.19.4.3.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 64. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	—	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 65. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	—	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low impedance

Table 65. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Note:
1. Measured at the package pins with a test load of 50 Ω to GND on each pin.

2.19.4.4 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 66. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Rx DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50 k	—	—	Ω	Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 67. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	—	1200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Rx DC Differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required Rx D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

2.19.4.5 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.19.4.5.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 68. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 40 and measured over any 250 consecutive Tx UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 69. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 40 and measured over any 250 consecutive Tx UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

2.19.4.5.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications 2.5 GT/s and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 70. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2, 3 and 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 40 must be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 71. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 400 ps ±300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Max Rx inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common RefClk Rx architecture
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-TJ-DC}$	—	—	0.34	UI	Max Rx inherent total timing error
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture

Note:
1. No test load is necessarily associated with this value.

2.19.4.6 Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

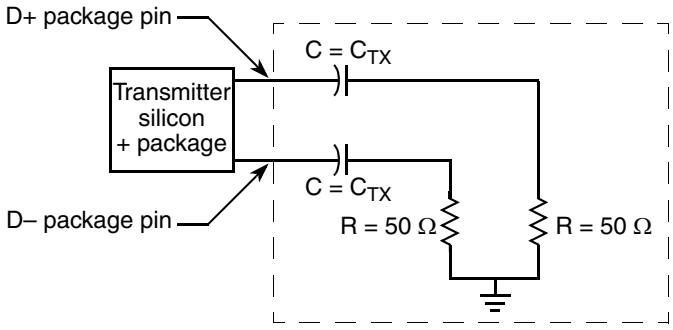


Figure 40. Test/Measurement Load

2.19.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates:

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

2.19.5.1 Signal Definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. The following figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals—TD, $\overline{TD}$, RD, and $\overline{RD}$—each have a peak-to-peak swing of A – B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts.

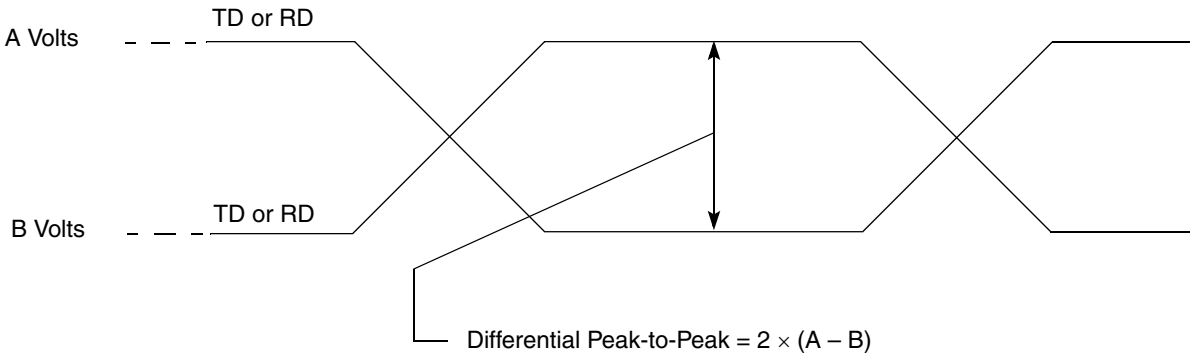


Figure 41. Differential Peak-to-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.19.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

2.19.5.3 Serial RapidIO Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

SerDes bank 1 and bank 3 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for various SerDes Serial RapidIO configurations based on the RCW Configuration field SRDS_PRTCL. Serial RapidIO is not supported on SerDes banks 2.

For more information on these specifications, see Section 2.19.2, “SerDes Reference Clocks.”

2.19.5.4 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.19.5.4.1 DC Serial RapidIO Timing Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case is better than the following:

- –10 dB for (Baud Frequency) ÷ 10 < Freq(f) < 625 MHz
- –10 dB + 10log(f ÷ 625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 20 ps at 2.50 GBaud and 15 ps at 3.125 GBaud.

This table defines the transmitter DC specifications for Serial RapidIO operating at XV_{DD} = 1.5 V or 1.8 V.

Table 72. Serial RapidIO Transmitter DC Timing Specifications—2.5 GBaud, 3.125 GBaud, 5 GBaud

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage,	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

2.19.5.4.2 DC Serial RapidIO Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

This table defines the receiver DC specifications for Serial RapidIO operating at XV_{DD} = 1.5 V or 1.8 V.

Table 73. Serial RapidIO Receiver DC Timing Specifications—2.5 GBaud, 3.125 GBaud, 5 GBaud

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1

Note:
1. Measured at the receiver.

2.19.5.5 AC Requirements for Serial RapidIO

This section explains the AC requirements for the Serial RapidIO interface.

2.19.5.5.1 AC Requirements for Serial RapidIO Transmitter

This table defines the transmitter AC specifications for the Serial RapidIO. The AC timing specifications do not include RefClk jitter.

Table 74. Serial RapidIO Transmitter AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

This table defines the receiver AC specifications for Serial RapidIO. The AC timing specifications do not include RefClk jitter.

Table 75. Serial RapidIO Receiver AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance[2]	J_T	0.65	—	—	UI p-p	1
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100 ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.

This figure shows the single-frequency sinusoidal jitter limits.

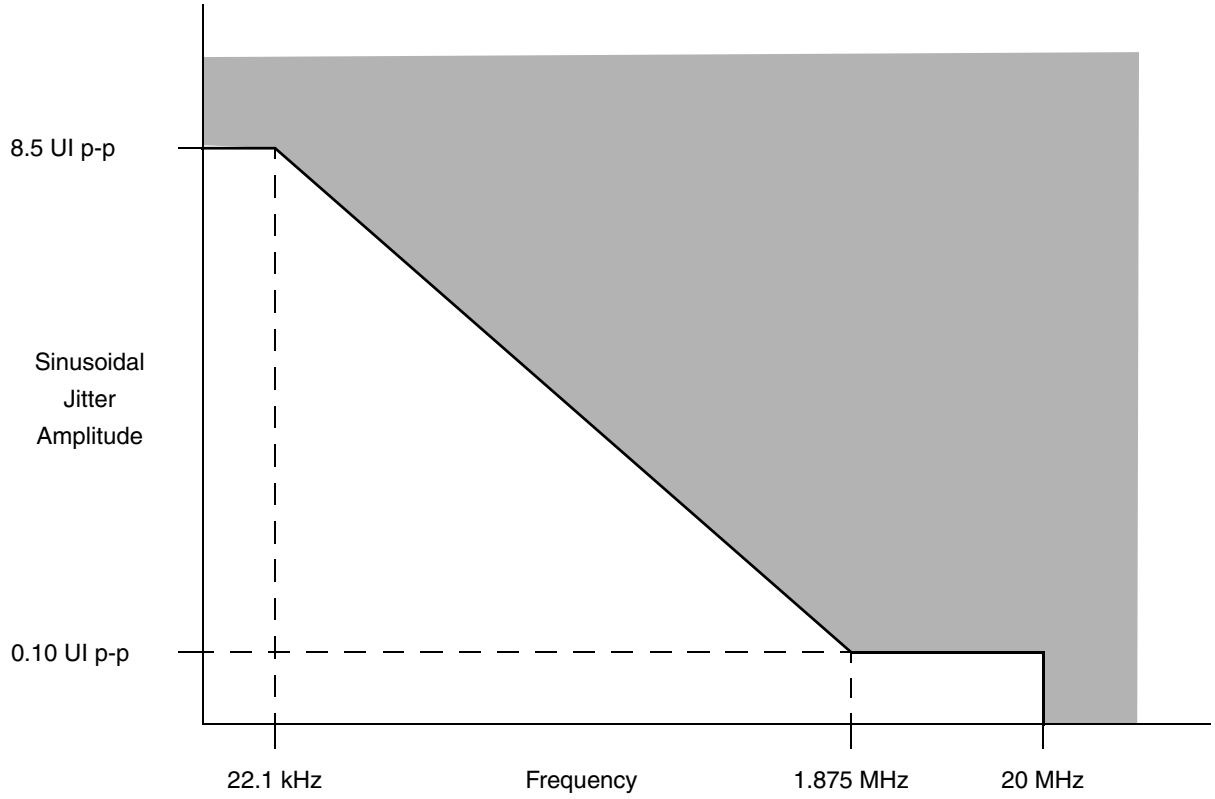


Figure 42. Single-Frequency Sinusoidal Jitter Limits

2.19.6 XAUI

This section describes the DC and AC electrical specifications for the XAUI bus.

2.19.6.1 XAUI DC Electrical Characteristics

This section discusses the XAUI DC electrical characteristics for the clocking signals, transmitter, and receiver.

2.19.6.1.1 DC Requirements for XAUI SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes banks 2-3 (SD_REF_CLK[2:3] and $\overline{\text{SD\_REF\_CLK}}$[2:3]) may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL. XAUI is not supported on SerDes bank 1.

For more information on these specifications, see Section 2.19.2, "SerDes Reference Clocks."

2.19.6.1.2 XAUI Transmitter DC Electrical Characteristics

This table defines the XAUI transmitter DC electrical characteristics.

Table 76. XAUI Transmitter DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—

Note:

1. Absolute output voltage limit

2.19.6.1.3 XAUI Receiver DC Electrical Characteristics

This table defines the XAUI receiver DC electrical characteristics.

Table 77. XAUI Receiver DC Timing Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	900	1600	mV p-p	1

Note:

1. Measured at the receiver.

2.19.6.2 XAUI AC Timing Specifications

This section discusses the XAUI AC timing specifications for the clocking signals, transmitter, and receiver.

2.19.6.2.1 AC Requirements for XAUI SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

This table specifies AC requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$, where n = [2:3]. Only SerDes banks 2–3 may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL. XAUI is not supported on SerDes bank 1.

Table 78. XAUI AC SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ Input Clock Requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	125/156.25	—	MHz	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–100	—	100	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ cycle to cycle jitter (period jitter at refClk input)	t_{CLK_CJ}	—	—	100	ps	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter (peak-to-peak phase jitter at refClk input)	t_{CLK_PJ}	-50	—	50	ps	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	1
Differential input high voltage	V_{IH}	200	—	—	mV	2
Differential input low voltage	V_{IL}	—	—	–200	mV	2
Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching	Rise-Fall Matching	—	—	20	%	3, 4

Notes:
1. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus $\overline{\text{SD\_REF\_CLK}n}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 37.
2. Measurement taken from differential waveform
3. Measurement taken from single-ended waveform
4. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD\_REF\_CLK}n}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD\_REF\_CLK}n}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* must be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}n}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38.

2.19.6.2.2 XAUI Transmitter AC Timing Specifications

This table defines the XAUI transmitter AC timing specifications. RefClk jitter is not included.

Table 79. XAUI Transmitter AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

2.19.6.2.3 XAUI Receiver AC Timing Specifications

This table defines the receiver AC specifications for XAUI. RefClk jitter is not included.

Table 80. XAUI Receiver AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

2.19.7 Aurora

This section describes the Aurora clocking requirements and its AC and DC electrical characteristics.

2.19.7.1 Aurora DC Electrical Characteristics

This section describes the DC electrical characteristics for Aurora.

2.19.7.1.1 Aurora DC Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2-3.

For more information on these specifications, see Section 2.19.2, “SerDes Reference Clocks.”

2.19.7.1.2 Aurora Transmitter DC Electrical Characteristics

This table defines the Aurora transmitter DC electrical characteristics.

Table 81. Aurora Transmitter DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p

2.19.7.1.3 Aurora Receiver DC Electrical Characteristics

This table defines the Aurora receiver DC electrical characteristics for Aurora.

Table 82. Aurora Receiver DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	120	900	1200	mV p-p	1

Note:
1. Measured at receiver

2.19.7.2 Aurora AC Timing Specifications

This section describes the AC timing specifications for Aurora.

2.19.7.2.1 Aurora AC Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2-3.

2.19.7.2.2 Aurora Transmitter AC Timing Specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 83. Aurora Transmitter AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps

2.19.7.2.3 Aurora Receiver AC Timing Specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 84. Aurora Receiver AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—

Table 84. Aurora Receiver AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps	—

Note:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

2.19.8 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

2.19.8.1 SATA DC Electrical Characteristics

This section describes the DC electrical characteristics for SATA.

2.19.8.1.1 SATA DC Transmitter Output Characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 85. Gen1i/1.5G Transmitter (Tx) DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	—	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Notes:

1. Terminated by 50 Ω load.
2. DC impedance

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 86. Gen 2i/3G Transmitter (Tx) DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx diff output voltage	V_{SATA_TXDIFF}	400	—	700	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Note:

1. Terminated by 50 Ω load.

2.19.8.1.2 SATA DC Receiver (Rx) Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 87. Gen1i/1.5 G Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	600	mV p-p	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	2

Note:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 88. Gen2i/3 G Receiver (Rx) Input DC Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	275	—	750	mV p-p	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

2.19.8.2 SATA AC Timing Specifications

This section discusses the SATA AC timing specifications.

2.19.8.2.1 AC Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock listed in this table are to be guaranteed by the customer's application design.

Table 89. SATA Reference Clock Input Requirements

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	+350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	–50	—	+50	ps	2, 3, 4

Notes:
1. **Caution:** Only 100 and 125MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.

This figure shows the reference clock timing waveform.

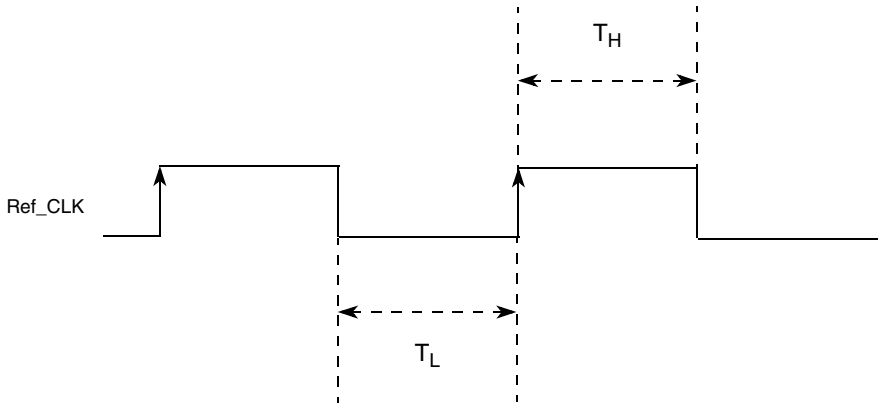


Figure 43. Reference Clock Timing Waveform

2.19.8.3 AC Transmitter Output Characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 90. Gen1i/1.5 G Transmitter (Tx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI p-p	1

Note:

1. Measured at Tx output pins peak to peak phase variation, random data pattern

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 91. Gen 2i/3 G Transmitter (Tx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.3	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at Tx output pins peak-to-peak phase variation, random data pattern

2.19.8.4 AC Differential Receiver Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 92. Gen 1i/1.5G Receiver (Rx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 93. Gen 2i/3G Receiver (Rx) AC Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver.

2.19.9 SGMII Interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 44, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 39.

2.19.9.0.1 SGMII Clocking Requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD_REF_CLK[1:3] and $\overline{\text{SD\_REF\_CLK}}$[1:3] pins. SerDes banks 1-3 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.19.2, “SerDes Reference Clocks.”

2.19.9.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.19.9.1.1 SGMII Transmit DC Timing Specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) as shown in Figure 45.

Table 94. SGMII DC Transmitter Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	—	—	mV	1
Output differential voltage[2, 3, 4] (XV_{DD-Typ} at 1.5 V and 1.8 V)	$\lvert V_{OD}\rvert$	320	500.0	725.0	mV	B(1–3)TECR(lane)0 [AMP_RED] =0b000000
		293.8	459.0	665.6		B(1–3)TECR(lane)0 [AMP_RED] =0b000010
		266.9	417.0	604.7		B(1–3)TECR(lane)0 [AMP_RED] =0b000101
		240.6	376.0	545.2		B(1-3)TECR(lane)0[AMP_RED] =0b001000
		213.1	333.0	482.9		B(1–3)TECR(lane)0 [AMP_RED] =0b001100
		186.9	292.0	423.4		B(1–3)TECR(lane)0 [AMP_RED] =0b001111
		160.0	250.0	362.5		B(1–3)TECR(lane)0 [AMP_RED] =0b010011
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:
1. This does not align to DC-coupled SGMII.
2. $\lvert V_{OD}\rvert = \lvert V_{SD\_TXn} - V_{\overline{SD\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{OD}\rvert$.
3. Example amplitude reduction setting for SGMII on SerDes bank 1 lane E: B1TECRE0[AMP_RED] = 0b000010 for an output differential voltage of 459 mV typical.
4. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.5 V or 1.8 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD_TX*n* and $\overline{\text{SD\_TX}n}$.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

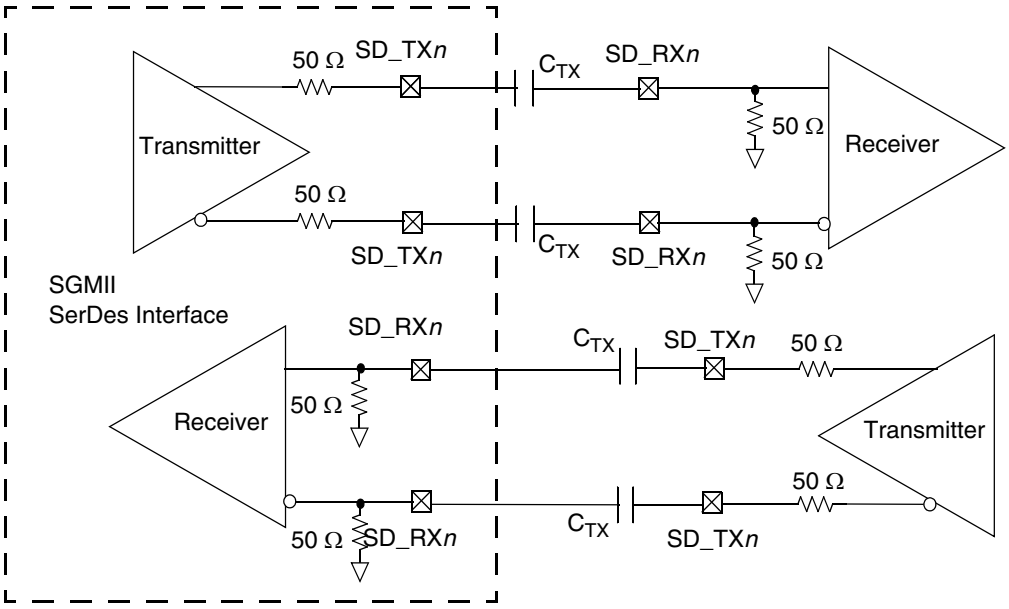


Figure 44. 4-Wire AC-Coupled SGMII Serial Link Connection Example

This figure shows the SGMII transmitter DC measurement circuit.

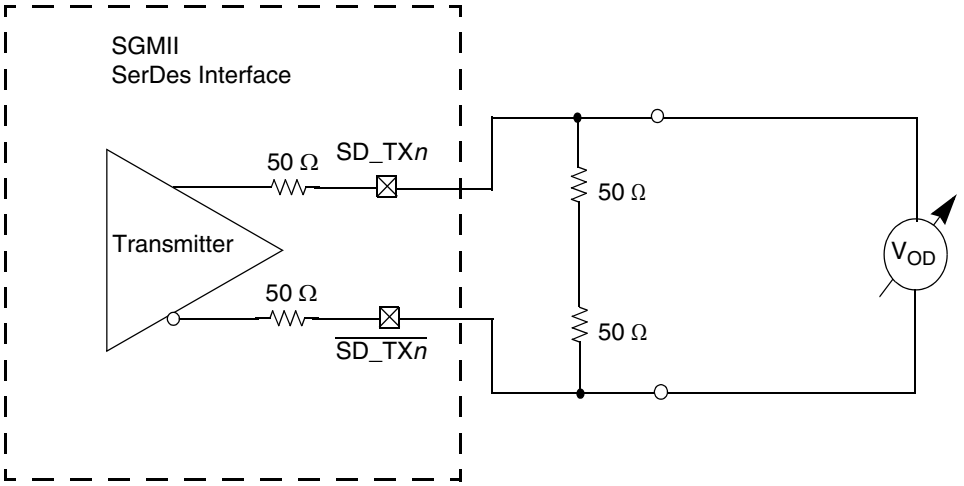


Figure 45. SGMII Transmitter DC Measurement Circuit

This figure defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 95. SGMII 2.5x Transmitter DC Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—

Note:
1. Absolute output voltage limit

2.19.9.1.2 SGMII DC Receiver Electrical Characteristics

This figure lists the SGMII DC receiver electrical characteristics for 1.25 GBaud. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 96. SGMII DC Receiver Electrical Characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—	N/A			—	1
Input differential voltage	REIDL_CTL = 001xx	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	REIDL_CTL = 100xx		175	—			
Loss of signal threshold	REIDL_CTL = 001xx	V_{LOS}	30	—	100	mV	3, 4
	REIDL_CTL = 100xx		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Notes:
1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 2.19.4.4, "PCI Express DC Physical Layer Receiver Specifications," and Section 2.19.4.5.2, "PCI Express AC Physical Layer Receiver Specifications," for further explanation.
4. The REIDL_CTL shown in the table refers to the chip's SerDes control register B(1-3)GCR(lane)1[REIDL_CTL] bit field.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 97. SGMII 2.5x Receiver DC Timing Specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	900	1600	mV p-p	1

Note:
1. Measured at the receiver

2.19.9.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.19.9.2.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 98. SGMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	1
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
AC coupling capacitor	C_{TX}	10		200	nF	2

Notes:
1. See Figure 42 for single frequency sinusoidal jitter measurements.
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.19.9.2.2 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$) respectively, as depicted in this figure.

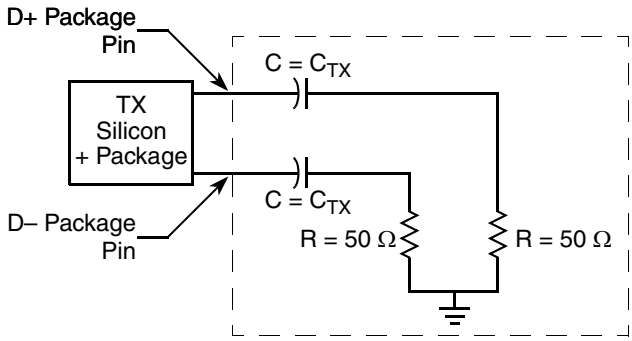


Figure 46. SGMII AC Test/Measurement Load

2.19.9.2.3 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 99. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2, 3

Table 99. SGMII Receive AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver
2. See *RapidIO® 1×/4× LP Serial Physical Layer Specification* for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 42.

3 Hardware Design Considerations

3.1 System Clocking

This section describes the PLL configuration of the chip.

This device includes 7 PLLs, as follows:

- There are two selectable core cluster PLLs, which generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 and platform can select from CC1 PLL and core complex 2–3 can select from CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3, “e500mc Core Cluster to SYSCLK PLL Ratio.” The frequency for each core complex 0–3 is selected using the configuration bits as described in Table 103.
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, “Platform to SYSCLK PLL Ratio.”
- The DDR block PLL generates the DDR clock from the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in Section 3.1.5, “DDR Controller PLL Ratios.”
- Each of the three SerDes blocks has a PLL, which generate a core clock from their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in Section 3.1.6, “Frequency Options.”

3.1.1 Clock Ranges

This table provides the clocking specifications for the processor core, platform, memory, and local bus.

Table 100. Processor Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	1200 MHz		1333 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max		
e500mc core PLL frequency	800	1200	800	1333	800	1500	MHz	1, 4
e500mc core Frequency	400	1200	400	1333	400	1500	MHz	4, 8
Platform clock Frequency	600	600	600	667	600	750	MHz	1
Memory bus clock frequency	400	600	400	667	400	667	MHz	1, 2, 5, 6
Local bus clock frequency	—	83	—	83	—	83	MHz	3
PME	—	300	—	333	—	375	MHz	7
FMan	—	500	—	541	—	583	MHz	—

Notes

1. **Caution:** The platform clock to SYSCLK ratio and e500-mc core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, e500mc (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3 memory bus clock frequency is limited to min = 400 MHz.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. Refer to the *P3041 QorIQ Integrated Multicore Communication Processor Family Reference Manual,* for more information.
4. The e500mc core can run at e500mc core complex PLL/1 or PLL/2. With a minimum core complex PLL frequency of 800 MHz, this results in a minimum allowable e500mc core frequency of 400 MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. The PME runs synchronously to the platform clock, running at a frequency of platform clock/2.
8. Core frequency must be at least as fast as the platform frequency (Rev 1.1 silicon).

3.1.2 Platform to SYSCLK PLL Ratio

The allowed platform clock to SYSCLK ratios are shown in the following table.

Note that in synchronous DDR mode, the DDR data rate is the determining factor for selecting the platform bus frequency because the platform frequency must equal to the DDR data rate.

In asynchronous DDR mode, the memory bus clock frequency is decoupled from the platform bus frequency. The platform frequency must be greater than or equal to ½ the DDR data rate.For platform clock frequency targeting 667 MHz and above, set the RCW Configuration field SYS_PLL_CFG = 0b00, and for 533–666-MHz frequencies, set SYS_PLL_CFG= 0b01.

Table 101. Platform to SYSCLK PLL Ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0100	4:1
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
0_1001	9:1
0_1010	10:1
All Others	Reserved

3.1.3 e500mc Core Cluster to SYSCLK PLL Ratio

The clock ratio between SYSCLK and each of the two core cluster PLLs is determined at power up by the binary value of the RCW field CCn_PLL_RAT. The following table describes the supported ratios. Note that a core cluster PLL frequency targeting 1 GHz and above must set RCW field CCn_PLL_CFG = 0b00 for a frequency targeting below 1 GHz set CCn_PLL_CFG = 0b01.

This table lists the supported Core Cluster to SYSCLK ratios.

Table 102. e500mc Core Cluster PLL to SYSCLK Ratios

Binary Value of CCn_PLL_RAT	Core Cluster:SYSCLK Ratio
0_1000	8:1
0_1001	9:1
0_1010	10:1
0_1011	11:1
0_1100	12:1
0_1101	13:1
0_1110	14:1
0_1111	15:1
1_0000	16:1
1_0001	17:1
1_0010	18:1
All Others	Reserved

3.1.4 e500mc Core Complex PLL Select

The clock frequency of each core 0–3 complex is determined by the binary value of the RCW field CC*n*_PLL_SEL. The following table describes the supported ratios for each core complex 0–3, where each individual core complex can select a frequency from the table.

Table 103. e500mc Core Complex [0,1] PLL Select

Binary Value of C*n*_PLL_SEL for n = [0,1]	e500mc:Core Cluster Ratio
0000	CC1 PLL /1
0001	CC1 PLL /2
0100	CC2 PLL /1
All Others	Reserved

Table 104. e500mc Core Complex [2,3] PLL Select

Binary Value of C*n*_PLL_SEL for n=[0,1]	e500mc:Core Cluster Ratio
0000	CC1 PLL /1
0100	CC2 PLL /1
0101	CC2 PLL /2
All Others	Reserved

3.1.5 DDR Controller PLL Ratios

The single DDR memory controller complexes can be synchronous with or asynchronous to the platform, depending on configuration.

The following table describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in Table 105. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

The RCW Configuration field MEM_PLL_CFG[8:9] must be set to MEM_PLL_CFG[8:9] = 0b01 if the applied DDR PLL reference clock frequency is greater than the cutoff frequency listed in Table 105 and Table 106 for asynchronous and synchronous DDR clock ratios respectively, else set MEM_PLL_CFG[8:9] = 0b00.

NOTE

- The RCW Configuration field DDR_SYNC (bit 184) must be set to 0b0 for asynchronous mode and 0b1 for synchronous mode.
- The RCW Configuration field DDR_RATE (bit 232) must be set to b’0 for asynchronous mode, and b’1 for synchronous mode.
- The RCW Configuration field DDR_RSV0 (bit 234) must be set to b’0 for all ratios.

Table 105. Asynchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:SYSCLK Ratio	Set MEM_PLL_CFG = 01 for SYSCLK Freq[1]
0_0101	5:1	>96.7 MHz
0_0110	6:1	>80.6 MHz
0_1000	8:1	>120.9 MHz
0_1001	9:1	>107.4 MHz
0_1010	10:1	>96.7 MHz

Table 105. Asynchronous DDR Clock Ratio (continued)

0_1100	12:1	>80.6 MHz
0_1101	13:1	>74.4 MHz
1_0000	16:1	>60.4 MHz
1_0010	18:1	>53.7 MHz
1_0011	19:1	>50.9 MHz
1_0100	20:1	>48.4 MHz
All Others	Reserved	—

Notes:
1. Set RCW field MEM_PLL_CFG = 0b01 if the applied DDR PLL reference clock (SYSCLK) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in Table 106. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

Table 106. Synchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:Platform CLK Ratio	Set MEM_PLL_CFG=01 for Platform CLK Freq[1]
0_0001	1:1	>600 MHz
All Others	Reserved	—

Notes:
1. Set MEM_PLL_CFG=0b01 if the applied DDR PLL reference clock (Platform clock) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.

3.1.6 Frequency Options

This section discusses interface frequency options.

3.1.6.1 SYSCLK and Platform Frequency Options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 107. SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	66.66	83.33	100.00	111.11	133.33
	Platform Frequency (MHz)[1]				
5:1					667
6:1			600	667	
7:1			700		

Table 107. SYSCLK and Platform Frequency Options (continued)

8:1		667
9:1	600	750
10:1	667	
11:1	733	

1 Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in these figures.

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 47. Gen 1 PEX Minimum Platform Frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

Figure 48. Gen 2 PEX Minimum Platform Frequency

See Section 18.1.3.2 “Link Width,” in the *P3041 QorIQ Integrated Multicore Communication Processor Family Reference Manual* for PCI Express interface width details. Note that “PCI Express link width” in the above equation refers to the negotiated link width of the single widest port used (not combined width of the number ports used) as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

Figure 49. Serial RapidIO Minimum Platform Frequency

See Section 19.4 “LP-Serial Signal Descriptions,” in the *P3041 QorIQ Integrated Multicore Communication Processor Family Reference Manual* for serial RapidIO interface width and frequency details.

3.1.7 SerDes PLL Ratio

The clock ratio between each of the three SerDes PLLs and their respective externally supplied SD_REF_CLK*n*/SD_REF_CLK*n* inputs is determined by the binary value of the RCW Configuration field SRDS_RATIO_B*n* as shown in Table 108. Furthermore, each SerDes lane grouping can be run at a SerDes PLL frequency divider determined by the binary value of the RCW field SRDS_DIV_B*n* as shown in Table 109 and Table 110.

This table lists the supported SerDes PLL Bank *n* to SD_REF_CLK*n* ratios.

Table 108. SerDes PLL Bank *n* to SD_REF_CLK*n* Ratios

Binary Value of SRDS_RATIO_B1	SRDS_PLL_*n*:SD_REF_CLK*n* Ratio		
	***n* = 1 (Bank 1)**	***n* = 2 (Bank 2)**	***n* = 3 (Bank 3)**
000	Reserved	Reserved	Reserved
001	Reserved	20:1	20:1
010	25:1	25:1	25:1
011	40:1	40:1	40:1
100	50:1	50:1	50:1
101	Reserved	Reserved	24:1
110	Reserved	Reserved	30:1
All Others	Reserved	Reserved	Reserved

These tables list the supported SerDes PLL dividers. Table 109 shows the PLL divider support for each pair of lanes on SerDes Bank 1.

Table 109. SerDes Bank 1 PLL Dividers

Binary Value of SRDS_DIV_B1[0:4]	SerDes Bank 1 PLL Divider
0b0	Divide by 1 off Bank 1 PLL
0b1	Divide by 2 off Bank 1 PLL

Notes:

1. One bit (of 5 total SRDS_DIV_B1 bits) controls each pair of lanes where first bit controls the configuration of lanes A/B (or 0/1) and last bit controls the configuration of lanes I/J (or 8/9).

This table shows the PLL dividers supported for each 4 lane group for SerDes Banks 2 and 3.

Table 110. SerDes Banks 2 and 3 PLL Dividers

Binary Value of SRDS_DIV_B*n*	SerDes Bank *n* PLL Divider
0b0	Divide by 1 off Bank *n* PLL
0b1	Divide by 2 off Bank *n* PLL

Notes:

1. One bit controls all 4 lanes of each bank.
2. n = 2 or 3 (SerDes bank 2 or bank 3)

3.1.8 Frame Manager Clock Select

Each frame managers (FMs) can be synchronous to the platform.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields FM_CLK_SEL.

Table 111. Frame Manager Clock Select

Binary Value of FM_CLK_SEL	FM Frequency
0b0	Platform Clock Frequency /2
0b1	Core Cluster 2 Frequency /2 [1]

Notes:

1. For asynchronous mode, max frequency refer to Table 100.

3.2 Supply Power Default Setting

This chip is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in this table, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

Table 112. I/O Voltage Selection

Signals	Value (Binary)	VDD Voltage Selection		
		BVDD	CVDD	LVDD
IO_VSEL[0:4] Default (0_0000)	0_0000	3.3 V	3.3 V	3.3 V
	0_0001			2.5 V
	0_0010			Reserved
	0_0011		2.5 V	3.3 V
	0_0100			2.5 V
	0_0101			Reserved
	0_0110		1.8 V	3.3 V
	0_0111			2.5 V
	0_1000			Reserved
	0_1001	2.5 V	3.3 V	3.3 V
	0_1010			2.5 V
	0_1011			Reserved
	0_1100		2.5 V	3.3 V
	0_1101			2.5 V
	0_1110			Reserved
	0_1111		1.8 V	3.3 V
	1_0000			2.5 V
	1_0001			Reserved
	1_0010	1.8 V	3.3 V	3.3 V
	1_0011			2.5 V
	1_0100			Reserved
	1_0101		2.5 V	3.3 V
	1_0110			2.5 V
	1_0111			Reserved
	1_1000		1.8 V	3.3 V
	1_1001			2.5 V
	1_1010			Reserved
	1_1011	3.3 V	3.3 V	3.3 V
	1_1100			
	1_1101			
	1_1110			
	1_1111			

3.3 Power Supply Design

3.3.1 PLL Power Supply Filtering

Each of the PLLs described in Section 3.1, "System Clocking," is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR}, and AV_{DD_SRDSn}). AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR} voltages must be derived directly from the SVDD source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 50, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to a 10-MHz range.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

The following figure shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%

C1 = 10µF ± 10%, 0603, X5R, with ESL <= 0.5 nH

C2 = 1.0 µF ± 10%, 0402, X5R, with ESL <= 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL <= 0.5 nH).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD}.

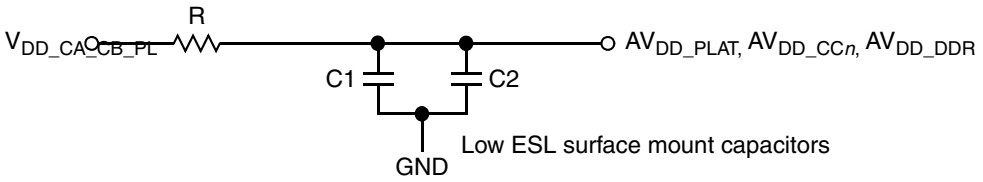


Figure 50. PLL Power Supply Filter Circuit

The AV_{DD_SRDS} signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in the following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD_SRDSn} balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide, and direct.

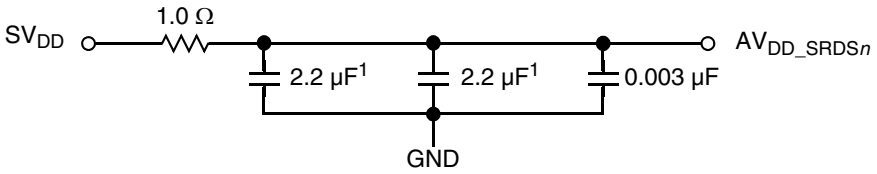


Figure 51. SerDes PLL Power Supply Filter Circuit

NOTE

- AV_{DD_SRDSn} must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Voltage for AV_{DD_SRDSn} is defined at the PLL supply filter and not the pin of AV_{DD_SRDSn}.
- An 0805 sized capacitor is recommended for system initial bring-up.

3.3.2 XV_{DD} Power Supply Filtering

XV_{DD} may be supplied by a linear regulator or sourced by a filtered GV_{DD}. Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for XV_{DD} filtering, where XV_{DD} is sourced from GV_{DD}, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 μF ± 10%, X5R, with ESL <= 0.5 nH
C2 = 2.2 μF ± 10%, X5R, with ESL <= 0.5 nH
F1 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite
F2 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

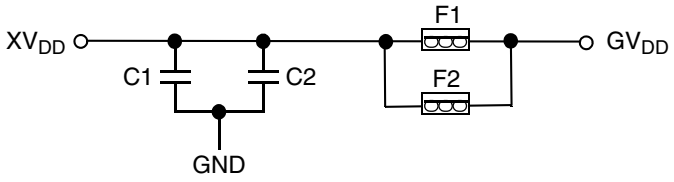


Figure 52. XV_{DD} Power Supply Filter Circuit

3.3.3 $USB\_V_{DD}\_1P0$ Power Supply Filtering

$USB\_V_{DD}\_1P0$ must be sourced by a filtered $V_{DD\_CA\_CB\_PL}$ using a star connection. An example solution for $USB\_V_{DD}\_1P0$ filtering, where $USB\_V_{DD}\_1P0$ is sourced from $V_{DD\_CA\_CB\_PL}$, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 μF ± 20%, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)
F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)
Bulk and decoupling capacitors are added, as needed, per power supply design.

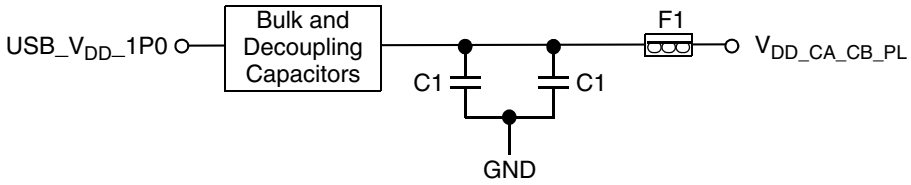


Figure 53. $USB\_V_{DD}\_1P0$ Power Supply Filter Circuit

3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

3.5 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a 1-µF ceramic chip capacitor on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

3.6 Connection Recommendations

Recommendations for proper connection are as follows:

- To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND pins of the device.
- The Ethernet controllers 1 and/or 2 input pins may be disabled by setting their respective RCW Configuration field EC1 (bits 360–361), and EC2 (bits 363–364), to 0b11 = No parallel mode Ethernet. When disabled, these inputs do not need to be externally pulled to an appropriate signal level.
- EC*n*_GTX_CLK125 is a 125-MHz input clock on the dTSEC ports. If the dTSEC ports are not used for RGMII, the EC*n*_GTX_CLK125 input can be tied off to GND.
- If RCW field DMA1 = 0b1 (RCW bit 384), the DMA1 external interface is not enabled and this pin must be left as a no connect.
- If RCW field I2C = 0b100 or 0b101 (RCW bits 355–357), the SDHC_WP and $\overline{\text{SDHC\_CD}}$ input signals are enabled for external use. If SDHC_WP and $\overline{\text{SDHC\_CD}}$ are selected and not used, they must be externally pulled low such that SDHC_WP = 0 (write enabled) and $\overline{\text{SDHC\_CD}}$ = 0 (card detected). If RCW field I2C != 0b100 or 0b101, thereby

selecting either I2C3 or GPIO functionality, SDHC_WP and SDHC_CD are internally driven such that SDHC_WP = write enabled and SDHC_CD = card detected and the selected I2C3 or GPIO external pin functionality may be used.

- TMP_DETECT pin and LP_TMP DETECT pin are active low input to the Security Monitor (see the "Secure Boot and Trust Architecture" chapter of the applicable chip reference manual). If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. 1K pull-down resistor strongly recommended. If Trust is used without tamper sensors, tie high.VDD_LP must be connected even if Low Power features are not used. Otherwise the LP_Section will generate internal errors, which will prevent the high power trust section from reaching Trusted/Secure state.

3.6.1 Legacy JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 55. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to PORESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 55 allows the COP port to independently assert PORESET or TRST, while ensuring that the target can drive PORESET as well.

The COP interface has a standard header, shown in Figure 54, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 54 is common to all known emulators.

3.6.1.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- TRST must be tied to PORESET through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (PORESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in the following figure. If this is not possible, the isolation resistor will allow future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS or TDO.

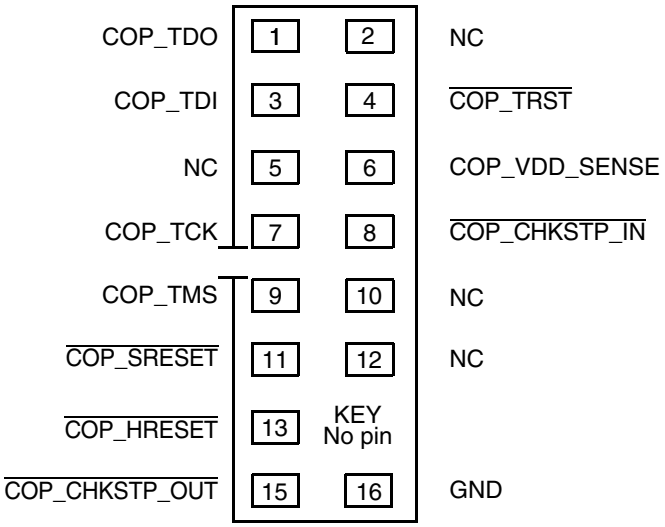
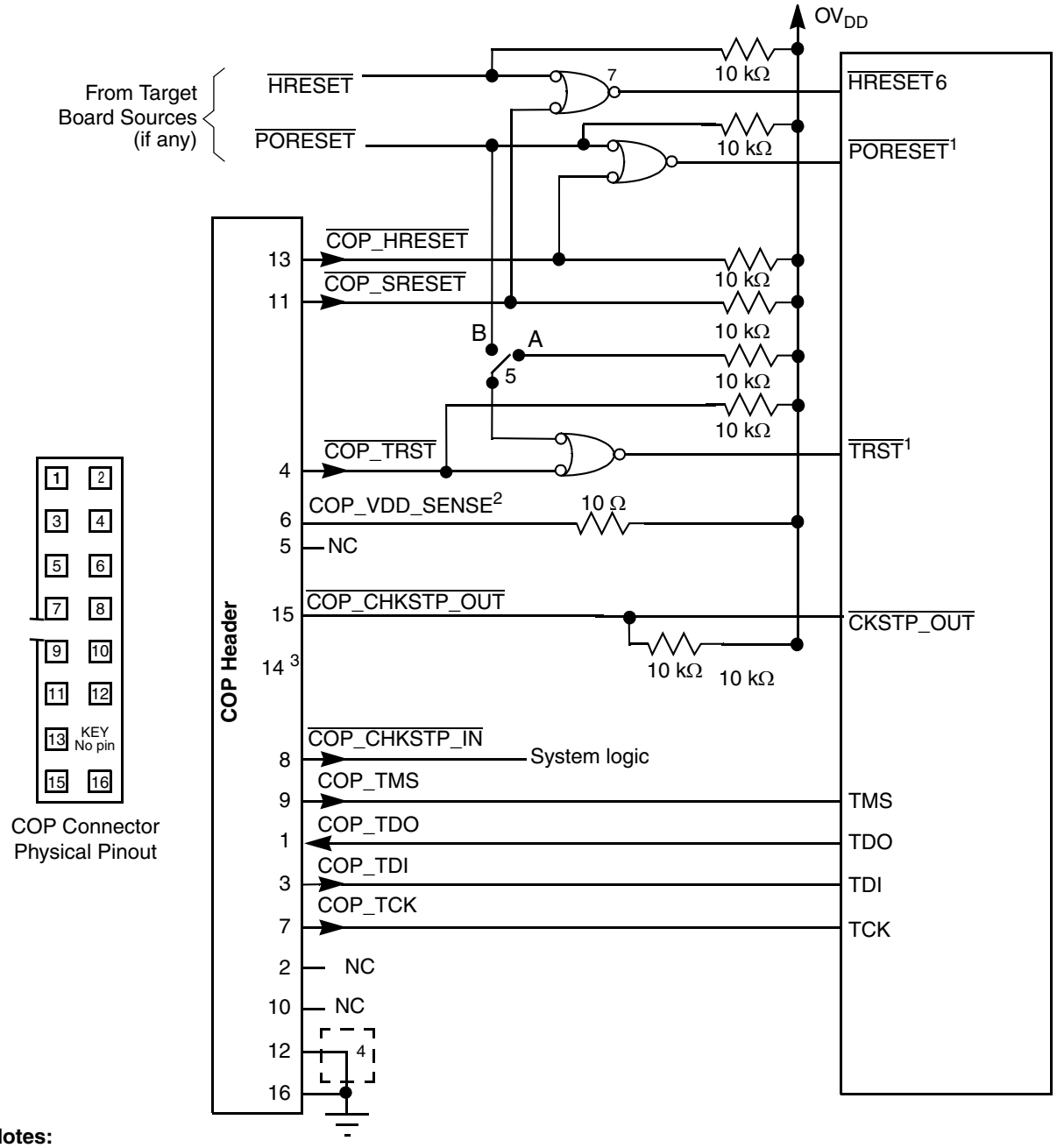


Figure 54. Legacy COP Connector Physical Pinout



Notes:

1. The COP port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
6. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.
7. This is an open-drain gate.

Figure 55. Legacy JTAG Interface Connection

3.6.2 Aurora Configuration Signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in Figure 56 and Figure 57. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Freescale recommends that the Aurora 22 pin duplex connector be designed into the system as shown in Figure 58 or the 70 pin duplex connector be designed into the system as shown in Figure 59.

If the Aurora interface is not used, Freescale recommends the legacy COP header be designed into the system as described in Section 3.6.1.1, “Termination of Unused Signals.”

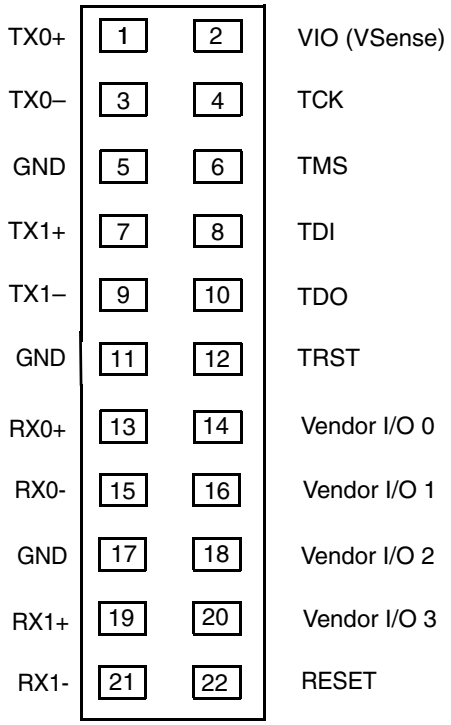


Figure 56. Aurora 22 Pin Connector Duplex Pinout

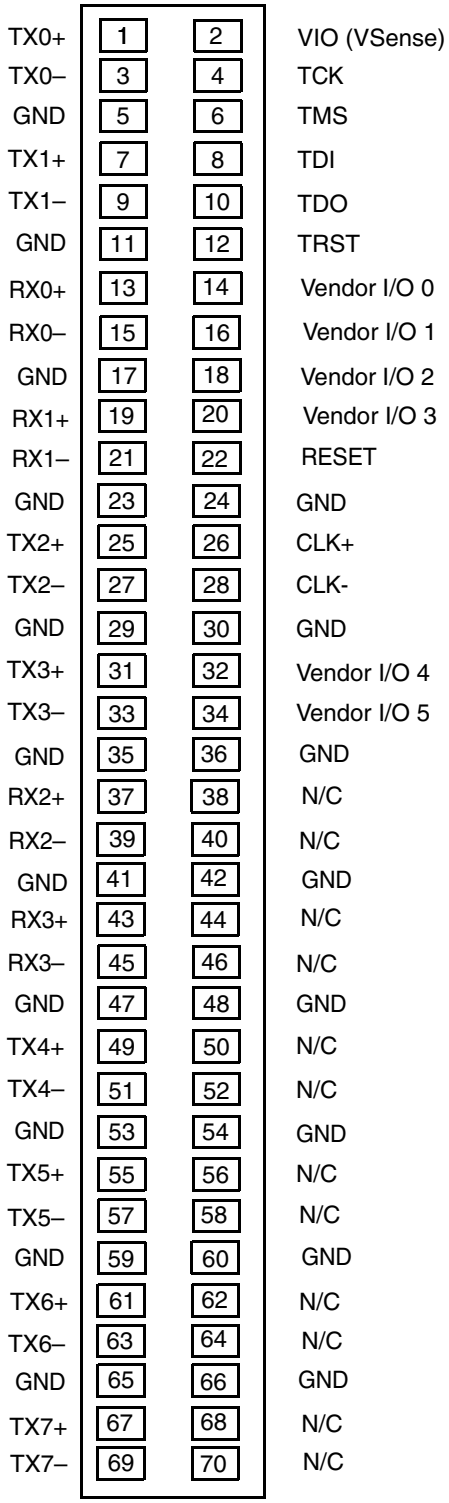
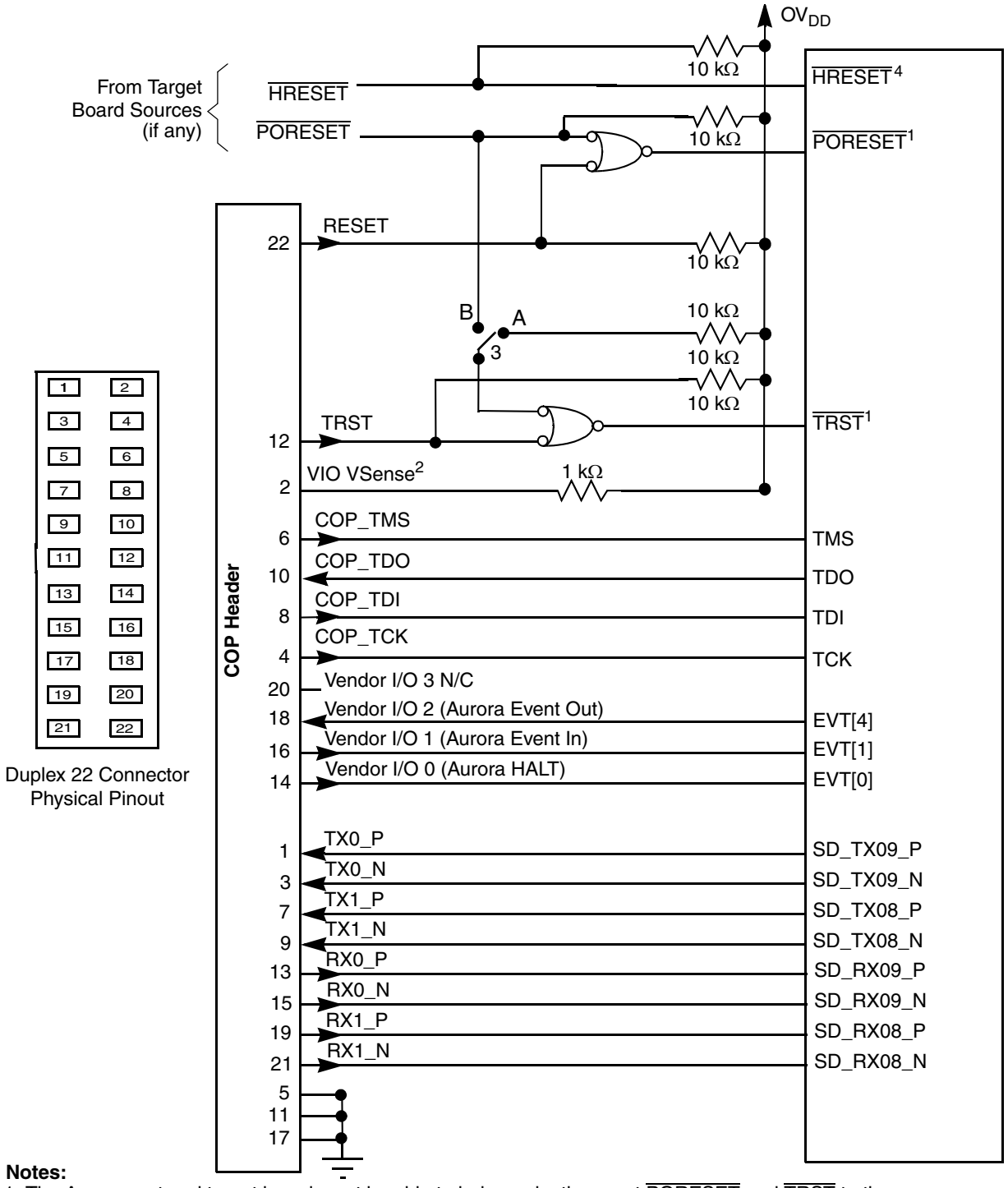


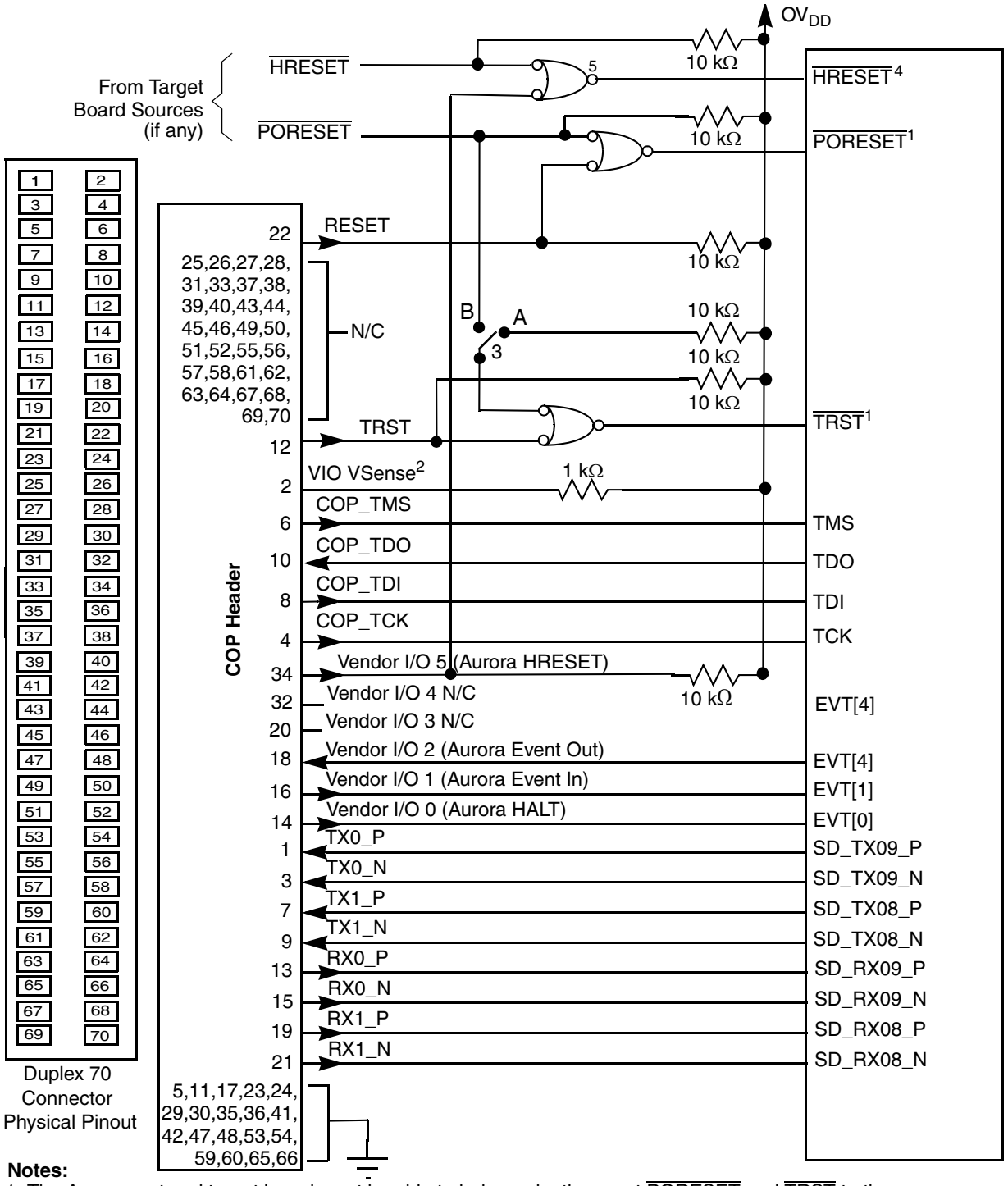
Figure 57. Aurora 70 Pin Connector Duplex Pinout



Notes:

1. The Aurora port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device. $\overline{\text{HRESET}}$ is not used by the Aurora 22 pin connector.

Figure 58. Aurora 22 Pin Connector Duplex Interface Connection



Notes:

1. The Aurora port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device. 5. This is an open-drain gate.

Figure 59. Aurora 70 Pin Connector Duplex Interface Connection

3.6.3 Guidelines for High-Speed Interface Termination

3.6.3.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[17:0]
- $\overline{\text{SD\_TX}}$[17:0]
- SD_IMP_CAL_RX
- SD_IMP_CAL_TX

The following pins must be connected to SGND:

- SD_RX[17:0]
- $\overline{\text{SD\_RX}}$[17:0]
- SD_REF_CLK1, SD_REF_CLK2, SD_REF_CLK3
- $\overline{\text{SD\_REF\_CLK1}}$, $\overline{\text{SD\_REF\_CLK2}}$, $\overline{\text{SD\_REF\_CLK3}}$

The RCW configuration fields SRDS_LPD_B1, SRDS_LPD_B2, and SRDS_LPD_B3, all bits must be set to power down all the lanes in each bank.

The RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. Setting RCW[SRDS_EN] = 0 powers down the PLLs of all three banks.

Additionally, software may configure SRDSB*n*RSTCTL[SDRD] = 1 for the unused banks to power down the SerDes bank PLLs to save power.

Note that both SV_{DD} and XV_{DD} must remain powered.

3.6.3.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following unused pins must be left unconnected:

- SD_TX[*n*]
- $\overline{\text{SD\_TX}}$[*n*]

The following unused pins must be connected to SGND:

- SD_RX[*n*]
- $\overline{\text{SD\_RX}}$[*n*]
- SD_REF_CLK1, $\overline{\text{SD\_REF\_CLK1}}$ (If entire SerDes bank 1 unused)
- SD_REF_CLK2, $\overline{\text{SD\_REF\_CLK2}}$ (If entire SerDes bank 2 unused)
- SD_REF_CLK3, $\overline{\text{SD\_REF\_CLK3}}$ (If entire SerDes bank 3 unused)

In the RCW configuration field for each bank SRDS_LPD_B*n* with unused lanes, the respective bit for each unused lane must be set to power down the lane.

3.6.4 USB Controller Connections

This section details the hardware connections required for the USB controllers.

3.6.4.1 USB Divider Network

This figure shows the required divider network for the VBUS interface for the P3041. Additional requirements for the external components are:

- Both resistors require 0.1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5 V–5.25 V.
- The 0.6 V diode requires an I_F = 10 mA, I_R < 500 nA and $V_{F(Max)}$ = 0.8 V.

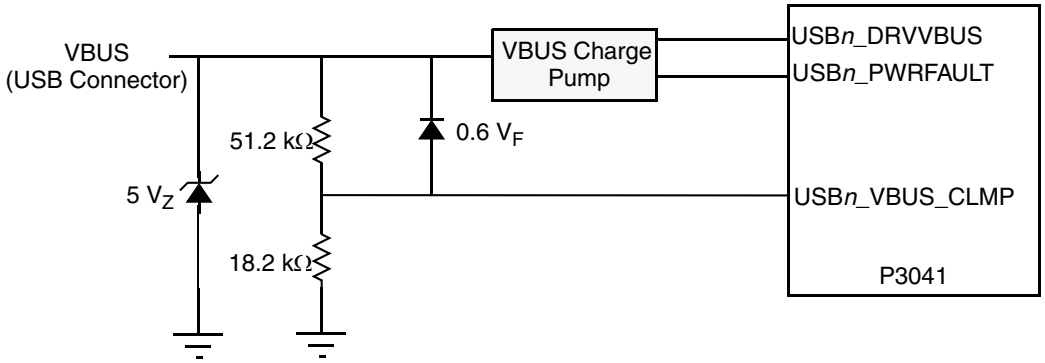


Figure 60. Divider Network at VBUS

USB1_DRVVBUS and USB1_PWRFAULT are muxed on GPIO[4:5] pins, respectively. USB2_DRVVBUS and USB2_PWRFAULT are muxed on GPIO[6:7] pins, respectively. Setting the RCW[GPIO] bit selects USB functionality on the GPIO pins.

3.6.4.2 USB*n*_V_{DD}_1P8_DECAP Capacitor Options

The USB*n*_V_{DD}_1P8_DECAP pins require a capacitor connected to GND. This table lists the recommended capacitors for the USB*n*_V_{DD}_1P8_DECAP signal.

Table 113. Recommended Capacitor Parts for USB*n*_V_{DD}_1P8_DECAP

Manufacturer	Part Number	Value	ESR	Package
Kemet	T494B105(1)025A(2)	1 μF, 25 V	2 Ω	B(3528)
	T494B155(1)025A(2)	1.5 μF, 25 V	1.5 Ω	—
NIC	NMC0603X7R106KTRPF	1 μF, 10 V	Low ESR	0603
TDK Corporation	CERB2CX5R0G105M	1 μF, 4 V	200 m-Ω	0603
Vishay	TR3B105(1)035(2)1500	1 μF, 35 V	1.5 Ω	B(3528)

3.7 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.8 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in this figure. The heat sink must be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

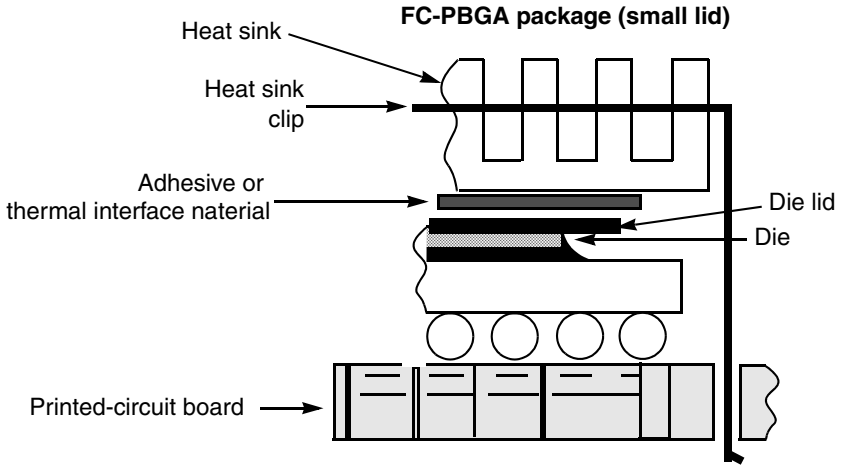


Figure 61. Package Exploded Cross-Sectional View—FC-PBGA (with Lid) Package

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.8.1 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

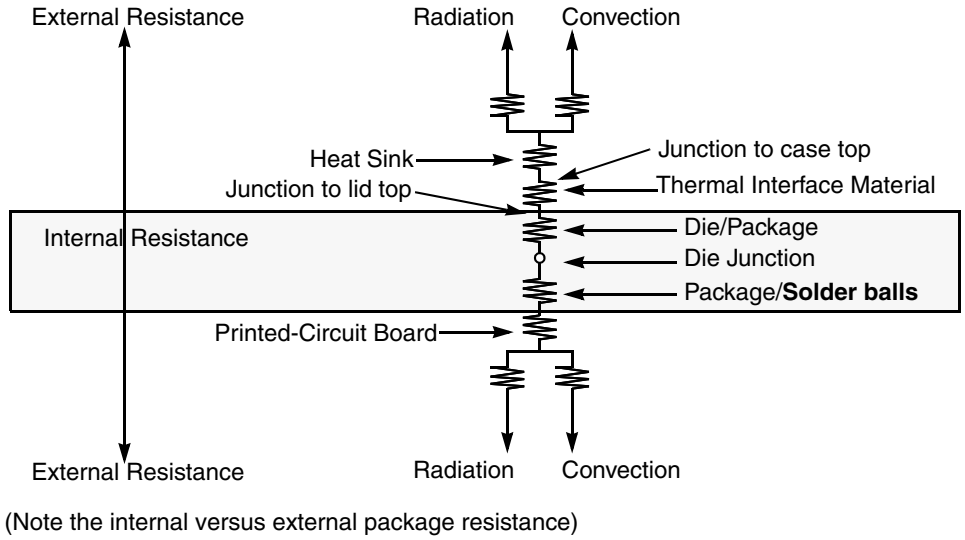


Figure 62. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.8.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 61).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.8.3 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

- Operating range: 10 – 230µA
- Ideality factor over 13.5 – 220 µA: n = 1.00592 ± 0.008

4 Package Information

The following section describes the detailed content and mechanical description of the package.

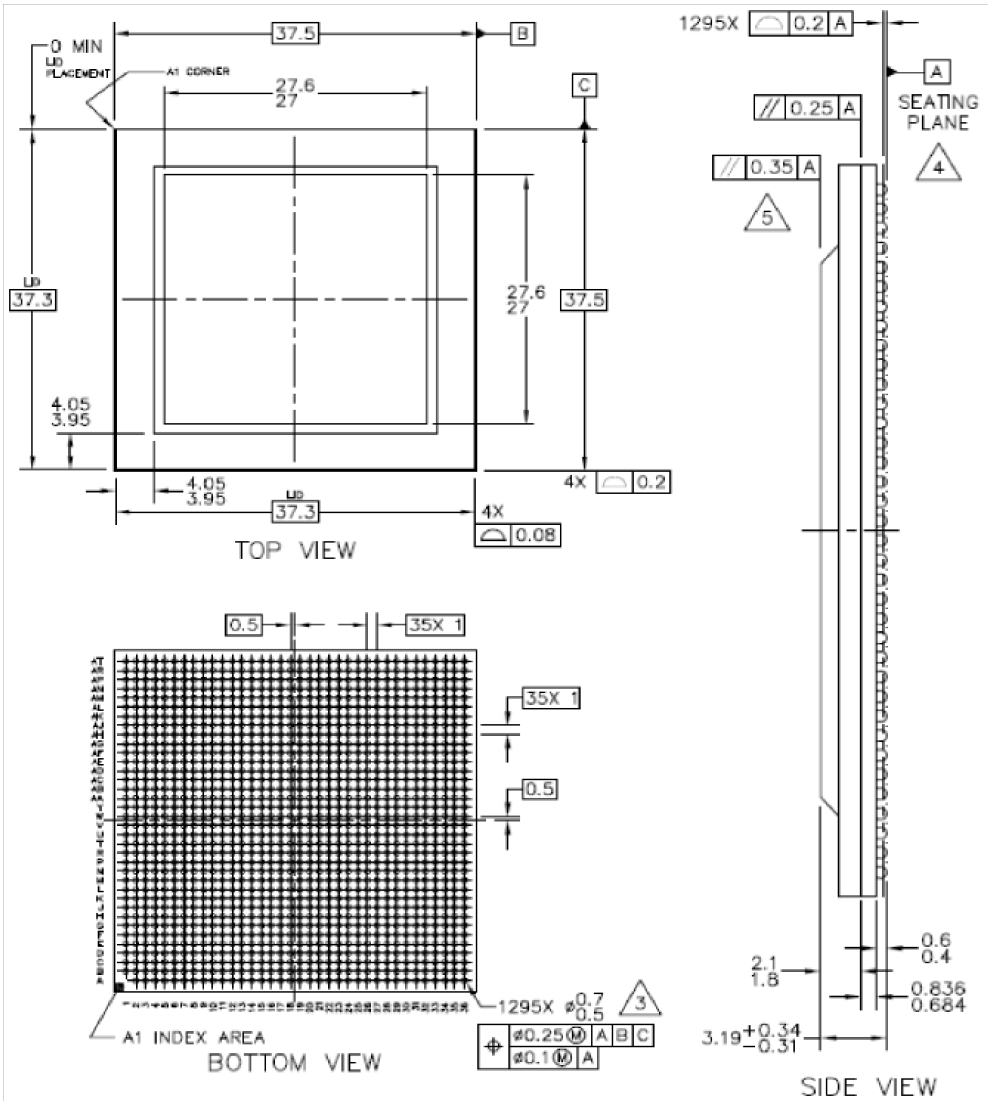
4.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 37.5 mm × 37.5 mm, 1295 flip chip plastic ball grid array (FC-PBGA).

Package outline	37.5 mm × 37.5 mm
Interconnects	1295
Ball Pitch	1.0 mm
Ball Diameter (typical)	0.60 mm
Solder Balls	96.5% Sn, 3% Ag, 0.5% Cu
Module height (typical)	2.88 mm to 3.53 mm (Maximum)

4.2 Mechanical Dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.



NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

6. Parallelism measurement excludes any effect of mark on the top surface of package.

Figure 63. Mechanical Dimensions of the FC-PBGA with Full Lid

5 Security Fuse Processor

This chip implements the QorIQ platform's trust architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per Section 2.2, "Power-Up Sequencing." POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times POV_{DD} must be connected to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering Information

Please contact your local Freescale sales office or regional marketing team for ordering information.

6.1 Part Numbering Nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature.Not all possible combinations of part numbers implied by the part numbering scheme are supported. For a list of available part numbers, please contact your Freescale Sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 114. Part Numbering Nomenclature

p	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temperature Range**	**Encryption**	**Package Type**	**CPU Freq**	**DDR Data Rate**	**Die Revision**
P = 45 nm	1–5	01 = 1 core 02 = 2 core 04 = 4 core	0–9	P = Prototype N = Industrial qualification	S = Std temp X= Extended temp (–40 to 105 C)	E = SEC present N = SEC not present	1 = FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	M = 1200 MHz N = 1333 MHz P = 1500 MHz	M = 1200 MT/s N = 1333 MT/s	A = Rev 1.0 B= Rev 1.1 C = Rev 2.0

6.2 Orderable Part Numbers Addressed by this Document

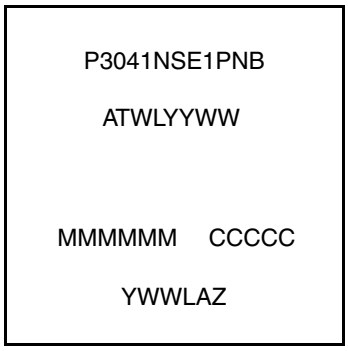
This table provides the Freescale orderable part numbers addressed by this document for the chip.

Table 115. Orderable Part Numbers Addressed by This Document

Part Number	*p*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
P3041NSE1MMB P3041NSE7MMC	P	3	04 = 4 cores	1	N = Industrial qualification	S = Std temp	E = SEC present	1 = FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free	M = 1200 MHz	M = 1200 MT/s	B C
P3041NSN1MMB P3041NSN7MMC							N = SEC not present				
P3041NSE1NNB P3041NSE7NNC							E = SEC present		N = 1333 MHz	N = 1333 MT/s	
P3041NSN1NNB P3041NSN7NNC							N = SEC not present				
P3041NSE1PNB P3041NSE7PNC							E = SEC present		P = 1500 MHz		
P3041NSN1PNB P3041NSN7PNC							N = SEC not present				
P3041NXE1MMB P3041NXE7MMC						X= Extended temp	E = SEC present		M = 1200 MHz	M = 1200 MT/s	
P3041NXN1MMB P3041NXN7MMC							N = SEC not present				
P3041NXE1NNB P3041NXE7NNC							E = SEC present		N = 1333 MHz	N = 1333 MT/s	
P3041NXN1NNB P3041NXN7NNC							N = SEC not present				
P3041NXE1PNB P3041NXE7PNC							E = SEC present		P = 1500 MHz		
P3041NXN1PNB P3041NXN7PNC							N = SEC not present				

6.2.1 Part Marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Notes:

P3041NSE1PNB is the orderable part number. See Table 115 for details.

ATWLYYWW is the test traceability code.

MMMMMM is the mask number.

CCCCC is the country code.

YWWLAZ is the assembly traceability code.

Figure 64. Part Marking for FC-PBGA Device

7 Revision history

This table provides a revision history for this document.

Table 116. Revision history

Rev. number	Date	Description
2	02/2013	• In Table 7, “P3041 I/O Power Supply Estimated Values”, updated the USB power supply with USB_Vdd_3P3 and updated the typical value with “0.003” in the Others (Reset, System Clock, JTAG & Misc.) row. • In Table 8, “AVDD Power Dissipation,” removed V_{DD_LP} from table. • Added Table 10, “VDD_LP Power Dissipation”. • In Table 55, “MPIC Input AC Timing Specifications,” added Trust inputs AC timing and footnote 2. • In Table 100, “Processor Clocking Specifications,” updated footnote 8 with Rev 1.1 silicon. • In Table 114, “Part Numbering Nomenclature,” added “C” in the Die Revision collumn. • In Table 115, “Orderable Part Numbers Addressed by This Document,” added the device part numbers for Rev 2.0 silicon.

Table 116. Revision history (continued)

Rev. number	Date	Description
1	10/2012	• In Table 1, “Pins List by Bus”, added note 27 for pin V_{DD_LP}. • Updated Table 8, “AVDD Power Dissipation.” • In Table 12, “SYSCLK DC Electrical Characteristics (OVDD = 3.3 V)”, updated the input current max value and added input capacitance max value. • In Table 53, “eSDHC AC Timing Specifications”, updated input setup times from 5 ns to 2.5 ns. • In Section 3.1.6.2, “Minimum Platform Frequency Requirements for High-Speed Interfaces”, updated the note description for “PCI Express link width”. • In Section 3.6, “Connection Recommendations”, removed the sentence “If no aspect of Trust Architecture is to be used, all Trust Architecture pins can be tied to GND.” • In Section 4.1, “Package Parameters for the FC-PBGA”, updated the solder ball composition and module height.
0	06/2012	Initial public release

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Rev. 2
02/2013

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