Shanghai Fudan Microelectronics Group Company Limited

FM25F01C

1M-BIT SERIAL FLASH MEMORY

Datasheet

Sep.2023

Trademarks

1. Description

The FM25F01C is a 1M-BIT (128K-byte) Serial Flash memory, with advanced write protection mechanisms. The FM25F01C supports the standard Serial Peripheral Interface (SPI), and a high performance Dual output as well as Dual I/O.

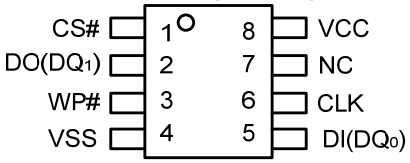
The FM25F01C can be programmed 1 to 256 bytes at a time, using the Page Program instruction. It is designed to allow either single Sector/Block at a time or full chip erase operation. The FM25F01C can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

2. Features

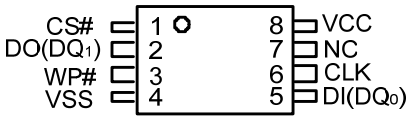
- **1Mbit of Flash memory**
  - 32 uniform sectors with 4K-byte each
  - 2 uniform blocks with 64K-byte each
  - 4 uniform blocks with 32K-byte each
  - 256 bytes per programmable page
- **Wide Operation Range**
  - 2.3V~3.6Vsingle voltage supply
  - Industrial temperature range
- **Serial Interface**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#
  - Continuous READ mode support
- **High Performance**
  - Max FAST_READ clock frequency: 100MHz
  - Max READ clock frequency: 50MHz
  - Typical page program time: 0.5ms
  - Typical sector erase time: 60ms
  - Typical block erase time: 250/400ms
  - Typical chip erase time: 1s
- **Low Power Consumption**
  - Typical standby current: <1μA
- **Flexible Architecture with 4KB sector**
  - Uniform Sector Erase(4K-bytes)
  - Uniform Block Erase(32K and 64K-bytes)
  - Program 1 to 256 bytes per programmable page
- **Security**
  - Software and hardware write protection
  - 64-Bit Unique ID for each device
- **High Reliability**
  - Endurance: 100,000 program/erase cycles
  - Data retention: 20 years
- **Green Package**
  - 8-pin SOP (150mil)
  - 8-pin TSSOP
  - 8-pin USON (2*3mm,0.55mm thickness)
  - 8-pin USON(1.5*1.5mm, 0.45mm thickness)
  - All Packages are RoHS Compliant and Halogen-free

3. Packaging Type

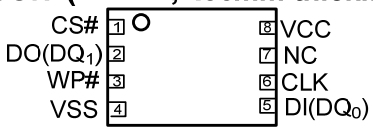
SOP8 (150mil)



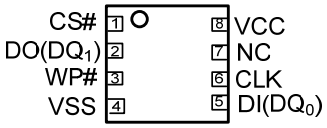
TSSOP8



USON8(2*3mm,0.55mm thickness)



USON8(1.5*1.5mm,0.45mm thickness)



4. Pin Configurations

PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO (DQ_1)	I/O	Data Output (Data Input Output 1)(1)
3	WP#	I	Write Protect Input
4	VSS		Ground
5	DI (DQ_0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	NC		No Connection
8	VCC		Power Supply

Note:
1 DQ_0 and DQ_1 are used for Dual SPI instructions.

5. Block Diagram

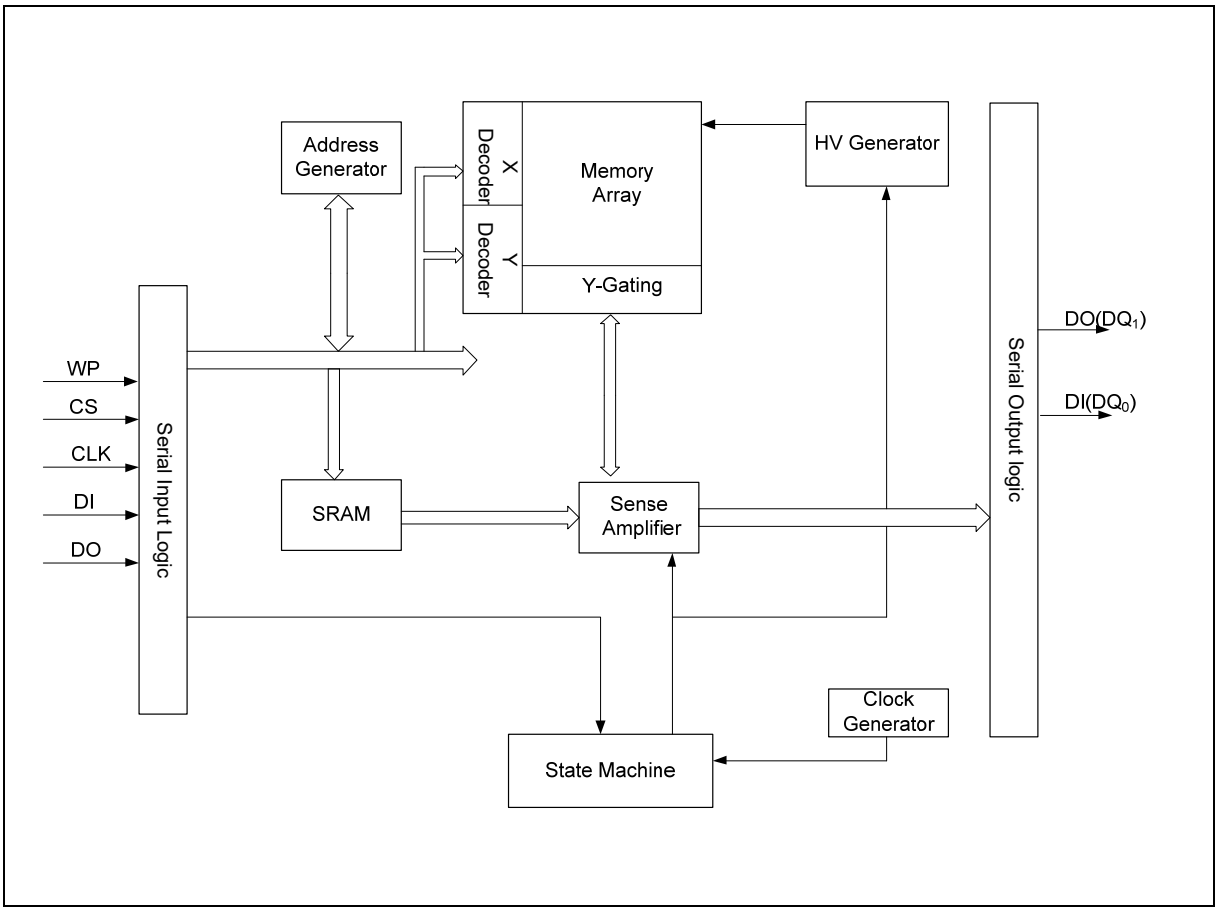


Figure 1 FM25F01C Serial Flash Memory Block Diagram

6. Pin Descriptions

Serial Clock (CLK): The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

Serial Data Input, Output and I/Os (DI, DO and DQ_0, DQ_1): The FM25F01C supports standard SPI and Dual SPIoperation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual/Quad SPI instructions use the bidirectional DQ pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Chip Select (CS#): The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted. The CS# input must track the VCC supply level at power-up (see “9Write Protection” and Figure 27). If needed a pull-up resister on CS# can be used to accomplish this.

Write Protect (WP#): The Write Protect (WP#) pin can be used to prevent the Status Registers from being written. Used in conjunction with the Status Register’s Block Protect (BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The WP# pin is active low.

7. Memory Organization

The FM25F01C array is organized into 512 programmable pages of 256-bytes each.Upto 256bytes can be programmed (bits are programmed from 1 to 0) at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The FM25F01C has 32 erasable sectors, 4 erasable 32-k byte blocks and 2 erasable 64-k byte blocks respectively. The small 4KB sectorsallowforgreater flexibility in applications that requiredata and parameter storage.

Table 1Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
1	3 | 2	31	01F000h	01FFFFh
		…	…	…
		16	010000h	010FFFh
0	1 | 0	15	00F000h	00FFFFh
		…	…	…
		2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

8. Device Operations

8.1. Standard SPI

The FM25F01C is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

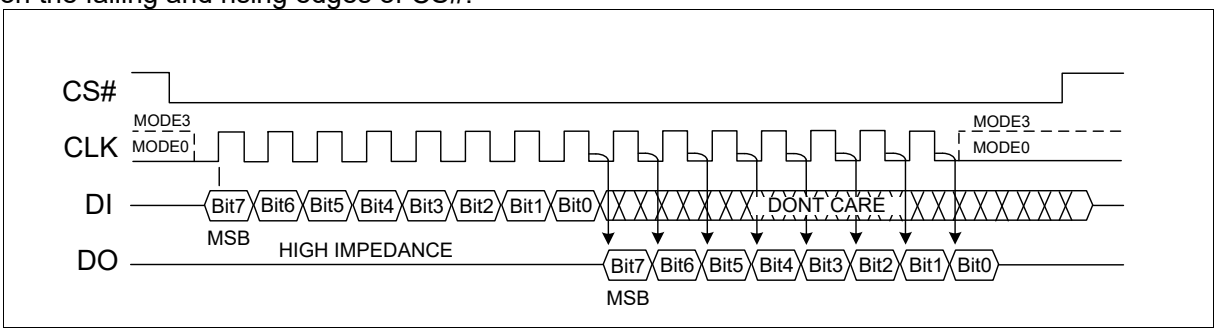


Figure 2 The difference between Mode 0 and Mode 3

8.2. Dual SPI

The FM25F01C supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

9. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the FM25F01C provides several means to protect the data from inadvertent writes.

Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up

Upon power-up or at power-down, the FM25F01C will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See "12.3Power Up/Down Timing" and Figure 27). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (CS#) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (BP2, BP1 and BP0) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

10. Status Register

The Read Status Register instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection. The Write Status Register instruction can be used to configure the device write protection features. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP), the Write Enable instruction, and the WP# pin.

Factory default for all Status Register bits are 0.

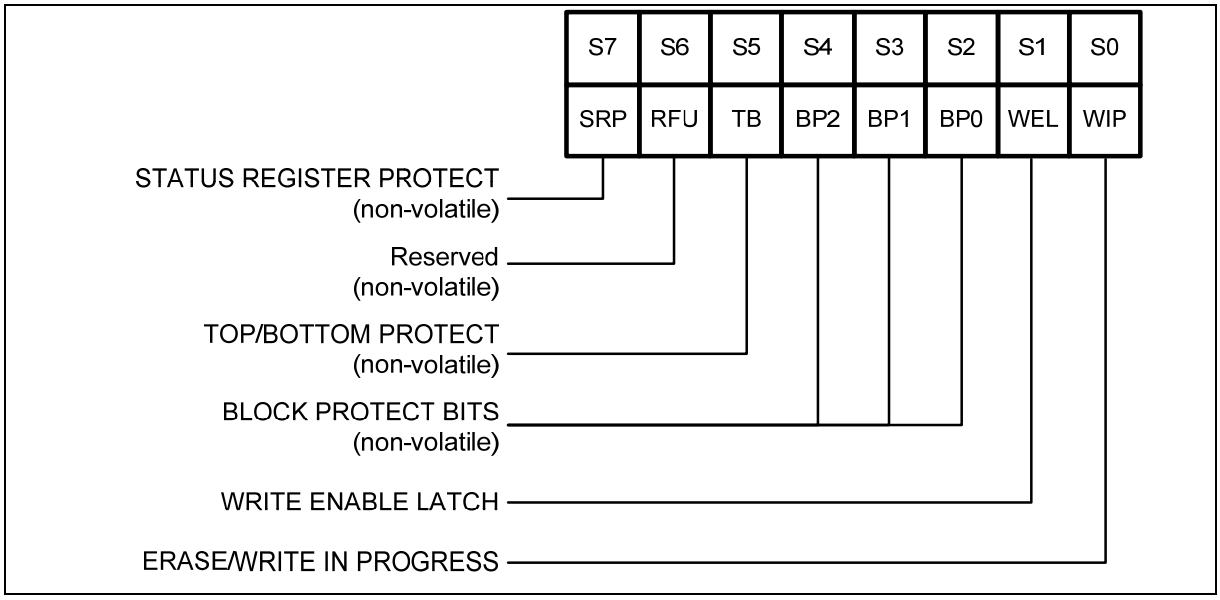


Figure 3Status Register1

10.1. WIP Bit

WIP is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Sector instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in "12.6AC Electrical Characteristics"). When the program, erase or write status register (or security sector) instruction has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

10.2. Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Sector and Program Security Sector.

10.3. Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2-0) are non-volatile read/write bits in the status register (S4-2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in "12.6AC Electrical Characteristics"). All, none or a portion of the

memory array can be protected from Program and Erase instructions (see Table 2Status Register Memory Protection). The factory default setting for the Block Protection Bits is 0, none of the array protected.

10.4. Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2-0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 2Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP and WEL bits.

10.5. Status Register Protect (SRP)

The Status Register Protect(SRP) bit operates in conjunction with Write Protect(WP#) signal. The SRP bit and WP# signal set the device to the Hardware Protected mode(When SRP bit is set to 1,and WP# is driven Low). In this mode, the non-volatile bits of the Status Register(SRP, TB, BP2, BP1, BP0) become read-only bits and the Write Status Register(WRSR) instruction is no longer accepted for execution. The default value of SRP is 0.

10.6. Status Register Memory Protection

Table 2Status Register Memory Protection

STATUS REGISTER				FM25F01C (1M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	X	0	0	NONE	NONE	NONE	NONE
0	X	0	1	1	010000h – 01FFFFh	64KB	Upper 1/2
1	X	0	1	0	000000h – 00FFFFh	64KB	Lower 1/2
X	X	1	X	0 and 1	000000h – 01FFFFh	ALL	ALL

Notes:
1. X= don’t care
2. If and Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

11. Instructions

The Standard/Dual SPI instruction set of the FM25F01C consists of 22 basic instructions that are fully controlled through the SPI bus (see Table 4 ~ Table 5). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in Figure 4 through Figure 26. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

11.1. Manufacturer and Device Identification

Table 3Manufacturer and Device Identification

OP Code	MF7-MF0	ID15-ID0	ID7-ID0
ABh			10h
90h	A1h		10h
9Fh	A1h	3111h	

11.2. Standard SPI Instructions Set

Table 4Standard SPI Instructions Set (1)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register	**05h**	(S7-S0)(2)				
Write Status Register	**01h**	S7-S0				
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**C7h/60h**					
Power-down	**B9h**					
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Release Powerdown / ID(4)	**ABh**	dummy	dummy	dummy	(ID7-ID0)(2)	
Manufacturer/Device ID(4)	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID(4)	**9Fh**	(MF7-MF0) Manufacture	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Read Unique ID(5)	**4Bh**	dummy	dummy	dummy	dummy	(UID63-UID0)
Enable Reset	**66h**					
Reset	**99h**					

11.3. Dual SPI Instructions Set

Table 5Dual SPI Instructions Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)(8)
Fast Read Dual I/O	**BBh**	A23-A8(7)	A7-A0, M7-M0 (7)	(D7-D0, …)(8)		
Manufacturer/Device ID by Dual I/O(4)	**92h**	A23-A8(7)	A7-A0, M7-M0(7)	(MF7-MF0, ID7-ID0)		

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1 or 2 DQ pins.
2. The Status Register contents and Device ID will repeat continuously until CS# terminates the instruction.
3. At least one byte of data input is required for Page Programand Program Security Sectors, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. See Table 3Manufacturer and Device Identification table for device ID information.
5. Please contact Shanghai Fudan Microelectronics Group Co., Ltd for details.
6. Security Sector Address:
   Security Sector: A23-A16 = 00h; A15-A8=10~13h; A7-A0 = byte address
7. Dual SPI address input format:
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
8. Dual SPI data output format:
   DQ_0 = (D6, D4, D2, D0)
   DQ_1 = (D7, D5, D3, D1)

11.4. Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Sectors instruction. The Write Enable **(**WREN**)** instruction is entered by driving CS# low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

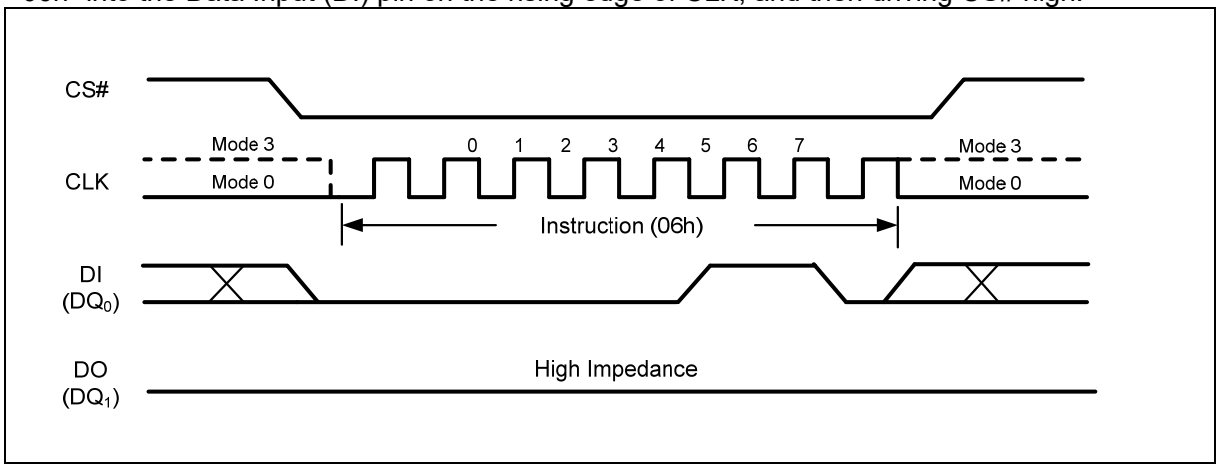


Figure 4 Write Enable Instruction

11.5. Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 10.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 5) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

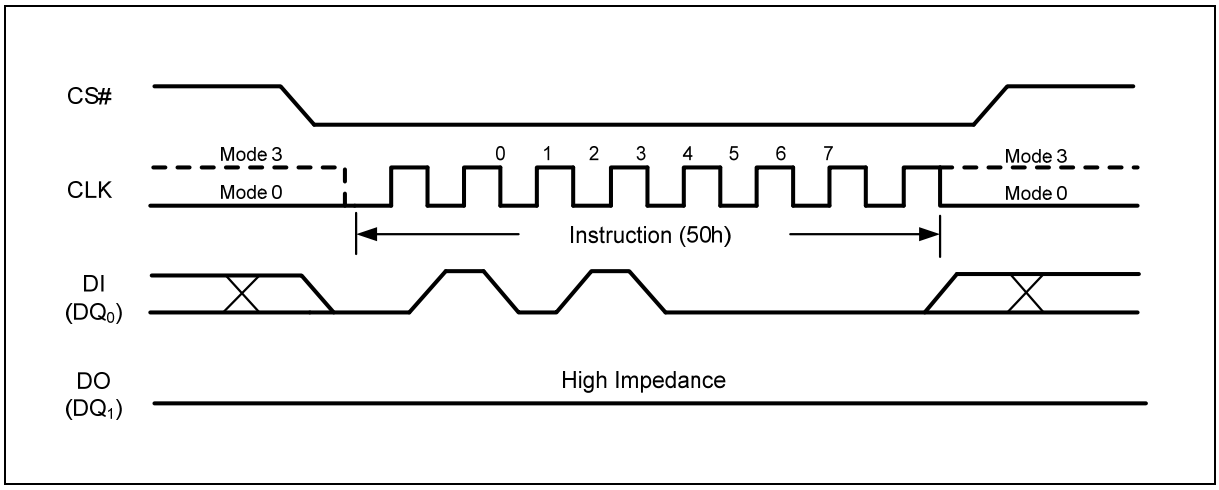


Figure 5 Write Enable for Volatile Status Register Instruction

11.6. Write Disable (WRDI) (04h)

The Write Disable (WRDI) instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable (WRDI) instruction is entered by driving CS# low, shifting the instruction code “04h” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Sectors, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

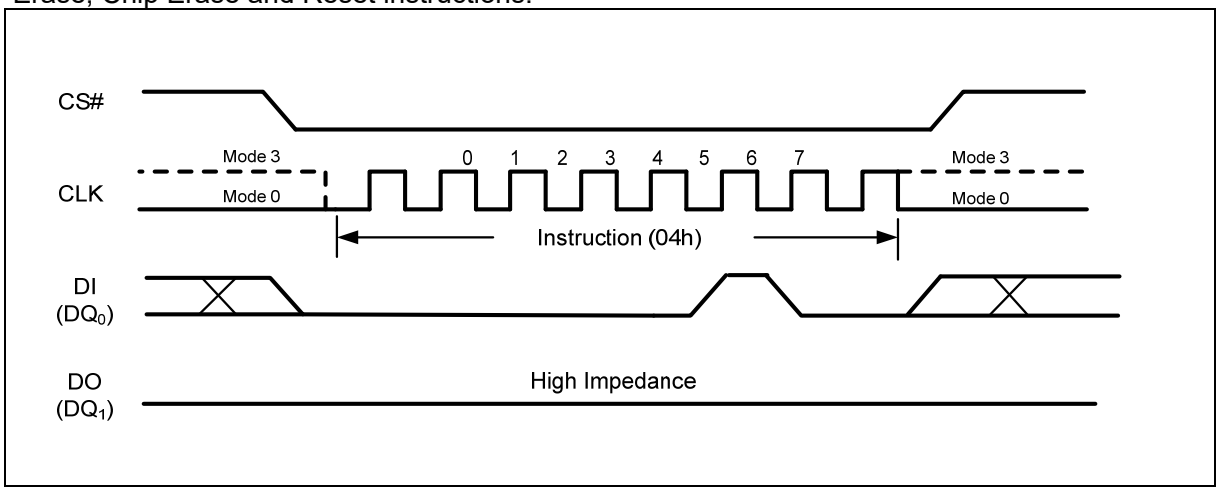


Figure 6 Write Disable Instruction

11.7. Read Status Register(RDSR) (05h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving CS# low and shifting the instruction code “05h” into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7. The Status Register bits are shown in Figure 3.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 7. The instruction is completed by driving CS# high.

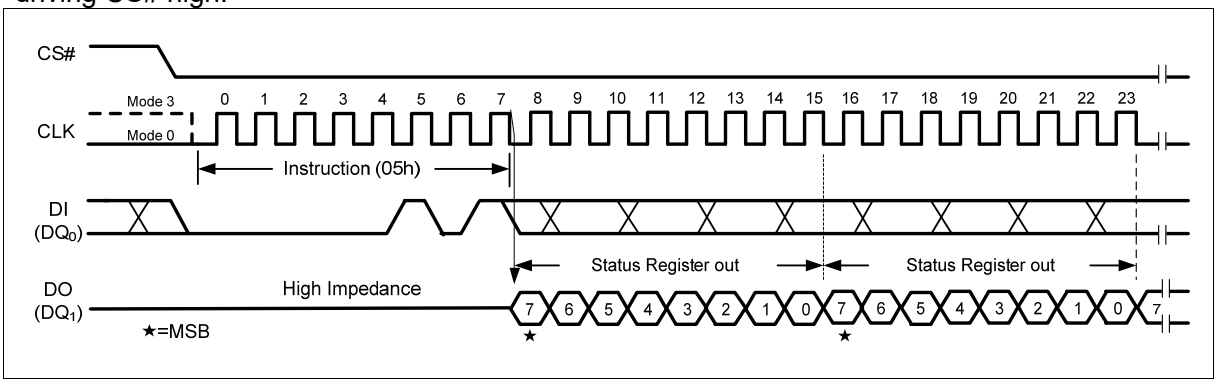


Figure 7 Read Status Register Instruction

11.8. Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows the Status Register to be written. Only non-volatile Status Register bits SRP, TB, BP2, BP1, BP0can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register (WRSR) instruction. The Status Register bits are shown in shown in Figure 3 and described in 10Status Register

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register (WRSR) instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in Figure 8.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register (WRSR) instruction (Status Register bit WEL remains 0). Upon power off or the execution of a “Reset (99h)” instruction, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

To complete the Write Status Register (WRSR) instruction, the CS# pin must be driven high after the eighth bit of data that is clocked in. If this is not done the Write Status Register (WRSR) instruction will not be executed.

During non-volatile Status Register write operation (06h combined with 01h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See “12.6AC Electrical Characteristics”). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h), after CS# is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See “12.6AC Electrical Characteristics”). WIP bit will remain 0 during the Status Register bit refresh period.

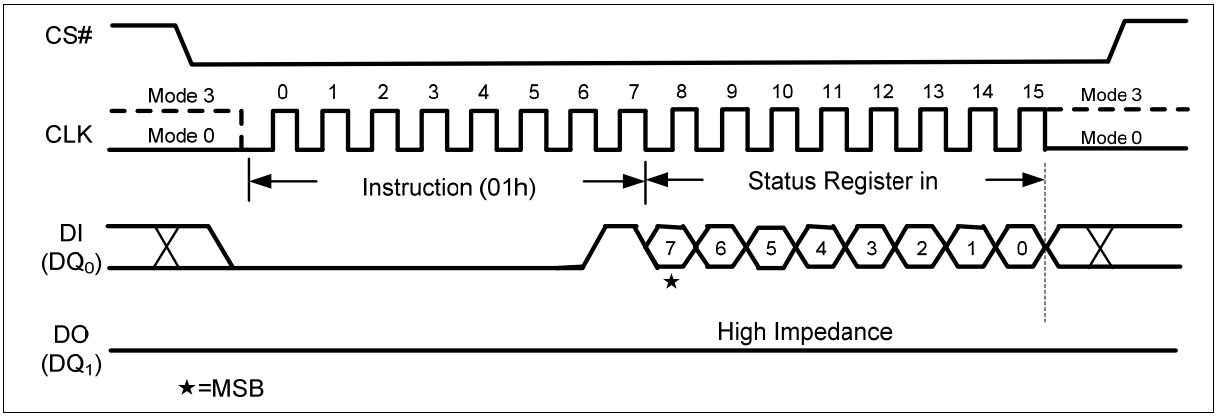


Figure 8 Write Status Register Instruction

11.9. Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address A23-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in Figure 9. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP =1) the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see “12.6AC Electrical Characteristics”).

The Read Data (03h) instruction is only supported in Standard SPI mode.

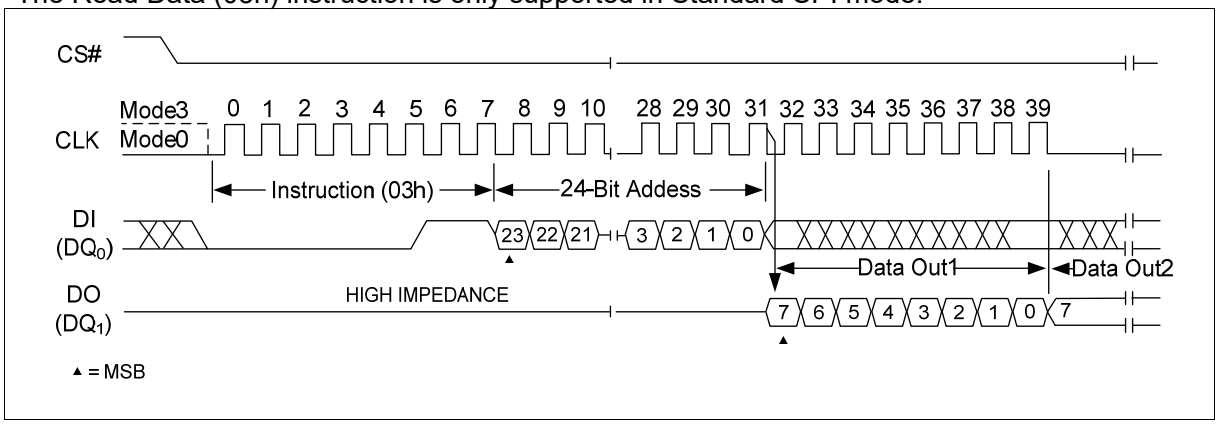


Figure 9 Read Data Instruction

11.10. Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see “12.6AC Electrical Characteristics”). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 10. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a “don’t care”.

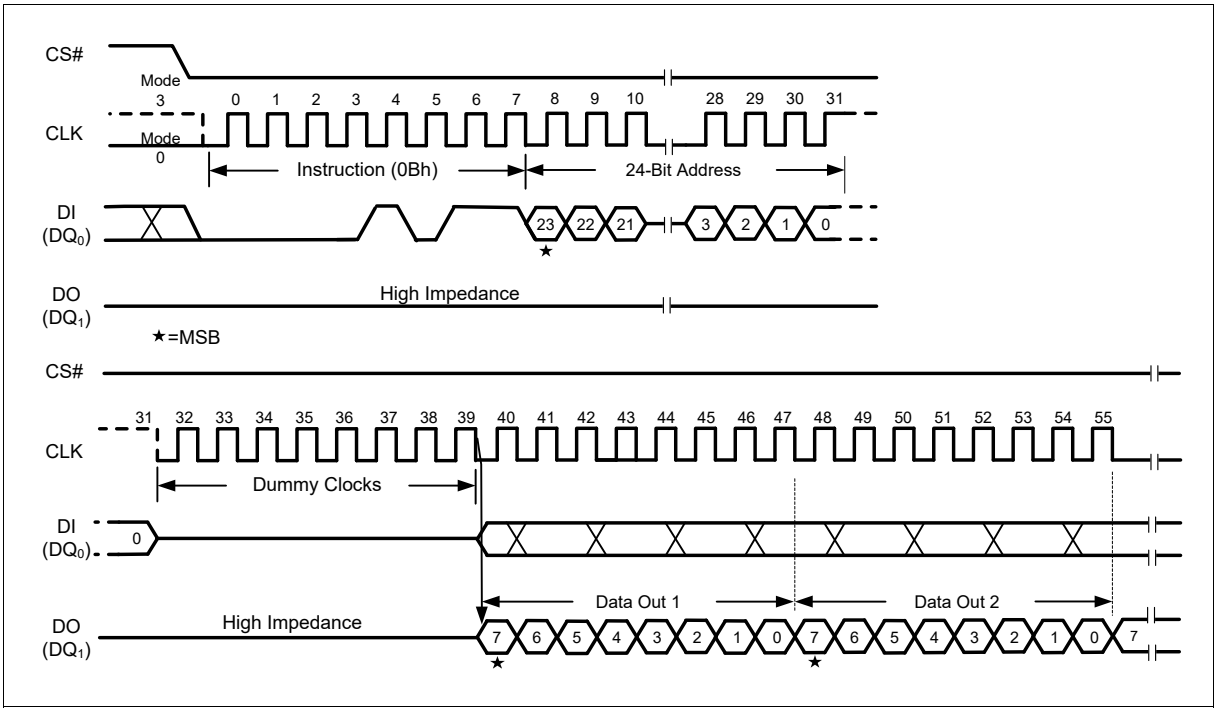


Figure 10 Fast Read Instruction

11.11. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; DQ_0 and DQ_1. This allows data to be transferred from the FM25F01C at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see “12.6AC Electrical Characteristics”). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DQ_0 pin should be high-impedance prior to the falling edge of the first data out clock.

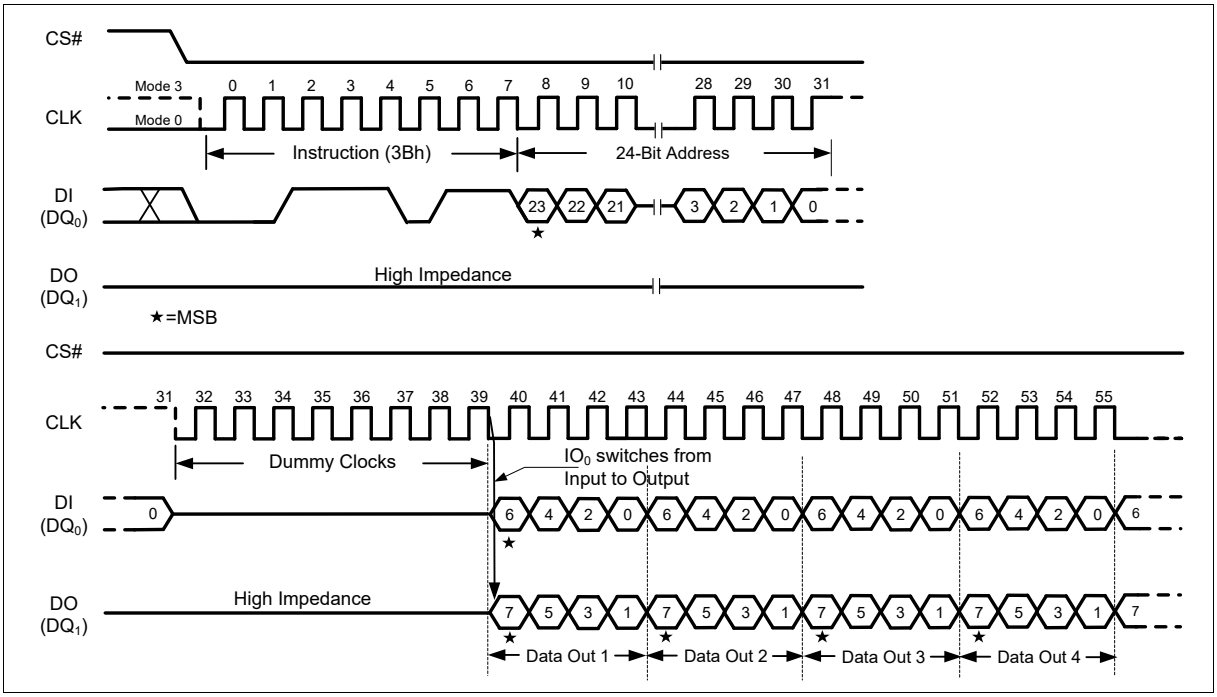


Figure 11Fast Read Dual Output Instruction

11.12. Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two I/O pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits A23-A0 two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 12. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are "don't care ("x")". However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 13. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (10), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next (8 clocks), to ensure M4 = 1 and return the device to normal operation.

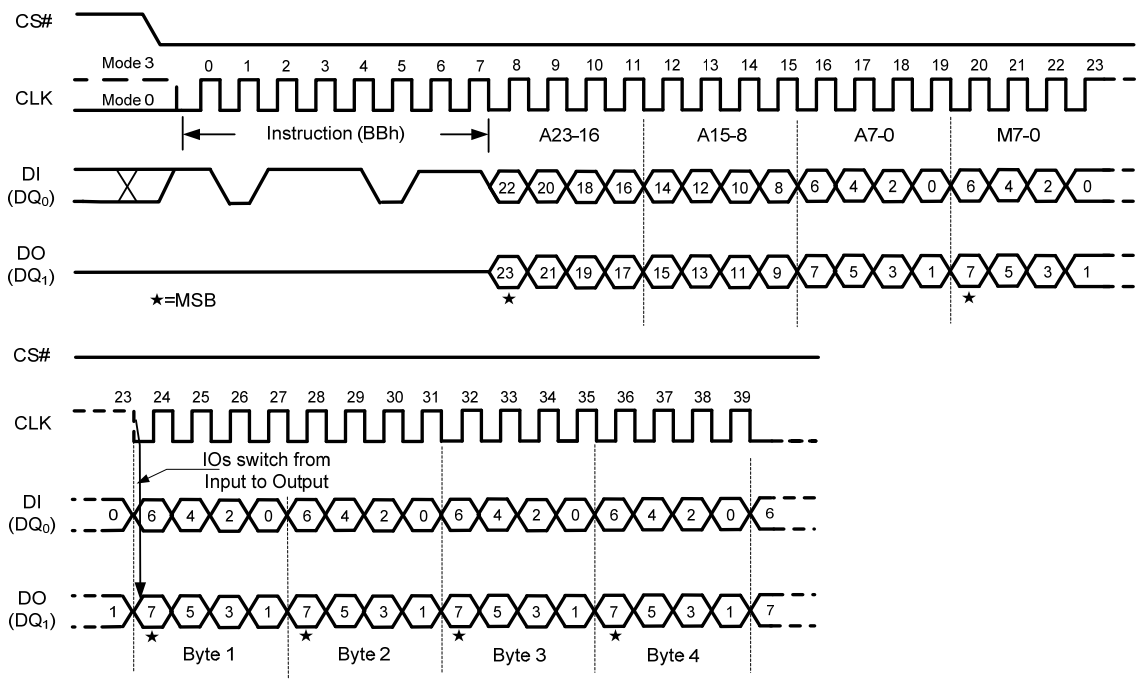


Figure 12 Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10)

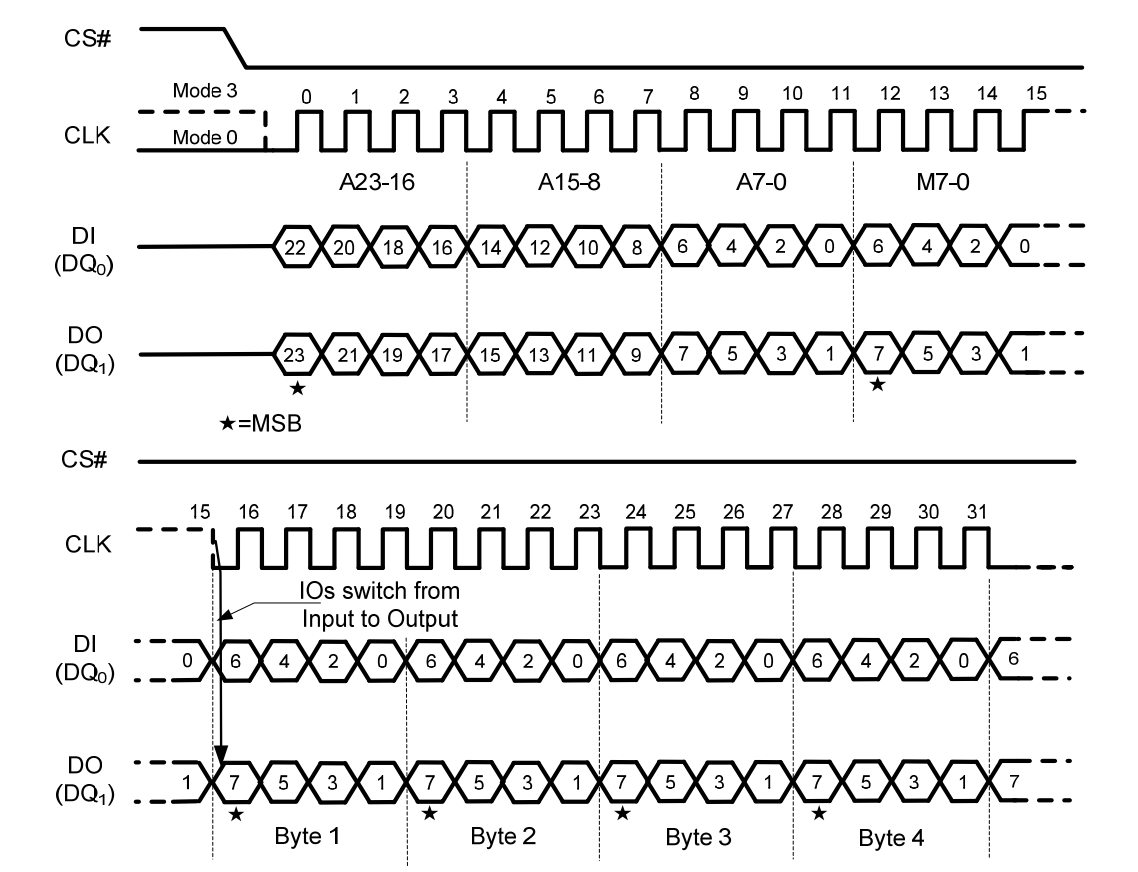


Figure 13 Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10)

11.13. Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 14.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for time duration of t_{PP} (See “12.6AC Electrical Characteristics”). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2-0) bits.

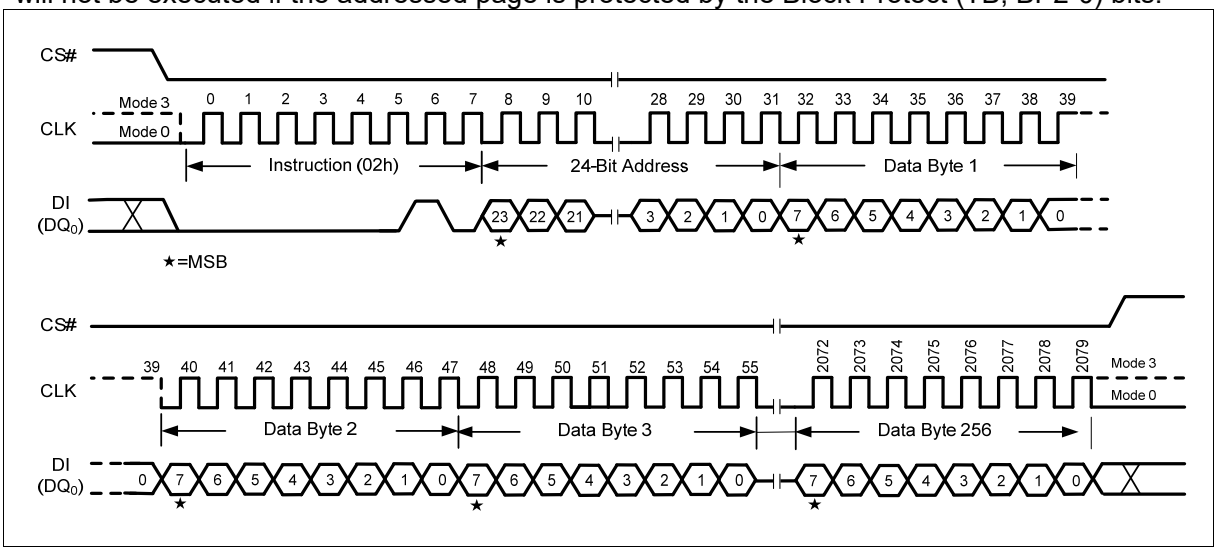


Figure 14 Page Program Instruction

11.14. Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address A23-A0. The Sector Erase instruction sequence is shown in Figure 15.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed

Sector Erase instruction will commence for a time duration of t_{SE} (See "12.6AC Electrical Characteristics"). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Table 2Status Register Memory Protection table).

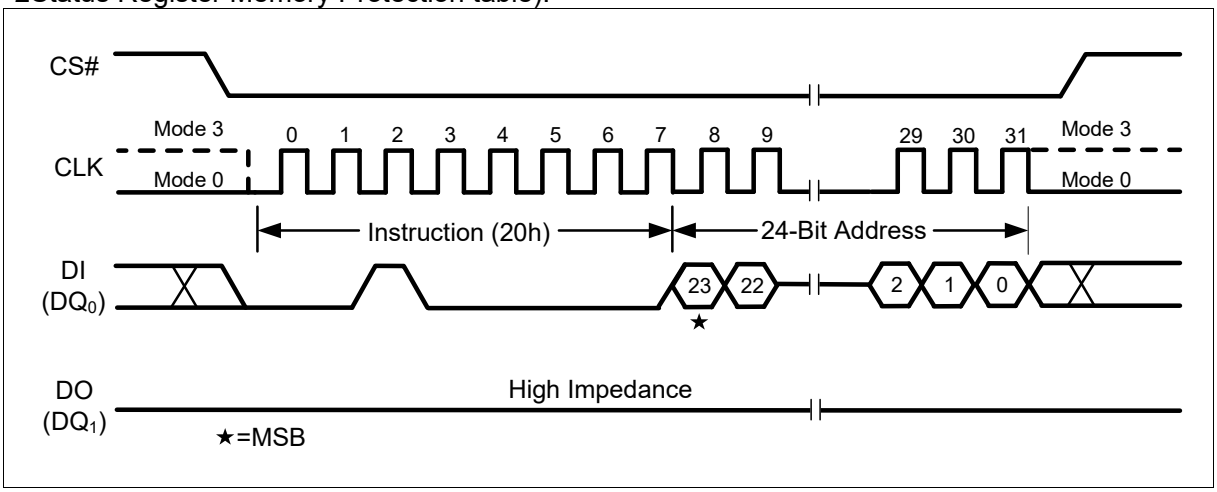


Figure 15 Sector Erase Instruction

11.15. 32KB Block Erase (BE32) (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "52h" followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 16.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for time duration of t_{BE1} (See "12.6AC Electrical Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB and BP2-0) bits (see Table 2Status Register Memory Protection table).

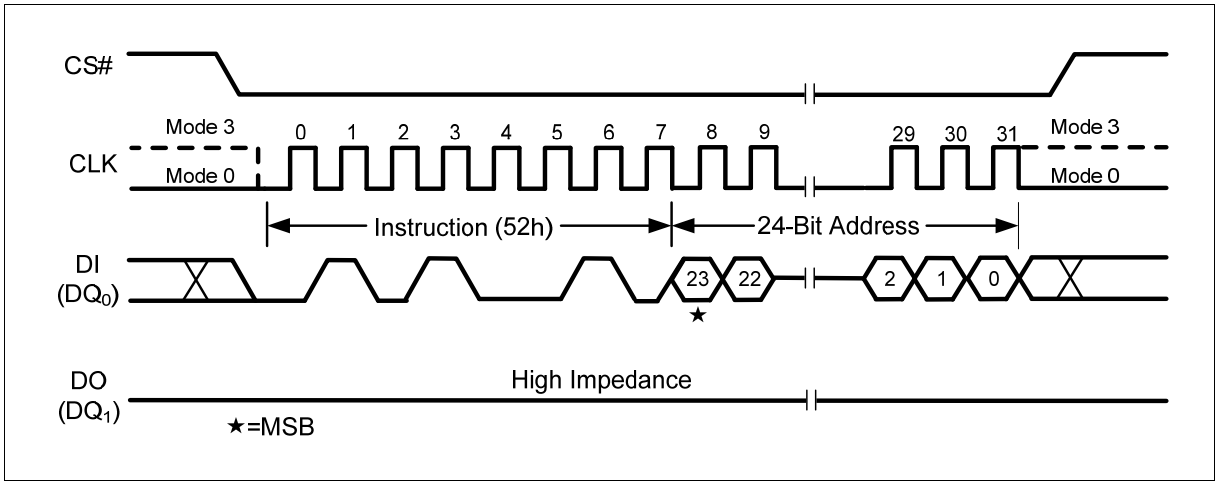


Figure 16 32KB Block Erase Instruction

11.16. 64KB Block Erase (BE) (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "D8h" followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 17.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See 12.6AC Electrical Characteristics"). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB and BP2-0) bits (see Table 2Status Register Memory Protection table).

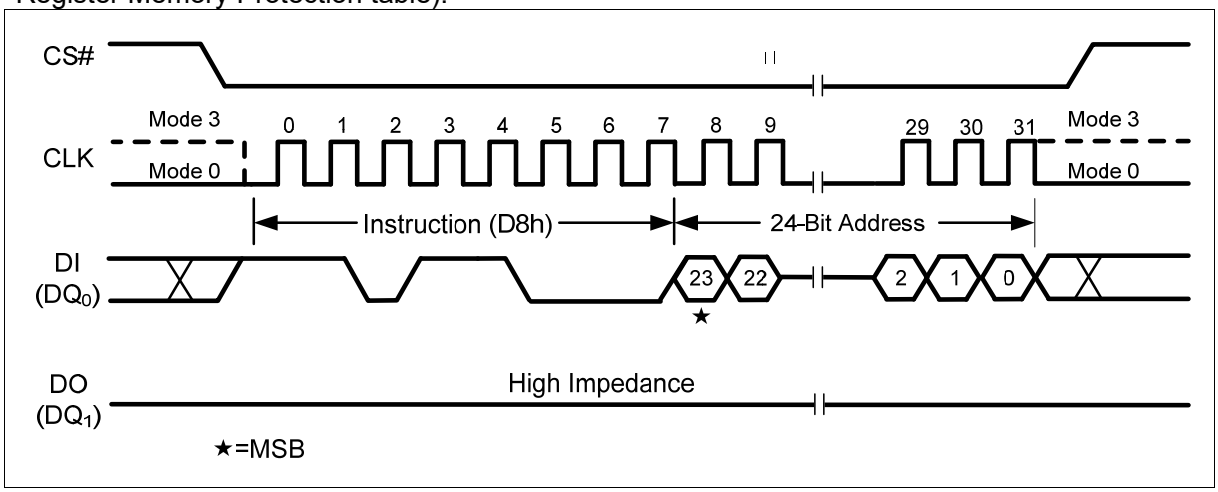


Figure 17 64KB Block Erase Instruction

11.17. Chip Erase (CE) (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 18.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for time duration of t_{CE} (See “12.6AC Electrical Characteristics”). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (TB and BP2-0) bits.

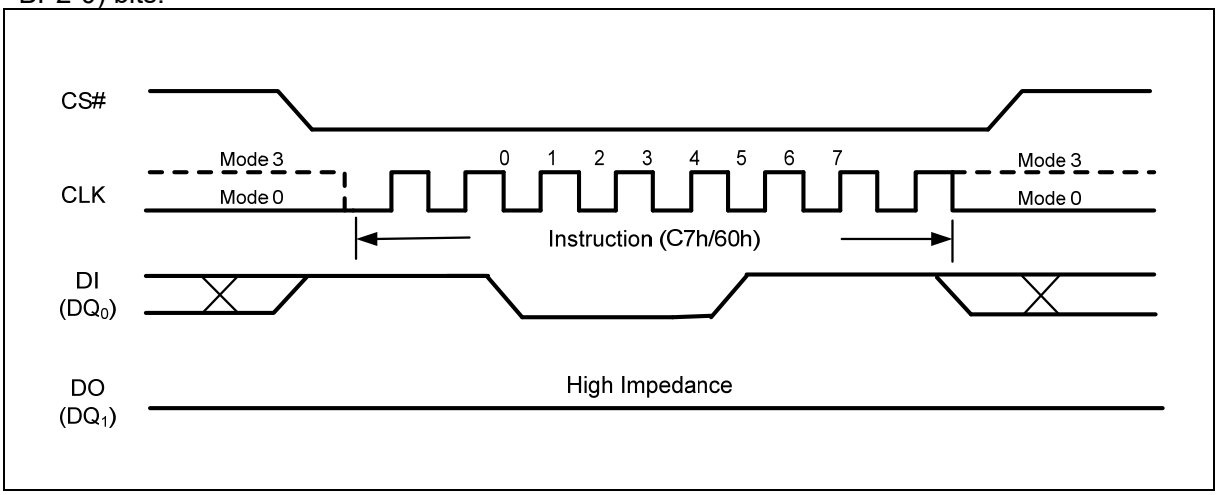


Figure 18 Chip Erase Instruction

11.18. Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See I_{CC1} and I_{CC2} in “12.4DC Electrical Characteristics”). The instruction is initiated by driving the CS# pin low and shifting the instruction code “B9h” as shown in Figure 19.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See “12.6AC Electrical Characteristics”). While in the power-down state only the Release from Power- down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

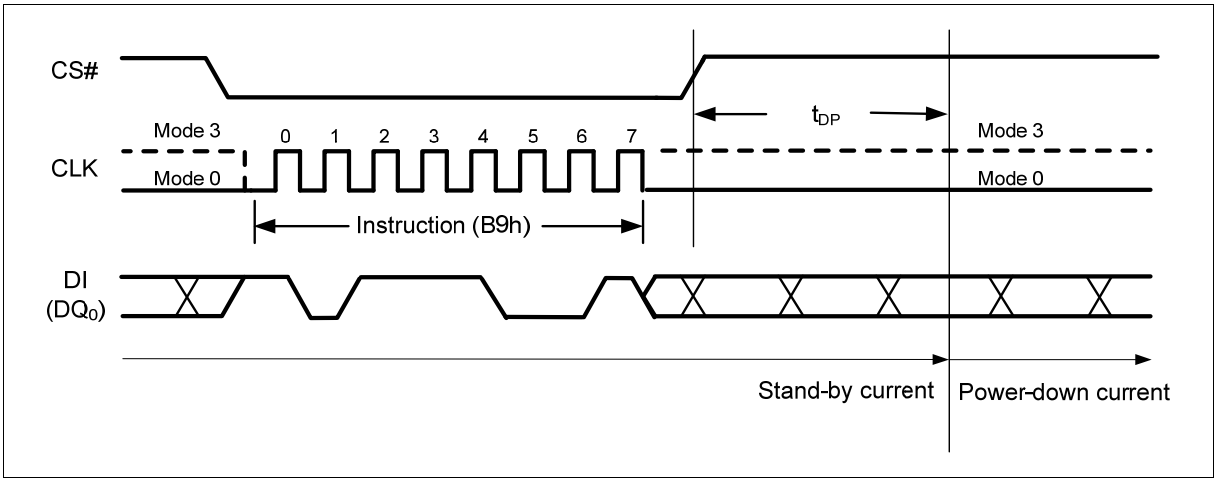


Figure 19 Deep Power-down Instruction

11.19. Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 20. Release from power-down will take the time duration of t_{RES1} (See “12.6AC Electrical Characteristics”) before the device will resume normal operation and other instructions are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown inFigure 21. The Device ID value for the FM25F01C is listed in Table 3Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 21, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See “12.6AC Electrical Characteristics”). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the instruction is ignored and will not have any effect on the current cycle.

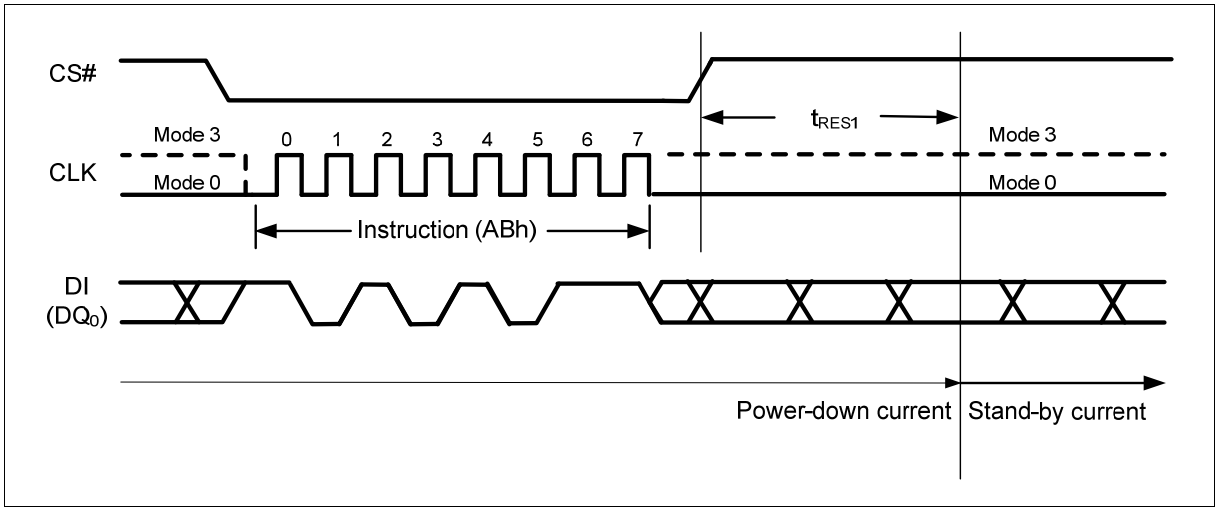


Figure 20 Release Power-down Instruction

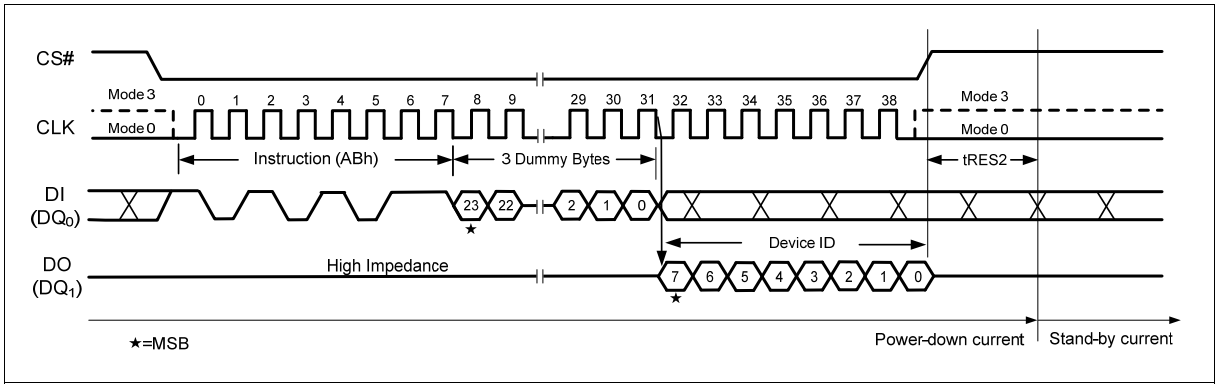


Figure 21 Release Power-down / Device ID Instruction

11.20. Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address A23-A0 of 000000h. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 22. The Device ID value for the FM25F01C is listed in Table 3Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

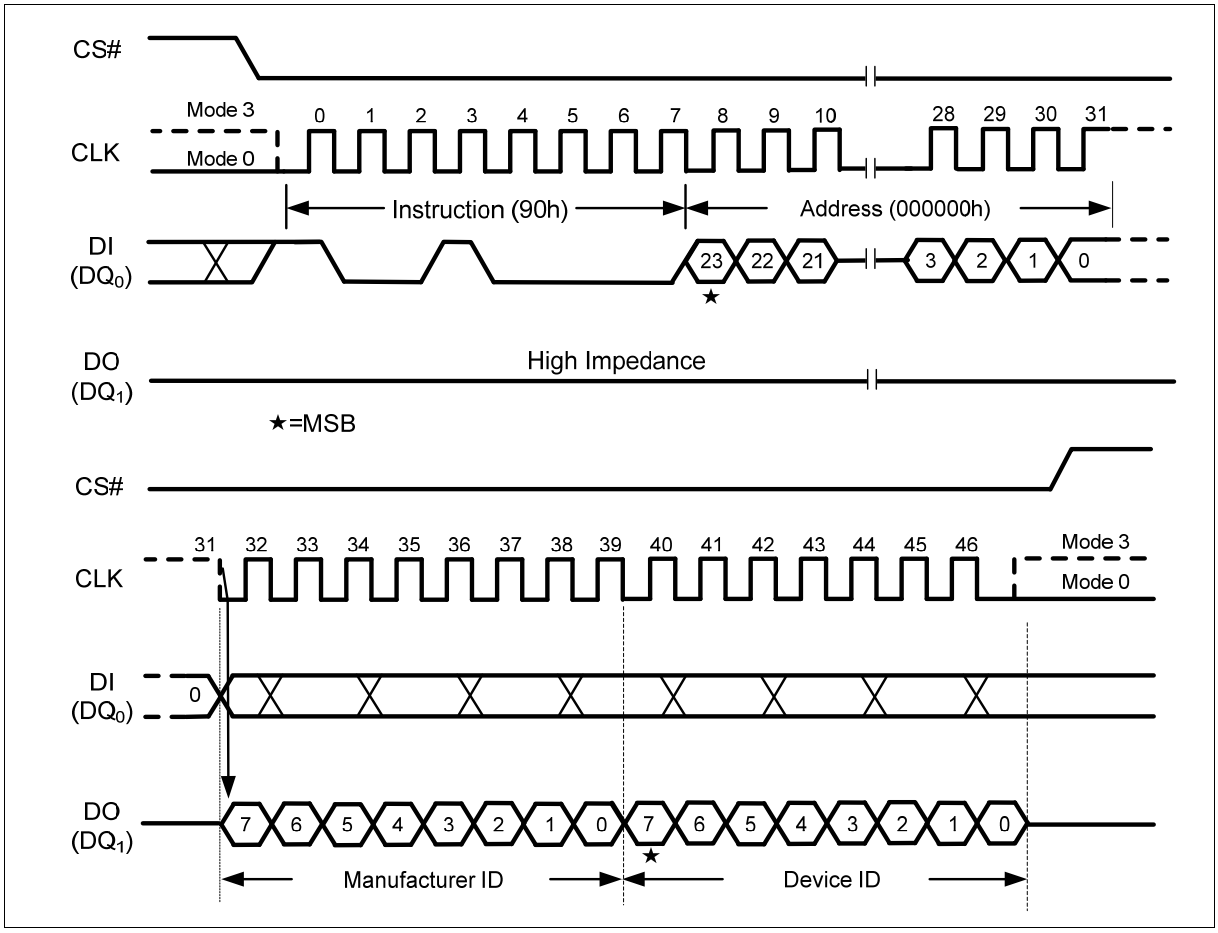


Figure 22 Read Manufacturer / Device ID Instruction

11.21. Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “92h” followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits, with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown inFigure 23. The Device ID value for the FM25F01C is listed in Table 3Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

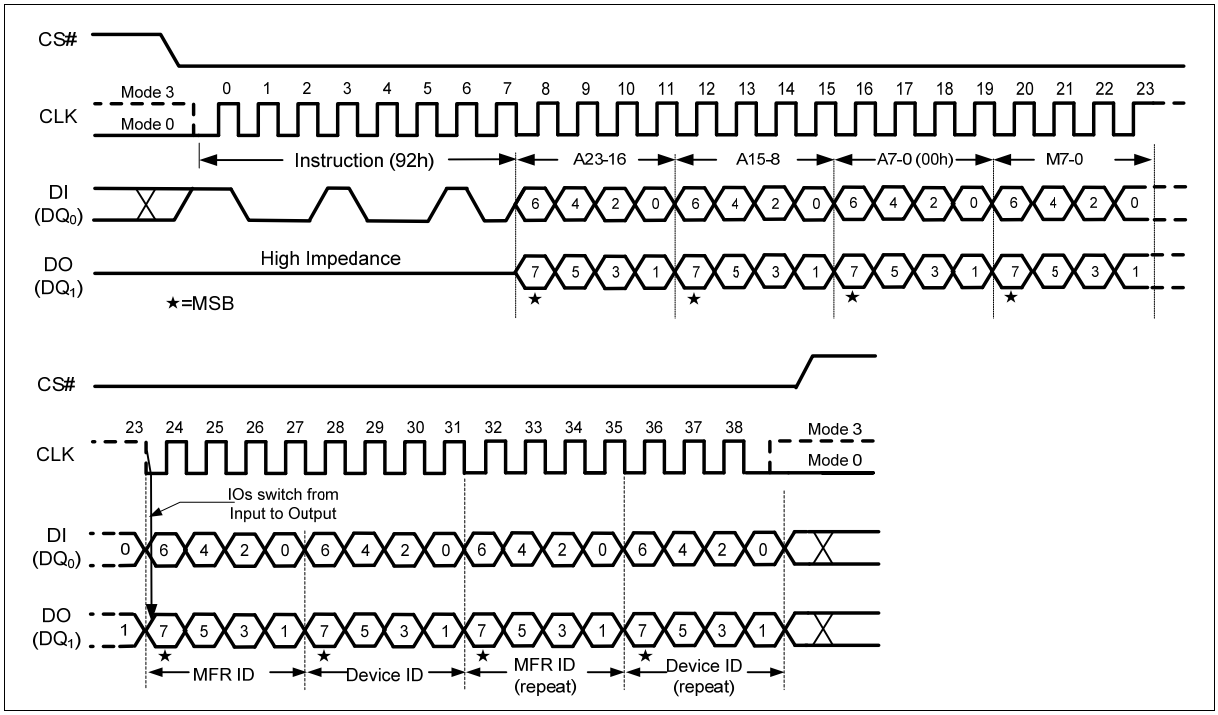


Figure 23 Read Manufacturer / Device ID Dual I/O Instruction

Note:
The “Continuous Read Mode” bits M5-M4 must be set to (1,0) to be compatible with Fast Read Dual I/O instruction.

11.22. Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each FM25F01C device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64- bit ID is shifted out on the falling edge of CLK as shown in Figure 24.

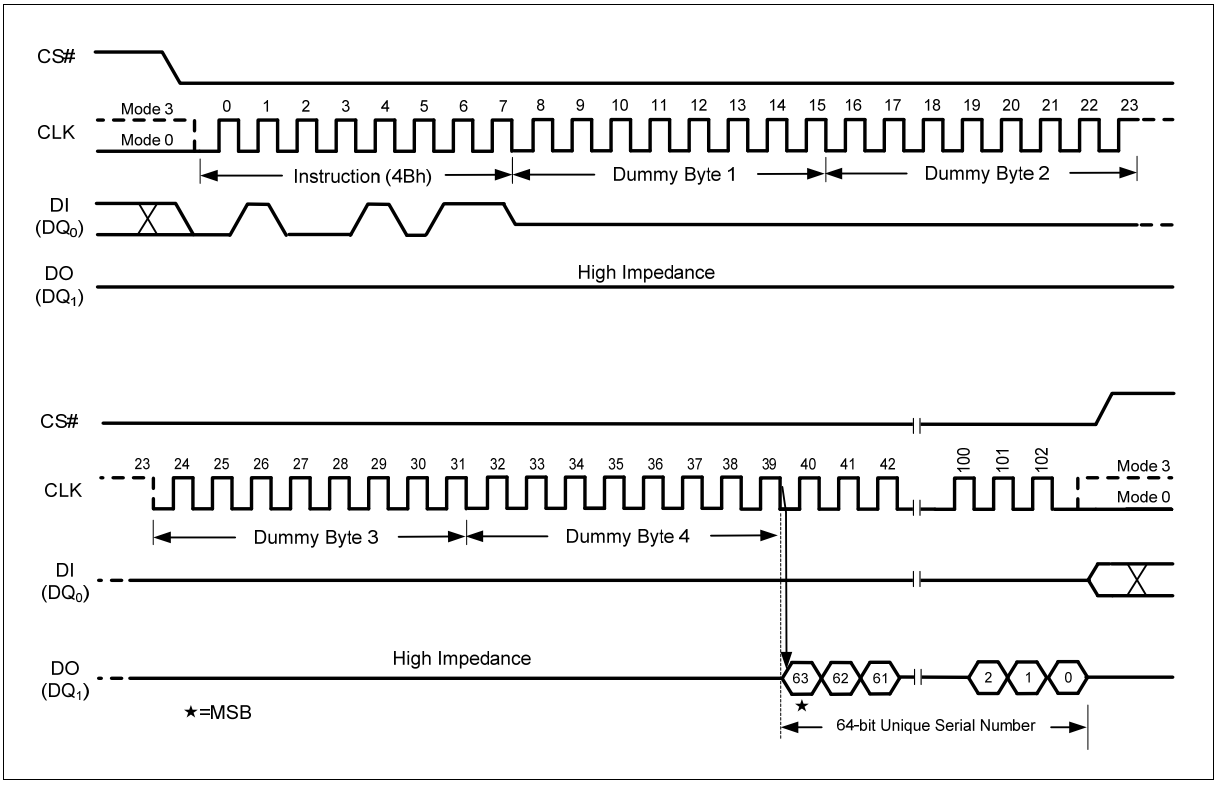


Figure 24 Read Unique ID Number Instruction

11.23. Read JEDEC ID (9Fh)

For compatibility reasons, the FM25F01C provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories. The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity ID7-ID0 are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 25. For memory type and capacity values refer to Table 3Manufacturer and Device Identification table.

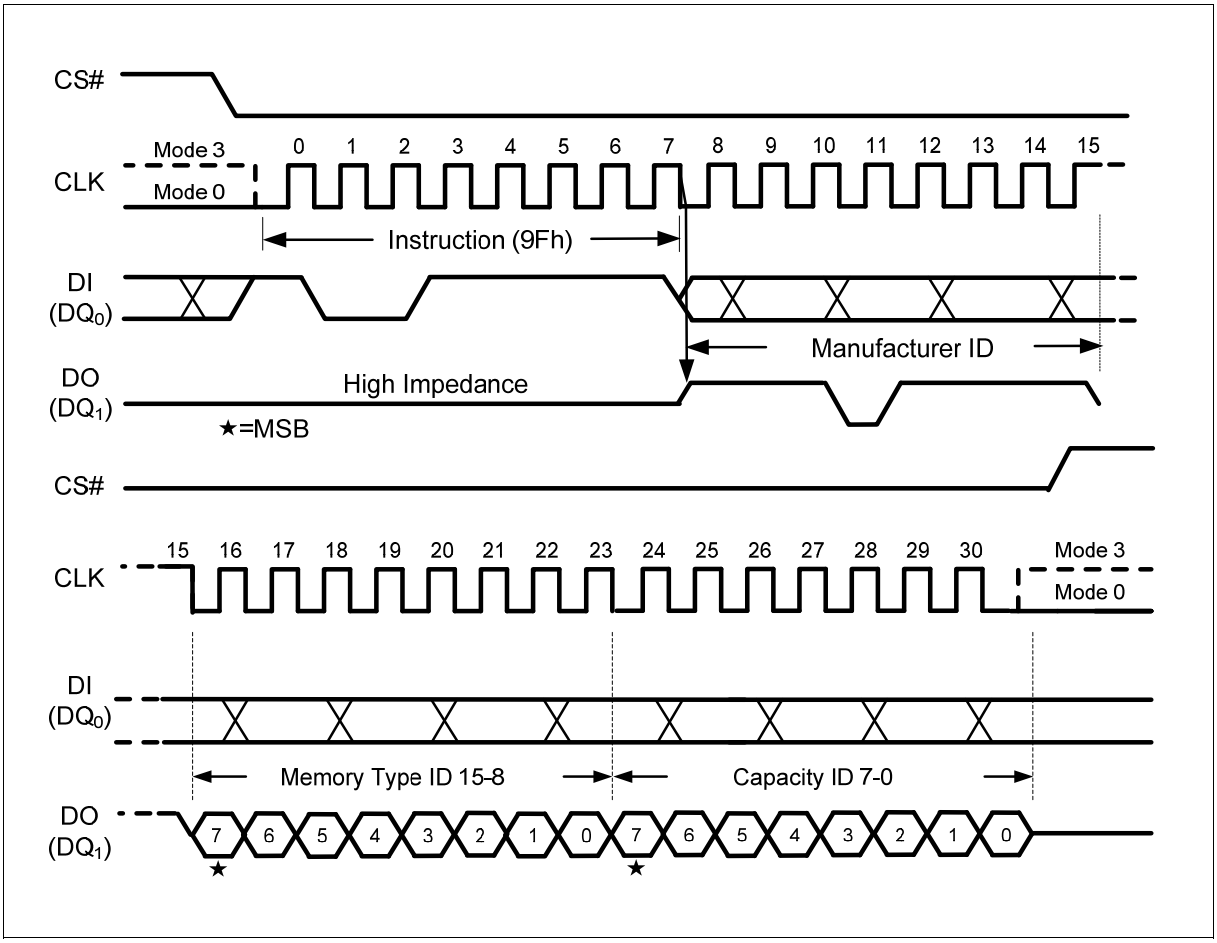


Figure 25 Read JEDEC ID Instruction (SPI Mode)

11.24. Enable Reset (66h) and Reset (99h)

Because of the small package and the limitation on the number of pins, the FM25F01C provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Continuous Read Mode bit setting M7-M0.

To avoid accidental reset, both “Enable Reset (66h)” and “Reset (99h)” instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately t_{RST} to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit in Status Register before issuing the Reset command sequence.

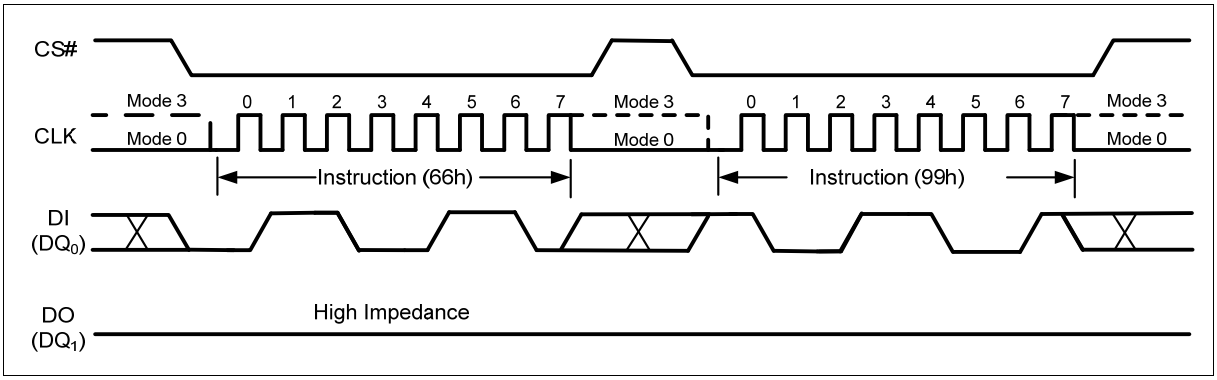


Figure 26 Enable Reset and Reset Instruction Sequence

12. Electrical Characteristics

12.1. Absolute Maximum Ratings

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on I/O Pin with Respect to Ground	-0.5V to V_{CC}+0.4V
V_{CC}	-0.5V to 4.0V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

12.2. Pin Capacitance

PARAMETER	SYMBOL	CONDITIONS	Max	Units
Input Capacitance	C_{IN}(1)	V_{IN} = 0V, f = 5 MHz	6	pF
Output Capacitance	C_{OUT}(1)	V_{OUT} = 0V, f = 5 MHz	8	pF

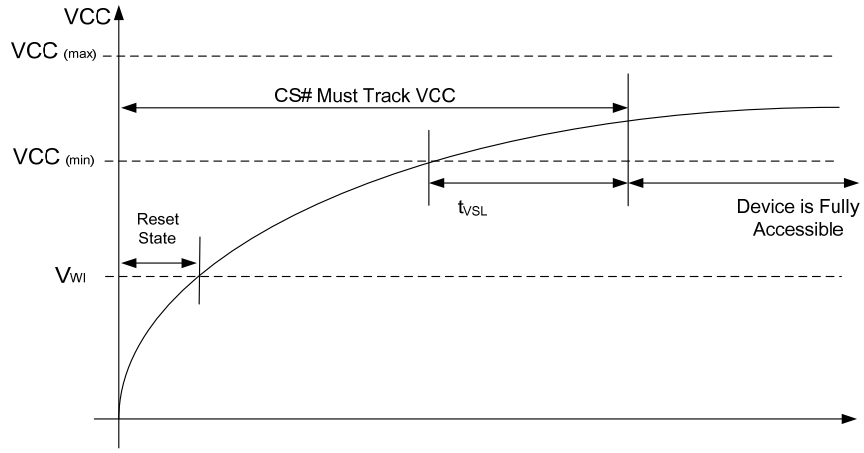
Note: 1. this parameter is characterized and not 100% tested.

12.3. Power Up/Down Timing

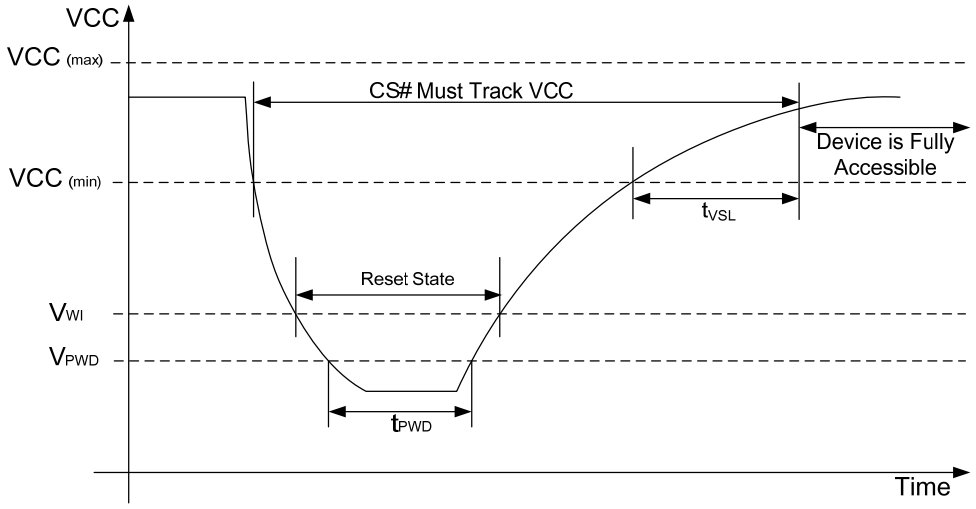
Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.3V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
t_{VSL}	VCC (min) to CS# Low	600		μs
V_{WI}	Write Inhibit Threshold Voltage	1.0	2.0	V
V_{PWD}	Power-down Reset Voltage		0.4	V
t_{PWD}	Power-down Duration Time Before Next Power Up	100		μs

Note: These parameters are characterized and not 100% tested.



Power-up Timing



Power Up/Down and Voltage Drop

Figure 27 Power-up Timing& Power Up/Down and Voltage Drop

12.4. DC Electrical Characteristics

Table 6DC Characteristics

Applicable over recommended operating range from: T_A= -40°C to 85°C, V_{CC} = 2.3V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Vcc	Supply Voltage		2.3		3.6	V
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = Vss or V_{CC}		1	5	μA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = Vss or V_{CC}		1	5	μA
I_{CC3}(1)	Read Data Current (1)	CLK=0.1V_{CC}/0.9V_{CC} at 33MHz, DQ open			15	mA
I_{CC3}(1)		CLK=0.1V_{CC}/0.9V_{CC}, at 100MHz, DQ open			25	mA

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
I_{CC4}	Operating Current (WRSR)	CS#=V_{CC}		10	20	mA
I_{CC5}	Operating Current (PP)	CS#=V_{CC}		10	20	mA
I_{CC6}	Operating Current (SE)	CS#=V_{CC}		10	20	mA
I_{CC7}	Operating Current (BE)	CS#=V_{CC}		10	20	mA
V_{IL}	Input Low Voltage		-0.5		0.3V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}		V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 μA	V_{CC}-0.2			V

Notes:
1. Checker Board Pattern.
2. V_{IL}min and V_{IH}max are reference only and are not tested.

12.5. AC Measurement Conditions

Table 7AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
CL	Load capacitance(including jig capacitance)		20	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V

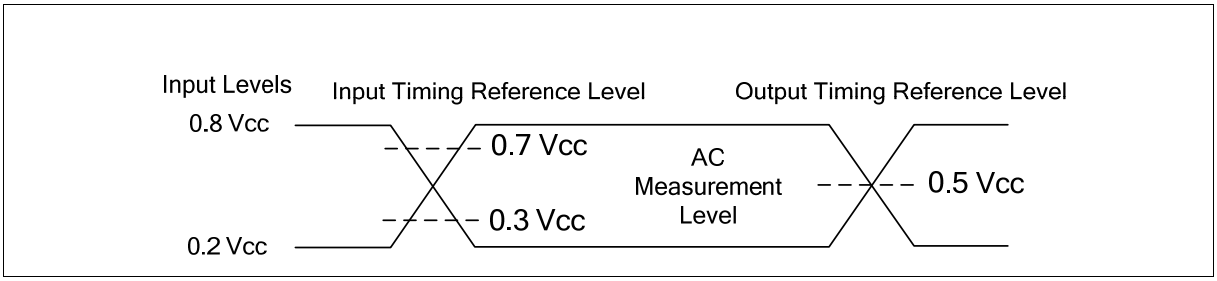


Figure 28 AC Measurement I/O Waveform

12.6. AC Electrical Characteristics

Table 8AC Characteristics

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.3V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_R	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR			100	MHz
f_R	Serial Clock Frequency for READ, RDSR, RDID			50	MHz
t_{CH1}(1)	Serial Clock High Time	4.5			ns

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
t_{CL1}(1)	Serial Clock Low Time	4.5			ns
t_{CLCH}(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}(2)	CS# Active Setup Time	5			ns
t_{CHSH}(2)	CS# Active Hold Time	5			ns
t_{SHCH}(2)	CS# Not Active Setup Time	5			ns
t_{CHSL}(2)	CS# Not Active Hold Time	5			ns
t_{SHSL}(2)	CS# High Time	7			ns
t_{SHQZ}(2)	Output Disable Time			7	ns
t_{CLQX}(2)	Output Hold Time	1.5			ns
t_{DVCH}(2)	Data In Setup Time	2			ns
t_{CHDX}(2)	Data In Hold Time	3			ns
t_{CLQV}(2)	Output Valid from CLK			8	ns
t_{WHSL}(2)	Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}(2)	Write Protect Hold Time after CS# High	100			ns
t_{DP}(2)	CS# High to Deep Power-down Mode			3	μs
t_{RES1}(2)	CS# High to Standby Mode without Electronic Signature Read			3	μs
t_{RES2}(2)	CS# High to Standby Mode with Electronic Signature Read			1.8	μs
t_{RST}(2)	CS# High to next Instruction after Reset(C0/C1)			20/200	us
t_W	Write Status Register Cycle Time		10	15	ms
t_{BP}	Byte Program Time		30	50	μs
t_{PP}	Page Program Time		0.6	3	ms
t_{SE}	Sector Erase Time		60	300	ms
t_{BE}	Block Erase Time (32KB)		250	1500	ms
t_{BE}	Block Erase Time (64KB)		400	2000	ms
t_{CE}	Chip Erase Time (2.7~3.6V)		1	4	s

Notes:
1. $t_{CH}+t_{CL} >= 1 / F_R$ or $1/f_R$;
2. This parameter is characterized and is not 100% tested.

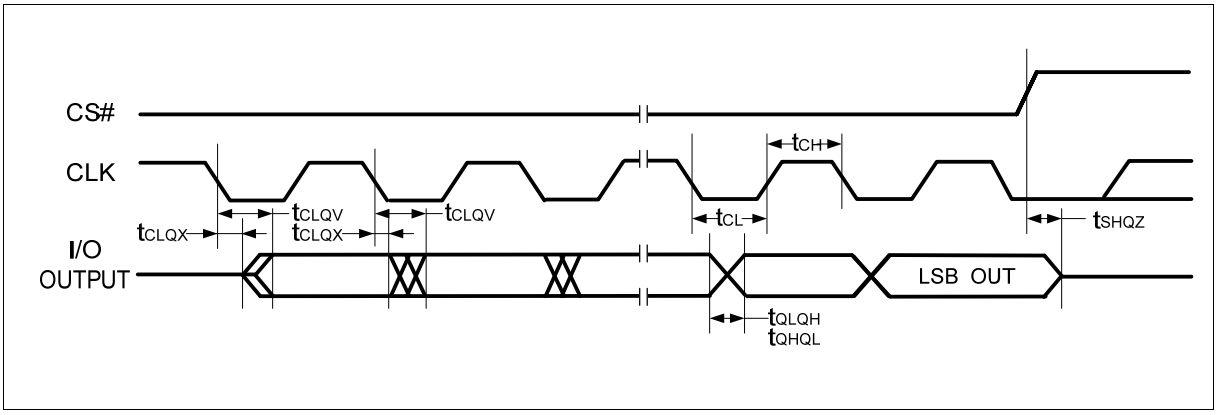


Figure 29 Serial Output Timing

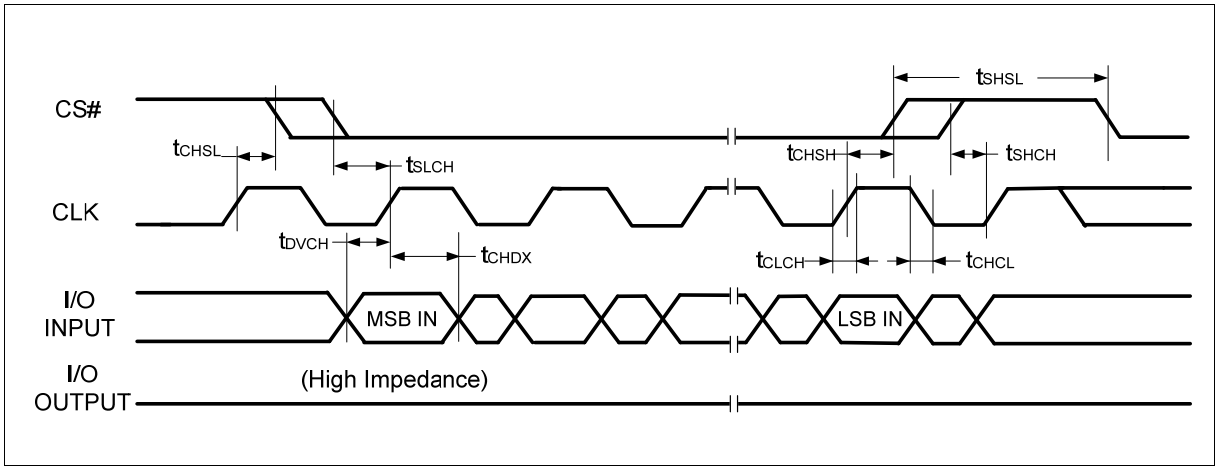


Figure 30 Serial Input Timing

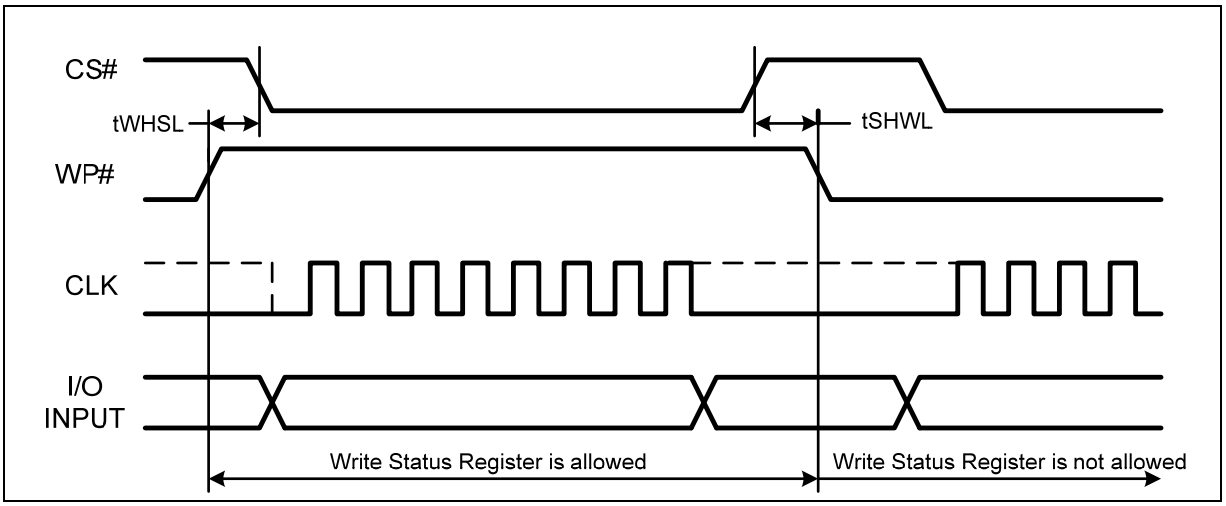


Figure 31 WP# Timing

13. Ordering Information

FM 25F 01 C -XXX -C -H -OP

Company Prefix

FM = Fudan Microelectronics Group Co.,ltd

Product Family

25F = 2.3~3.6V Serial Flash with 4KB Uniform-Sector,
Standard / Dual SPI

Product Density

01= 1M-bit

Product Version

Package Type

SO = 8-pin SOP（150mil）
TS = 8-pin TSSOP
US = 8-pin USON (2*3mm,0.55mm thickness)
SNA = 8-pin USON (1.5*1.5mm,0.45mm thickness)

Product Carrier

U = Tube
T = Tape and Reel (1)
TC = Tape（12mm） and Reel (2)

HSF ID Code

G = RoHS Compliant, Halogen-free, Antimony-free

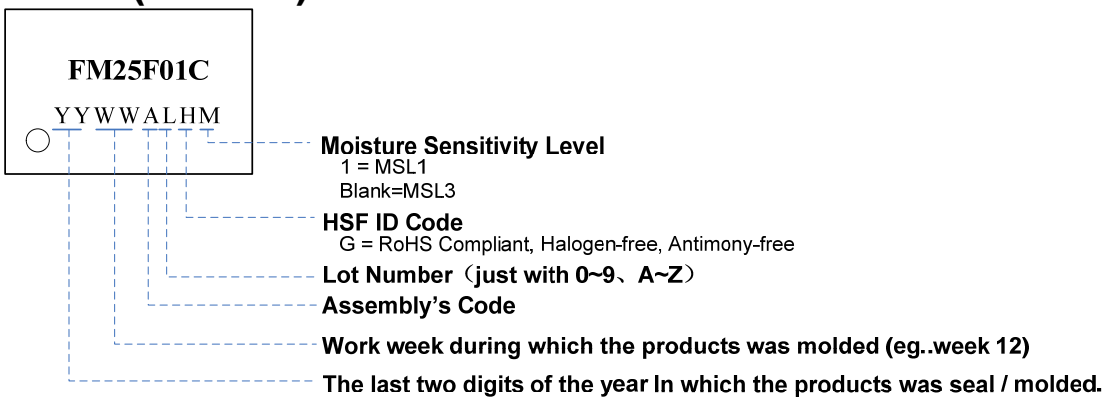
OPTION

C0 = Over-erase recover disabled during power up
C1 = Over-erase recover enabled during power up

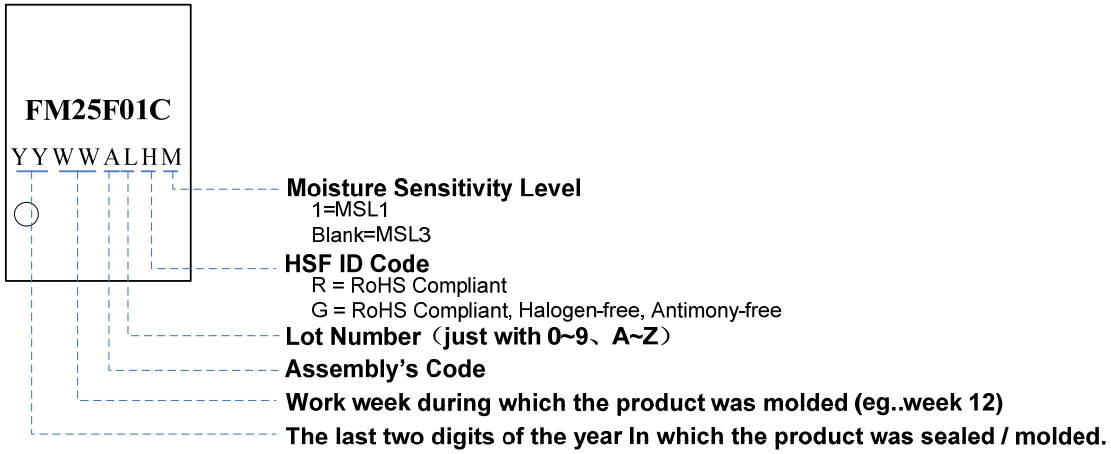
Note:
1. “T = Tape and reel” only for SO/TS/ SNA package.
2. “TC=Tape(12mm) and Reel” only for US package.

14. Part Marking Scheme

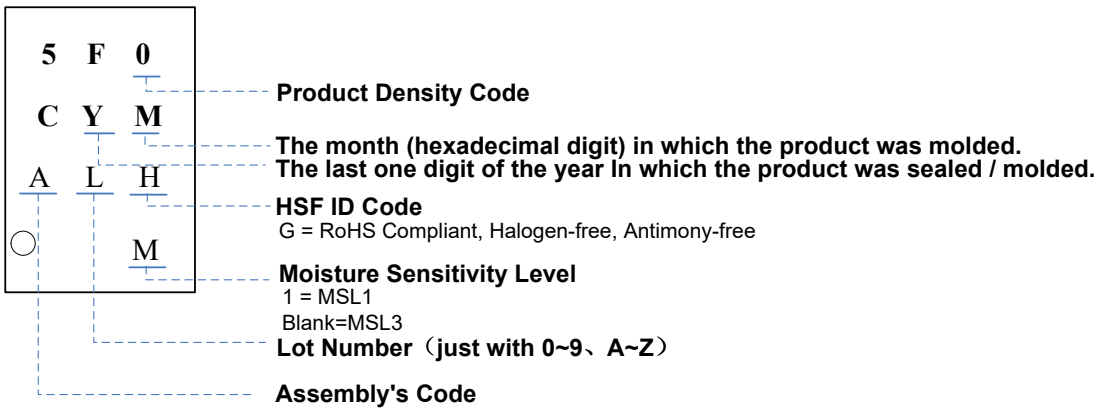
14.1. SOP8(150mil)



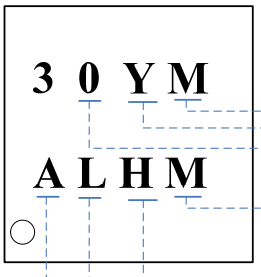
14.2. TSSOP8



14.3. USON8(2*3mm, 0.55mm thickness)



14.4. USON8(1.5*1.5mm, 0.45mm thickness)



The month (hexadecimal digit) in which the product was molded.
The last one digit of the year In which the product was sealed / molded.
Product Density Code

Moisture Sensitivity Level
1 = MSL1
Blank=MSL3

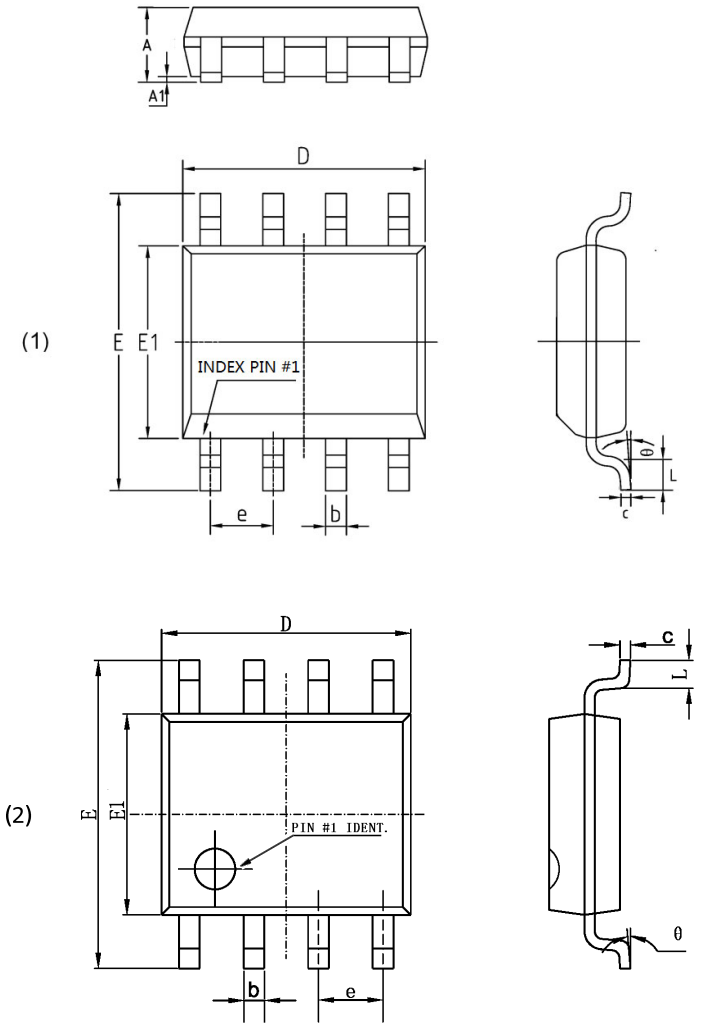
HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

Assembly's Code

15. Packaging Information

SOP 8 (150mil)

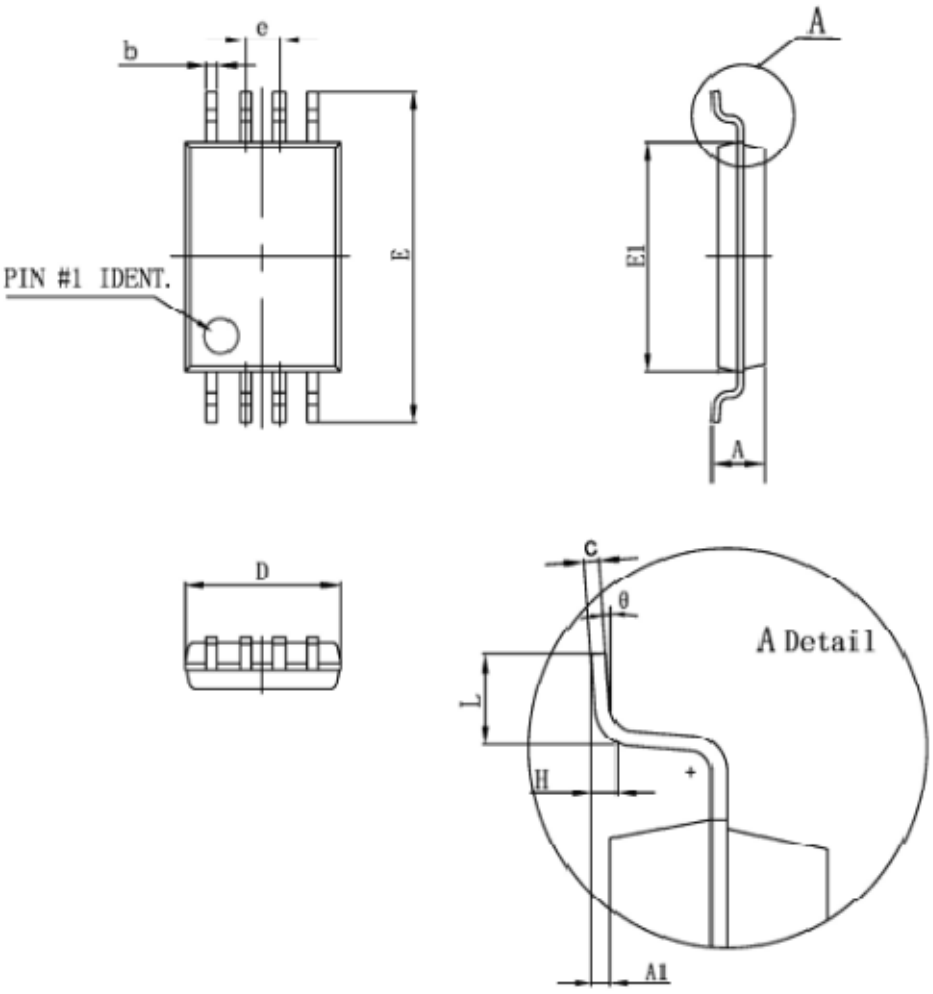


Symbol	MIN	MAX
A	1.350	1.750
A1	0.050	0.250
b	0.330	0.510
c	0.150	0.250
D	4.700	5.150
E1	3.700	4.100
E	5.800	6.200
e	1.270(BSC)	
L	0.400	0.900
θ	0°	8°

NOTE:

1. **Dimensions are in Millimeters.**

TSSOP8

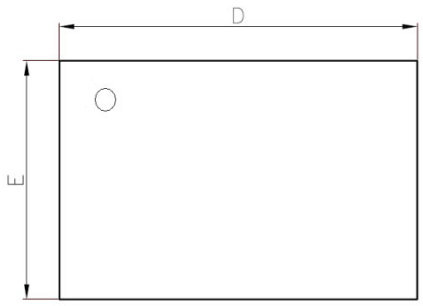


Symbol	MIN	MAX
D	2.900	3.100
E1	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E	6.200	6.600
A		1.200
A1	0.050	0.150
e	0.650 (BSC)	
L	0.450	0.750
θ	0°	8°

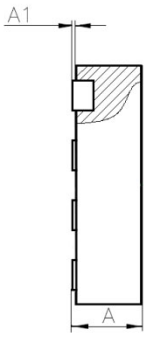
NOTE:

1. **Dimensions are in Millimeters.**

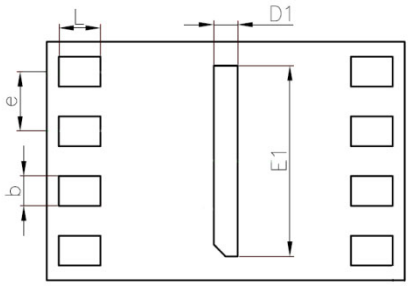
USON8 (2*3mm,0.55mm thickness)



TOP VIEW



SIDE VIEW



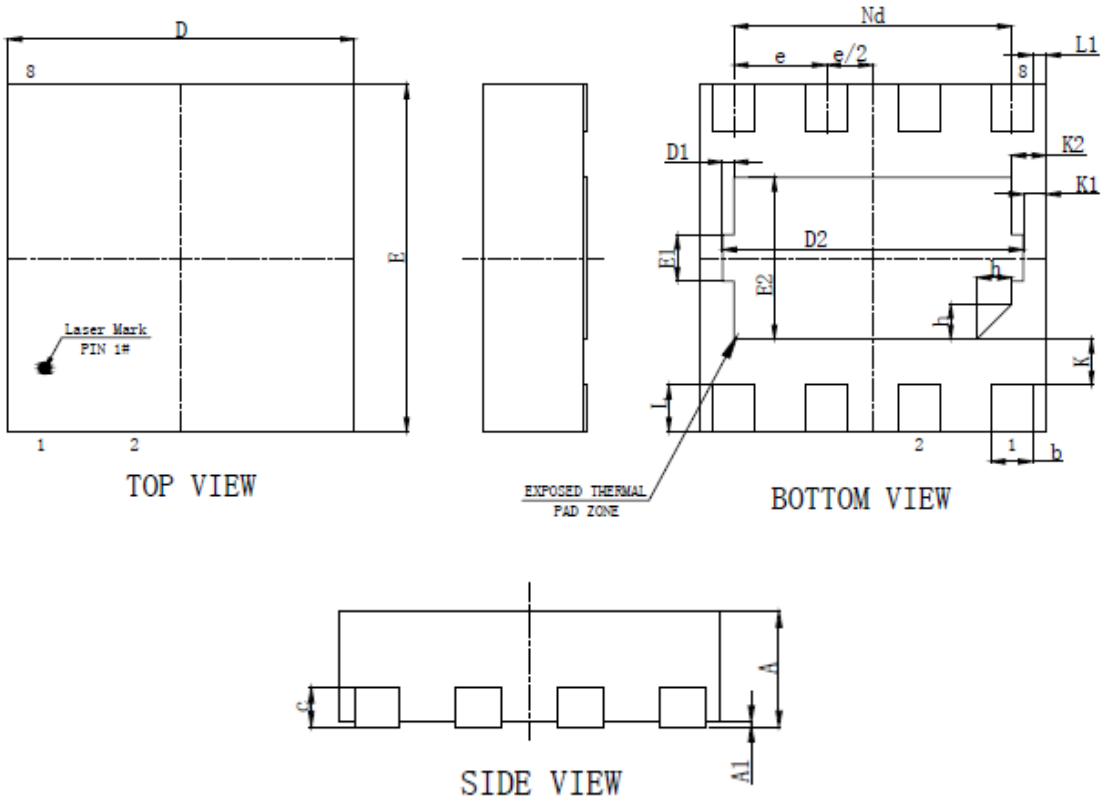
BOTTOM VIEW

Symbol	MIN	MAX
A	0.500	0.600
A1	0.000	0.050
D	2.900	3.100
E	1.900	2.100
D1	0.100	0.300
E1	1.500	1.700
b	0.180	0.300
e	0.500(BSC)	
L	0.300	0.400

NOTE:

1. Dimensions are in Millimeters.

USON8 (1.5*1.5mm,0.45mm thickness)



Symbol	MIN	MAX
A	0.400	0.500
A1	0.000	0.050
b	0.130	0.230
D	1.450	1.550
D2	1.200	1.400
E	1.450	1.550
E2	0.600	0.800
e	0.400(BSC)	
L	0.150	0.250

NOTE:

1. **Dimensions are in Millimeters.**

16. Revision History

VERSION	DATE	PAGE	Revise Description
1.0	Apr. 2021	44	Initial Document Release.
1.1	Aug.2021	44	1. Updated AC characteristics 2. Updated Ordering Information 3. Updated Packaging Information
1.2	Dec.2021	44	1. Updated AC characteristics 2. Updated Packaging Information
1.3	Jul.2022	46	1.Updated Packaging Information of USON8(1.5*1.5mm, 0.45mm thickness)
1.4	Sep.2023	46	1.Updated Packaging Information

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