Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM34C04D
Serial Presence Detect (SPD) EEPROM
with Reversible Software Write Protection

Data Sheet

Apr. 2017

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Description

The FM34C04D provides 4,096 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 512 words of 8 bits each, with 128-bit UID and 16-bytes Security Sector. This device is JEDEC JC42.4 (EE1004-v) Serial Presence Detect (SPD) compliant and includes reversible software write protection for each of four independent 128 x 8-bit blocks. The device features a page write capability of up to 16 bytes of data. Address pins allow up to eight devices on the same bus.

Features

- **Low Operation Voltage: V_{CC} = 1.7V to 3.6V**
- **Internally Organized: 512 x 8**
- **JEDEC JC42.4 (EE1004-v) Serial Presence Detect (SPD) Compliant for DRAM(DDR4) modules**
- **2-wire Serial Interface: I^2C Fast-Mode Plus Compatible**
  - **100kHz, 400kHz, and 1MHz Compatibility**
  - **SMBus-compatible bus Timeout Supported**
- **EEPROM memory array:**
  - **4 Kbits organized as two 256 x 8-bit banks**
  - **Each bank is composed of two 128-byte blocks**
- **Write Protect Pin for Hardware Data Protection**
- **Software data protection for each 128-byte block**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **16-Byte Page Write Modes (Partial Page Writes are Allowed)**
- **Lockable 16-Byte Security Sector**
- **128-Bit Unique ID for each device**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 1,000,000 Write Cycles**
  - **Data Retention: 40 Years**
- **TSSOP8、TDFN8 (RoHS Compliant and Halogen-free)**

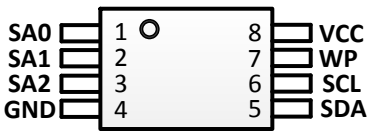
Absolute Maximum Ratings

Ambient temperature with power applied		-55℃ to +125℃
Storage Temperature		-65℃ to +150℃
Voltage on Any Pin with Respect to Ground	SA0	-0.5V to +11.0V
	Others	-0.5V to +6.5V
Maximum Operating Voltage		6.5V
DC Output Current		20.0 mA

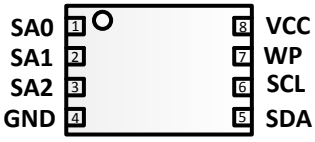
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Packaging Type

TSSOP 8



TDFN8

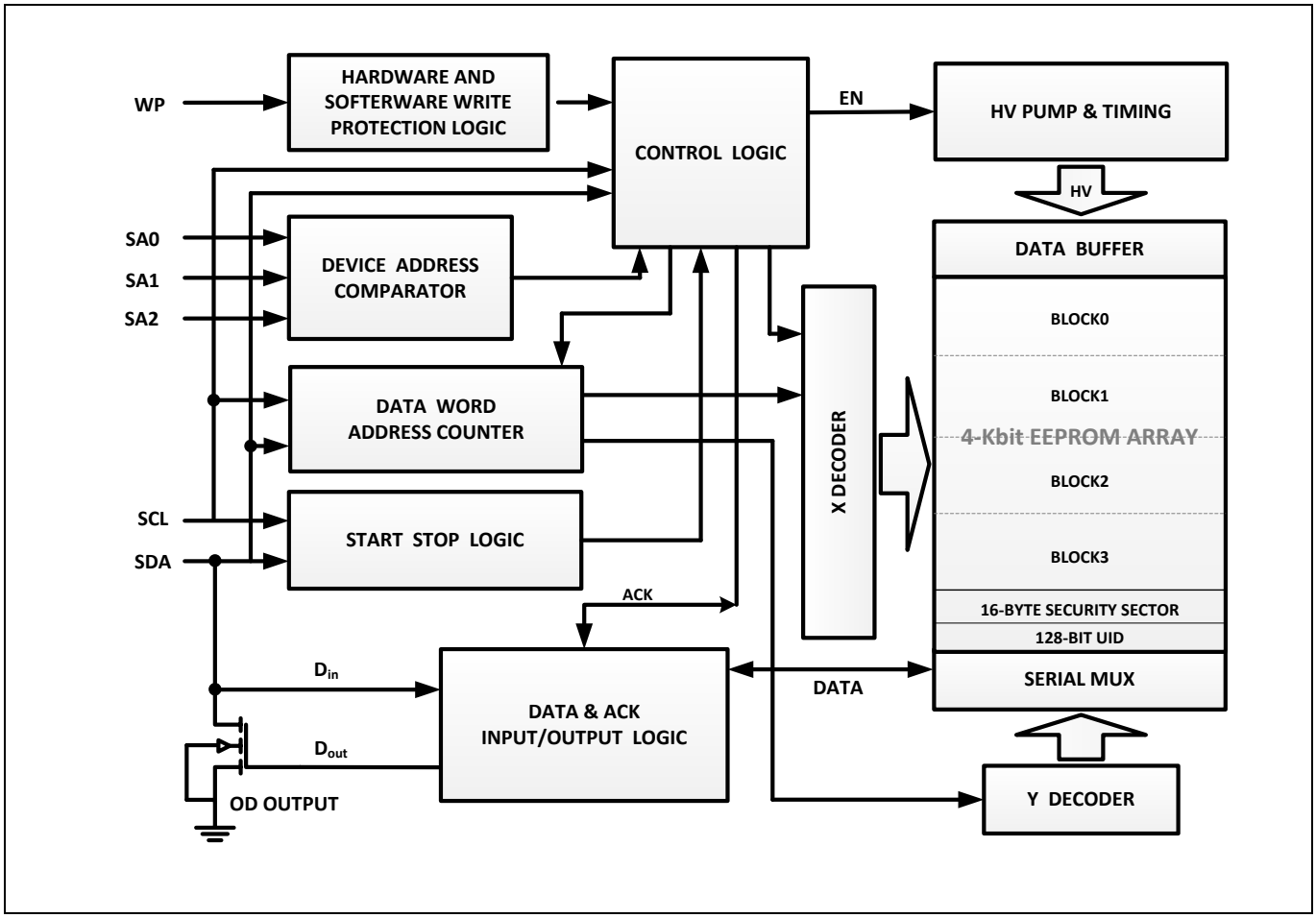


Note:
For Thinner package please contact local sales office.

Pin Configurations

Pin Name	Function
SA0~SA2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply
GND	Ground

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL):
The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA):
The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices. A pull-up resistor must be connected from Serial Data (SDA) to VCC. (Figure 9 indicates how the value of the pull-up resistor can be calculated).

DEVICE ADDRESSES (SA2, SA1, SA0):
The SA2, SA1 and SA0 pins are device address inputs that are hardwired or left not connected. When the pins are hardwired, as many as eight 4K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the SA2, SA1 and SA0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board VCC plane is <3pF, if coupling is >3pF, FMSH recommends connecting the address pins to GND.

The SA0 input is used to detect the V_{HV} voltage, when decoding a SWPn or CWP instruction.

WRITE PROTECT (WP):
The FM34C04D has a WP pin that provides hardware data protection. When the WP pin is connected to VCC, all write operations to the memory are inhibited. When the WP pin is connected to GND or left floating, the write protection of the memory is determined by the status defined by the execution of the previous SWPn instructions. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is <3pF. If coupling is >3pF, FMSH recommends connecting the WP to GND.

Write Protect Description

WP Pin Status	Part of the Memory Protected
WP=V_{CC}	Full Memory
WP=GND	Normal Read/Write Operations

Memory Organization

Data Memory: The FM34C04D includes a 4-Kbit serial EEPROM organized as two banks of 256 bytes each, or 512 bytes of total memory. Each bank is composed of two 128-byte blocks. The device is able to selectively lock the data in any or all of the four 128-byte blocks.

Security Sector： The FM34C04D offers 16-byte Security Sectors which can be written and (later) permanently locked in Read-only mode. This memory may be used by the system manufacturers to store security and other important information separately from the main memory array.

Unique ID(UID)： The FM34C04D utilizes a separate memory block containing a factory programmed 128-bit unique ID.

Input Parameters

SYMBOL	PARAMETER	CONDITIONS	Min	Max	Units
C_{IN}[1]	Input Capacitance(other pins)	V_{IN} = 0V, f = 1MHz	-	6	pF
C_{OUT}[1]	Output Capacitance(SDA)	V_{OUT} = 0V, f = 1MHz	-	8	pF
Z_{EIL}[1]	SA0/SA1/SA2 input impedance	VIN<0.3V_{CC}	30	-	KΩ
Z_{EIH}[1]	SA0/SA1/SA2 input impedance	VIN>0.7V_{CC}	800	-	KΩ
Z_{WPL}[1]	WP input impedance	VIN<0.3V_{CC}	5	-	KΩ
Z_{WPH}[1]	WP input impedance	VIN>0.7V_{CC}	500	-	KΩ

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +3.6V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Max	Units
V_{CC}	Supply Voltage	-	1.7	3.6	V
I_{CC1}	Supply Current(read)	fc = 400 kHz or 1 MHz	-	1.0	mA
I_{CC2}	Supply Current(write)	During $t_{W,}$ VIN = GND or V_{CC}	-	1.0	mA
I_{SB1}	Standby Current	V_{CC} < 2.2V, V_{IN} = V_{CC}/ GND	-	1.0	μA
I_{SB2}	Standby Current	V_{CC} ≥ 2.2V, V_{IN} = V_{CC}/ GND	-	2.0	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}/GND	-	±2.0	μA
I_{LO}	Output Leakage Current	SDA in Hi-Z, external voltage applied on SDA: GND or VCC	-	±2.0	μA
V_{IL}[1]	Input Low Level	-	-0.5	V_{CC} x 0.3	V
V_{IH}[1]	Input High Level	-	V_{CC} x 0.7	V_{CC} + 0.5	V
V_{HV}	SA0 high voltage detect	V_{CC} < 2.2V	7	10	V
		V_{CC} ≥ 2.2V	V_{CC} + 4.8	10	V
V_{OL}	Output Low voltage	V_{CC} ≥ 2.2V, I_{OL} = 20 mA	-	0.4	V
		V_{CC} ≤ 2.2V, I_{OL} = 6 mA	-	0.6	V
		V_{CC} ≤ 2.2V, I_{OL} = 3 mA	-	0.4	V
V_{OL1}	Output Low Level 1	V_{CC} =1.7V, I_{OL} = 0.15 mA	-	0.2	V
V_{PON}[1]	Power on reset threshold	Monotonic rise between V_{PON} and V_{CC}(min) without ringback	1.6	-	V
V_{POFF}[1]	Power Off threshold for warm power on cycle	No ringback above V_{POFF}	-	0.7	V

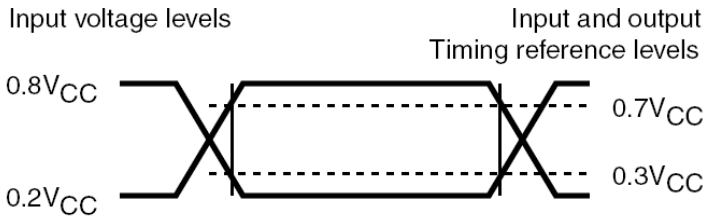
Note: 1. Measured during characterization, not tested in production.

AC Characteristics

AC measurement conditions

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance	100		pF
T_R, T_F	SCL input rise and fall time, SDA input fall time		50	ns
V_{IN}	Input levels	0.2Vcc to 0.8Vcc		V
IN, OUT	Input and output timing reference levels	0.3Vcc to 0.7Vcc		V

AC measurement I/O waveform



AC characteristics

Recommended operating conditions: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +3.6V, CL = 100 pF (unless otherwise noted).

Symbol	Parameter	V_{CC} < 2.2V		V_{CC} ≥ 2.2V				Units
		100 kHz		400 kHz		1000 kHz		
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	10	100	10	400	10	1000	kHz
t_{LOW}	Clock Pulse Width Low	4700	-	1300	-	500	-	ns
t_{HIGH}	Clock Pulse Width High	4000	-	600	-	260	-	ns
$t_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	25	35	ms
t_I [1]	Noise Suppression Time	-	50	-	50		50	ns
t_{BUF} [1]	Time the bus must be free before a new transmission can Start	4700	-	1300	-	500	-	ns
$t_{HD.STA}$	Start Hold Time	4000	-	600	-	260	-	ns
$t_{SU.STA}$	Start Setup Time	4700	-	600	-	260	-	ns
$t_{HD.DAT}$	Data In Hold Time	0	-	0	-	0	-	ns
$t_{SU.DAT}$	Data In Setup Time	250	-	100	-	50	-	ns
t_R [1]	Inputs Rise Time	-	1000	20	300		120	ns
t_F [1]	Inputs Fall Time	-	300	20	300		120	ns
$t_{SU.STO}$	Stop Setup Time	4000		600		260		ns
$t_{HD.DAT}$	Data Out Hold Time	200	3450	200	900	0	350	ns
t_{WR}	Write Cycle Time	-	5		5		5	ms
t_{POFF} [1]	Warm power cycle off time	1	-	1	-	1	-	ms
t_{INIT}	Time from power on to first command	10	-	10	-	10	-	ns
Endurance [1]	3.3V, 25°C, Page Mode	1,000,000						Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.
2. The minimum frequency is specified at 10kHz to avoid activating the timeout feature.

Device Operation

CLOCK AND DATA TRANSITIONS:
The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION:
A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

STOP CONDITION:
A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

ACKNOWLEDGE:
All address and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE:
The FM34C04D features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

TIMEOUT FUNCTION:
The FM34C04D supports the industry standard bus Timeout feature to help prevent potential system bus hang-ups. The device resets its serial interface and will stop driving the bus (will let SDA float high) if the SCL pin is held low for more than the minimum Timeout ($t_{TIMEOUT}$) specification. The FM34C04D will be ready to accept a new Start condition before the maximum $t_{TIMEOUT}$ has elapsed (refer to Figure 7). This feature does require a minimum SCL clock speed of 10kHz to avoid any timeout issues.

DEVICE RESET AND INITIALIZATION:
The FM34C04D incorporates an internal Power-On Reset (POR) circuit to help prevent inadvertent operations during power-up and power down cycles. On a cold power-up, the supply voltage must rise monotonically between V_{PON}(max) and V_{CC}(min) without any ringback to ensure a proper power-up. Once the supply voltage has passed the V_{PON}(max) threshold, the device is reset.

Before selecting the device and issuing instructions, a valid and stable supply voltage must be applied and no command should be issued to the device for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the instructions transmission, and for a Write instruction, until the end of the internal write cycle (t_{WR}).

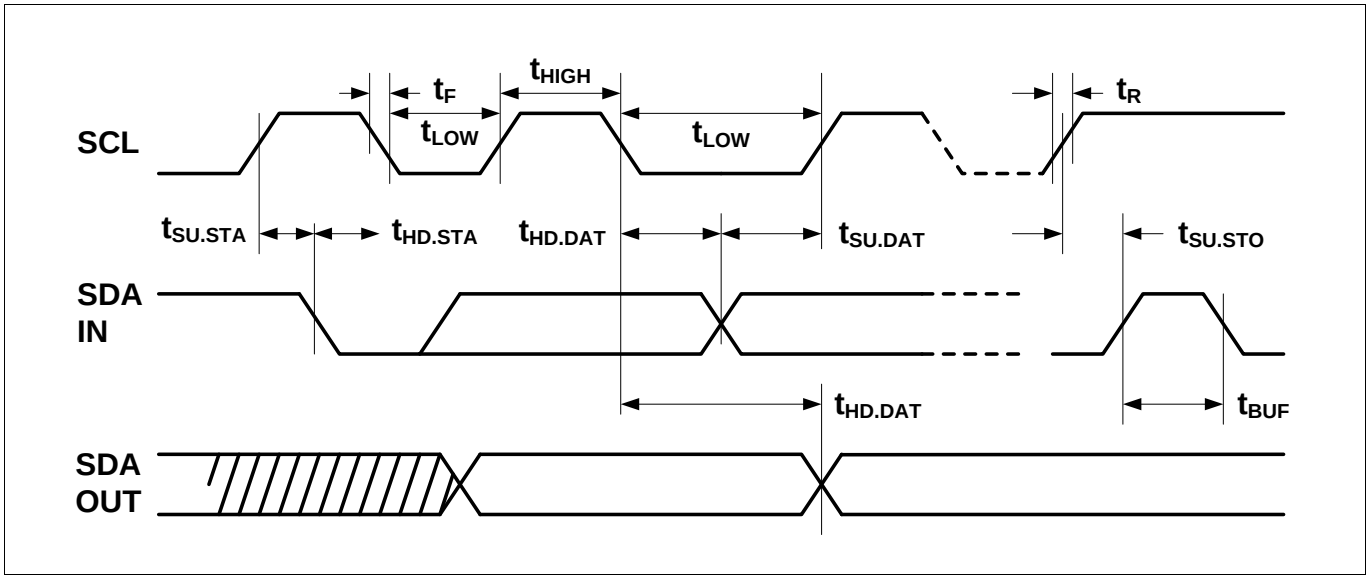
At power down (phase during which V_{CC} decreases continuously), as soon as V_{CC} drops from V_{PON}(max), the device stops responding to commands.

On warm power cycling, V_{CC} must remain below V_{POFF}(min) for t_{POFF}, and must meet cold power on reset timing when restoring power(refer to Figure 8).

2-WIRE SOFTWARE RESET:
After an interruption in protocol, power loss or system reset, any 2-wire part can be reset in following these steps:
1. Clock up to 9 Cycles,
2. Look for SDA high in each cycle while SCL is high and then,
3. Create a start condition as SDA is high.

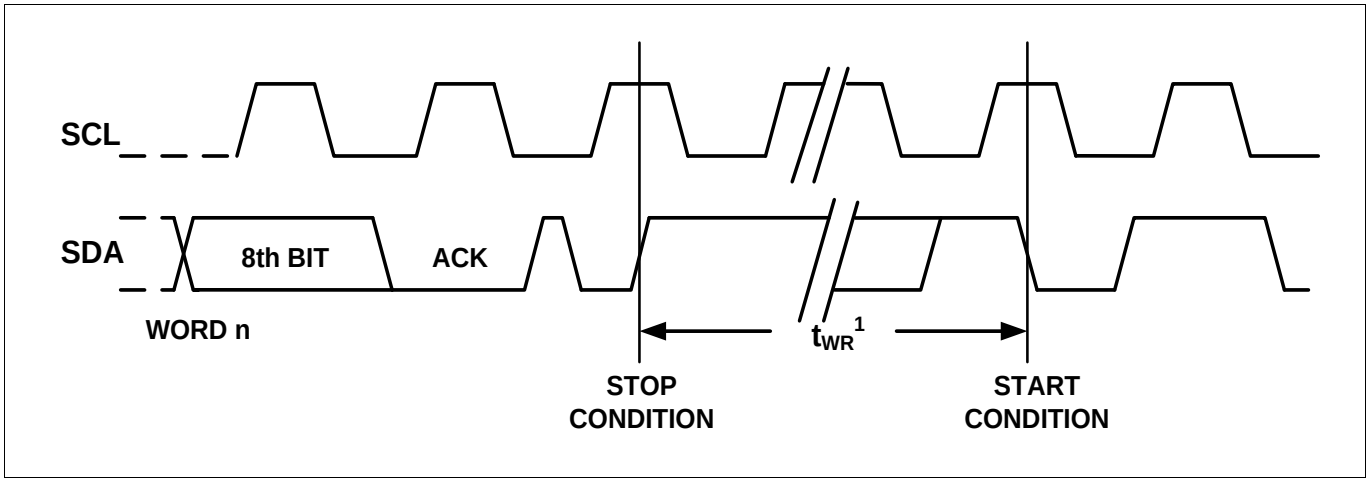
Bus Timing

Figure 2. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 3. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4. Data Validity

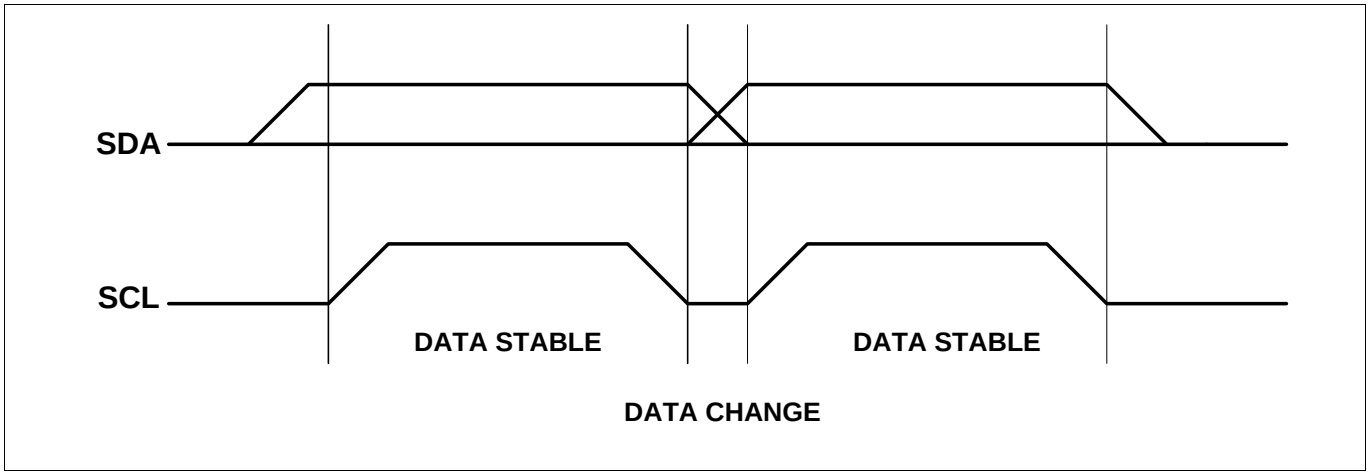


Figure 5. Start and Stop Definition

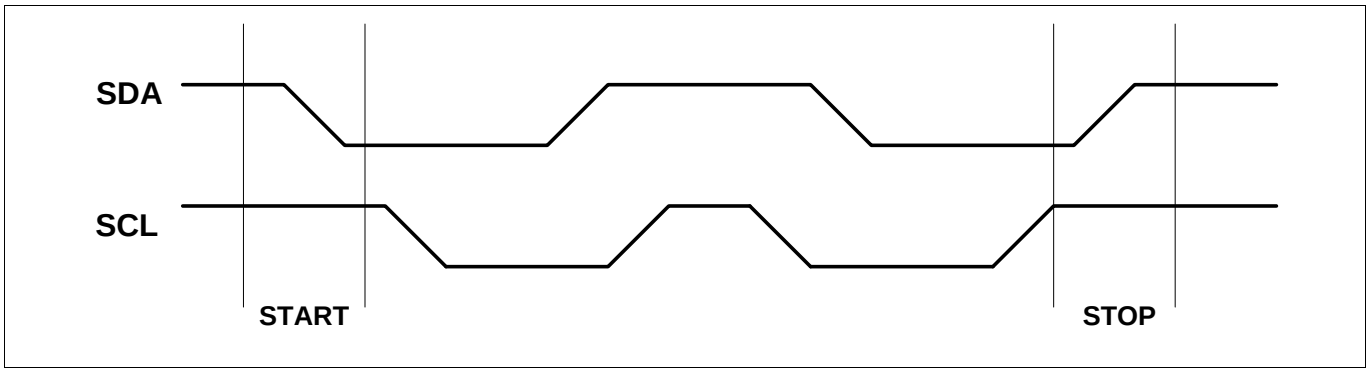
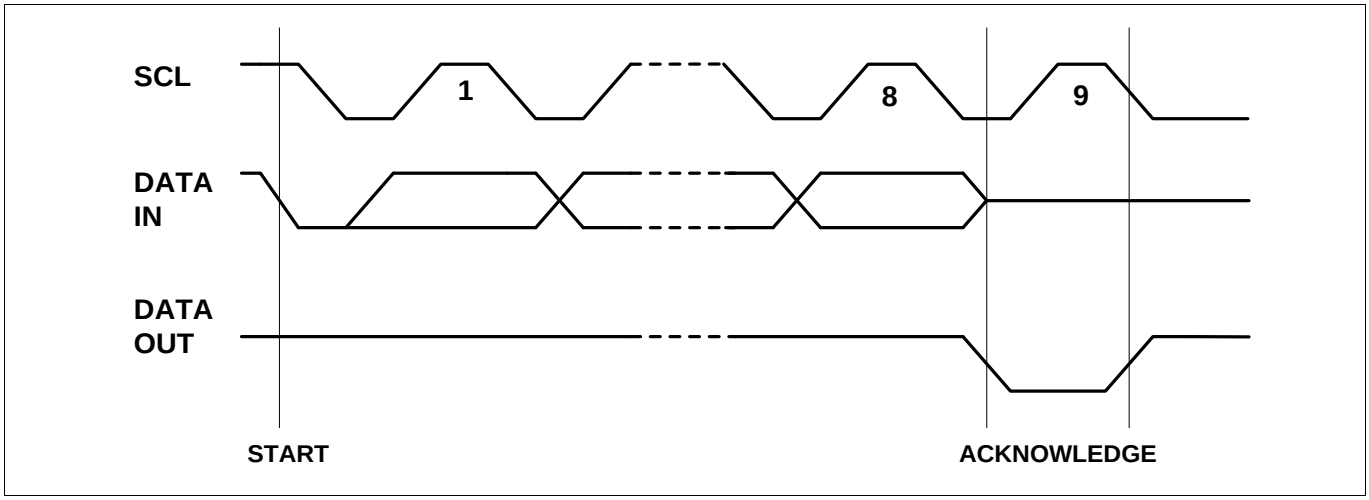
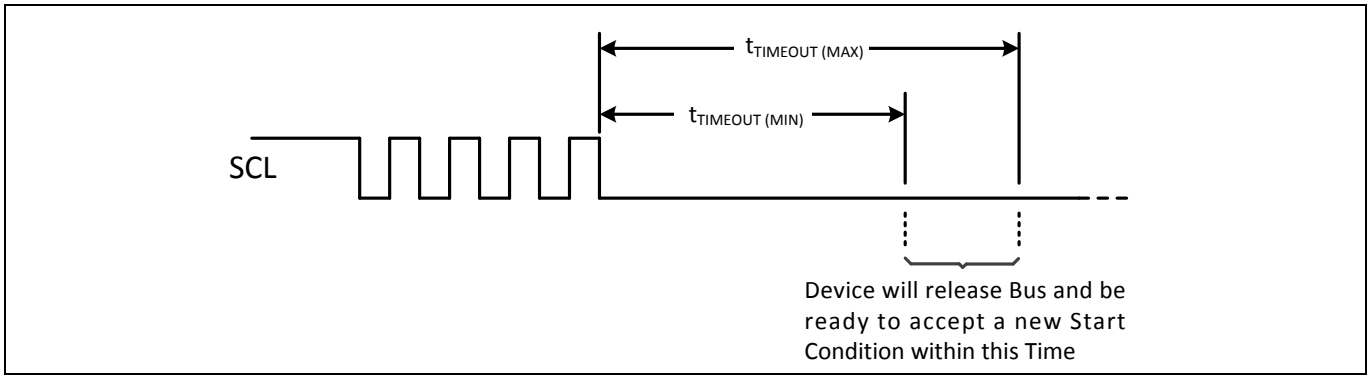


Figure 6. Output Acknowledge



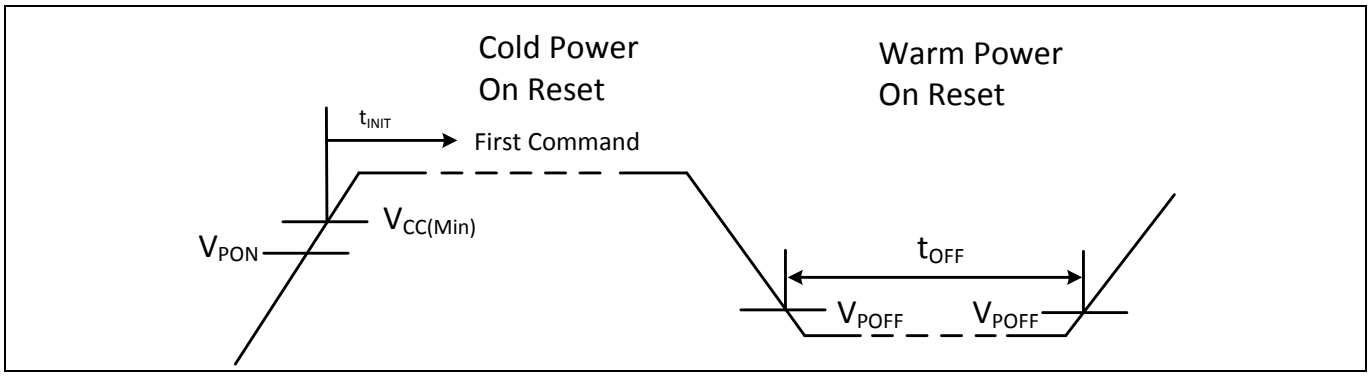
Timeout Timing

Figure 7. Time Out



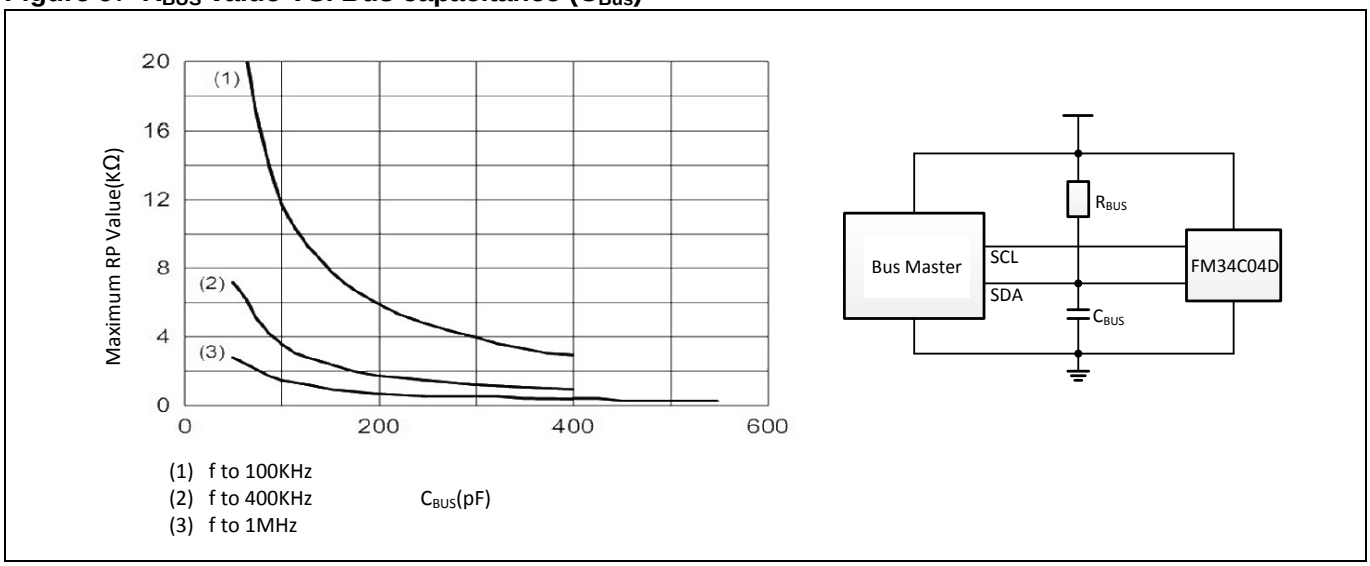
Power-up Timing

Figure 8. VCC Ramp Up and Ramp Down



Maximum R_{BUS} value VS. Bus capacitance (C_{Bus})

Figure 9. R_{BUS} value VS. Bus capacitance (C_{Bus})



Device Addressing

To start a communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in Table 1 (on Serial Data (SDA), most significant bit first).

The Device Type Identifier Code (DTIC) consists of a 4-bit device type identifier, and a 3-bit Logical Serial Address (LSA2, LSA1, LSA0). To address the Data memory, the 4-bit device type identifier is 1010b; to access the write-protection settings, it is 0110b; to access the Security Sector and UID, it is 1011b.

Table 1. Device Type Identifier Code (DTIC)

Function	Abbr	Device type identifier (1)				Select address (2) (3)			R/W	SA0 pin
		b7	b6	b5	b4	b3	b2	b1	b0	
Read Data Memory	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write Data Memory	WSPD								0	0 or 1
Read Security Sector	RSS	1	0	1	1	LSA2	LSA1	LSA0	1	0 or 1
Write Security Sector	WSS					LSA2	LSA1	LSA0	0	0 or 1
Read UID	RUID	1	0	1	1	LSA2	LSA1	LSA0	1	0 or 1
Set Write Protection, block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, block 0 (5)	RPS0					0	0	1	1	0,1 or V_{HV}
Read Protection Status, block 1 (5)	RPS1					1	0	0	1	0,1 or V_{HV}
Read Protection Status, block 2 (5)	RPS2					1	0	1	1	0,1 or V_{HV}
Read Protection Status, block 3 (5)	RPS3					0	0	0	1	0,1 or V_{HV}
Set Bank Address to 0 (6)	SBA0					1	1	0	0	0,1 or V_{HV}
Set Bank Address to 1 (6)	SBA1					1	1	1	0	0,1 or V_{HV}
Read Bank Address (7)	RBA					1	1	0	1	0,1 or V_{HV}
Reserved	-					All other encodings				0,1 or V_{HV}

Note:

1. The most significant bit, b7, is sent first.
2. Logical Serial Addresses (LSA) are generated by the combination of inputs on the SA2~SA0 pins.
3. For backward compatibility with previous devices, the order of block select bits (b3 and b1) is not a simple binary encoding of the block number.
4. SA0 pin is driven to 0=GND, 1=V_{CC}, or VHV.
5. Reading the block protection status results in Ack when the block is not write-protected, and results in NoAck when the block is write-protected.
6. Setting the EE bank address to 0 selects the lower 256 bytes of EEPROM; setting it to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE bank.
7. Reading the EE bank address results in Ack when the current bank is 0, and NoAck when the current bank is 1.

Table 2. Word Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	A7	A6	A5	A4	A3	A2	A1	A0
Security Sector	0	0	x	x	A3	A2	A1	A0
Security Sector Lock Bit	x	1	x	x	x	x	x	x
Unique ID Number	1	0	x	x	0	0	0	0
	MSB							LSB

Note:

1. x = Don`t care bit.
2. The value of word address is ‘don’t care’ for SWPn/CWP/RPSn/SBAn/RBA instructions

Write Operations

The FM34C04D supports single Byte Write and Page Write operations up to the maximum page size of 16 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes sent to the device. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s).

CAUTION: All Byte Write and Page Write operations should be preceded by the SBA and or RBA commands to ensure the internal address counter is located in the desired half of the memory. If a Byte Write or Page Write operation is attempted to a protected block, the FM34C04D will respond (ACK or NoACK) to the write operation according to Table 3.

Table 3 Acknowledge Status When Writing Data or Defining Write Protection (instructions with R/W bit = 0)

Status	Instruction	Ack	Word Address	Ack	Data byte	Ack	Write cycle (tW)
Protected	SWPn	NoAck	Not significant	NoAck	Not significant	NoAck	No
	CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write in protected block	Ack	Address	Ack	Data	NoAck	No
Not Protected	SWPn or CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write	Ack	Address	Ack	Data	Ack	Yes

BYTE WRITE:
A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 9).

PAGE WRITE:
The 4K EEPROM is capable of 16-byte page writes. A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 15 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 10).

ACKNOWLEDGE POLLING:
Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

WRITE SECURITY SECTOR:
Write the Security Sector is similar to the page write but requires use of device address, and the special word address seen in Table 1~2. Address bits A<7:6> which must be equal to ‘00b’. Lower address bits A<3:0> define the byte address inside the Security Sector (refer to Figure 14).And other address bits are don’t care.

If the Security Sector is locked, the data bytes transferred during the Write Security Sector operation are not acknowledged (NoAck).

LOCK SECURITY SECTOR:
Lock the Security Sector is similar to the byte write but requires use of device address, and special word address seen in Table 1. The word address bits A<7:6> must be ‘x1b’, all other word address bits are don’t care. The data byte must be equal to the binary value xxxx xx1x, where x is don't care (see Figure 16).

If the Security Sector is locked, the data bytes transferred during the Lock Security Sector operation are not acknowledged (NoAck).

Read Operations

All Read operations are initiated by the Master transmitting a Start bit, a device type identifier of '1010' (Ah), three Logical Serial Address bits (LSA2, LSA1, LSA0) that match their corresponding hard-wired address pins (SA2, SA1, SA0), and the R/W select bit with a Logic 1 state. In the following clock cycle, the device should respond with an ACK. The subsequent protocol depends on the type of Read operation desired.

CAUTION: For 4-Kbit Data Memory, all Read operations should be preceded by the SBA and/or RBA commands to ensure the desired half of the memory is selected. The reason this is important, for example, during a Sequential Read operation on the last byte in the first half of the memory (address FFh) with SBA=0 (indicating first half is selected), the internal address counter will roll-over to address 00h in the first half of memory as opposed to the first byte in the second half of the memory. For more information on the SBA and RBA commands, see Table 1.

CURRENT ADDRESS READ:
The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 11).

RANDOM READ:
A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 12).

SEQUENTIAL READ:
Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an ACK. As long as the EEPROM receives an ACK, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 13)

UNIQUE ID READ:
Reading the serial number is similar to the sequential read but requires use of the device address, a dummy write, and the use of specific word address seen in Table 1~2. Address bits A<7:6> which must be equal to '10b'. Lower address bits A<3:0> define the byte address inside the UID. And other address bits are don't care. If the application desires to read the first byte of the UID, the lower address bits A<3:0> would need to be '0000b'.

When the end of the 128-bit UID number is reached (16 bytes of data), the data word address will roll-over back to the beginning of the 128-bit UID number. The Unique ID Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (refer to Figure 18).

READ SECURITY SECTOR：
Read the Security Sector is similar to the random read but requires use of device address, a dummy write, and the use of specific word address seen in Table 1~2. The higher address bits are don't care except for address bits A<7:6>，which must be equal to '00b'. The lower address bits A<3:0> define the byte address inside the Security Sector.
The internal byte address is automatically incremented to the next byte address after each byte of data is clocked out. When the last byte (0Fh) is reached, it will roll over to 00h, the first byte of the Security Sector, and continue to increment (refer to Figure 15).

READ LOCK STATUS：

There are two ways to check the lock status of the Security Sector.

1 The first way is initiated by a Security Sector Write, the EEPROM will acknowledge if the Security Sector is unlocked, while it will not acknowledge if the Security Sector is locked.

Once the acknowledge bit is read, it is recommended to generate a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic
- Stop: the device is then set back into Standby mode by the Stop condition.

2 The second way is initiated by a Lock Status Read. Lock Status Read is similar to the random read but requires use of device address seen in Table 1~2, a dummy write, and the use of specific word address. The address bits A<7:6> must be ‘x1b’, all other address bits are Don't Care. The Lock bit is the BIT1 of the byte read on SDA. It is at “1” when the lock is active and at “0” when the lock is not active. The same data is shifted out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 17).

Setting the write protection

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

– Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), Bank address = 0
– Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), Bank address = 0
– Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), Bank address = 1
– Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), Bank address = 1

The device has three software commands for setting, clearing, or interrogating the write protection status.

– SWPn: Set Write Protection for block n
– CWP: Clear Write Protection for all blocks
– RPSn: Read Protection status for block n

The level of write protection (set or cleared), that has been defined using these instructions, remains defined even after a power cycle.

The DTICs of the SWP, CWP and RPS instructions are defined in Table 1.

SET AND CLEAR THE WRITE PROTECTION (SWPn and CWP):

If the software write protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears the write protection for all blocks.When decoded, SWPn and CWPn trigger a write cycle lasting t_{WR} (Write Cycle Time). (refer to Figure 19)

The DTICs of the SWPn and CWP instructions are defined in Table 1.

READ THE PROTECTION STATUS (RPSn)

The serial bus master issues an RPSn command specifying which block to report upon. If the software write protection has not been set, the device replies to the data byte with an Ack. If it has been set, the device replies to the data byte with a NoAck.

The DTIC of the RPSn instruction is defined in Table 1.

Set the bank address (SBAn)

The SBAn command selects the lower 256 bytes (SBA0) or upper 256 bytes (SBA1). After a cold or warm power-on reset, the bank address is always 0, selecting the lower 256 bytes. (refer to Figure 20)

The DTIC of the SBAn instruction is defined in Table 1.

Read the bank address (RBA)

The RBA command determines if the currently selected bank is 0 (device returns Ack) or 1 (device returns NoAck). (refer to Figure 21)

The DTIC of the RBA instruction is defined in Table 1.

Figure 9. Byte Write

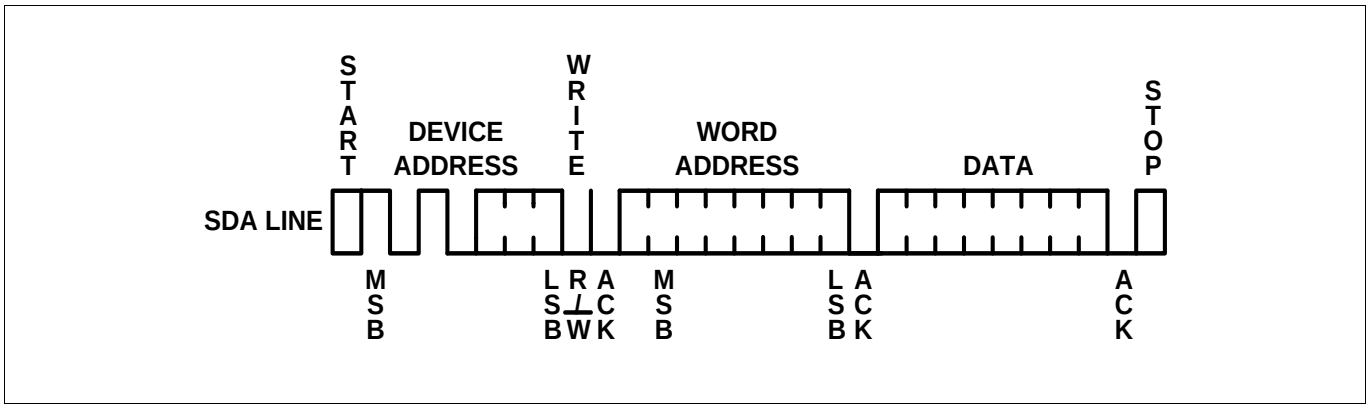


Figure 10. Page Write

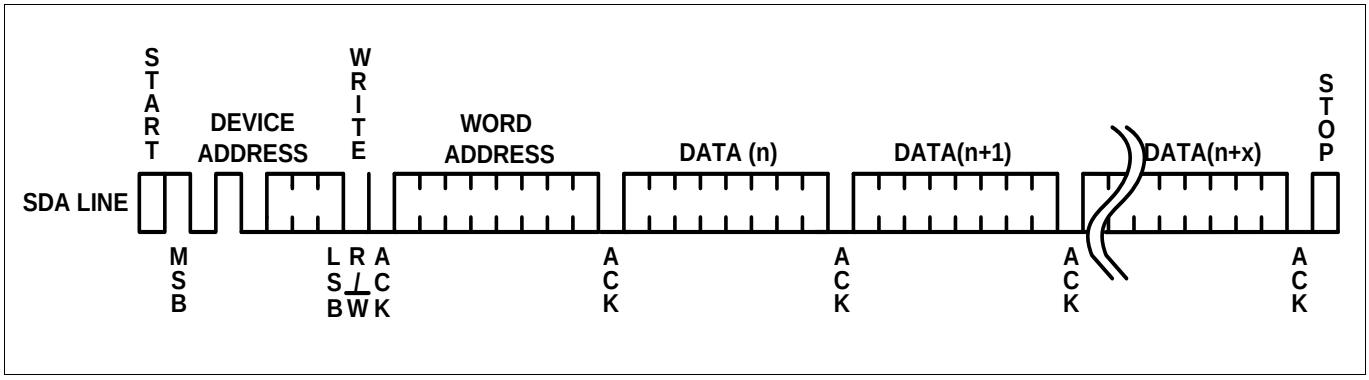


Figure 11. Current Address Read

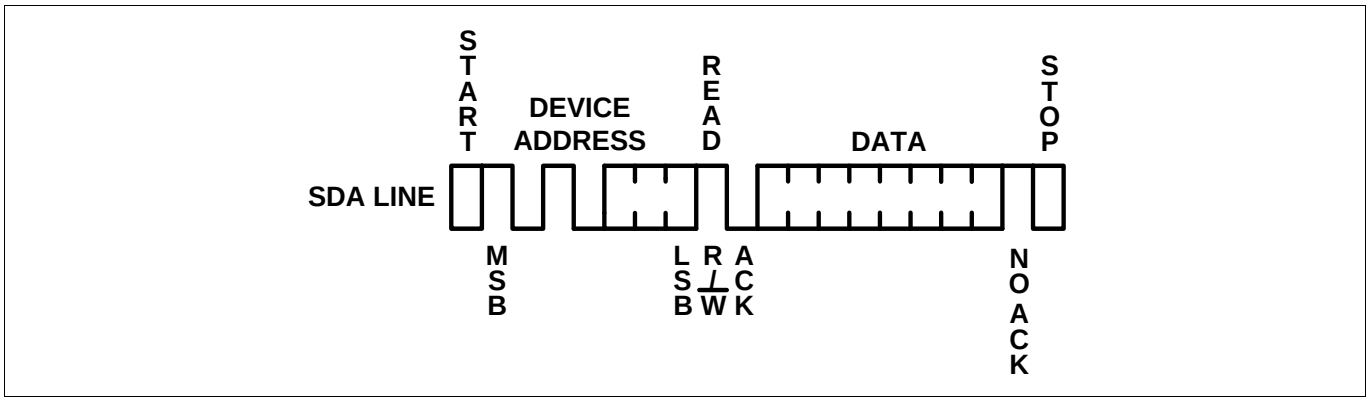


Figure 12. Random Read

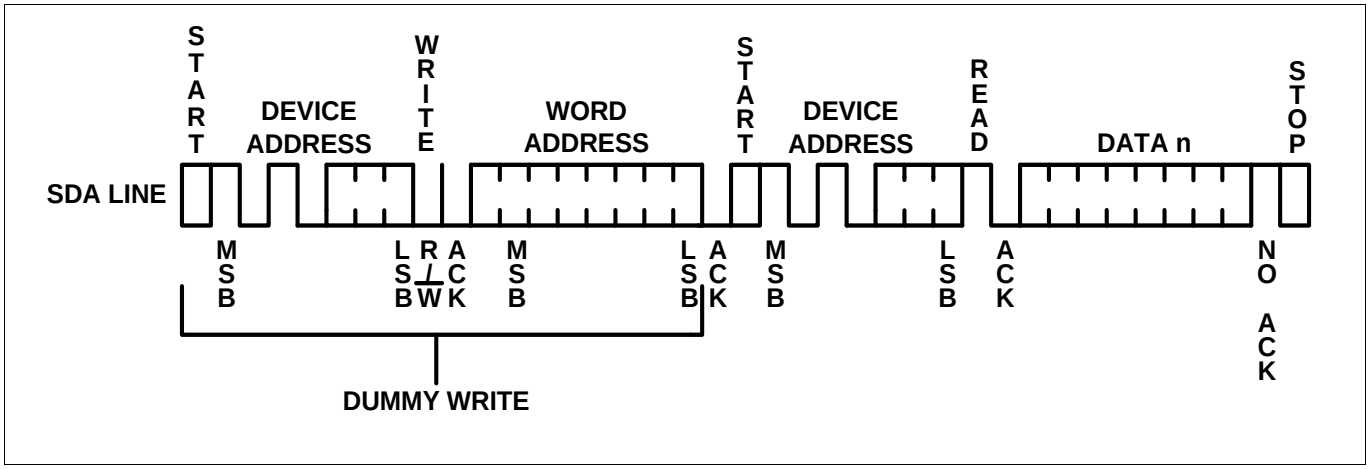


Figure 13. Sequential Read

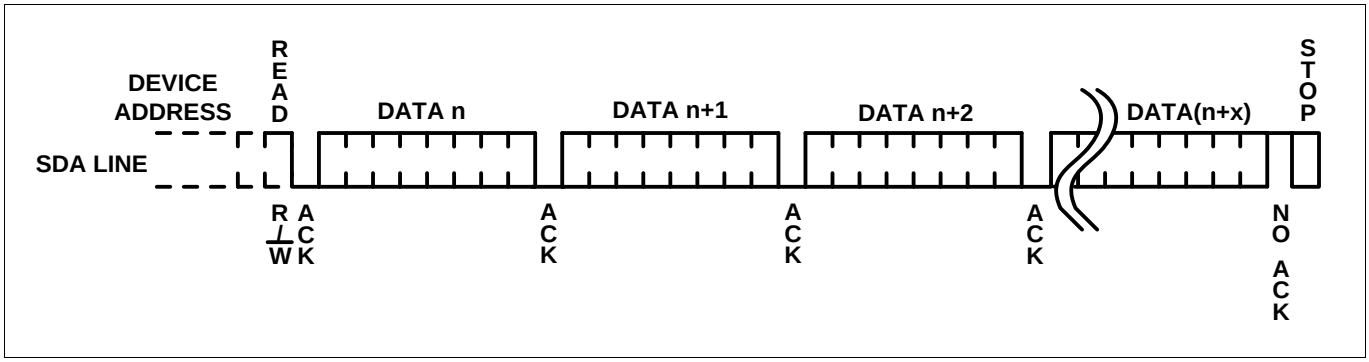
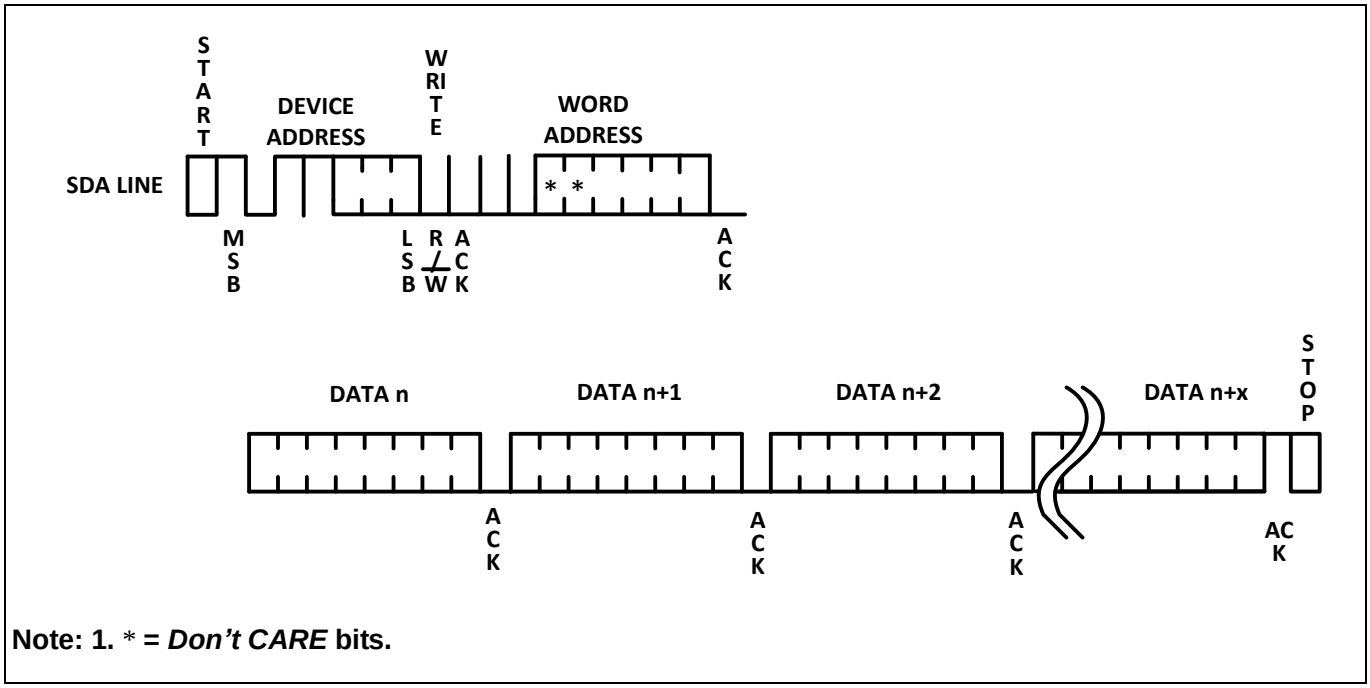
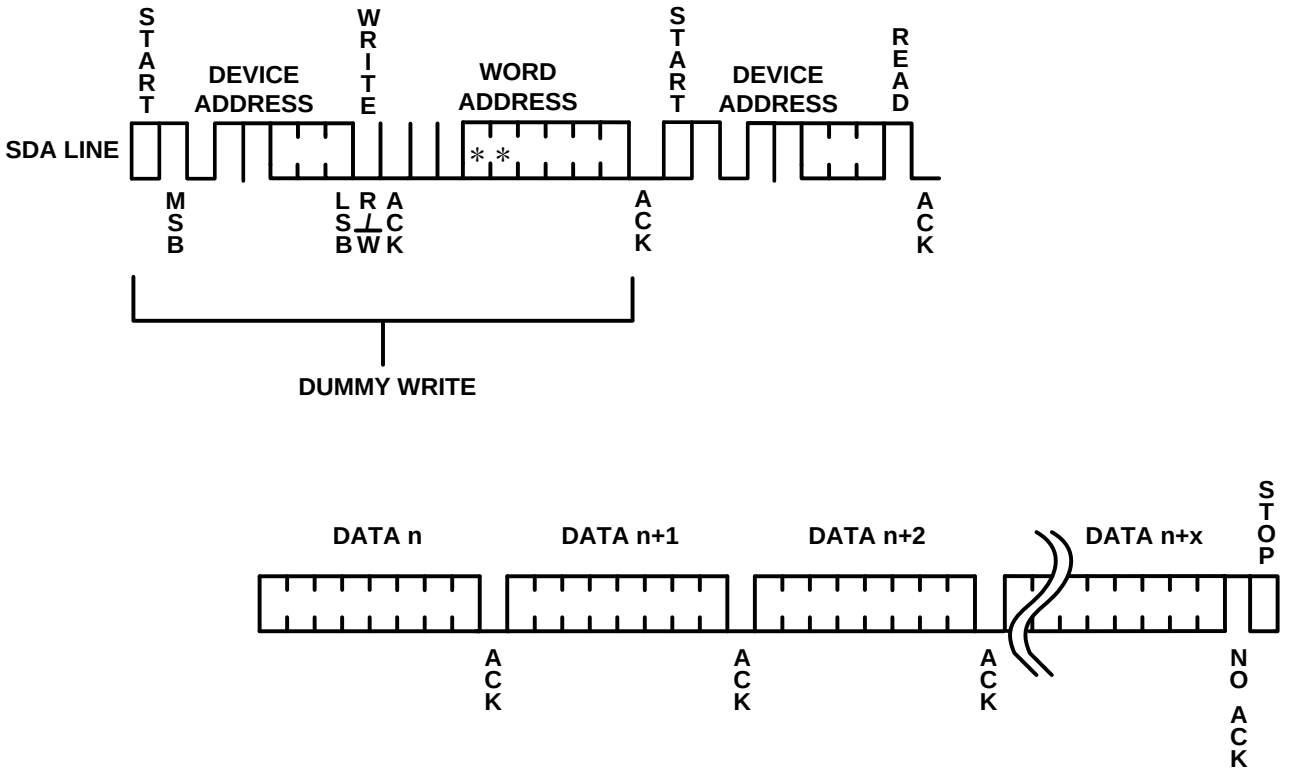


Figure 14. Write Security Sector



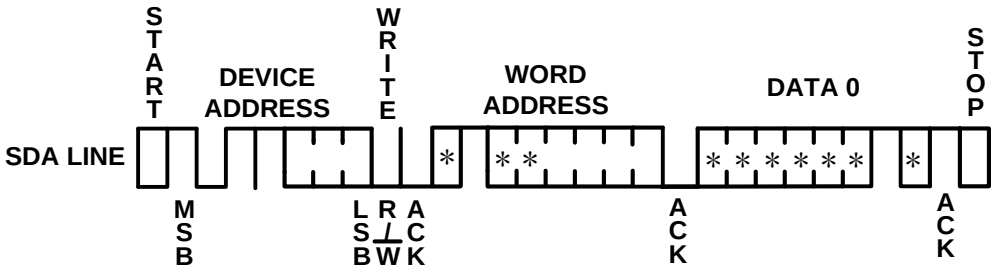
Note: 1. * = *Don't CARE* bits.

Figure 15. Read Security Sector



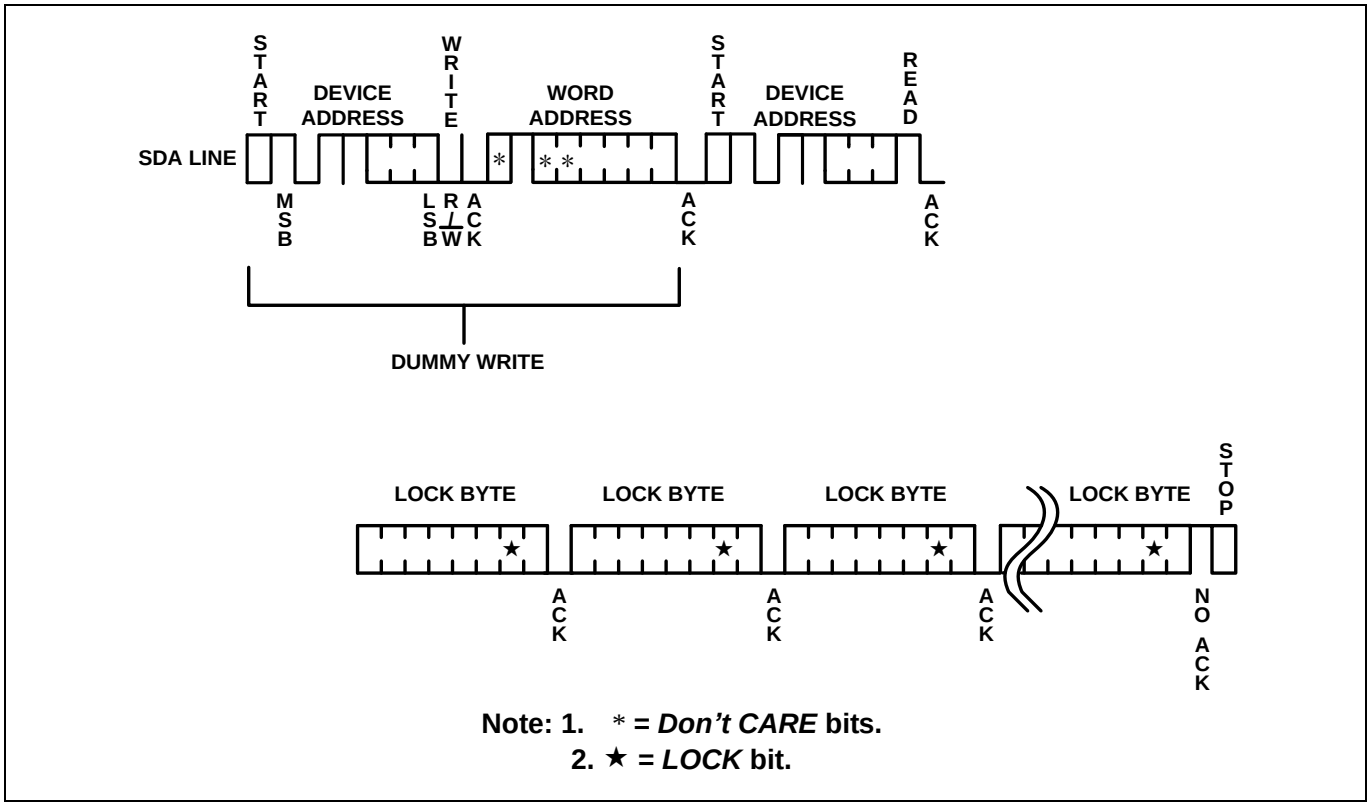
Note: 1. * = *Don't CARE* bits.

Figure 16. Lock Security Sector



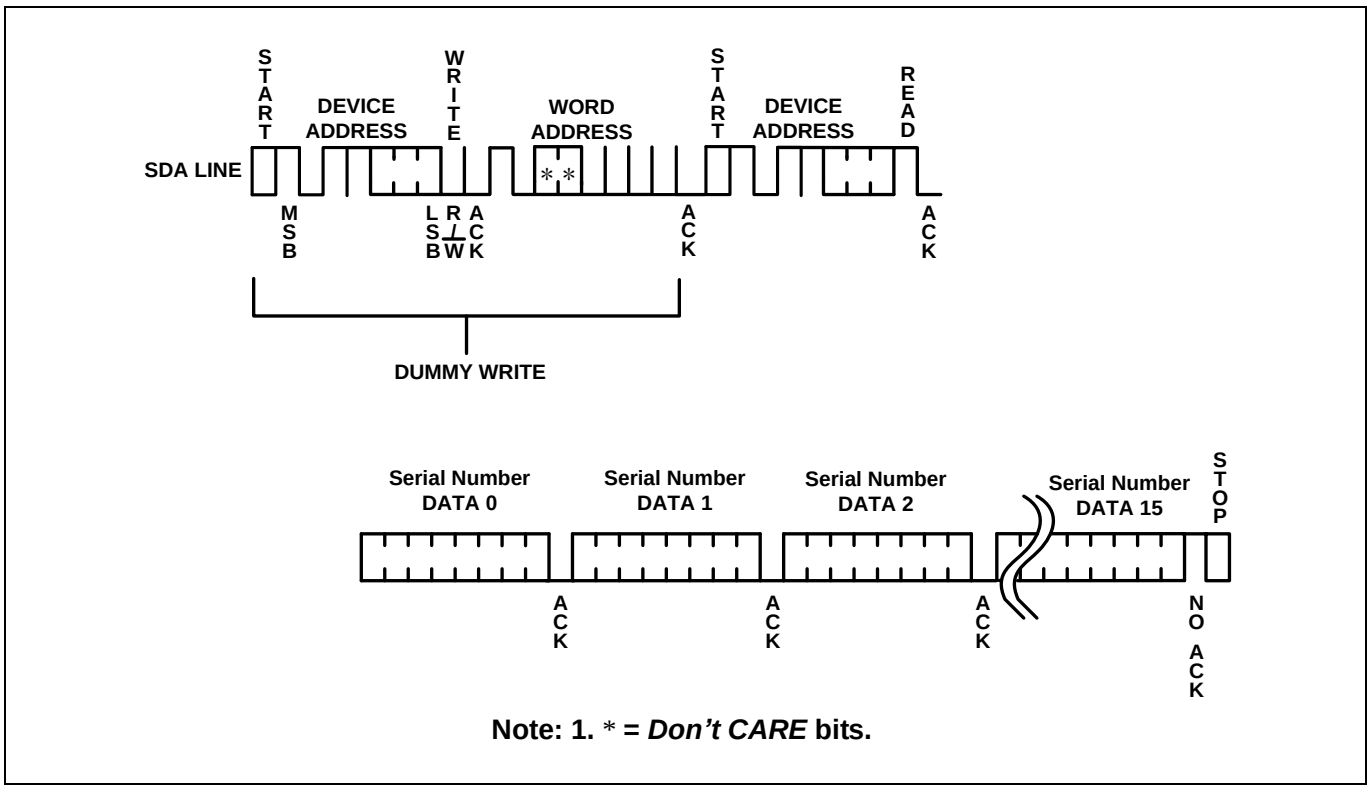
Note: 1. * = *Don't CARE* bits.

Figure 17. Read Lock Status



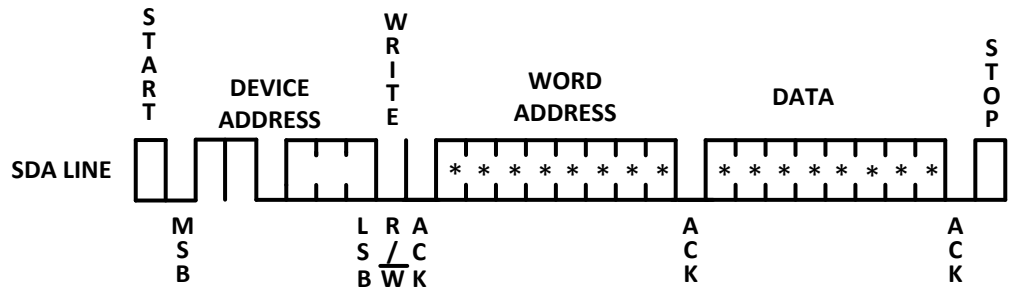
Note: 1. * = *Don't CARE* bits.
2. ★ = *LOCK* bit.

Figure 18. Read Unique ID



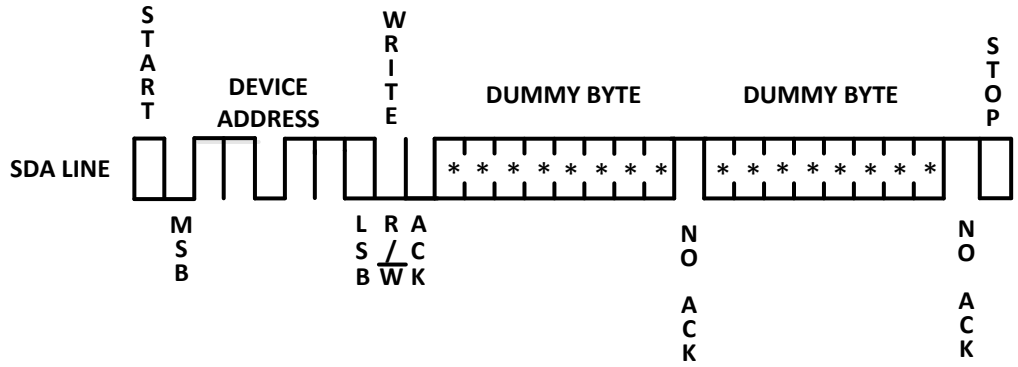
Note: 1. * = *Don't CARE* bits.

Figure 19. Set and clear the write protection (SWPn and CWP)



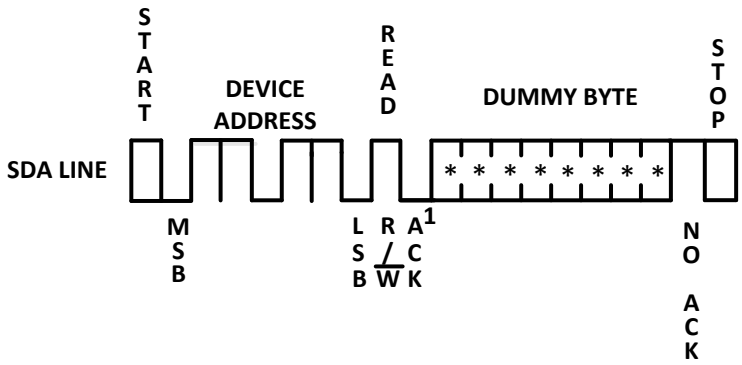
Note: 1. * = *Don't CARE* bits.

Figure 20. Set Bank Address (SBA)



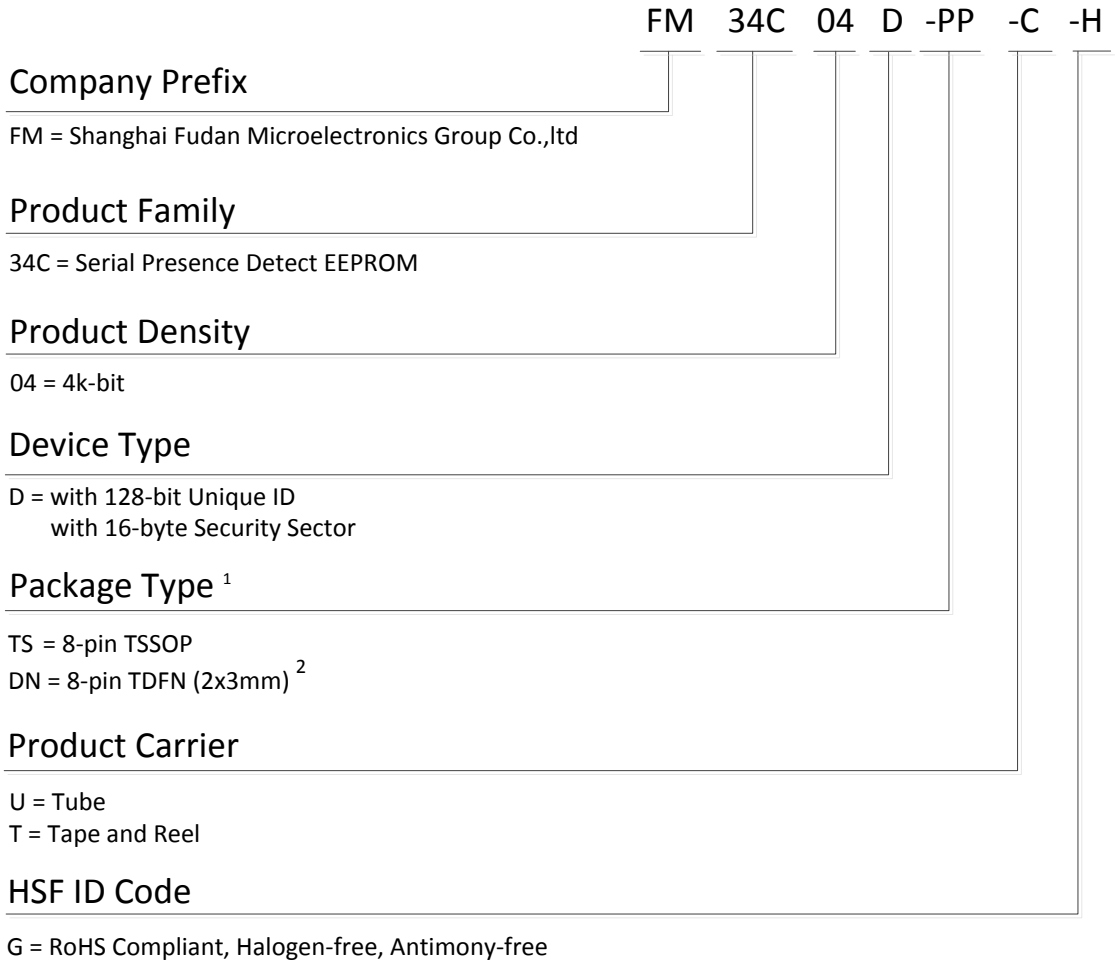
Note: 1. * = *Don't CARE* bits.

Figure 21. Read Bank Address (RBA)



Note:
1. **The FM34C04D will only acknowledge if Bank 0 is currently selected.**
2. *** = *Don't CARE* bits.**
3. **In accordance with the JEDEC spec, the master is allowed to read multiple dummy bytes, transmitting a NoAck after each byte.**

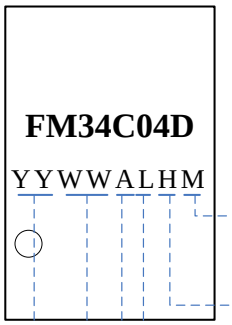
Ordering Information



Note:
1. For TS, DN package, MSL1 package are available, for detail please contact local sales office.
2. For Thinner package please contact local sales office.

Part Marking Scheme

TSSOP8



Moisture Sensitivity Level
1=MSL1

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

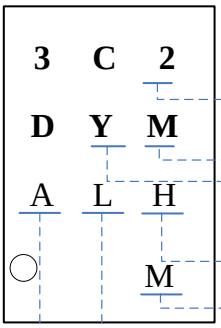
Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.

TDFN8 (2x3mm)



Product Density Code

The month (hexadecimal digit) in which the product was molded.

The year in which the product was sealed/molded, Using hexadecimal (1-9, A-C) representation

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

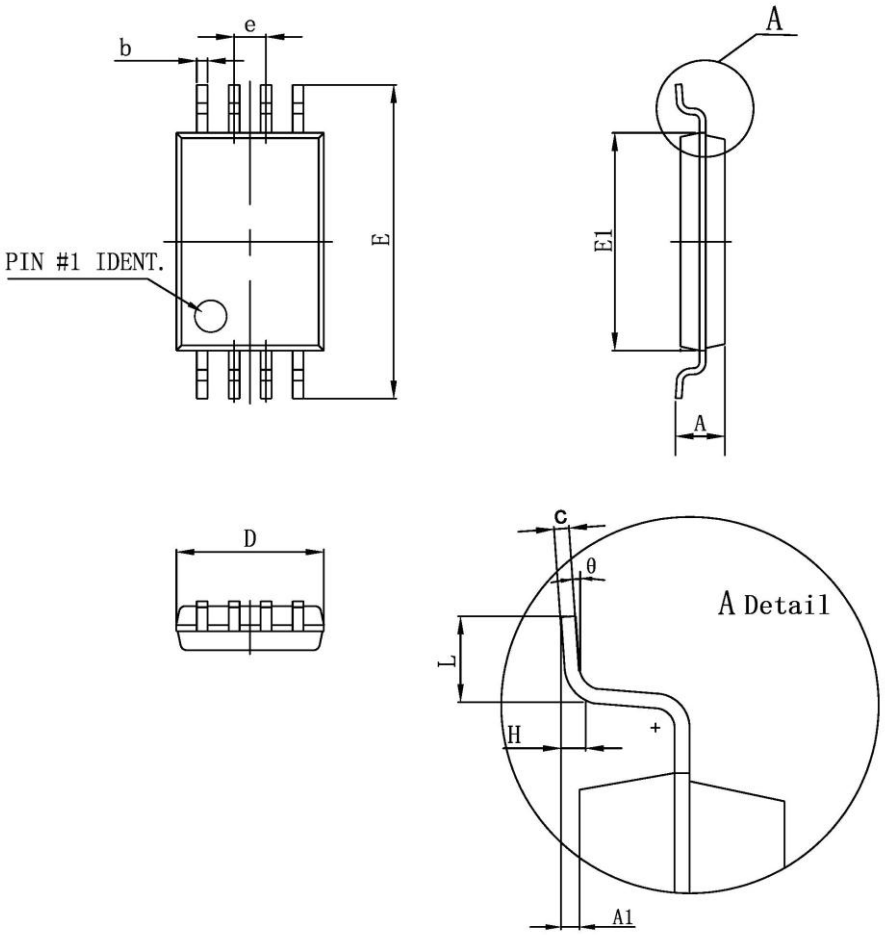
Moisture Sensitivity Level
1=MSL1

Lot Number（just with 0~9、A~Z）

Assembly's Code

Packaging Information

TSSOP8

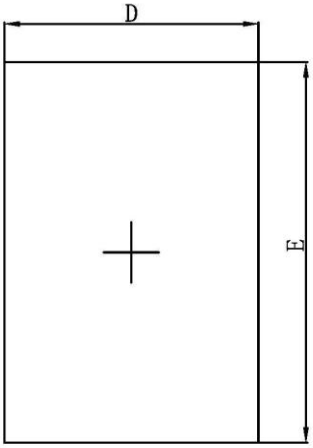


Symbol	MIN	MAX
D	2.900	3.100
E1	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E	6.200	6.600
A		1.200
A1	0.050	0.150
e	0.650 (BSC)	
L	0.450	0.750
θ	0°	8°

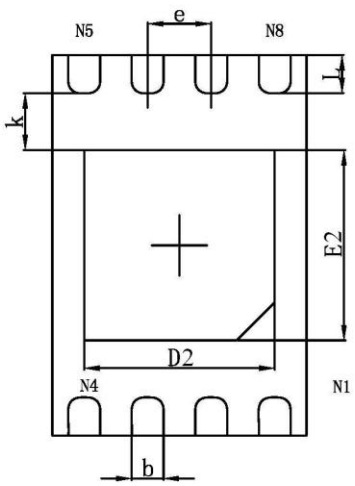
NOTE:

1. Dimensions are in Millimeters.

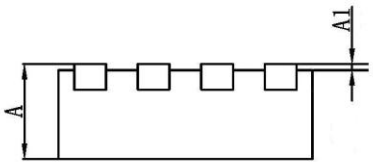
TDFN8 (2x3mm)



Top View



Bottom View



Side View

Symbol	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
D	1.900	2.100
E	2.900	3.100
D2	1.400	1.600
E2	1.400	1.700
k	0.150(MIN)	
b	0.200	0.300
e	0.500(TYP)	
L	0.200	0.500

NOTE:

1. **Dimensions are in Millimeters.**

Revision History

Version	Publication date	Pages	Revise Description
Preliminary	Oct. 2015	26	Initial document Release.
1.0	Apr. 2017	26	Corrected the typo.

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