



复旦微电子

# ***FM93C46A/56A/66A*** ***Three-wire Serial EEPROM***

**Datasheet**

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**Aug. 2017**



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## Description

FM93C46A/56A/66A provides 1k/2k/4k bits of serial electrically erasable programmable read-only memory (EEPROM), organized as 64/128/256 words of 16 bits each (when the ORG pin is connected to VCC), and 128/256/512 words of 8 bits each (when the ORG pin is connected to ground).

The FM93C46A/56A/66A is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Serial Clock (SK). Upon receiving a read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The write cycle is completely self-timed and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable State. When CS is brought "high" following the initiation of a write cycle, The DO pin outputs the Ready/ Busy status of the part.

The device is the best choice for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

## Features

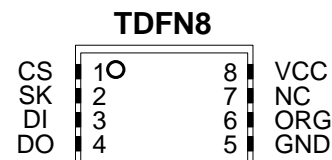
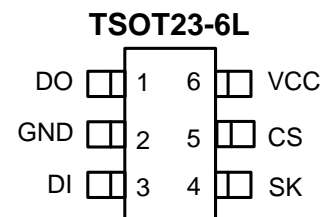
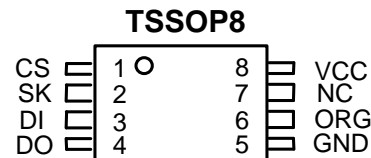
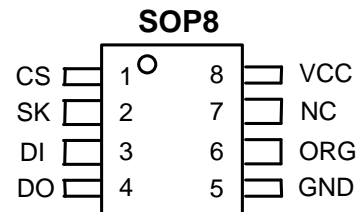
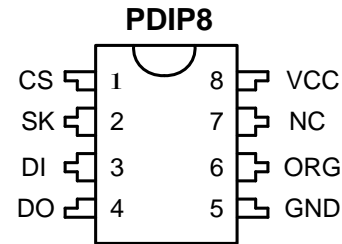
- **Three-wire Serial Interface**
- **Low-voltage and Standard-voltage Operation**  
1.7V~5.5V
- **2MHz (2.5V) and 1MHz (1.7V) Compatibility**
- **Dual organization: by word (x16) or byte (x8)**
- **Sequential read operation**
- **Programming instructions that work on: byte, word or entire memory**
- **Self-timed Write Cycle (5 ms max)**
- **READY/ BUSY signal during programming**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 40 Years**
- **PDIP8, (RoHS Compliant)**
- **SOP8, TSSOP8, TDFN8, TSOT23-6L Packages**  
(RoHS Compliant and Halogen-free)

## Absolute Maximum Ratings

Operating Temperature	-55°C ~ +125°C
Storage Temperature	-65°C ~ +150°C
Voltage on Any Pin with Respect to Ground	-1.0V ~ +7.0V
Maximum Operating Voltage	6.25V
DC output current	5.0 mA

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

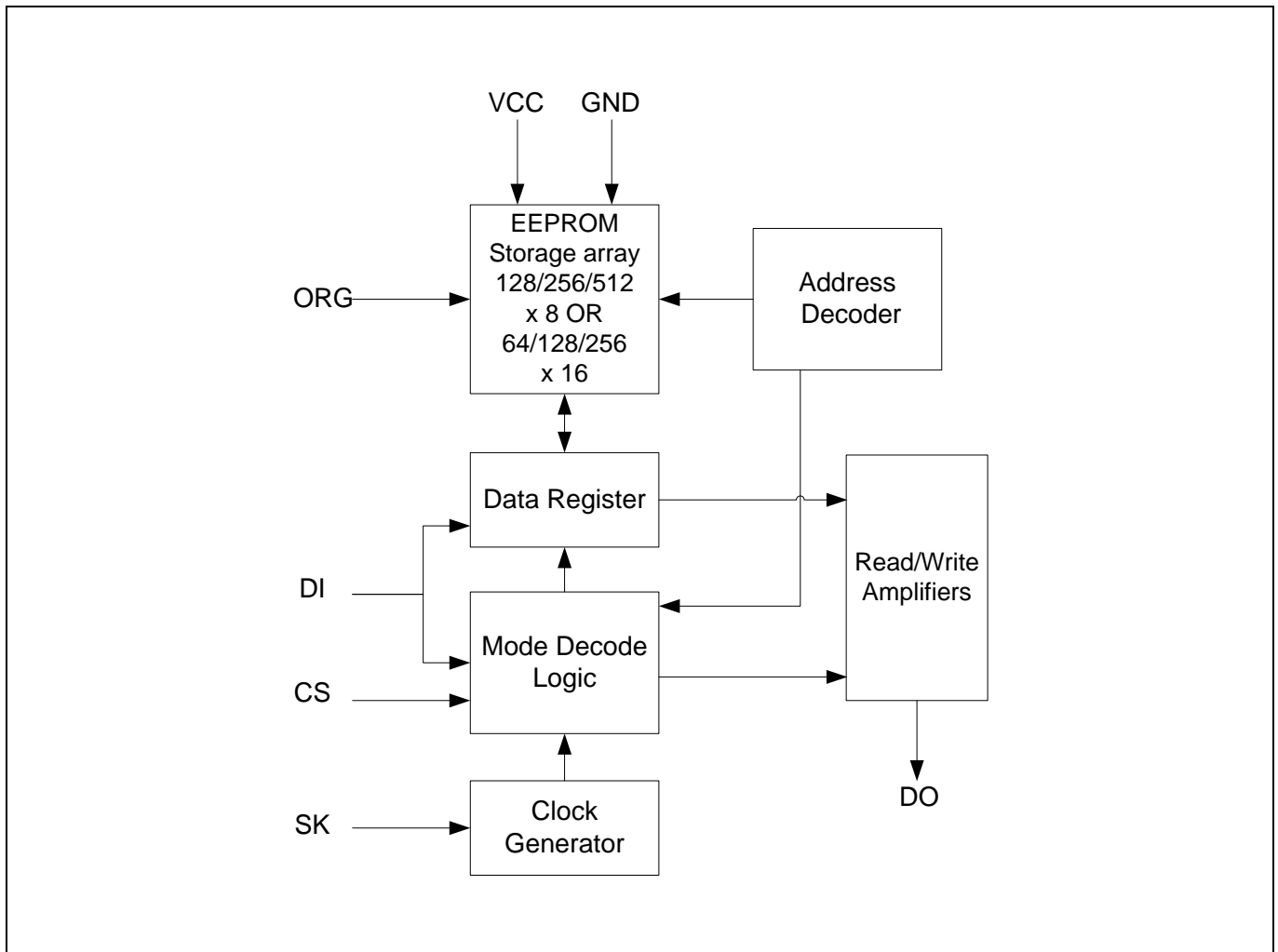
## Packaging Type



## Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
ORG	Organization Select
NC	No connect
VCC	Power Supply

Figure 1 Block Diagram





## Memory Organization

The FM93C46A/56A/66A memory is organized either as bytes (x8) or as words (x16). If Organization Select (ORG) is left unconnected (or connected to VCC) the x16 organization is selected; when Organization Select (ORG) is connected to Ground (VSS) the x8 organization is selected. When the FM93C46A/56A/66A is in Standby mode, Organization Select (ORG) should be set either to VSS or VCC for minimum power consumption. Any voltage between VSS and VCC applied to Organization Select (ORG) may increase the Standby current.

### Memory size versus organization

Device	Number of bits	Number of 8-bit bytes	Number of 16-bit words
FM93C66A	4096	512	256
FM93C56A	2048	256	128
FM93C46A	1024	128	64

## Instruction Set

The instruction set of the FM93C46A/56A/66A devices contains seven instructions, as summarized in *the table below*.

- Each instruction is preceded by a rising edge on Chip Select Input (CS) with Serial Clock (SK) being held low.
- A start bit, which is the first '1' read on Serial Data Input (DI) during the rising edge of Serial Clock (SK).
- Two op-code bits, read on Serial Data Input (DI) during the rising edge of Serial Clock (SK). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the FM93C46A, the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization. For the FM93C56A and FM93C66A, the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization.

Instruction	Device Type	SB	Op Code	Address		Data		Comments
				x8 (1) (2)	x16 (1) (3)	x8	x16	
READ	FM93C46A	1	10	A6-A0	A5-A0			Read Address AN-A0
	FM93C56A	1	10	A8-A0	A7-A0			
	FM93C66A	1	10	A8-A0	A7-A0			
EWEN	FM93C46A	1	00	11XXXXXX	11XXXX			Write Enable
	FM93C56A	1	00	11XXXXXXXX	11XXXXXXXX			
	FM93C66A	1	00	11XXXXXXXX	11XXXXXXXX			
ERASE	FM93C46A	1	11	A6-A0	A5-A0			Clear Address AN-A0
	FM93C56A	1	11	A8-A0	A7-A0			
	FM93C66A	1	11	A8-A0	A7-A0			
WRITE	FM93C46A	1	01	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN-A0
	FM93C56A	1	01	A8-A0	A7-A0	D7-D0	D15-D0	
	FM93C66A	1	01	A8-A0	A7-A0	D7-D0	D15-D0	
ERAL	FM93C46A	1	00	10XXXXXX	10XXXX			Clear All Addresses
	FM93C56A	1	00	10XXXXXXXX	10XXXXXXXX			
	FM93C66A	1	00	10XXXXXXXX	10XXXXXXXX			
WRAL	FM93C46A	1	00	01XXXXXX	01XXXX	D7-D0	D15-D0	Write All Addresses
	FM93C56A	1	00	01XXXXXXXX	01XXXXXXXX	D7-D0	D15-D0	
	FM93C66A	1	00	01XXXXXXXX	01XXXXXXXX	D7-D0	D15-D0	
EWDS	FM93C46A	1	00	00XXXXXX	00XXXX			Write Disable
	FM93C56A	1	00	00XXXXXXXX	00XXXXXXXX			
	FM93C66A	1	00	00XXXXXXXX	00XXXXXXXX			

Note:

1. X = Don't Care bit.
2. Address bit A8 is not decoded by the FM93C56A.
3. Address bit A7 is not decoded by the FM93C56A.

## Functional Description

The FM93C46A/56A/66A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. *A valid instruction starts with a rising edge of CS* and consists of a start bit (logic "1") followed by the appropriate op code and the desired memory address location.

**READ (READ):** The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock (SK).. It should be noted that a dummy bit (logic "0") precedes the 8- or 16-bit data output string.

**ERASE/WRITE (EWEN):** To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or VCC power is removed from the part.

**ERASE (ERASE):** The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/  $\overline{\text{Busy}}$  status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

**WRITE (WRITE):** The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle,  $t_{WP}$ , starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/  $\overline{\text{Busy}}$  status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/  $\overline{\text{Busy}}$  status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle,  $t_{WP}$ .

**ERASE ALL (ERAL):** The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the Ready/  $\overline{\text{Busy}}$  status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). The ERAL instruction is valid only at  $V_{CC} = 2.5V \sim 5.5V$

**WRITE ALL (WRAL):** The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/  $\overline{\text{Busy}}$  status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). The WRAL instruction is valid only at  $V_{CC} = 2.5V \sim 5.5V$ .

**ERASE/WRITE DISABLE (EWDS):** To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

**READY/  $\overline{\text{BUSY}}$  status:** While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal ( $DO=0$ ) is returned whenever Chip Select input (CS) is driven high. (Please note, though, that there is an initial delay, of  $t_{CS}$ , before this status information becomes available). In this state, the FM93C46A/56A/66A ignores any data on the bus. When the Write cycle is completed, and Chip Select Input (CS) is driven high, the Ready signal ( $DO=1$ ) indicates that the FM93C46A/56A/66A is ready to receive the next instruction. Serial Data Output (DO) remains set to 1 until the Chip Select Input (CS) is brought low or until a new start bit is decoded.

## Timing Diagrams

Figure 2 READ Timing

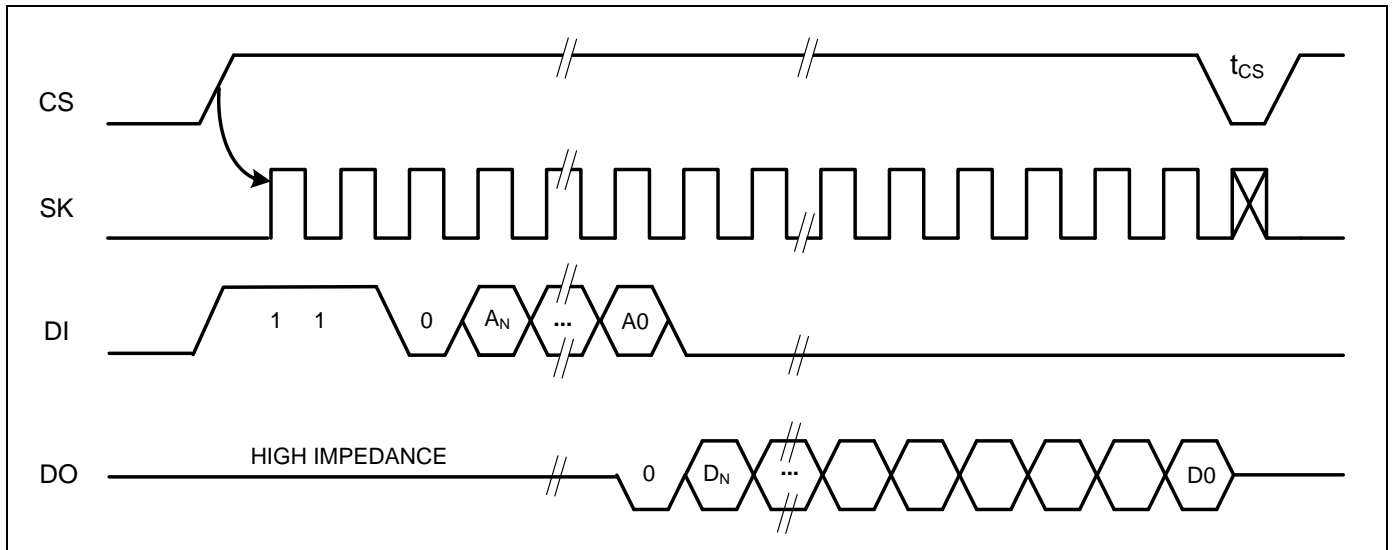
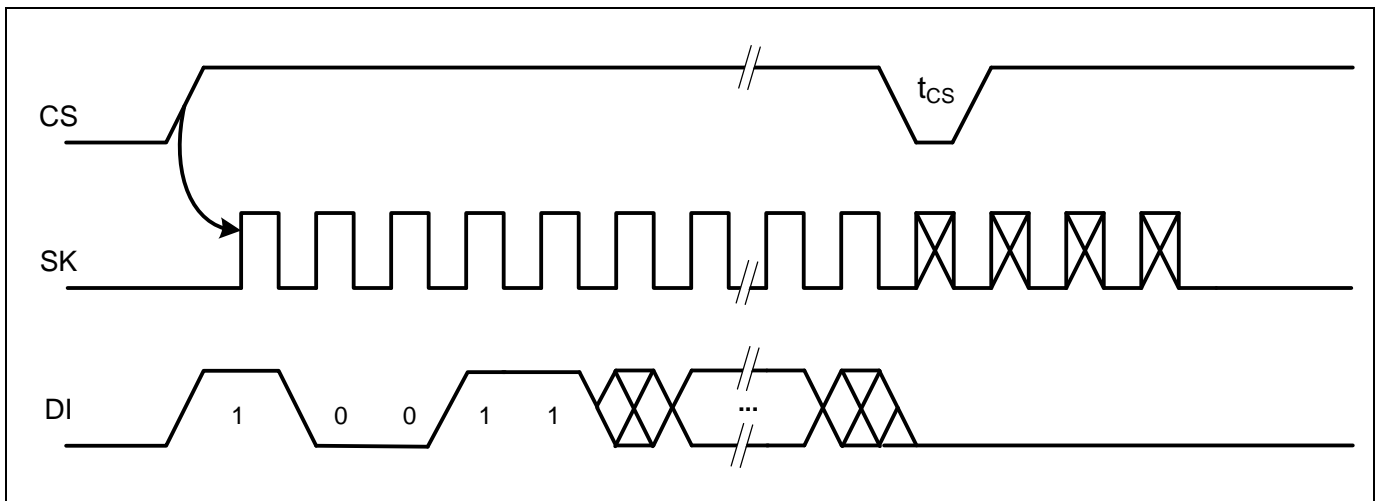
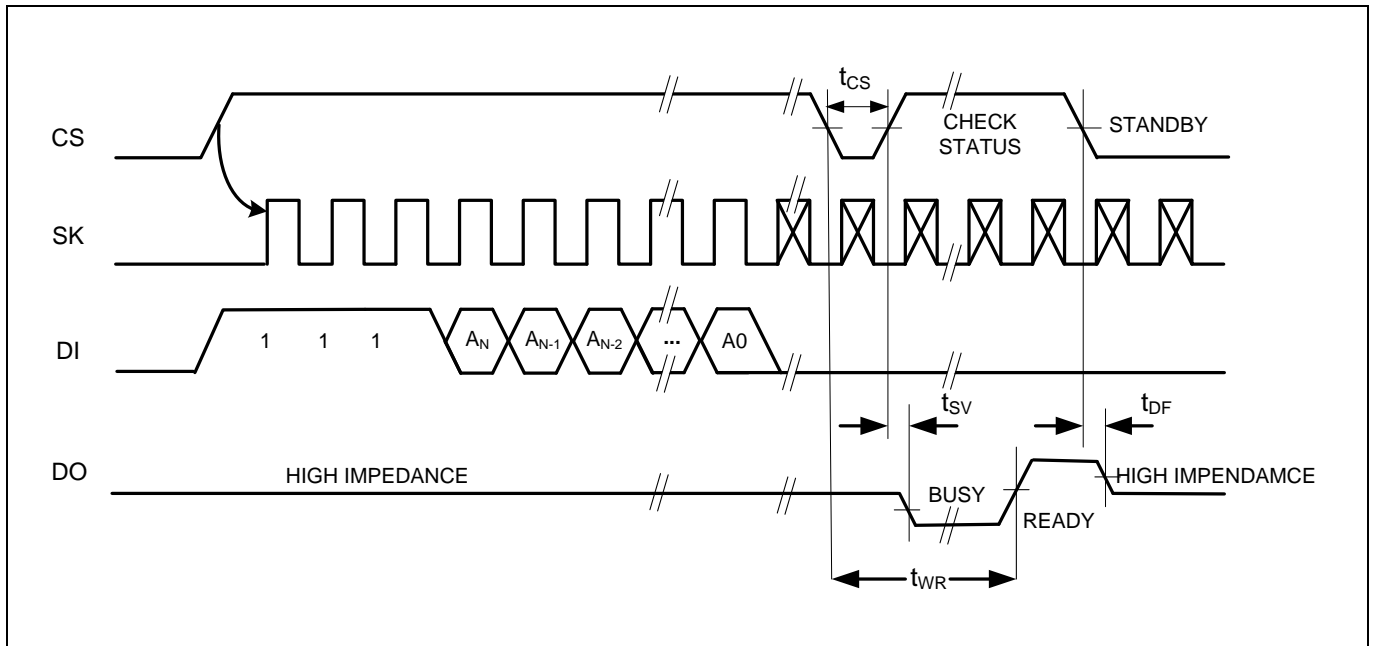


Figure 3 EWEN Timing





**Figure 4 ERASE Timing**



**Figure 5 WRITE Timing**

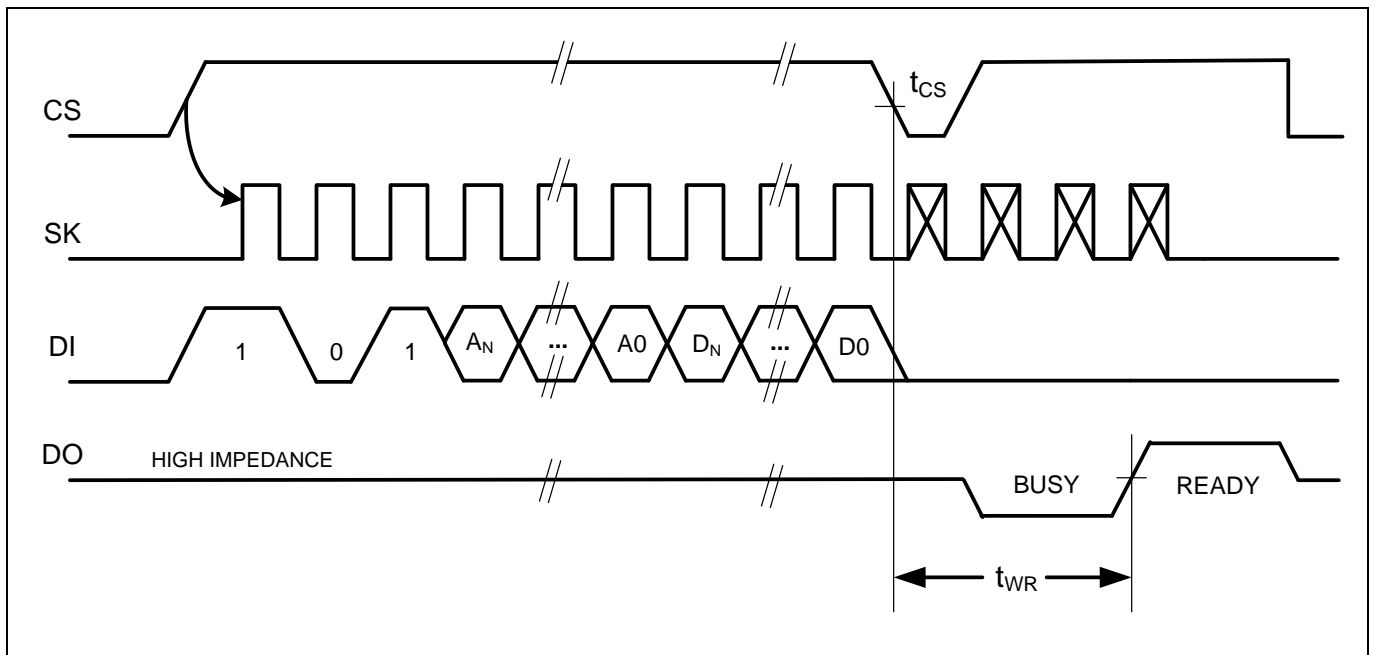


Figure 6 ERAL Timing

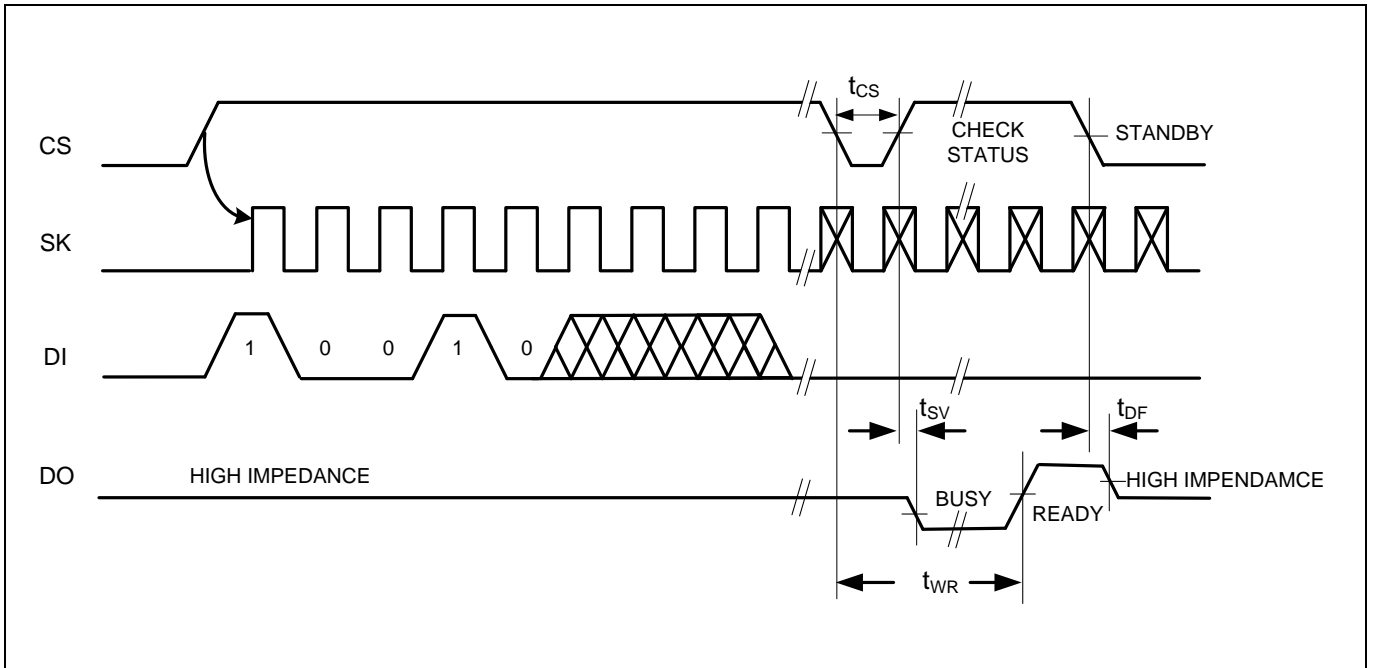


Figure 7 WRAL Timing

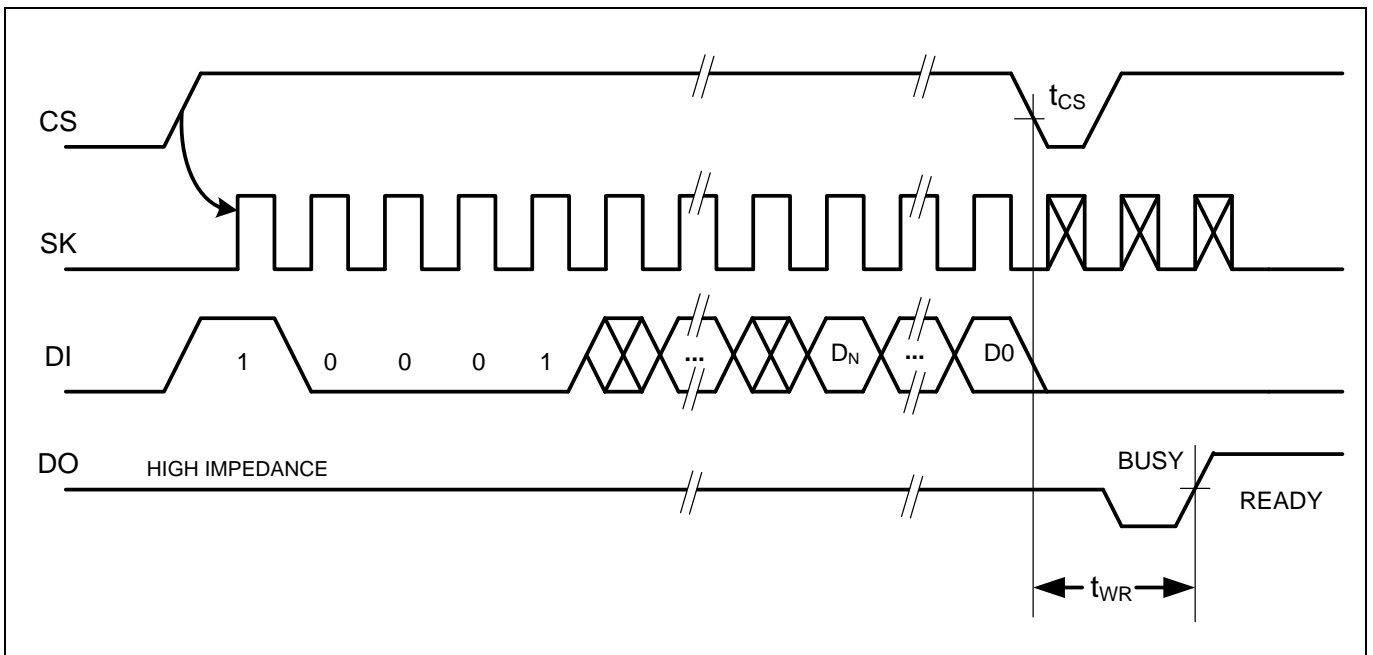


Figure 8 EWDS Timing

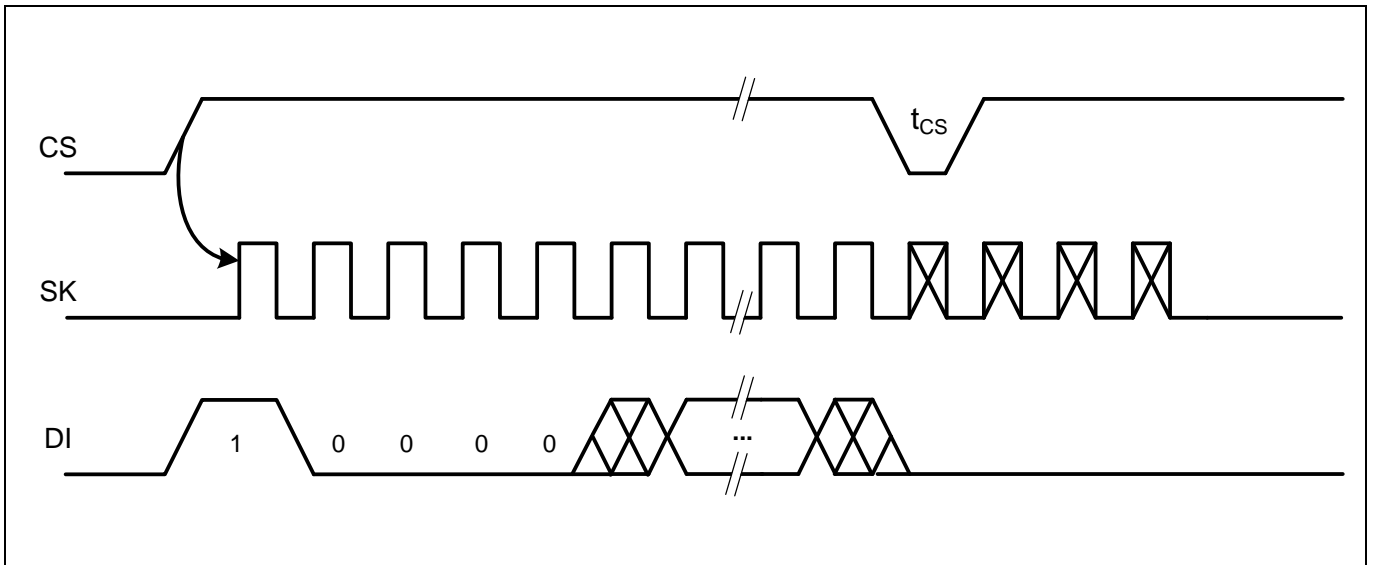
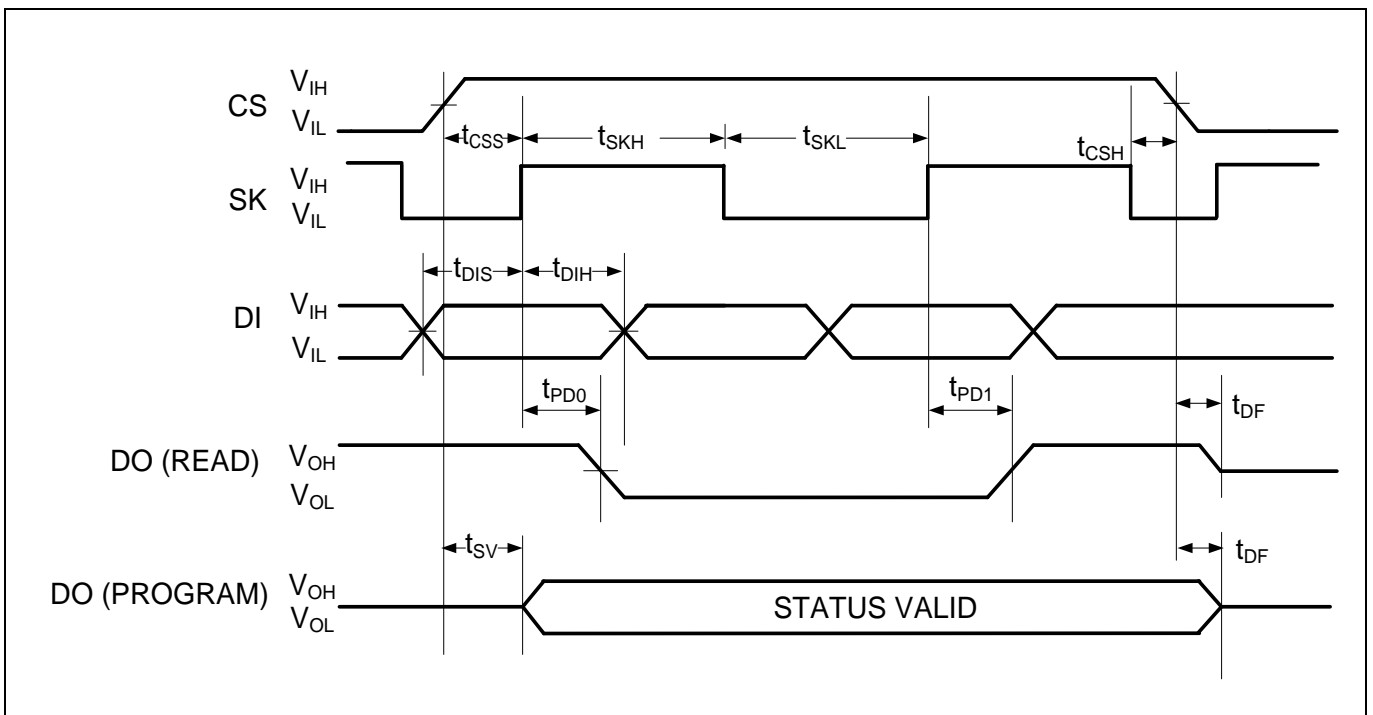


Figure 9 BUS Timing



## Pin Capacitance

Symbol	Parameter	Test Condition	Max	Units
$C_{IN}^{(1)}$	Input Capacitance	$V_{IN} = 0V, f = 1 \text{ MHz}$	6	pF
$C_{OUT}^{(1)}$	Output Capacitance	$V_{OUT} = 0V, f = 1 \text{ MHz}$	8	pF

**Note:** 1. This parameter is characterized and is not 100% tested.

## DC Characteristics

Applicable over recommended operating range from:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +1.7\text{V}$  to  $+5.5\text{V}$ , (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Max	Units
$V_{CC}$	Supply Voltage			1.7	5.5	V
$I_{CC}$	Supply	$V_{CC} = 5.0\text{V}, f_{sk} = 2.0 \text{ MHz}$	CS = $V_{IH}$ , DO = open		2.0	mA
		$V_{CC} = 1.7\text{V}, f_{sk} = 1.0 \text{ MHz}$			1.0	mA
$I_{SB}$	Standby Current	$V_{CC} = 5\text{V}$	CS = SK = GND, ORG = $V_{CC}/\text{GND}$		15.0	$\mu\text{A}$
		$V_{CC} = 1.7\text{V}$			2.0	$\mu\text{A}$
$I_{LI}$	Input Leakage	$0\text{V} \leq V_{IN} \leq V_{CC}$		-1.0	1.0	$\mu\text{A}$
$I_{LO}$	Output Leakage	$0\text{V} \leq V_{OUT} \leq V_{CC}; \text{DO} = \text{Hi-Z}$		-1.0	1.0	$\mu\text{A}$
$V_{IL}^{(1)}$	Input Low Voltage			-0.45	$0.2V_{CC}$	V
$V_{IH}^{(1)}$	Input High Voltage			$0.8V_{CC}$	$V_{CC} + 0.5$	V
$V_{OL}$	Output Low Voltage	$V_{CC} = 5\text{V}$	$I_{OL} = 2.1 \text{ mA}$		0.4	V
		$V_{CC} = 1.7\text{V}$	$I_{OL} = 100 \mu\text{A}$		0.2	V
$V_{OH}$	Output High Voltage	$V_{CC} = 5\text{V}$	$I_{OH} = -400 \mu\text{A}$	$0.8V_{CC}$		V
		$V_{CC} = 1.7\text{V}$	$I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$		V

**Note:** 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.

## AC Characteristics

Applicable over recommended operating range from:  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 1.7\text{V}$  to  $5.5\text{V}$ ,  $C_L = 100\text{ pF}$  (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	$1.7\text{V} \leq V_{CC} \leq 2.5\text{V}$		$2.5\text{V} < V_{CC} \leq 5.5\text{V}$		Units
		Min	Max	Min	Max	
$f_{SK}$	SK Clock Frequency		1		2	MHz
$t_{SKL}$	SK Low Time	250		200		ns
$t_{SKH}$	SK High Time	250		200		ns
$t_{CS}$	Minimum CS Low	250		200		ns
$t_{CSS}$	CS Setup Time	50		50		ns
$t_{CSH}$	CS Hold Time	0		0		ns
$t_{DIS}$	DI Setup Time	100		50		ns
$t_{DIH}$	DI Hold Time	100		50		ns
$t_{PD1}$	Output Delay to "1"		400		200	ns
$t_{PD0}$	Output Delay to "0"		400		200	ns
$t_{SV}$	CS to Status Valid		400		200	ns
$t_{DF}$	CS to DO in High		200		100	ns
$t_{WR}$	Write Cycle		5		5	ms
Endurance <sup>(1)</sup>	3.3V, 25°C	1,000,000				Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:

Input pulse voltages:  $0.2 V_{CC}$  to  $0.8 V_{CC}$

Input rise and fall times:  $\leq 50\text{ ns}$

Input and output timing reference voltages:  $0.3 V_{CC} \sim 0.7 V_{CC}$



## Ordering Information

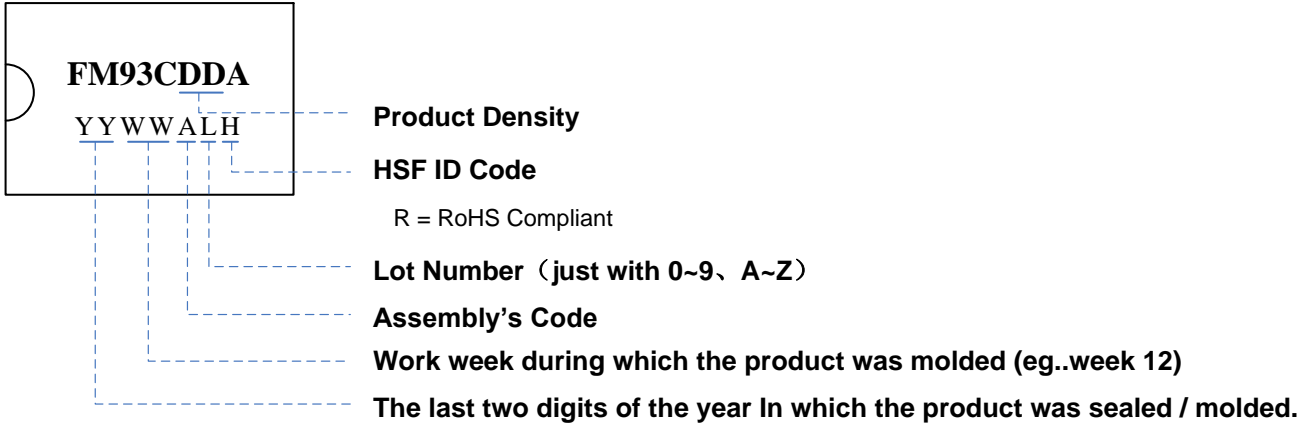
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<b>Company Prefix</b>							
FM = Shanghai Fudan Microelectronics Group Co.,ltd							
<b>Product Family</b>							
93C = Three-wire Serial EEPROM							
<b>Product Density</b>							
46 = 1K-bit 56 = 2K-bit 66 = 4K-bit							
<b>Supply Voltage</b>							
A = 1.7V to 5.5V							
<b>Package Type <sup>(1)</sup></b>							
PD = 8-pin PDIP SO = 8-pin SOP TS = 8-pin TSSOP DN = 8-pin TDFN ST = 6-pin TSOT23							
<b>Product Carrier</b>							
U = Tube T = Tape and Reel							
<b>HSF ID Code <sup>(2)</sup></b>							
Blank or R = RoHS Compliant G = RoHS Compliant, Halogen-free, Antimony-free							

Note:

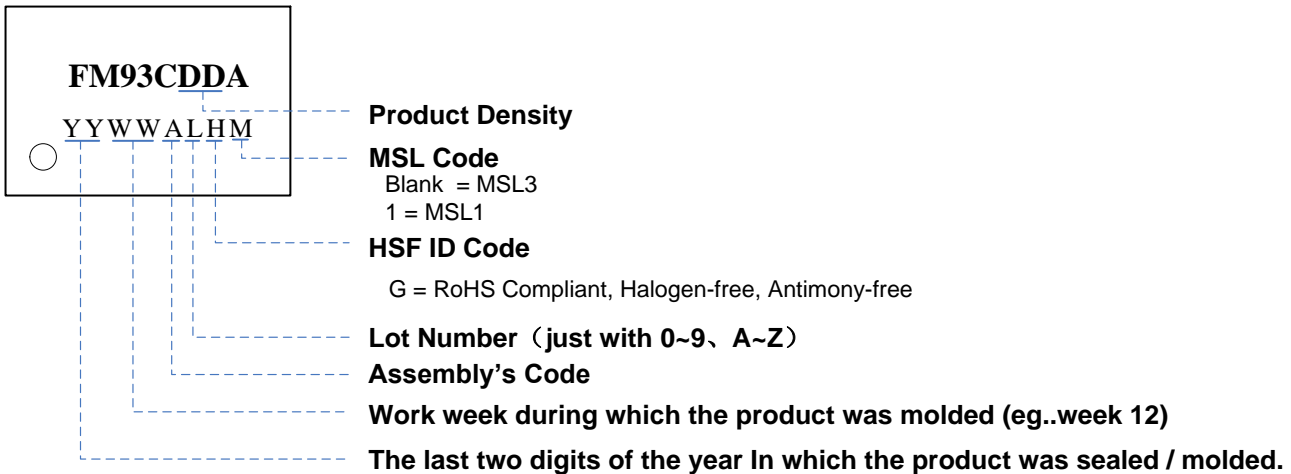
- For SO, TS, DN package, MSL1 package are available, for detail please contact local sales office..
- For PD package: R class offer only  
For SO, TS, DN and ST package: G class offer only.

## Part Marking Scheme

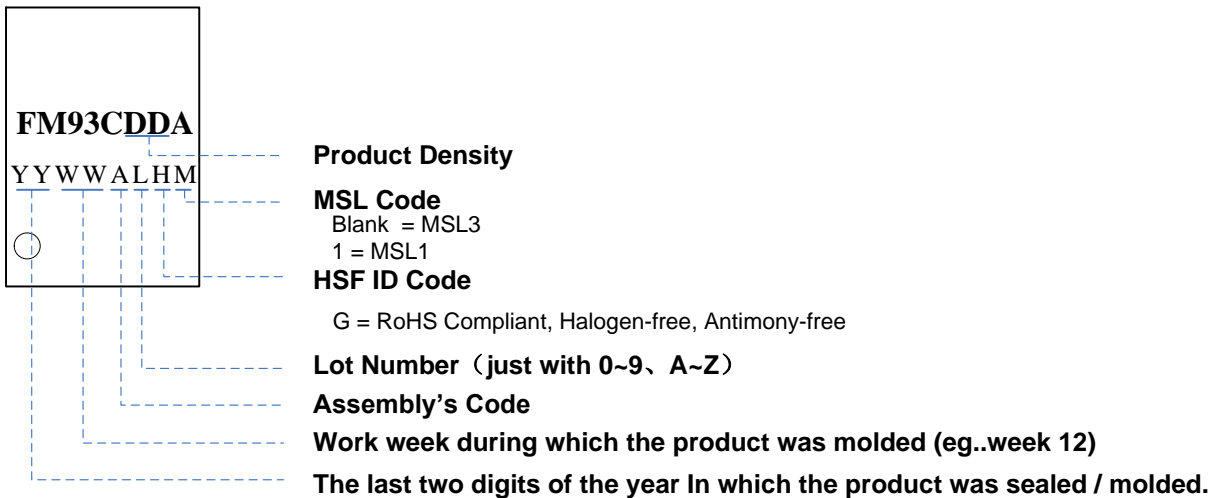
### PDIP8



### SOP8

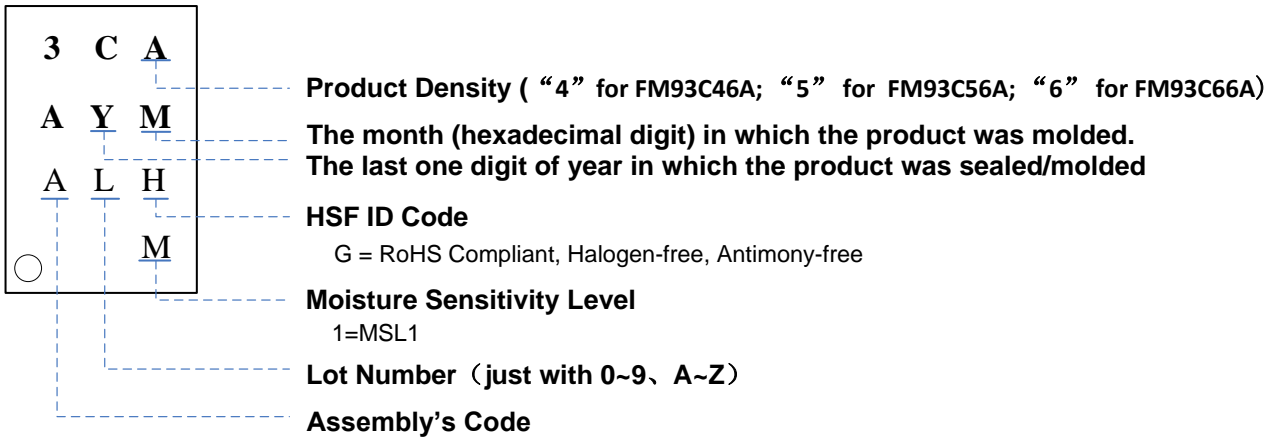


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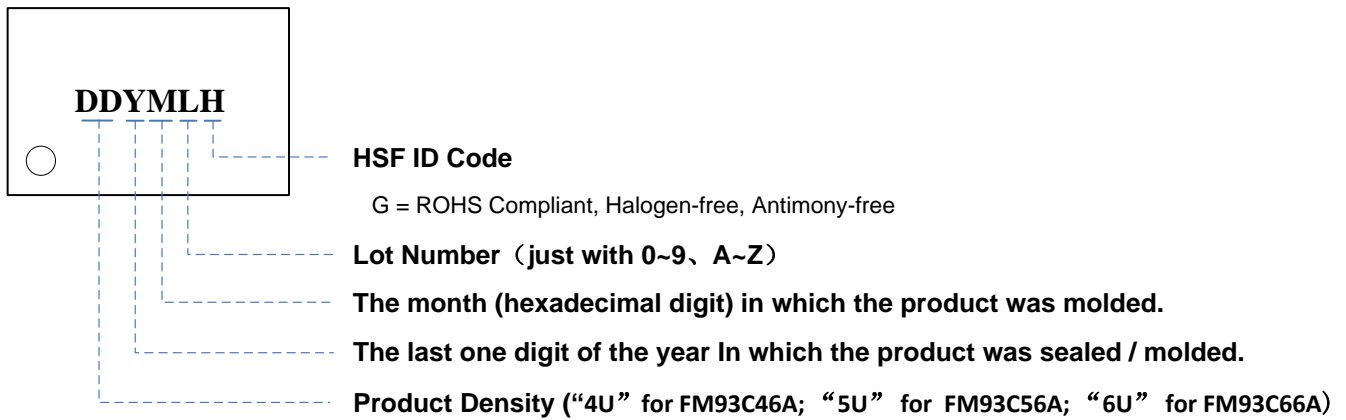




**TDFN8**



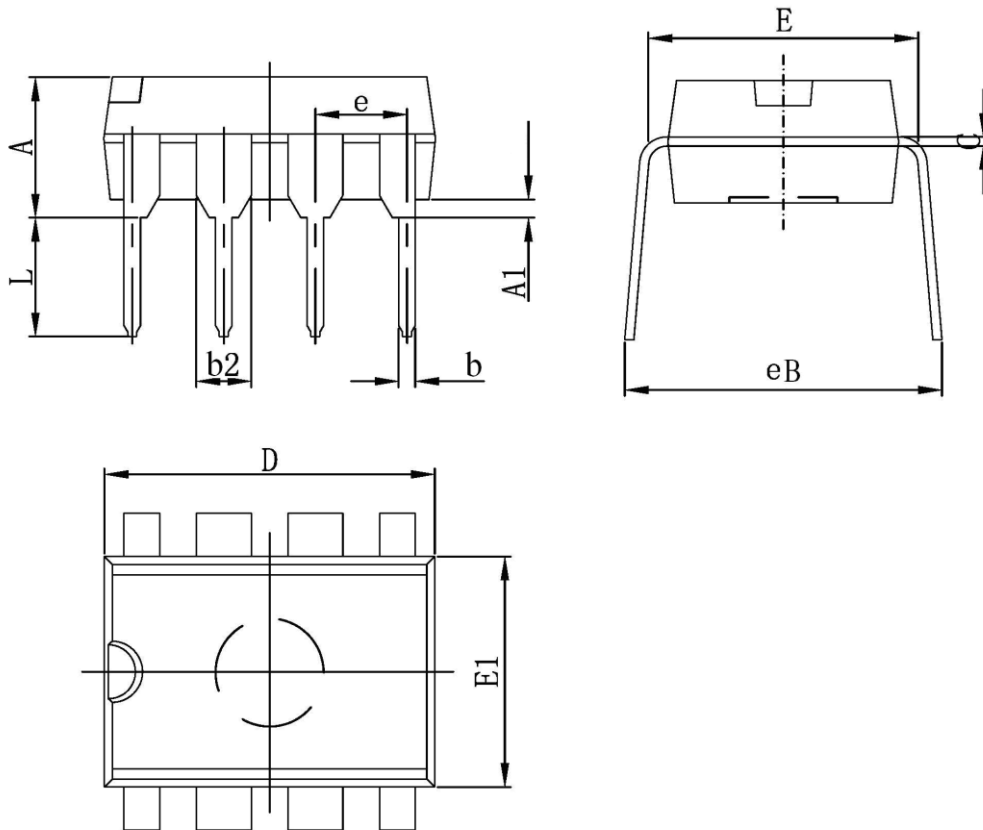
**TSOT23-6L**





## Packaging Information

### PDIP 8

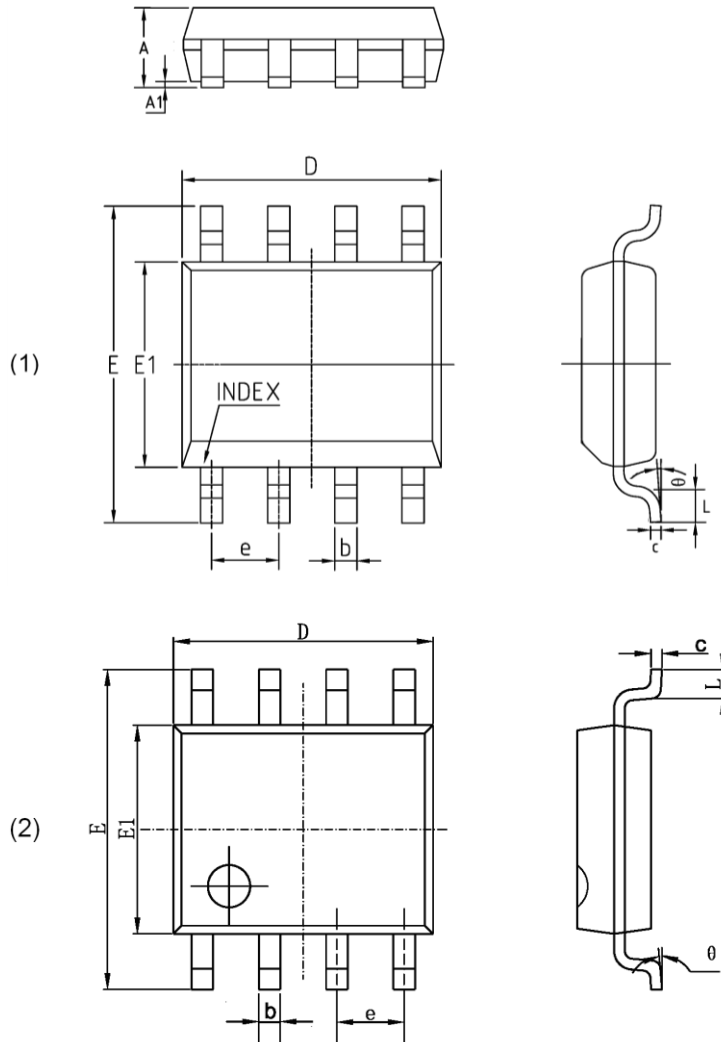


Symbol	MIN	MAX
A	---	5.000
A1	0.380	---
b	0.380	0.570
b2	1.300	1.700
C	0.200	0.360
D	9.000	10.000
E1	6.100	7.000
E	7.320	8.250
e	2.540(BSC)	
L	2.920	3.810
eB	---	10.900

**NOTE:**

1. Dimensions are in Millimeters.

SOP 8

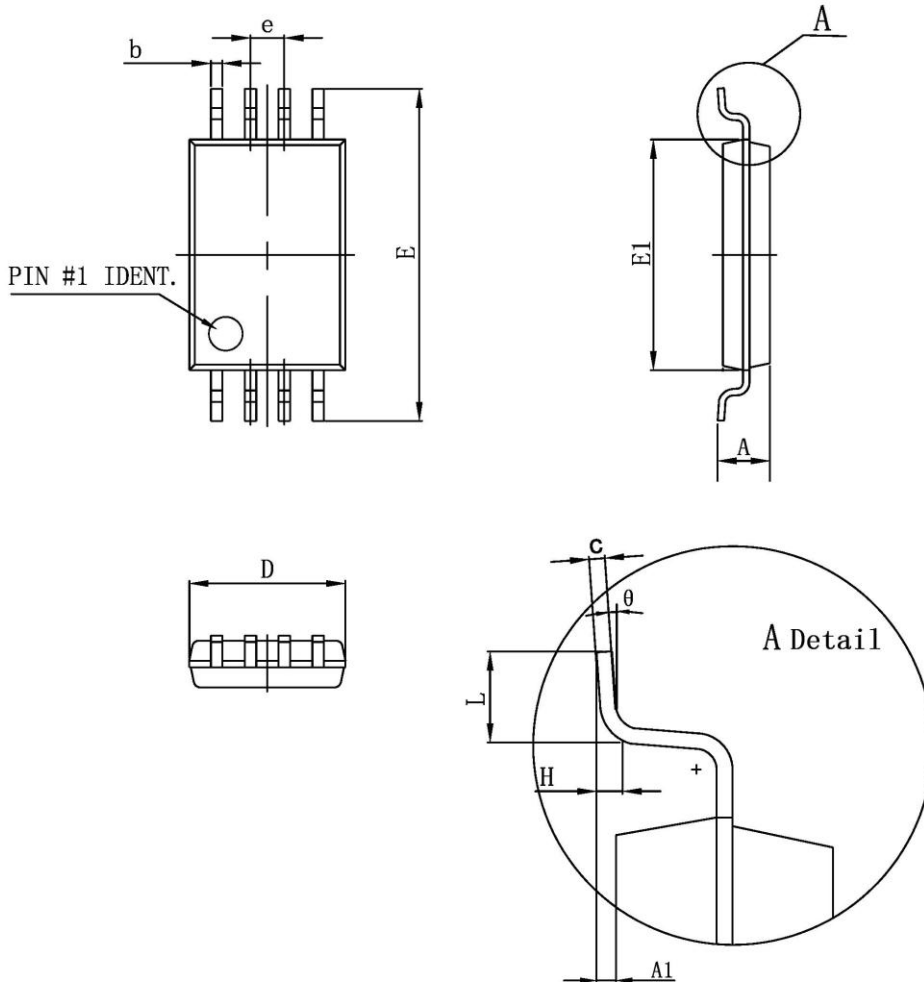


Symbol	MIN	MAX
A	1.350	1.750
A1	0.050	0.250
b	0.330	0.510
c	0.150	0.260
D	4.700	5.150
E1	3.700	4.100
E	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
$\theta$	0°	8°

NOTE:

1. Dimensions are in Millimeters.

## TSSOP8

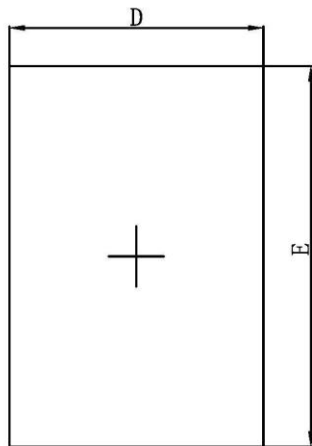


Symbol	MIN	MAX
D	2.900	3.100
E1	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E	6.200	6.600
A		1.200
A1	0.050	0.150
e	0.650 (BSC)	
L	0.450	0.750
θ	0°	8°

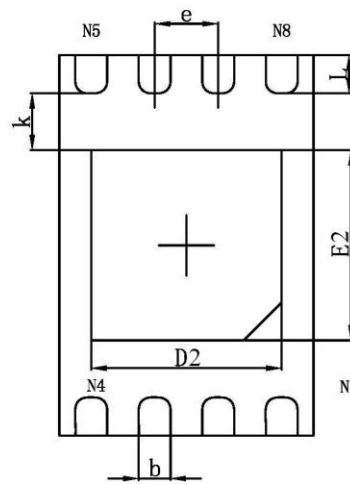
**NOTE:**

1. Dimensions are in Millimeters.

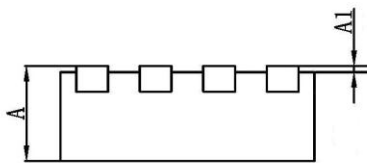
## TDFN8



Top View



Bottom View



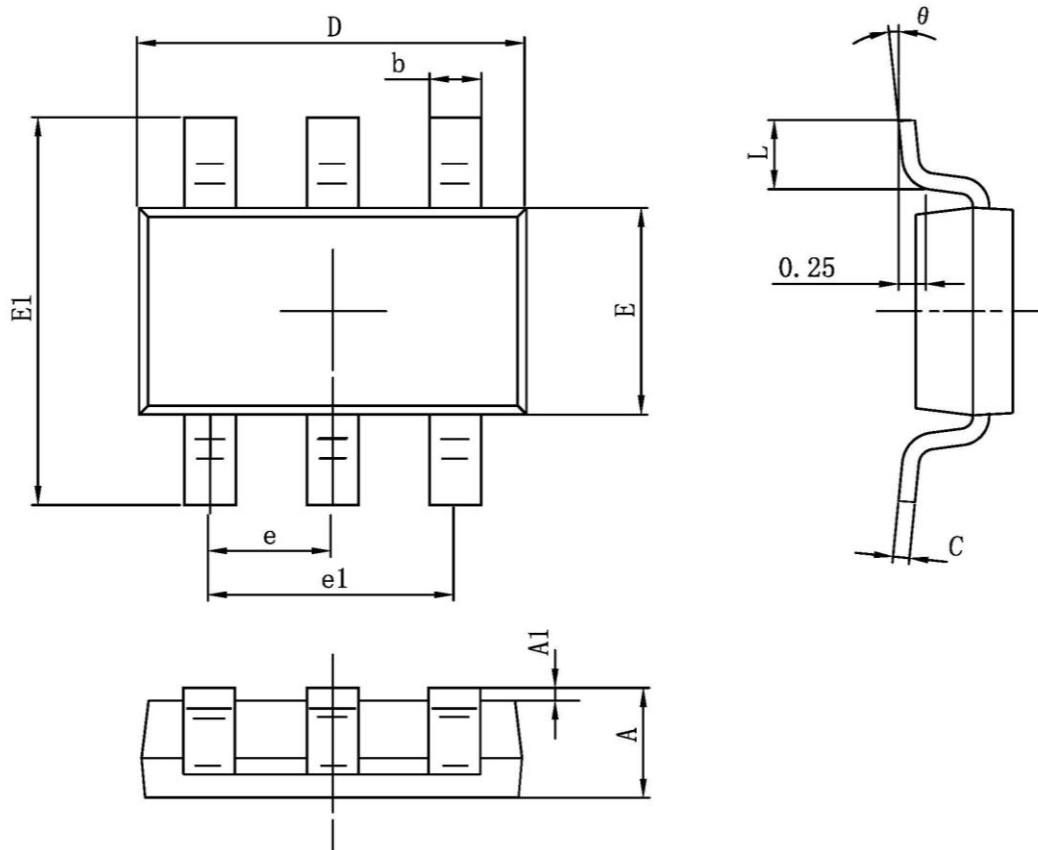
Side View

Symbol	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
D	1.900	2.100
E	2.900	3.100
D2	1.400	1.600
E2	1.400	1.700
k	0.150(MIN)	
b	0.200	0.300
e	0.500(TYP)	
L	0.200	0.500

## NOTE:

1. Dimensions are in Millimeters.

## TSOT23-6L



Symbol	MIN	MAX
A	0.700	0.900
A1	0.000	0.100
b	0.350	0.500
c	0.080	0.200
D	2.820	3.020
E	1.600	1.700
E1	2.650	2.950
e	0.950(BSC)	
e1	1.900(BSC)	
L	0.300	0.600
$\theta$	0°	8°

**NOTE:**

1. Dimensions are in Millimeters.



## Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	May. 2013	23		Initial Document Release
1.1	Feb. 2016	23		1. Updated " Part Marking Scheme" 2. Updated "packaging information"
1.2	Aug. 2017	23		1. Updated "packaging information"



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