



## Description

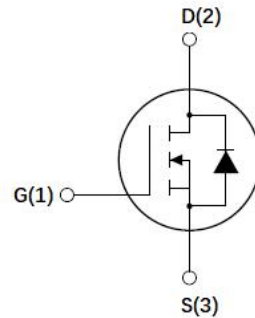
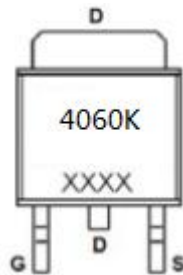
### Features

- 40V,60A
- $R_{DS(ON)}=6.8m\Omega$  (Typ.) @  $V_{GS} = 10V$
- $R_{DS(ON)}=9.5m\Omega$  (Typ.) @  $V_{GS} = 4.5V$
- High Density Cell Design for Ultra Low  $R_{DS(ON)}$
- Fully Characterized Avalanche Voltage and Current
- Good Stability and Uniformity with High  $E_{AS}$
- Excellent Package for Good Heat Dissipation

### Application

- Load Switch
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

## Package



## Absolute Maximum Ratings (T<sub>C</sub>=25°C unless otherwise specified)

Symbol	Parameter	Max.	Units
V <sub>DSS</sub>	Drain-Source Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25°C	60
		T <sub>C</sub> = 100°C	42
I <sub>DM</sub>	Pulsed Drain Current <sup>note1</sup>	210	A
E <sub>AS</sub>	Single Pulsed Avalanche Energy <sup>note2</sup>	106	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	42
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	2.8	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +175	°C



#### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.1	1.65	2.4	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note3</small>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	6.8	8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	9.5	12	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =15A	10	25	-	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1.0MHz	-	2246	-	pF
C <sub>oss</sub>	Output Capacitance		-	195	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	176	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V	-	52	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	8	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	14	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =20V, I <sub>D</sub> =30A, R <sub>L</sub> =1Ω, R <sub>GEN</sub> =3Ω, V <sub>GS</sub> =10V	-	13	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	37	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	46	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	15	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	60	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	210	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-	-	1.2	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	T <sub>J</sub> =25°C, I <sub>F</sub> =20A, dI/dt=100A/μs	-	15	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	8	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, R<sub>G</sub>=25Ω, L=0.5mH

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



### Typical Performance Characteristics

Figure 1: Output Characteristics

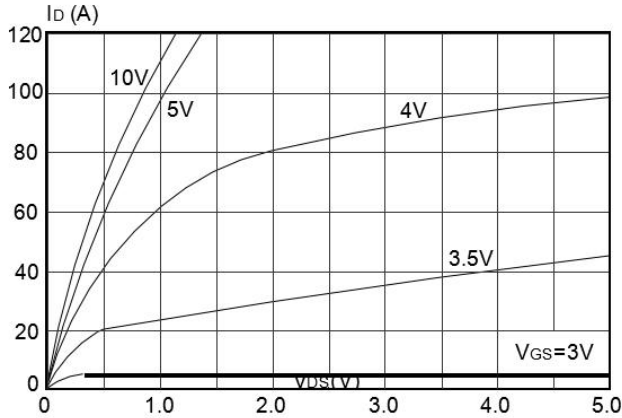


Figure 2: Typical Transfer Characteristics

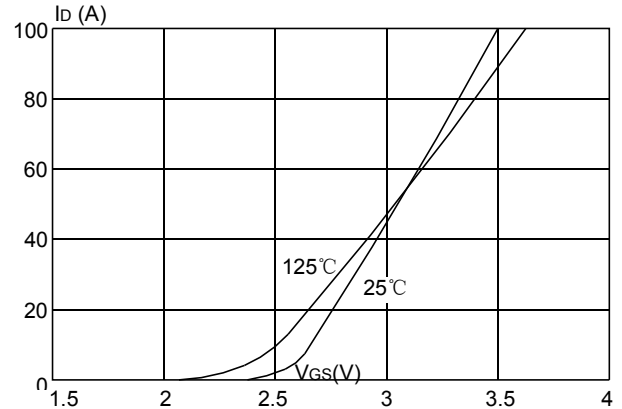


Figure 3: On-resistance vs. Drain Current

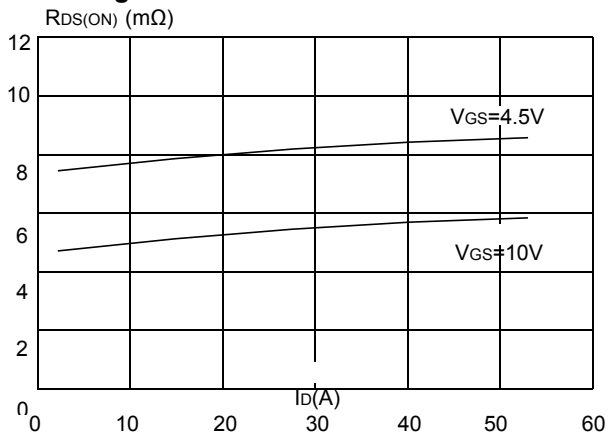


Figure 4: Body Diode Characteristics

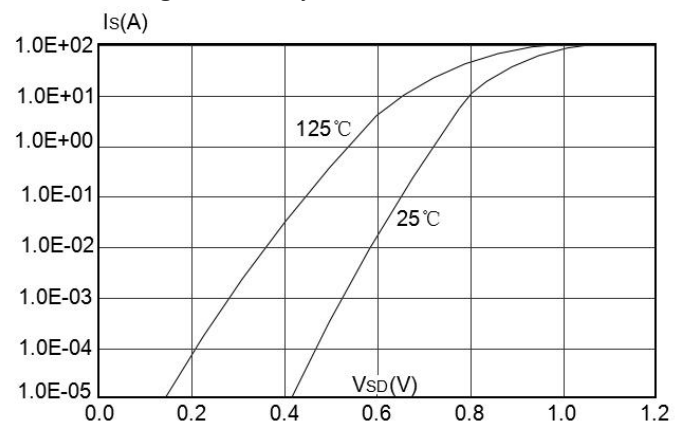


Figure 5: Gate Charge Characteristics

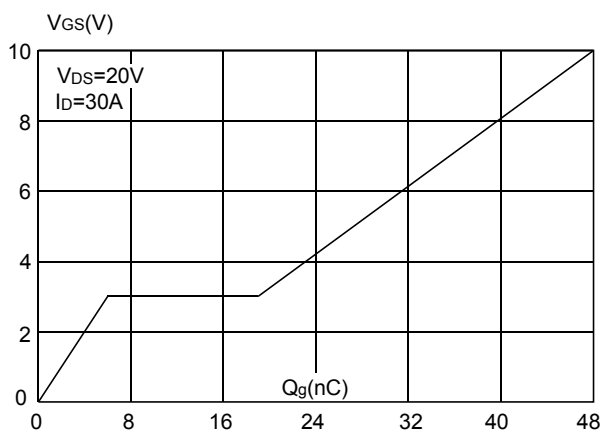
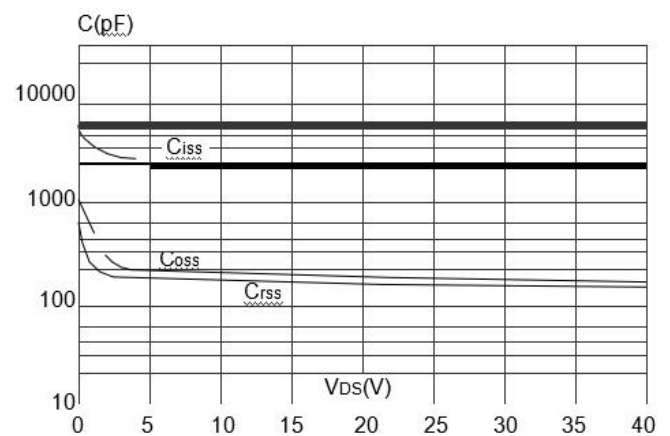
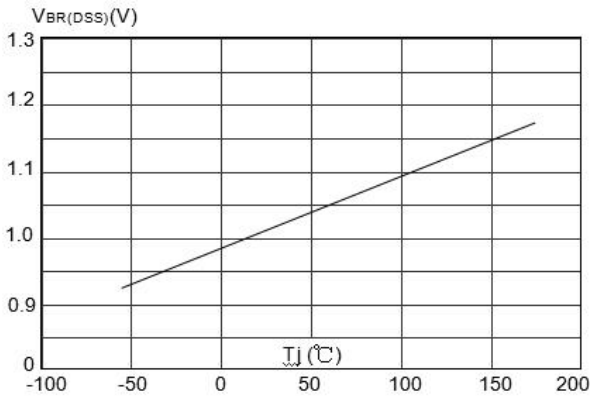


Figure 6: Capacitance Characteristics

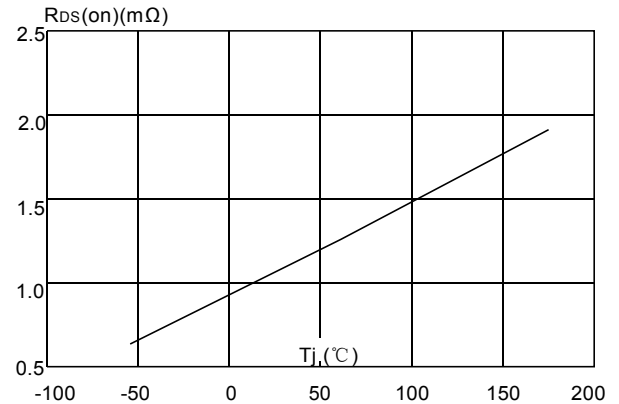




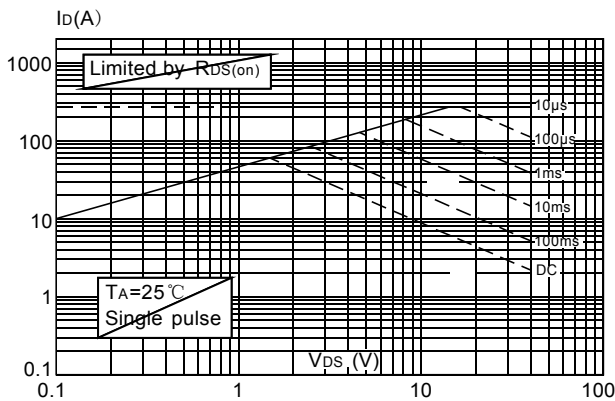
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



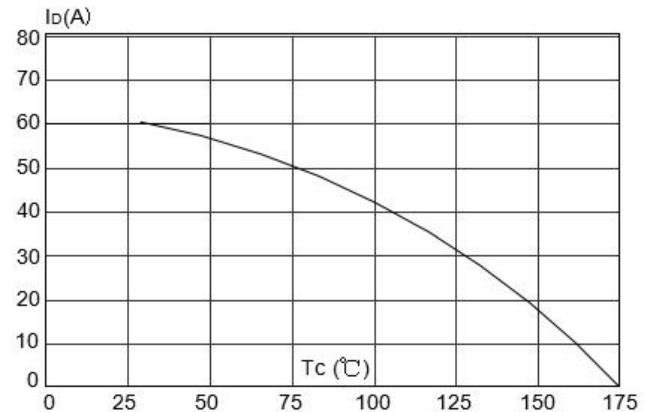
**Figure 8:** Normalized on Resistance vs. Junction Temperature



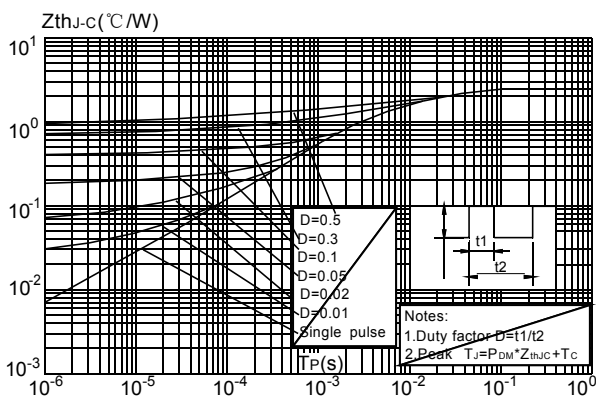
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-252,TO-251S)



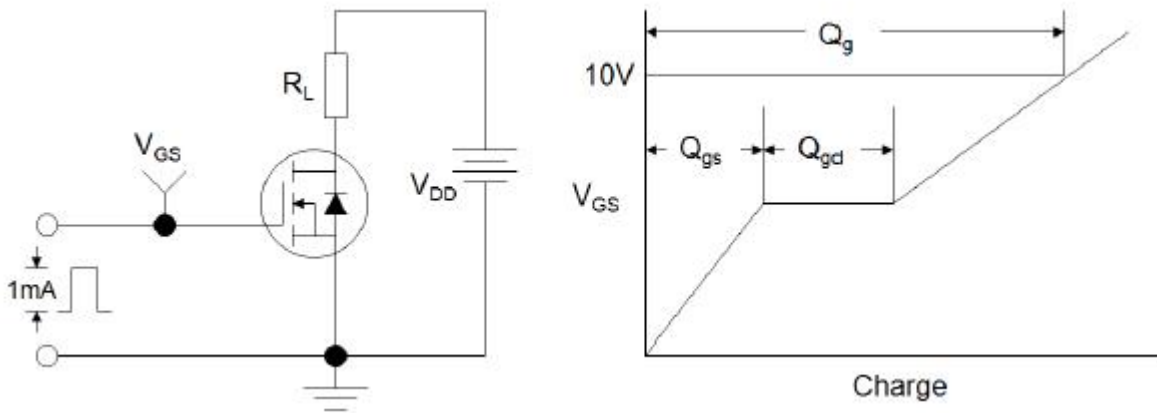


Figure1:Gate Charge Test Circuit & Waveform

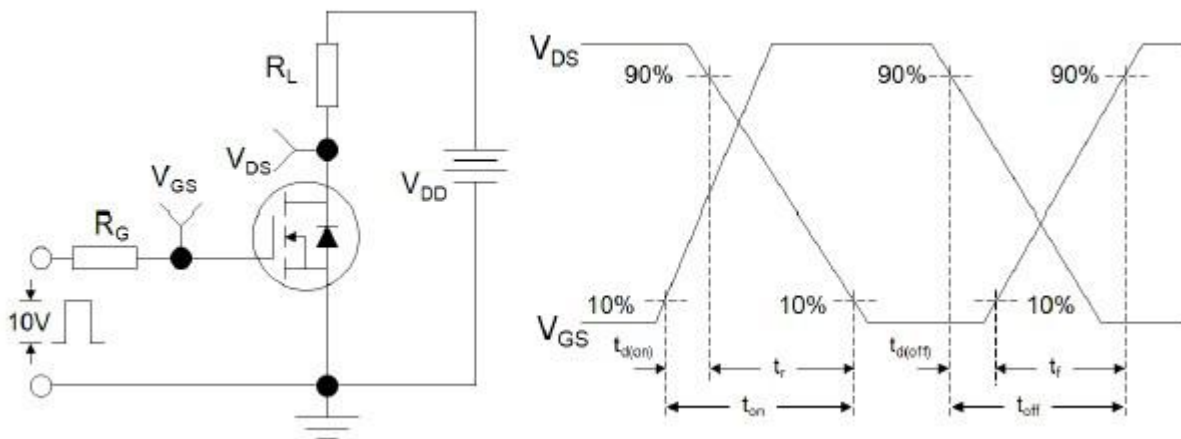


Figure 2: Resistive Switching Test Circuit & Waveforms

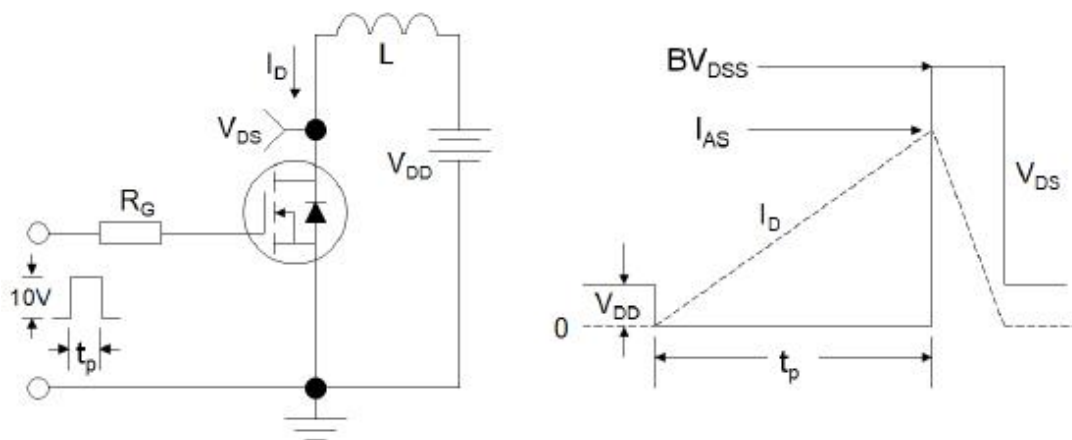
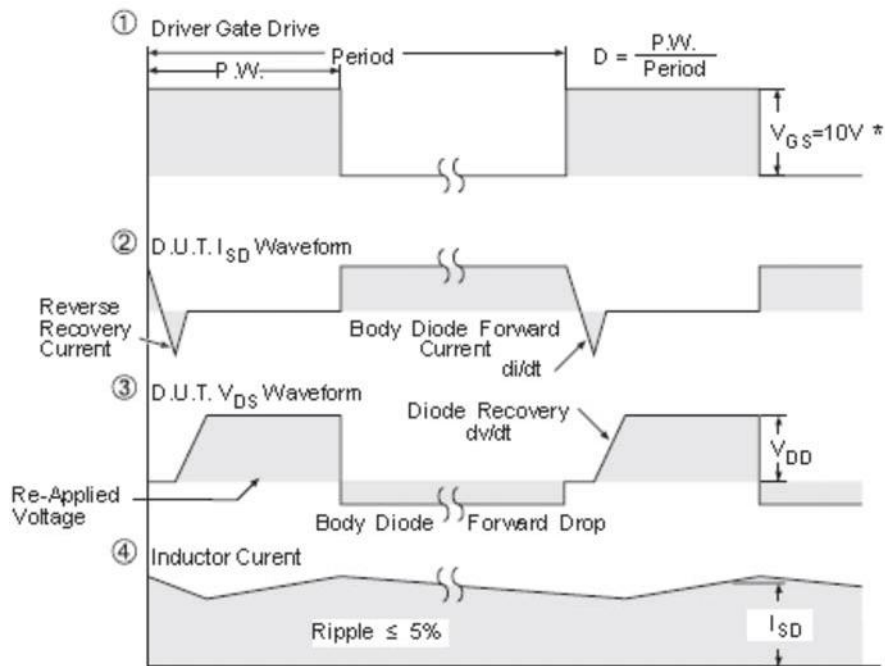
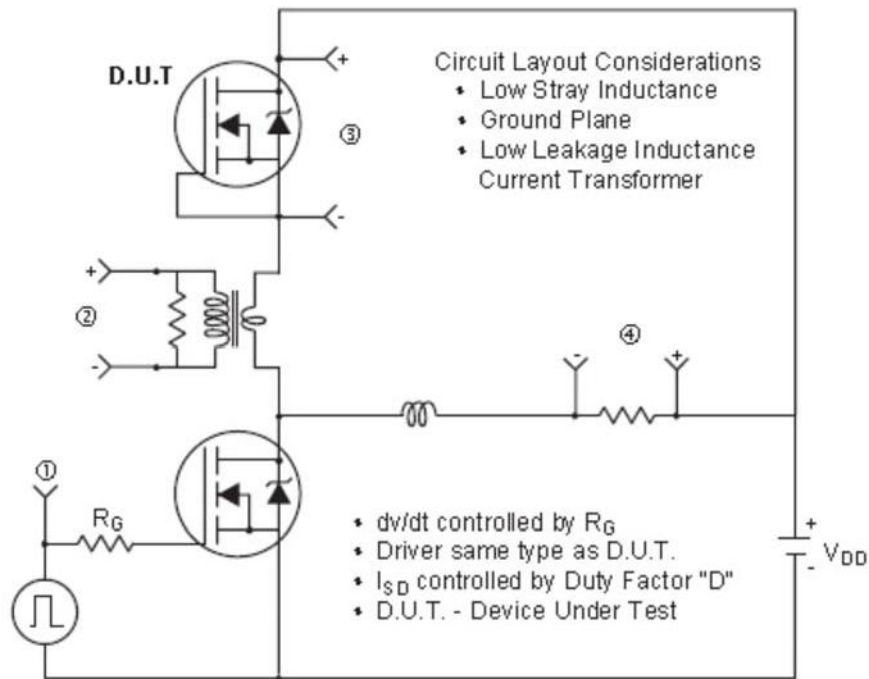


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

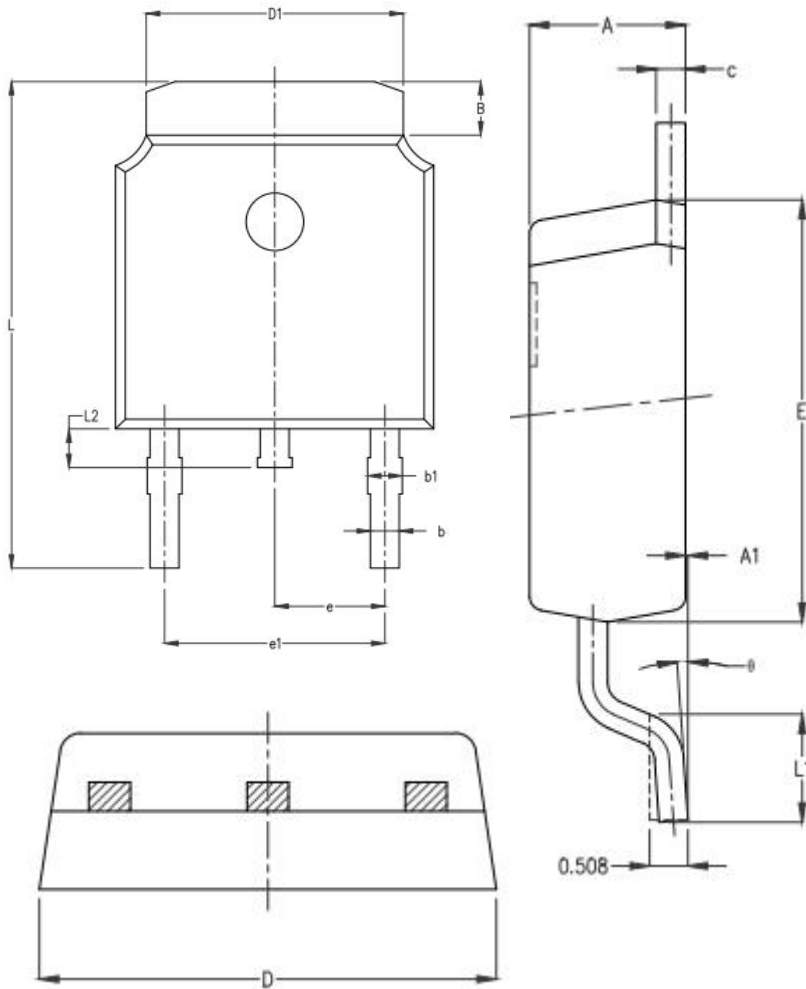


\*  $V_{GS} = 5V$  for Logic Level Devices

Figure 4: Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms (For N-channel)



### TO-252 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.15	2.25	2.35
A1	0.00	0.06	0.12
B	0.96	1.11	1.26
b	0.59	0.69	0.79
b1	0.69	0.81	0.93
c	0.34	0.42	0.50
D	6.45	6.60	6.75
D1	5.23	5.33	5.43
E	5.95	6.10	6.25
e	2.286TYP.		
e1	4.47	4.57	4.67
L	9.90	10.10	10.30
L1	1.40	1.55	1.70
L2	0.60	0.80	1.00
θ	0°	4°	8°

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