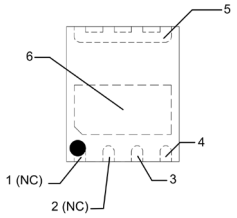
GS-065-008-1-L
650 V E-mode GaN transistor
Datasheet

Features

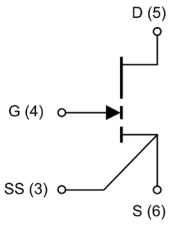
- 650 V enhancement mode power transistor
- Bottom-cooled, small 5x6 mm PDFN package
- $R_{DS(on)}$ = 225 mΩ
- $I_{DS(max)}$ = 8 A
- Ultra-low FOM
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- High switching frequency (> 1 MHz)
- Fast and controllable fall and rise times
- Reverse conduction capability
- Zero reverse recovery loss
- Source Sense (SS) pin for optimized gate drive
- RoHS 3 (6+4) compliant

Package Outline

Top view



Circuit Symbol



Applications

- Power Adapters
- LED Lighting Drivers
- Fast Battery Charging
- Power Factor Correction
- Appliance Motor Drives
- Wireless Power Transfer
- Industrial Power Supplies

Description

The GS-065-008-1-L is an enhancement mode GaN-on-Silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems innovates with industry leading advancements such as patented **Island Technology®** cell layout which realizes high-current die and high yield. The GS-065-008-1-L is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Submit datasheet feedback

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (Note 1)	$V_{DS(transient)}$	850	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (Note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C)	I_{DS}	8	A
Continuous Drain Current (T_{case} = 100 °C)	I_{DS}	5	A
Pulse Drain Current (Pulse width 10 µs, V_{GS} = 6 V) (Note 2)	$I_{DS\ Pulse}$	13.5	A

(1) For $\leq$ 1 µs

(2) Defined by product design and characterization. Value is not tested to full current in production.

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	2	°C /W
Thermal Resistance (junction-to-ambient) (Note 3)	$R_{\Theta JA}$	38	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS-065-008-1-L-TR	5x6 mm PDFN	Tape-and-Reel	3000	13”	12mm
GS-065-008-1-L-MR	5x6 mm PDFN	Mini-Reel	250	7”	12mm

Electrical Characteristics (Typical values at T_J = 25 °C , V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	V_{GS} = 0 V, $I_{DSS} \leq$ 13 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		225	285	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 2.2 A
Drain-to-Source On Resistance	$R_{DS(on)}$		569		mΩ	V_G = 6 V, T_J = 150 °C I_{DS} = 2.2 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 1.7 mA
Gate-to-Source Current	I_{GS}		40		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3.5		V	V_{DS} = 400 V, I_{DS} = 8 A
Drain-to-Source Leakage Current	I_{DSS}		0.5	13	µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		102		µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		2		Ω	f = 5 MHz
Input Capacitance	C_{ISS}		54		pF	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{OSS}		14		pF	
Reverse Transfer Capacitance	C_{RSS}		0.3		pF	
Effective Output Capacitance, Energy Related (Note 4)	$C_{O(ER)}$		21		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance, Time Related (Note 5)	$C_{O(TR)}$		34		pF	
Total Gate Charge	Q_G		1.6		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		0.5		nC	
Gate-to-Drain Charge	Q_{GD}		0.5		nC	
Output Charge	Q_{OSS}		14		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	
Output Capacitance Stored Energy	E_{OSS}		1.7		µJ	V_{DS} = 400 V V_{GS} = 0 V, f = 100 kHz

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Electrical Characteristics cont'd (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		2.4		ns	V_{DD} = 400 V, V_{GS} = 0-6 V, I_{DS} = 4 A, $R_{G(on)}$ = 15 Ω, $R_{G(off)}$ = 2 Ω, L = 200 µH, L_P = 9 nH (Notes 6,7,8)
Rise Time	t_R		4.8		ns	
Turn-Off Delay	$t_{D(off)}$		6		ns	
Fall Time	t_F		8		ns	
Switching Energy during turn-on	E_{on}		11		µJ	
Switching Energy during turn-off	E_{off}		4		µJ	
Output Capacitance Stored Energy	E_{OSS}		1.7		µJ	V_{DS} = 400 V V_{GS} = 0 V, f = 100 kHz

(6) See Figure 16 for switching test circuit diagram.
(7) See Figure 17 for switching time definition waveforms.
(8) L_P = parasitic inductance.

Electrical Performance Graphs

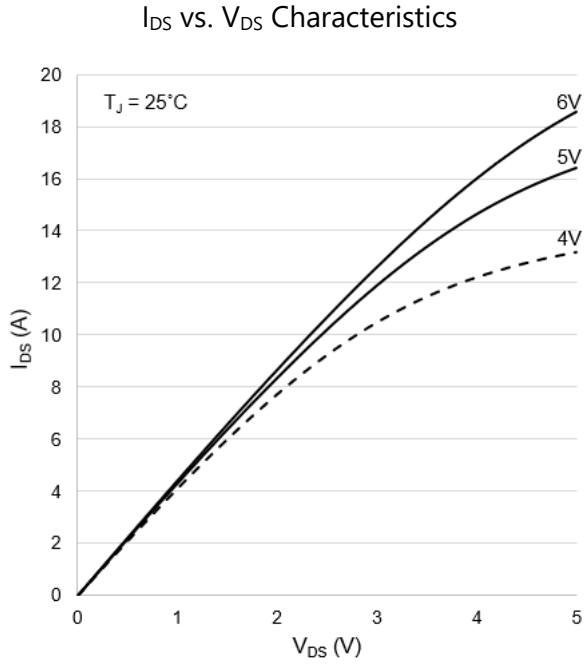


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

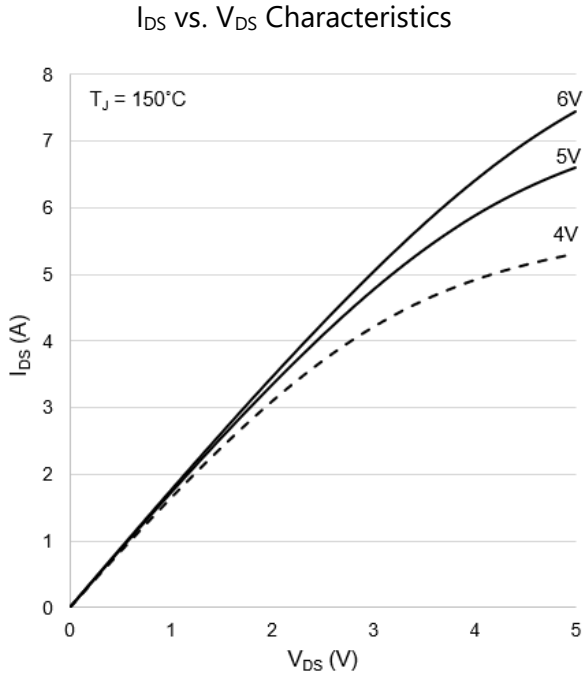


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

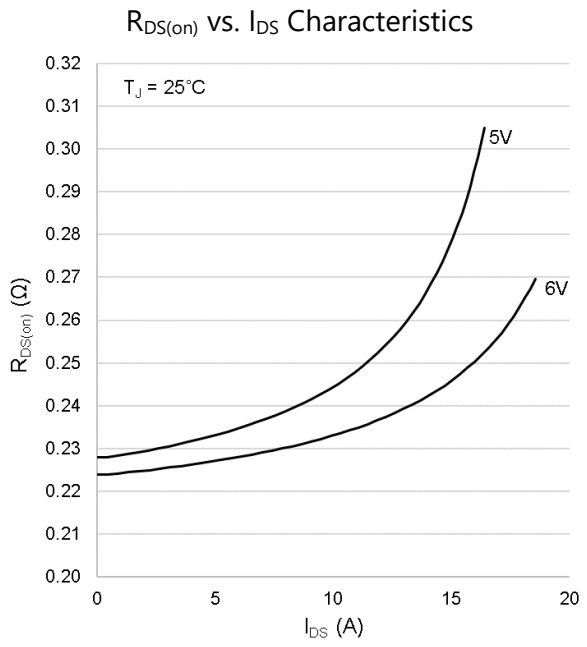


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

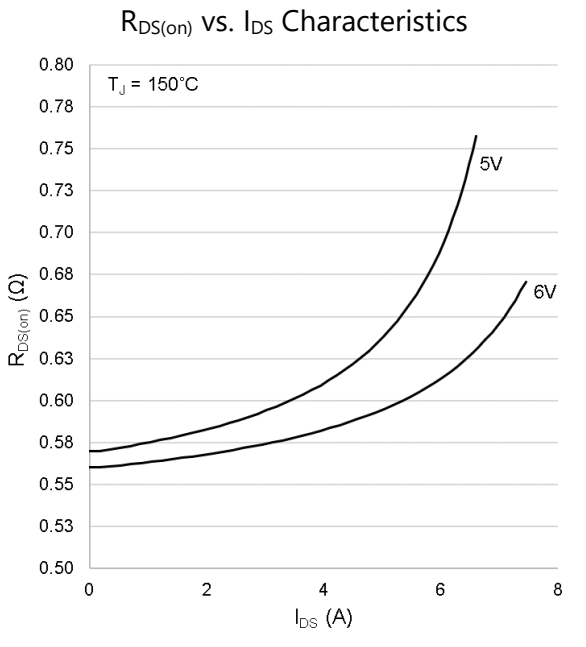


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

Electrical Performance Graphs

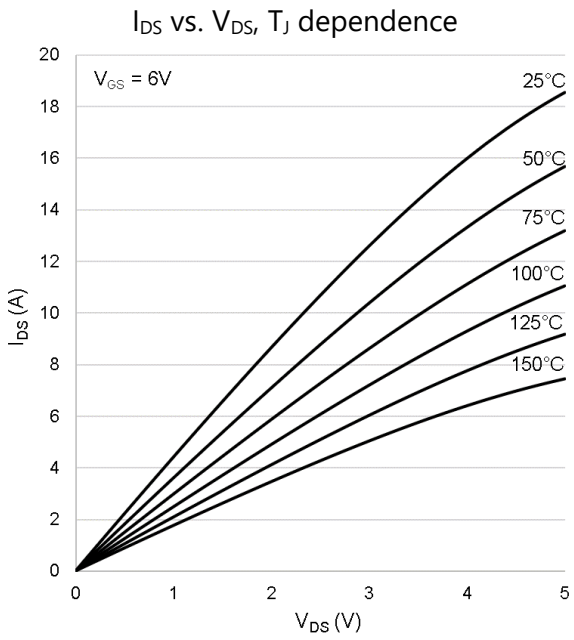


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

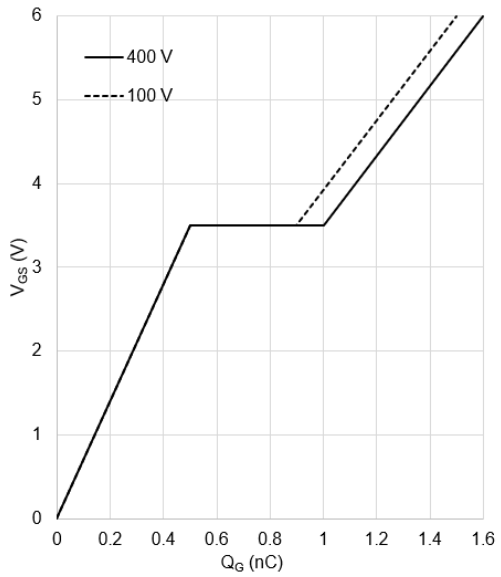


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} = 100, 400 V

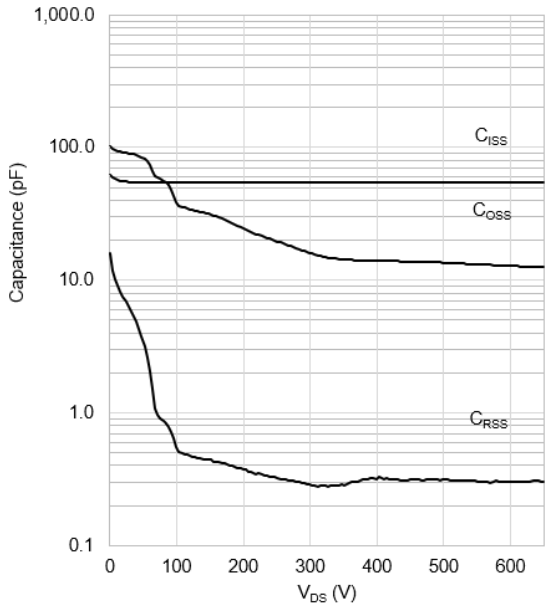


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

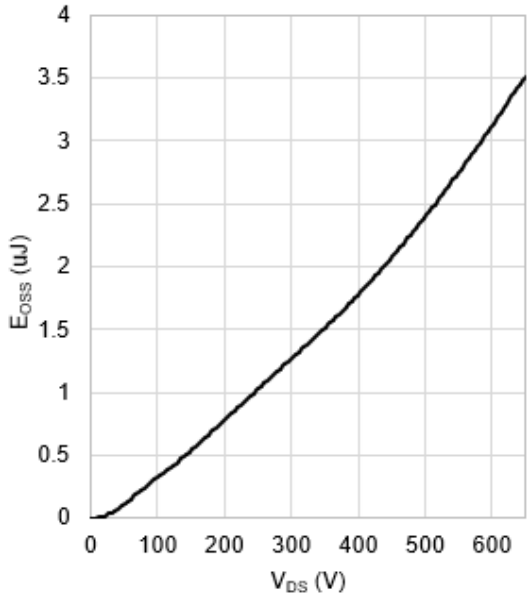


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

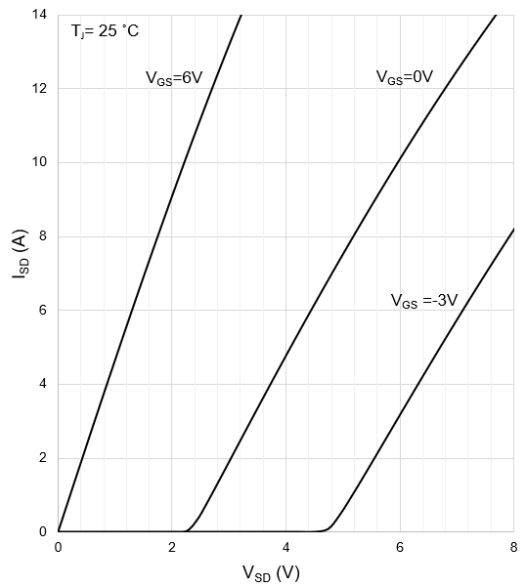


Figure 9: Typical I_{SD} vs. V_{SD} @ T_J = 25 °C

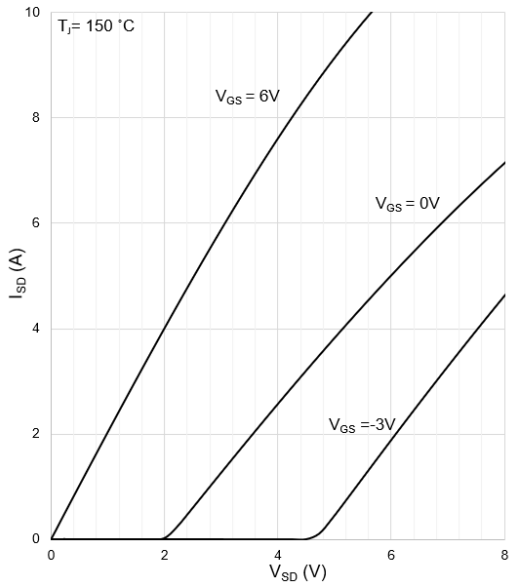


Figure 10: Typical I_{SD} vs. V_{SD} @ T_J = 150 °C

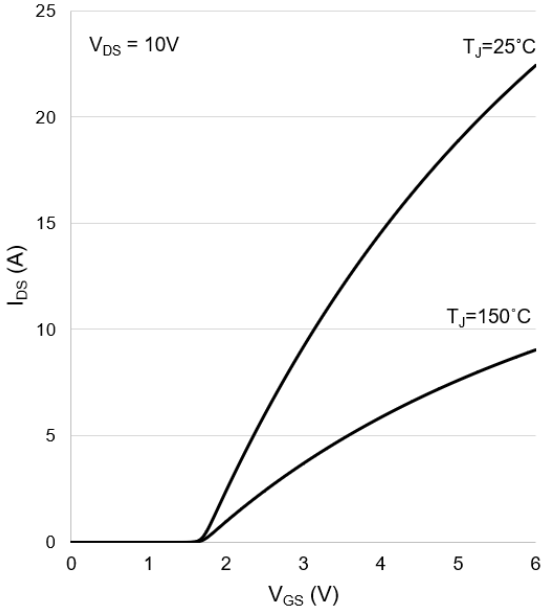


Figure 11: Typical I_{DS} vs. V_{GS}

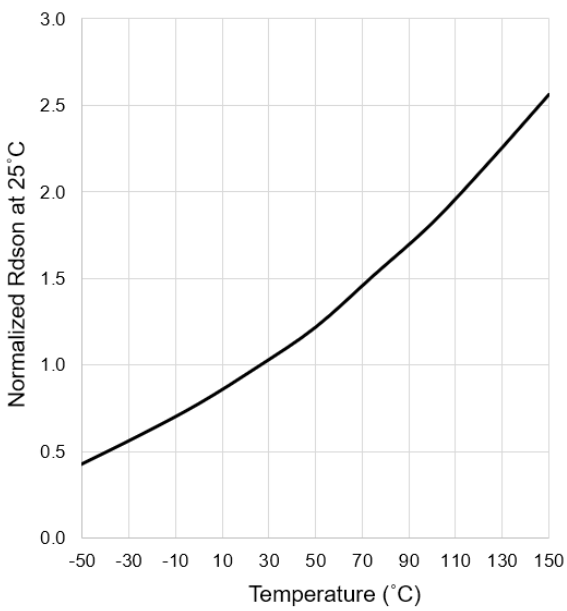


Figure 12: Normalized $R_{DS(on)}$ as a function of T_J

Thermal Performance Graphs

I_{DS} - V_{DS} SOA

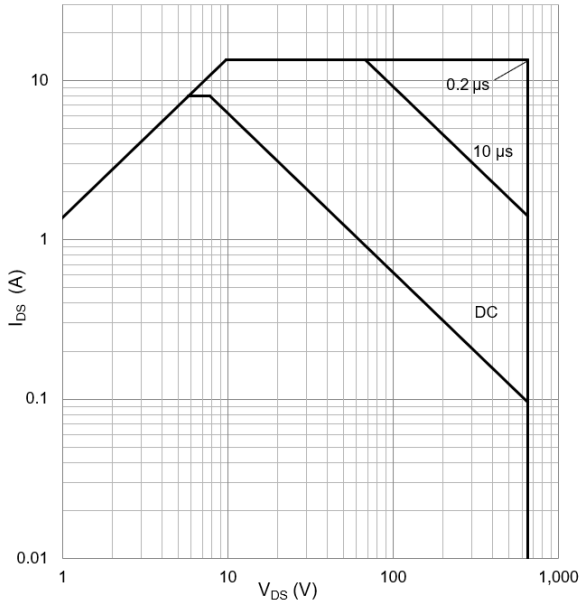


Figure 13: Safe Operating Area @ T_{case} = 25 °C

Power Dissipation Temperature Derating

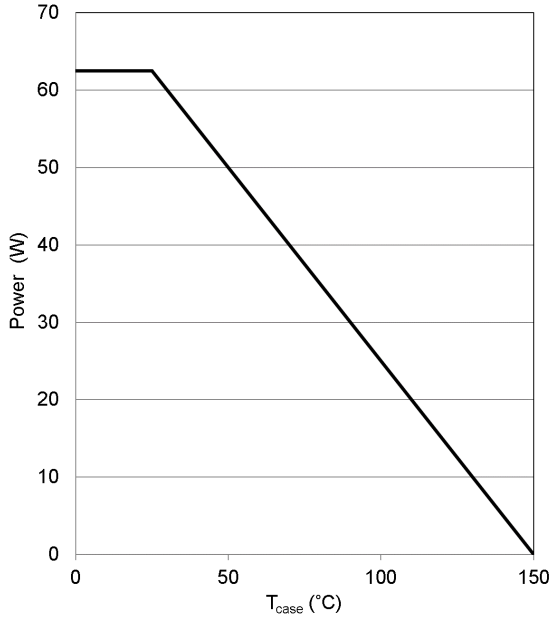


Figure 14: Power Derating vs. T_{case}

Transient $R_{\theta JC}$

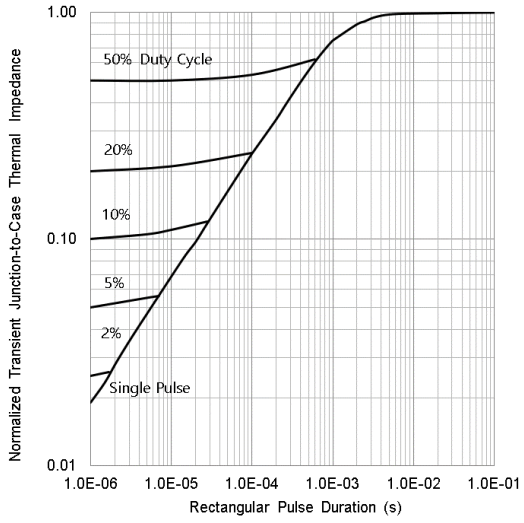


Figure 15: Transient Thermal Impedance

(1.00 = Nominal DC thermal impedance)

Test Circuits

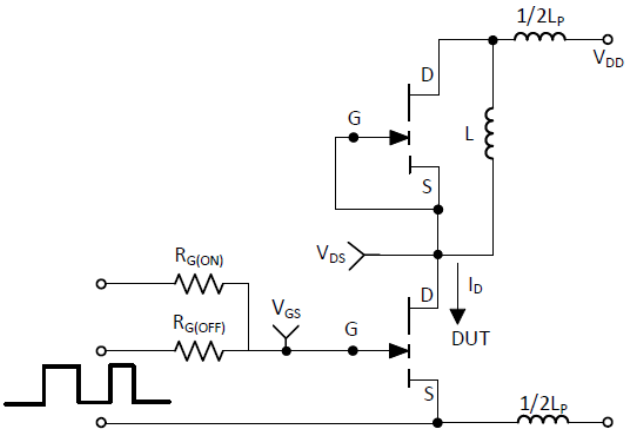


Figure 16: Switching Test Circuit

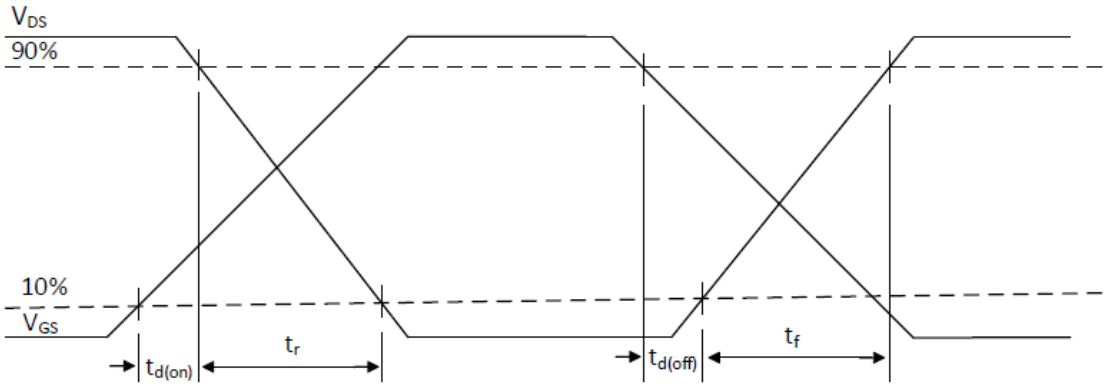


Figure 17: Switching Time Waveforms

Application Information

For more information, please refer to the application note entitled: "An Introduction to GaN Enhancement Mode HEMTs" at www.gansystems.com

Gate Drive

The recommended gate drive voltage range, V_{GS}, is 0 V to + 6 V for optimal $R_{DS(on)}$ performance. Also, the repetitive gate to source voltage, maximum rating, $V_{GS(AC)}$, is +7 V to -10 V. The gate can survive non-repetitive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias, typically V_{GS} = -3 V, ensures safe operation against the voltage spike on the gate, however it may increase reverse conduction losses if not driven properly. For more details, please refer to the gate driver application note "Gate Driver Circuit Design with GaN E-HEMTs" at www.gansystems.com

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note for more details.

A standard MOSFET driver can be used provided that it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

The package features a dedicated source sense pin which enhances the switching performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved by connecting the gate drive signal from the driver to the gate pad and returning from the source sense pad to the driver ground reference.

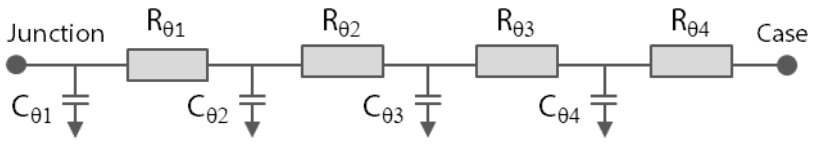
Thermal

The substrate is internally connected to the source/thermal pad on the bottom-side of the package. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under this pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available to support detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.1	$C_{\theta 1}$ = 2.0E-05
$R_{\theta 2}$ = 1.2	$C_{\theta 2}$ = 1.8E-04
$R_{\theta 3}$ = 0.62	$C_{\theta 3}$ = 1.8E-03
$R_{\theta 4}$ = 0.08	$C_{\theta 4}$ = 2.3E-03

For more detail, please refer to Application Note entitled "Modeling Thermal Behavior of GaN Systems' GaN*PX*® Using RC Thermal SPICE Models" available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $V_{(BL)DSS}$, is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated $V_{(BL)DSS}$. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and does not change with negative gate voltage. GaN Systems tests devices in production with a 850 V Drain-to-source voltage pulse to insure blocking voltage margin.

Packaging and Soldering

The package is a standard PDFN and it can withstand at least 3 reflow cycles.

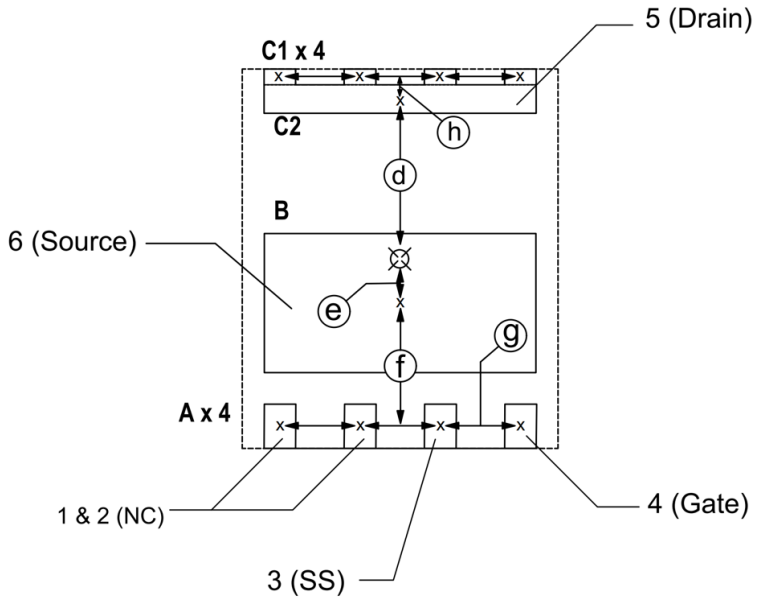
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "No-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "No-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "No-Clean" paste residues.

Recommended PCB Footprint



Top side view

Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	0.50	0.70	0.020	0.028
B	4.30	2.20	0.170	0.087
C1	0.50	0.25	0.020	0.001
C2	4.31	0.45	0.170	0.018

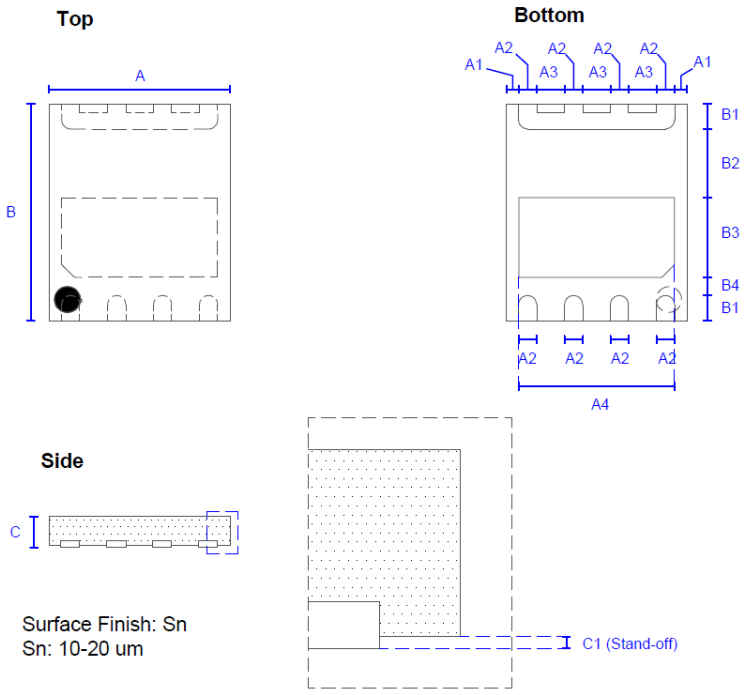
Dimensions

	mm	Inches
d	2.53	0.100
e	0.70	0.028
f	1.95	0.077
g	1.27	0.050
h	0.35	0.138

PCB pad openings

Package outline

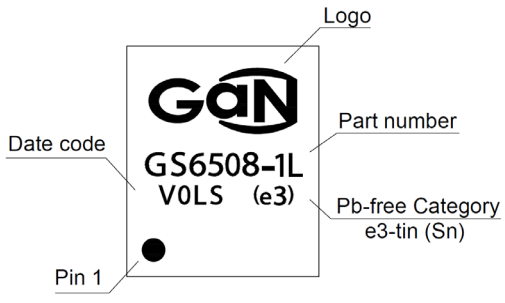
Package Dimensions



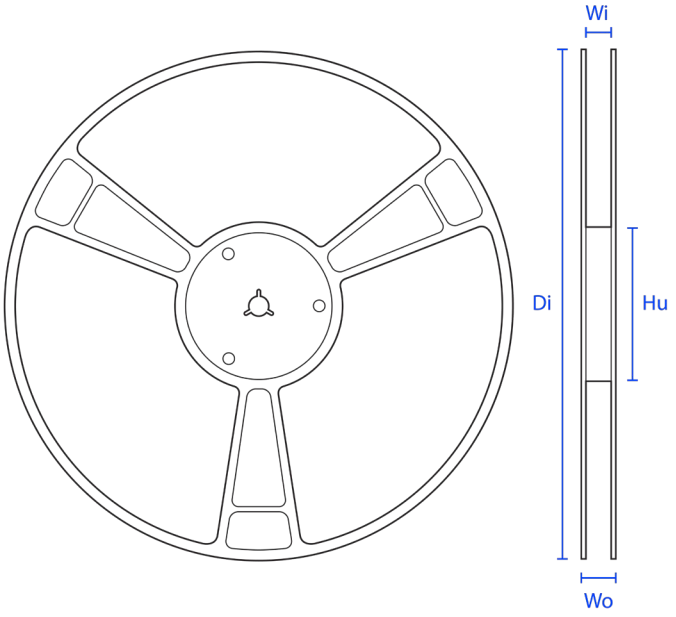
	mm	Inches*	
A	5.00	0.197	+/- 0.100 mm (0.004")
A1	0.35	0.014	+/- 0.050 mm (0.002")
A2	0.50	0.020	+/- 0.050 mm (0.002")
A3	0.77	0.030	+/- 0.050 mm (0.002")
A4	4.30	0.169	+/- 0.100 mm (0.004")
B	6.00	0.236	+/- 0.100 mm (0.004")
B1	0.70	0.028	+/- 0.100 mm (0.004")
B2	1.90	0.075	
B3	2.20	0.087	+/- 0.100 mm (0.004")
B4	0.50	0.020	
C	0.85	0.033	+/- 0.050 mm (0.002")
C1	0.03	0.001	+0.02/-0.03 mm (0.001")

*Inch measurements are approximate values

Part Marking

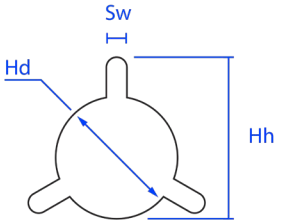


Tape and Reel Information

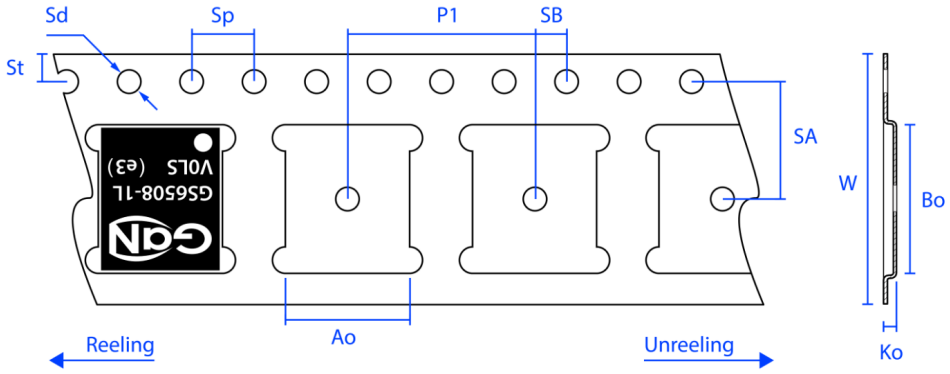


Dimensions (mm)

	13" reel (330 mm)		7" mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 2.0	180.0	+0.0 / - 3.0
Wo	18.4	MAX	18.4	MAX
Wi	12.4	+ 2.0 / - 0.0	12.4	+ 3.0 / - 0.05
Hu	100.0	+/- 2.0	55.0	+/- 5.0
Hh	20.2	MIN	20.2	MIN
Sw	1.5	MIN	1.6	MIN
Hd	13.0	+ 0.5 / - 0.2	13.0	+5.0 / - 0.2



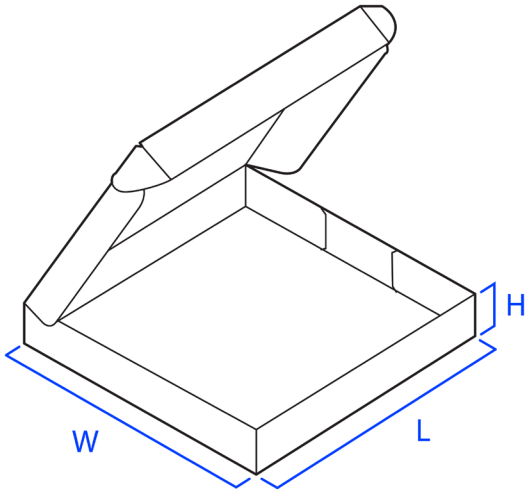
Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	8.00	+/- 0.1
W	12.00	+/- 0.3
Ko	1.20	+/- 0.1
Ao	5.30	+/- 0.1
Bo	6.30	+/- 0.1
Sp	4.00	+/- 0.1
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	5.50	+/- 0.05
SB	2.00	+/- 0.05

Tape and Reel Box Dimensions



Outside dimensions (mm)		
	7" mini-reel	13" tape-reel
W	203	346
L	203	346
H	35	35

Revision #	Changes from Previous	Owner
180720	Initial draft. Key specs from NPI requirements. (Rdson, Coss, operating temp range, Idss). Remainder of specs derived from scaling and simulation (thermals)	J. Ajersch
180803	Added DR and MR quantities and reel sizes	J. Ajersch
180928	Changed current to 8 A	P. Di Maso
181214	Started from version 180928. Changed part number from GS0-065-008-1-L to GS-065-008-1-L. Added note 2 in absolute rating table. Changed original note 2, 3, 4 to note 3, 4, 5. Changed Rdson test condition, IDS from 2.3A to 2.2A. Added VGS(th) test condition, Ids = 1.74 mA. Removed "CONFIDENTIAL" from title. Updated recommended PCB footprint drawing. Updated Package Dimensions drawing. . Added "Applications" section. Changed blocking voltage from BV_{DS} to $V_{(BL)DSS}$	Jason Xu J. Ajersch
190129	Started from 181214. Updated footer date. Added Vplat. Added Rdson @Tj=150C. Added Eoss. Changed Eoss test condition from 1 MHz to 100 kHz. Updated render, package outline, circuit symbol, recommended PCB footprint, Part Marking.	Jason Xu
190227	Started from 190129. Added reel and box dimensions. IDS_Pulse from 18 to 15A. $V_{GS(th)}$ from 1.3 to 1.4V. Ciss from 65 to 52. Coss from 17 to 14. Co(TR) from 35 to 37. Eoss from 1.9 to 1.8. Qoss from 14 to 14.7. Q_{GD} from 0.4 to 1. Changed 20MHz to 10 MHz.	Jason Xu
200423	Align the formatting with latest datasheet by using GS-065-011-1-L Rev 200309 as template. EC table parameters updated according to GS-065-008-1-D1 Rev 200325 • Changed IDS Pulse to 13.5A • Added Note 2 for Pulse drain current • Changed V(BL)DSS Condition: Idss = 13.3uA • Added RDS(ON)@25C: Max 285 mOhm • Added RDS(ON)@TJ=150C: Typ.569mOhm • VGS(th) condition: Ids = 1.7 mA • Vplat condition: Ids=8A • IDSS Max: added 13.3A • Added Idss typ. 102 uA • Changed Rg to 1 Ohm	D. Chen

	• Changed CV values (read out from CV curve):Ciss=45pF, Coss=14.4pF, Crss=0.3pF • Changed Qg values (read out from Qg curve): Qg=14.nC, Qgs=0.5nC, Qgd=0.5nC, Qoss=14nC Updated Reel drawing – Rev 2020-4-22-PDFN_12mm	
200427	SPEC CHANGES (Scaled from W3 data) • Coss from 14.4 to 14.2 nF • Co(er) from 22 to 21 nF • Co(tr) from 37 to 34 nF • Qg from 1.4 to 1.5 nC • Eoss from 1.8 to 1.7 uJ UPDATED EPGs • Cxxx (Rev 20042) • Qg (Rev 200427)	J Ajersch
200924	#Added figure 16 (original fig 18 from 08B datasheet) and fig 17, switching test circuits and waveform #Added rows for time delay at 25C #Added rows for Eon, Eoff #Added foot note 6,7,8 # pulse width changed from 50 µs to 10 µs #Ciss changed from 45pF to 54pF #Coss changed from 14.2pF to 14pF #Capacitance Characteristics (Fig.7) updated #Reverse Conduction Characteristics (Fig. 9 & 10) updated #SOA at 10 µs fig. 13 updated #Added arrow pointing to 0.2us corner for fig 13 # LP = changes from 15 to 9 nH # Tj changed from -40C to -55C # Vds(transient) changed from 750V to 850V # Vplat changed from 4V to 3.5V #Qg(6V,400V) changed from 1.5nC to 1.6nC #Figure 6 update (3.5/0.5/0.5/1.6)	Amira Ammar
201116	Preliminary removed from Header – GR4 Version Footer adjusted to GR4 regulation ":This product characteristics and specifications are subject to change without notice" Removed #Render changed new DC: V0LS #Part marking changed following V0LS #Tape & Reel changed following V0LS	Amira Ammar

	#Package dimension drawing changed due to change of C1 value for typical 0.03mm and tolerance +0.02/-0.03mm #Figures 1 & 2 remove Vgs = 3V, 2V and make Vgs=4V Dashed 1. IDSS Max: Changed from 13.3 to 13 uA 2. Rg: Changed from 1 to 2 Ohm	
210104	1- Figure 7 updated, y-axis changed 2- Tape and reel information updated, used Tape - GS-065-008-1-L - 2020-12-14-02 ECR disposition: No PCN required since FFF not affected. No adverse effects to quality or reliability.	Amira Ammar

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for MOSFET ***category:***

Click to view products by Gan Systems ***manufacturer:***

Other Similar products are found below :

614233C 648584F IRFD120 JANTX2N5237 2N7000 FCA20N60_F109 FDZ595PZ 2SK2545(Q,T) 405094E 423220D TPCC8103,L1Q(CM MIC4420CM-TR VN1206L 614234A 715780A NTNS3166NZT5G SSM6J414TU,LF(T 751625C IPS70R2K0CEAKMA1 BUK954R8-60E DMN3404LQ-7 NTE6400 SQJ402EP-T1-GE3 2SK2614(TE16L1,Q) 2N7002KW-FAI DMN1017UCP3-7 EFC2J004NUZTDG ECH8691-TL-W FCAB21350L1 P85W28HP2F-7071 DMN1053UCP4-7 NTE221 NTE2384 NTE2903 NTE2941 NTE2945 NTE2946 NTE2960 NTE2967 NTE2969 NTE2976 NTE455 NTE6400A NTE2910 NTE2916 NTE2956 NTE2911 US6M2GTR TK10A80W,S4X(S SSM6P69NU,LF