Silicon Carbide Junction Transistor/Schottky Diode Co-pack

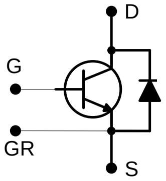
V_{DS}	**=**	**1200 V**
$R_{DS(ON)}$	**=**	**10 mΩ**
$I_{D\ (@\ 25°C)}$	**=**	**160 A**
$I_{D\ (@\ 115°C)}$	**=**	**100 A**
$h_{FE\ (@\ 25°C)}$	**=**	**85**

Features

- 175 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Optional Gate Return Pin
- Exceptional Safe Operating Area
- Integrated SiC Schottky Rectifier
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package

- RoHS Compliant



Pin D - Drain
Pin S - Source
Pin GR - Gate Return
Pin G - Gate

Isolated Baseplate
SOT-227

Please note: The Source and Gate Return pins are not exchangeable. Their exchange might lead to malfunction.

Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth
- Reduced cooling requirements
- Reduced system size

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Table of Contents

Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
SiC Junction Transistor					
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1200	V	
Continuous Drain Current	I_D	T_C = 25°C	160	A	Fig. 17
Continuous Drain Current	I_D	T_C = 115°C	100	A	Fig. 17
Continuous Gate Current	I_G		7	A	
Continuous Gate Return Current	I_{GR}		7		
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 175 °C, Clamped Inductive Load	$I_{D,max}$ = 100 @ $V_{DS} \le V_{DSmax}$	A	Fig. 19
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 175 °C, I_G = 1 A, V_{DS} = 800 V, Non Repetitive	>20	µs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Power Dissipation	P_{tot}	T_C = 25 °C / 115 °C, t_p > 100 ms	535 / 214	W	Fig. 16
Operating and storage temperature	T_{stg}		-55 to 175	°C	

Parameter	Symbol	Conditions	Value	Unit	Notes
Free-Wheeling SiC Diode					
Repetitive peak reverse voltage	V_{RRM}		1200	V	
Continuous forward current	I_F	$T_C \le 135$ °C	100	A	
RMS forward current	$I_{F(RMS)}$	$T_C \le 135$ °C	174	A	
Surge non-repetitive forward current, Half Sine Wave	$I_{F,SM}$	$T_C = 25$ °C, $t_P = 10$ ms $T_C = 135$ °C, $t_P = 10$ ms	700 626	A	
Non-repetitive peak forward current	$I_{F,max}$	$T_C = 25$ °C, $t_P = 10$ µs	3250	A	
I^2t value	$\int i^2\,dt$	$T_C = 25$ °C, $t_P = 10$ ms $T_C = 135$ °C, $t_P = 10$ ms	900 600	A^2s	

Thermal Characteristics

Parameter	Symbol	Conditions	Value	Unit	Notes
Thermal resistance, junction - case	R_{thJC}	SiC Junction Transistor	0.28	°C/W	Fig. 20
Thermal resistance, junction - case	R_{thJC}	SiC Diode	0.26	°C/W	Fig. 21

Section II: Static Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
A: On State							
Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 100$ A, $T_j = 25$ °C $I_D = 100$ A, $T_j = 150$ °C $I_D = 100$ A, $T_j = 175$ °C		10 15 18		mΩ	Fig. 5
Gate – Source Saturation Voltage	$V_{GS,SAT}$	$I_D = 100$ A, $I_D/I_G = 40$, $T_j = 25$ °C $I_D = 100$ A, $I_D/I_G = 30$, $T_j = 175$ °C		3.42 3.23		V	Fig. 7
DC Current Gain	h_{FE}	$V_{DS} = 8$ V, $I_D = 100$ A, $T_j = 25$ °C $V_{DS} = 8$ V, $I_D = 100$ A, $T_j = 125$ °C $V_{DS} = 8$ V, $I_D = 100$ A, $T_j = 175$ °C		85 57 51		–	Fig. 4
FWD forward voltage	V_F	$I_F = 100$ A, $T_j = 25$ °C $I_F = 100$ A, $T_j = 175$ °C		1.4 2.1	1.8 3.0	V	
B: Off State							
Drain Leakage Current	I_{DSS}	$V_{DS} = 1200$ V, $V_{GS} = 0$ V, $T_j = 25$ °C $V_{DS} = 1200$ V, $V_{GS} = 0$ V, $T_j = 150$ °C $V_{DS} = 1200$ V, $V_{GS} = 0$ V, $T_j = 175$ °C		100 300 600		µA	Fig. 8
Gate Leakage Current	I_{SG}	$V_{SG} = 20$ V, $T_j = 25$ °C		40		nA	

Section III: Dynamic Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
A: Capacitance and Gate Charge							
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 800$ V, $f = 1$ MHz		16.1		nF	Fig. 9
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	$V_{DS} = 1$ V, f = 1 MHz $V_{DS} = 400$ V, f = 1 MHz $V_{DS} = 800$ V, $f = 1$ MHz		6480 570 440		pF	Fig. 9
Total Output Capacitance Charge	Q_{oss}	$V_{DS} = 400$ V $V_{DS} = 800$ V		375 570		nC	
Output Capacitance Stored Energy	E_{OSS}	$V_{GS} = 0$ V, $V_{DS} = 800$ V, $f = 1$ MHz		170		µJ	Fig. 10
Effective Output Capacitance, time related	$C_{oss,tr}$	I_D = constant, $V_{GS} = 0$ V, $V_{DS} = 0…800$ V		715		pF	
Effective Output Capacitance, energy related	$C_{oss,er}$	$V_{GS} = 0$ V, $V_{DS} = 0…800$ V		535		pF	
Gate-Source Charge	Q_{GS}	$V_{GS} = -5…3$ V		130		nC	
Gate-Drain Charge	Q_{GD}	$V_{GS} = 0$ V, $V_{DS} = 0…800$ V		570		nC	
Gate Charge - Total	Q_G			700		nC	

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		

B: SJT Switching[1]

Parameter	Symbol	Conditions	Min.	Typical	Max.	Unit	Notes
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	V_{GS} > 2.5 V, V_{DS} = 0 V, T_j = 175 ºC		0.1		Ω	
Turn On Delay Time	$t_{d(on)}$	T_j = 25 ºC, V_{DS} = 800 V, I_D = 50 A, Resistive Load Refer to Section V for additional driving information.		12		ns	
Fall Time, V_{DS}	t_f			40		ns	Fig. 11, 13
Turn Off Delay Time	$t_{d(off)}$			37		ns	
Rise Time, V_{DS}	t_r			25		ns	Fig. 12, 14
Turn On Delay Time	$t_{d(on)}$	T_j = 175 ºC, V_{DS} = 800 V, I_D = 50 A, Resistive Load		10		ns	
Fall Time, V_{DS}	t_f			40		ns	Fig. 11
Turn Off Delay Time	$t_{d(off)}$			45		ns	
Rise Time, V_{DS}	t_r			20		ns	Fig. 12
Turn-On Energy Per Pulse	E_{on}	T_j = 25 ºC, V_{DS} = 800 V, I_D = 50 A, Inductive Load Refer to Section V.		1.8		mJ	Fig. 11, 13
Turn-Off Energy Per Pulse	E_{off}			1.4		mJ	Fig. 12, 14
Total Switching Energy	E_{tot}			3.2		mJ	
Turn-On Energy Per Pulse	E_{on}	T_j = 175 ºC, V_{DS} = 800 V, I_D = 50 A, Inductive Load		1.85		mJ	Fig. 11
Turn-Off Energy Per Pulse	E_{off}			1.3		mJ	Fig. 12
Total Switching Energy	E_{tot}			3.15		mJ	

[1] – All times are relative to the Drain-Source Voltage V_{DS}

Section IV: Figures

A: Static Characteristics

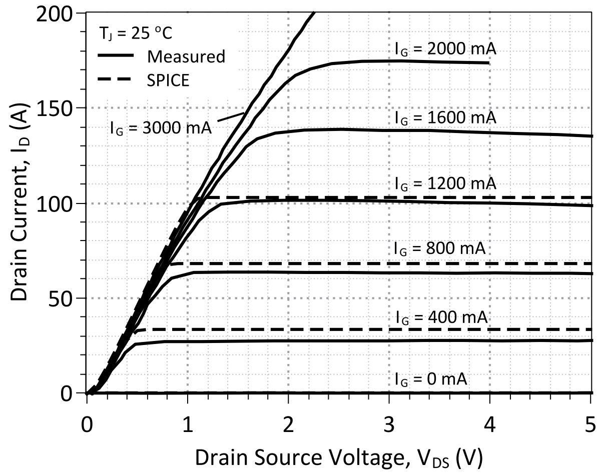


Figure 1: Typical Output Characteristics at 25 °C

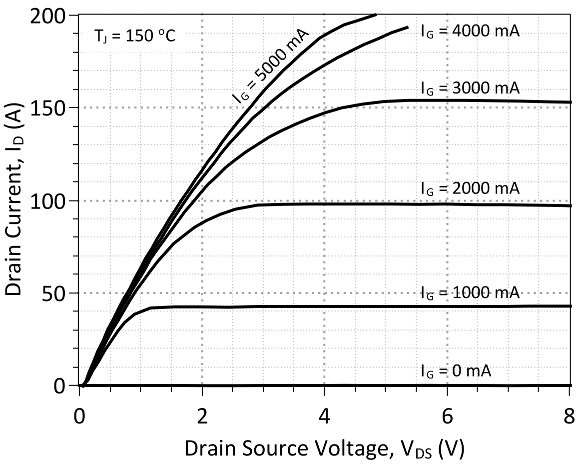


Figure 2: Typical Output Characteristics at 150 °C

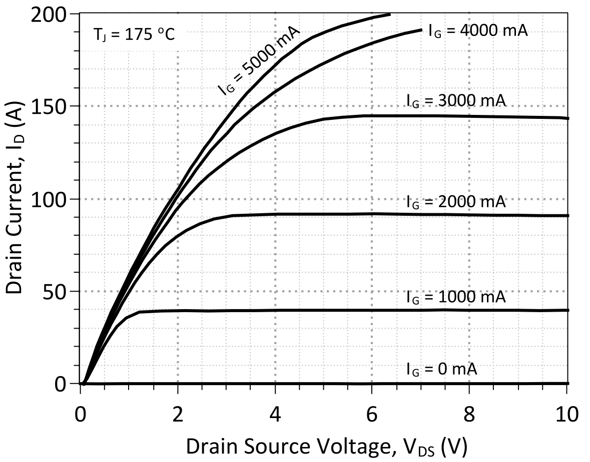


Figure 3: Typical Output Characteristics at 175 °C

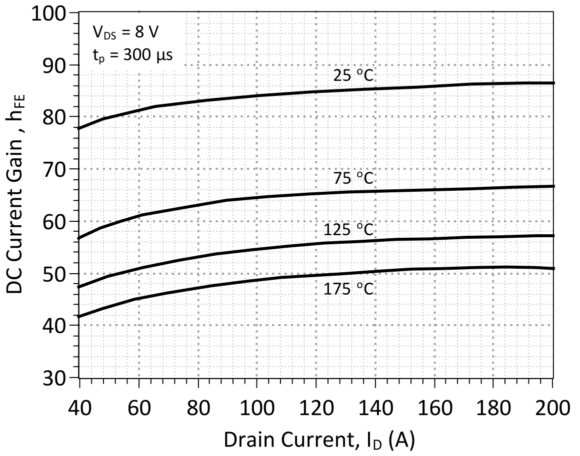


Figure 4: DC Current Gain vs. Drain Current

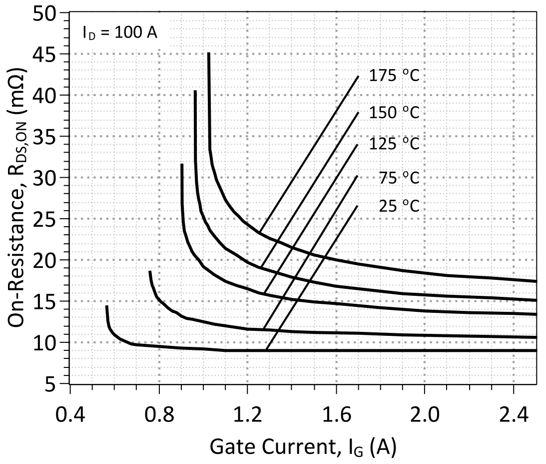


Figure 5: On-Resistance vs. Gate Current

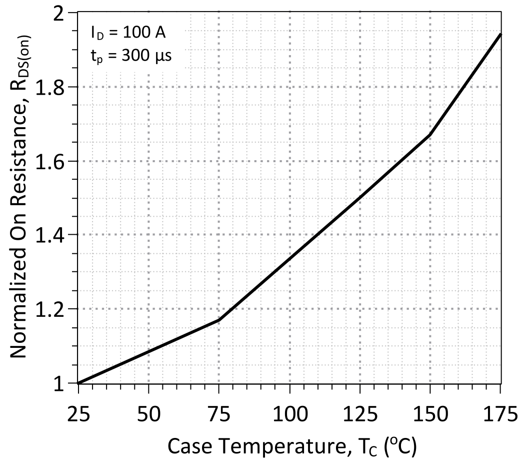


Figure 6: Normalized On-Resistance vs. Temperature

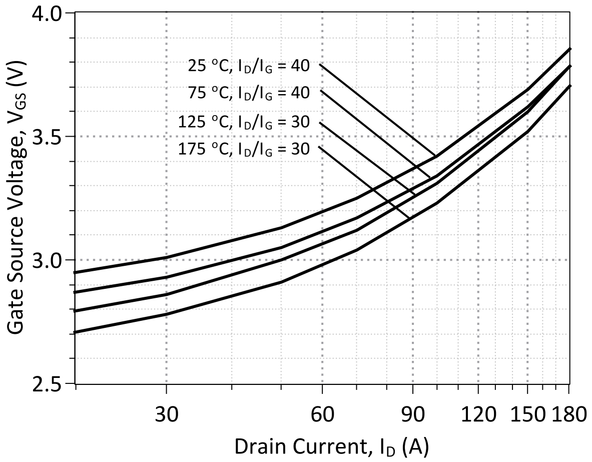


Figure 7: Typical Gate – Source Saturation Voltage

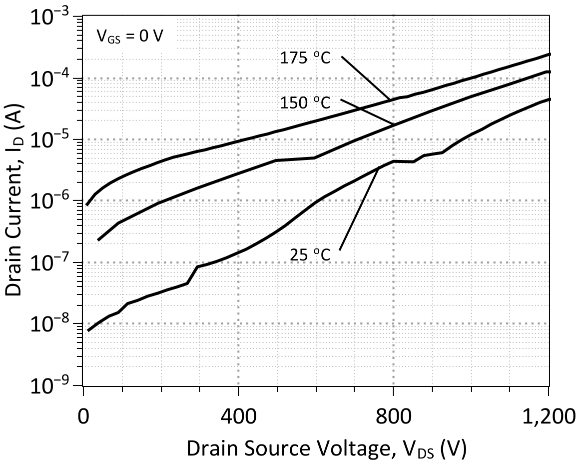


Figure 8: Typical Blocking Characteristics

B: Dynamic Characteristics

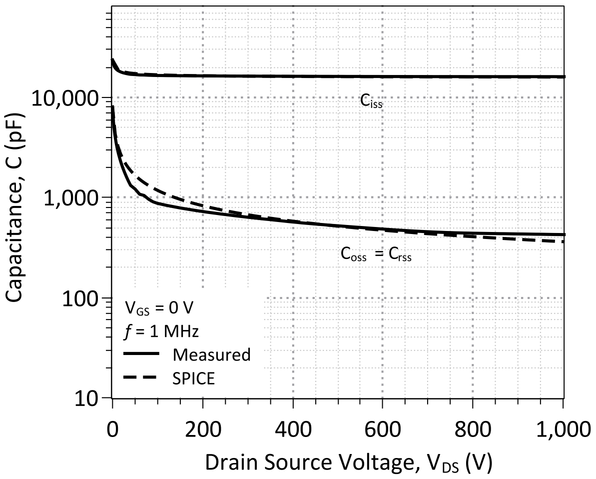


Figure 9: Input, Output, and Reverse Transfer Capacitance

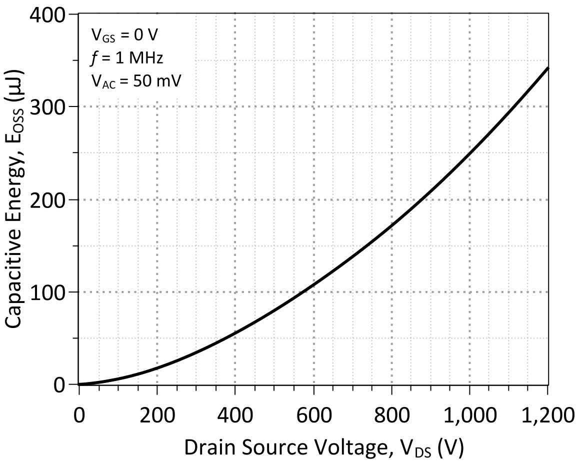


Figure 10: Energy Stored in Output Capacitance

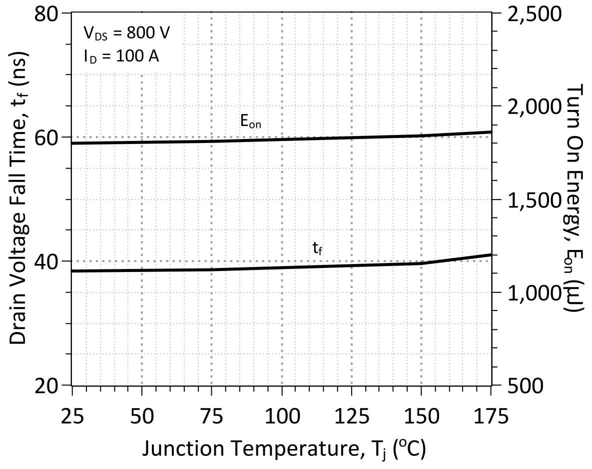


Figure 11: Typical Switching Times and Turn On Energy Losses vs. Temperature

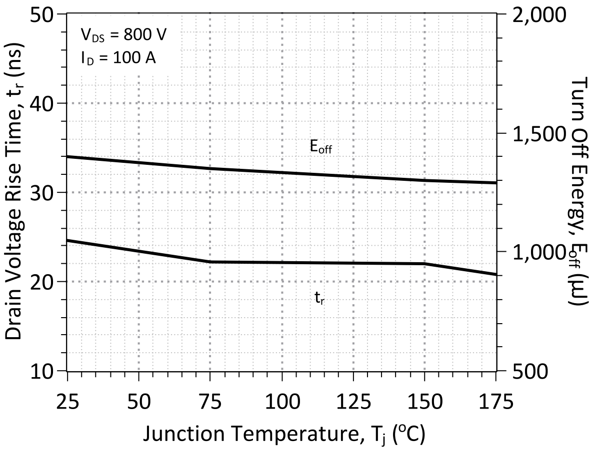


Figure 12: Typical Switching Times and Turn Off Energy Losses vs. Temperature

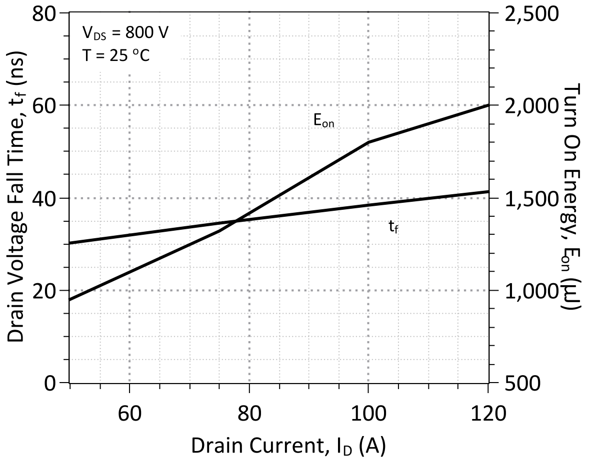


Figure 13: Typical Switching Times and Turn On Energy Losses vs. Drain Current

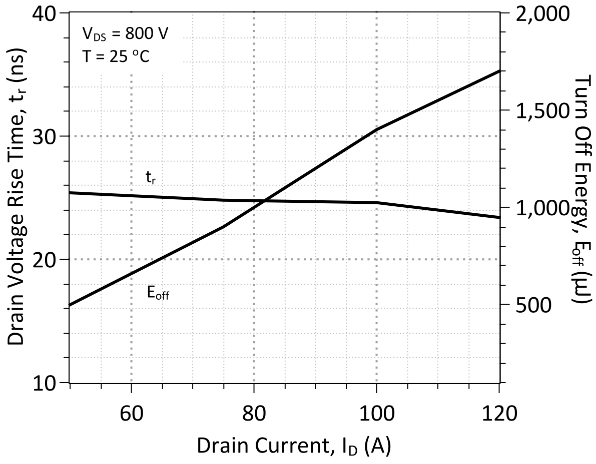


Figure 14: Typical Switching Times and Turn Off Energy Losses vs. Drain Current

C: Current and Power Derating

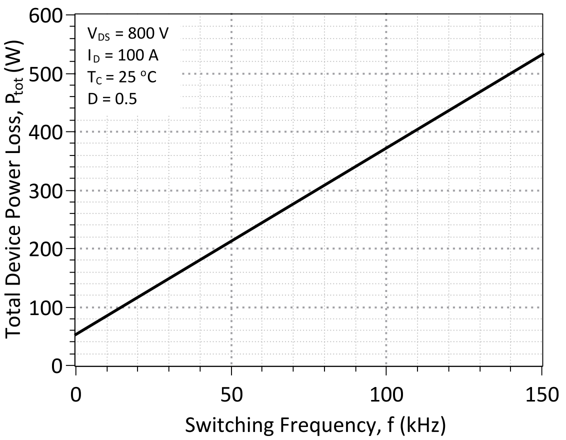


Figure 15: Typical Hard Switched Device Power Loss vs. Switching Frequency [2]

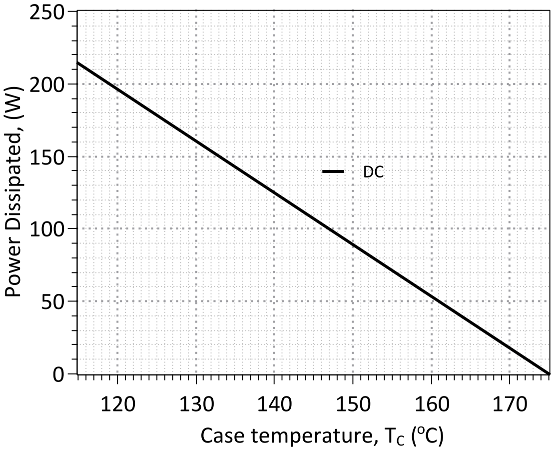


Figure 16: Power Derating Curve

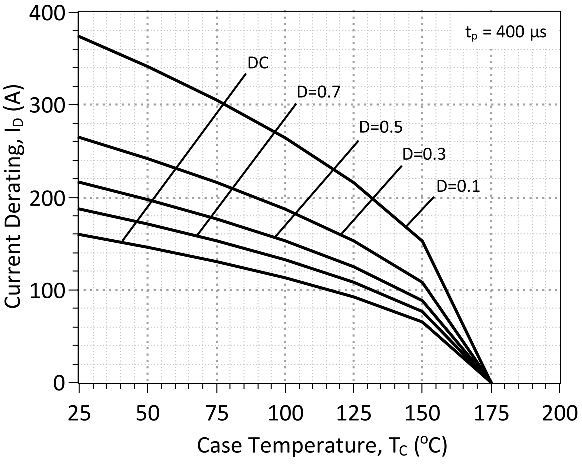


Figure 17: Drain Current Derating vs. Temperature

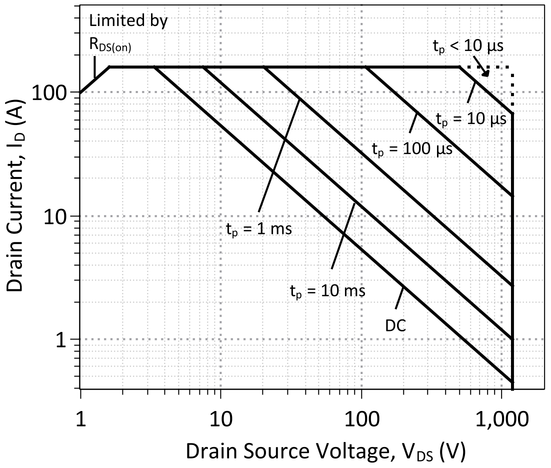


Figure 18: Forward Bias Safe Operating Area at T_c= 25 °C

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[2] – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

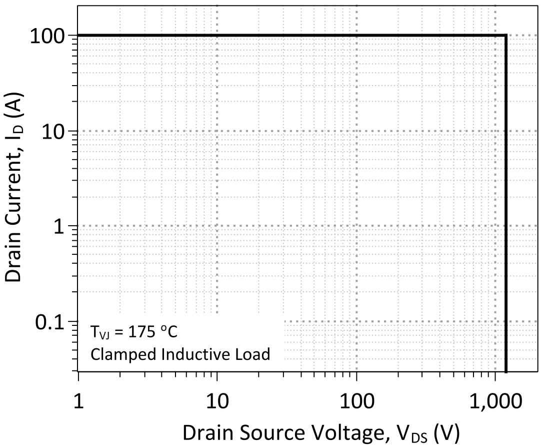

Figure 19: Turn-Off Safe Operating Area

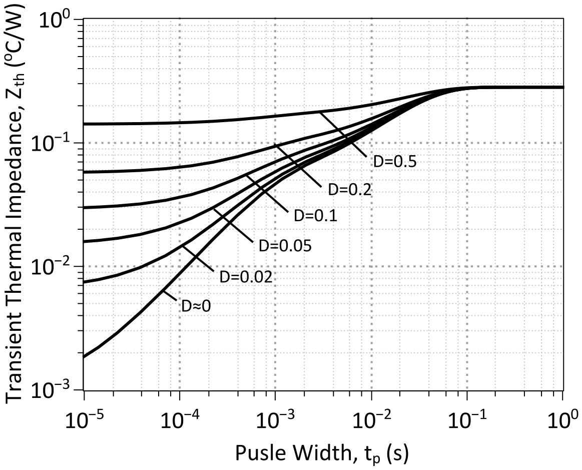

Figure 20: SJT Transient Thermal Impedance

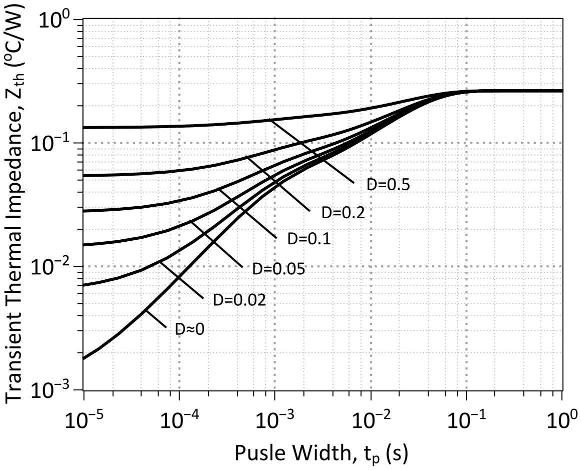

Figure 21: FWD Transient Thermal Impedance

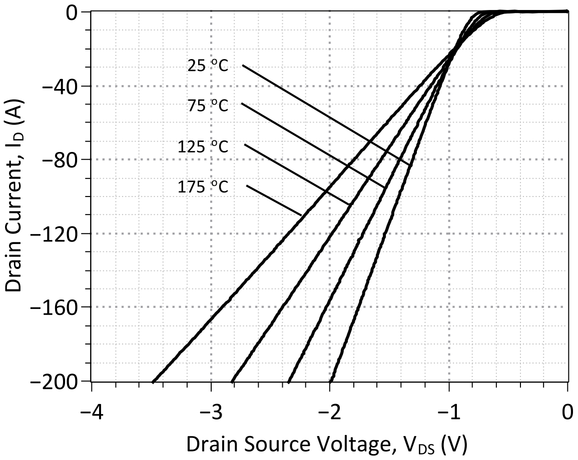

Figure 22: Typical FWD Forward Characteristics

Section V: Driving the GA100SICP12-227

Drive Topology	Gate Drive Power Consumption	Switching Frequency	Application Emphasis	Availability
TTL Logic	High	Low	Wide Temperature Range	Coming Soon
Constant Current	Medium	Medium	Wide Temperature Range	Coming Soon
High Speed – Boost Capacitor	Medium	High	Fast Switching	Production
High Speed – Boost Inductor	Low	High	Ultra Fast Switching	Coming Soon
Proportional	Lowest	High	Wide Drain Current Range	Coming Soon
Pulsed Power	Medium	N/A	Pulse Power	Coming Soon

A: Static TTL Logic Driving

The GA100SICP12-227 may be driven with direct (5 V) TTL logic and current amplification. The amplified current level of the supply must meet or exceed the steady state gate current ($I_{G,steady}$) required to operate the GA100SICP12-227. Minimum $I_{G,steady}$ is dependent on the anticipated drain current I_D through the SJT and the DC current gain h_{FE}, it may be calculated from the following equation. An accurate value of the h_{FE} may be read from Figure 4. An optional resistor R_G may be used in series with the gate pin to trim $I_{G,steady}$, also an optional capacitor C_G may be added in parallel with R_G to facilitate faster SJT switching if desired, further details on these options are given in the following section.

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

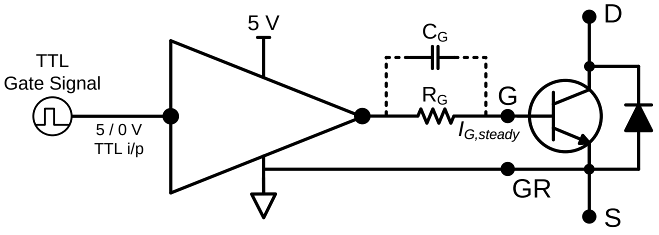

Figure 23: TTL Gate Drive Schematic

B: High Speed Driving

The SJT is a current controlled transistor which requires a positive gate current for turn-on and to remain in on-state. An idealized gate current waveform for ultra-fast switching of the SJT while maintaining low gate drive losses is shown in Figure 24, it features a positive current peak during turn-on, a negative current peak during turn-off, and continuous gate current during on-state.

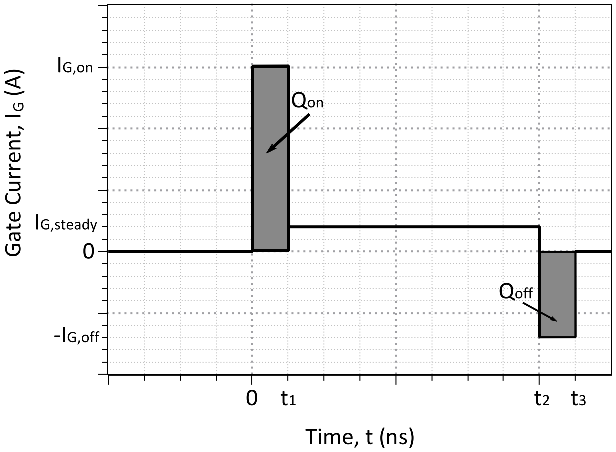

Figure 24: An idealized gate current waveform for fast switching of an SJT.

An SJT is rapidly switched from its blocking state to on-state when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the SJT gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$

Ideally, $I_{G,on}$ should terminate when the drain voltage falls to its on-state value in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The voltage applied to the gate pin should be maintained high enough, above the V_{GS},sat (see Figure 7) level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. Turn off can be achieved with V_{GS} = 0 V, however a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

Gate Return Pin

The optional gate return (GR) pin allows for a reduction of source path inductive and resistive coupling in the gate driver connection to the GA100SICP12-227. Drain currents through the source pin during transient and steady state operation induce an undesirable source voltage in all power transistors due to unavoidable source pin inductance and resistance. This voltage can negatively affect gate driving performance, however the gate return pin allows for decoupling from these source current path effects which results in faster switching and higher efficiency gate driving.

B:1: High Speed, Low Loss Drive with Boost Capacitor, GA15IDDJT22-FR4

The GA100SICP12-227 may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide fast switching current peaks at turn-on and turn-off and a continuous gate current while in on-state. An evaluation gate drive board (GA15IDDJT22-FR4) utilizing this topology is commercially available low-side driving, its datasheet provides additional details.

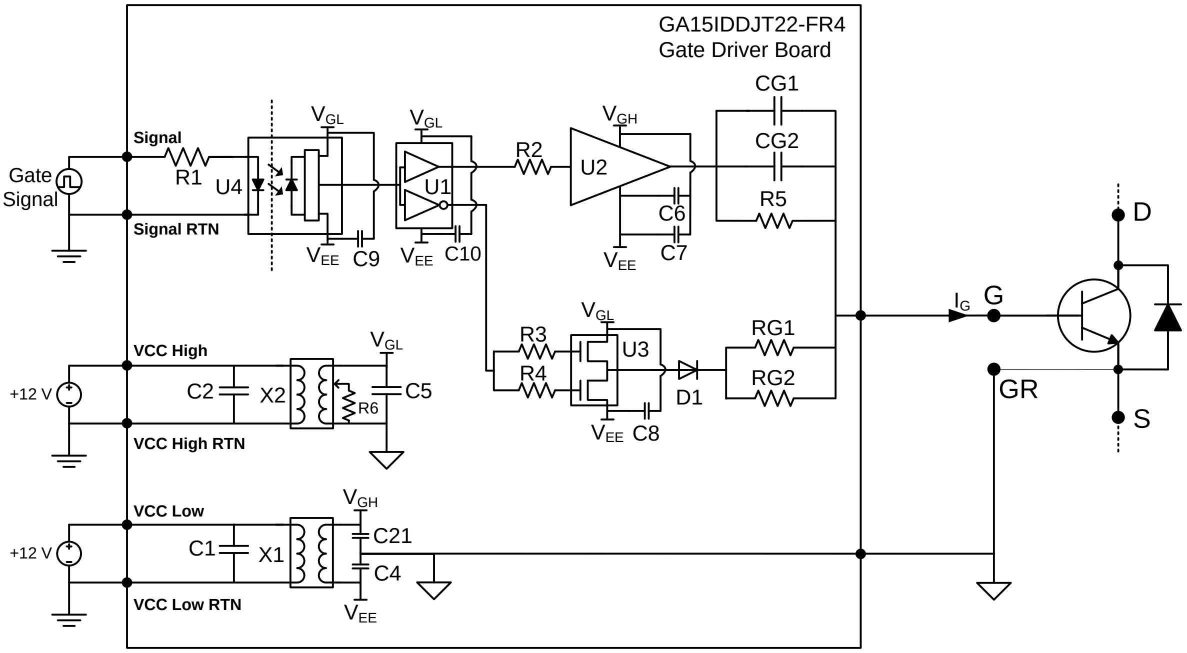

Figure 25: Topology of the GA15IDDJT22-FR4 Two Voltage Source gate driver.

The GA15IDDJT22-FR4 evaluation board comes equipped with two on board gate drive resistors (RG1, RG2) pre-installed for an effective gate resistance[3] of RG = 0.7 Ω. It may be necessary for the user to reduce RG1 and/or RG2 under high drain current conditions for safe operation of the GA100SICP12-227. The steady state current supplied to the gate pin of the GA100SICP12-227 with on-board RG = 0.7 Ω, is shown in Figure 26. The maximum allowable safe value of RG for the user's required drain current can be read from Figure 27.

For the GA100SICP12-227, R_G must be reduced or shorted for $I_D \geq$ ~40 A for safe operation with the GA15IDDJT22-FR4.

For operation at $I_D \geq$ ~40 A, R_G may be calculated from the following equation, which contains the DC current gain h_{FE} and the gate-source saturation voltage $V_{GS,sat}$ (Figure 7).

$$R_{G,max} = \frac{\left(4.7V - V_{GS,sat}\right) * h_{FE}(T, I_D)}{I_D * 1.5} - 0.1\Omega$$

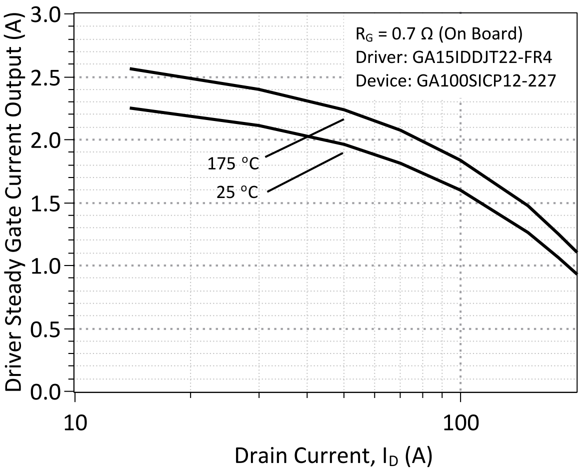

Figure 26: Typical steady state gate current supplied by the GA15IDDJT22-FR4 board for the GA100SICP12-227 with the on board resistance of 0.7 Ω

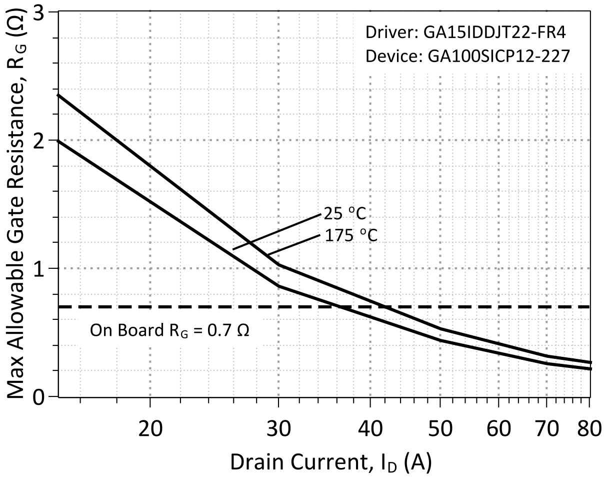

Figure 27: Maximum gate resistance for safe operation of the GA100SICP12-227 at different drain currents using the GA15IDDJT22-FR4 board.

B:2: High Speed, Low Loss Drive with Boost Inductor

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the GA100SICP12-227 at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses $I_{G,on}$ and $I_{G,off}$. During operation, inductor L is charged to a specified $I_{G,on}$ current value then made to discharge I_L into the SJT gate pin using logic control of S_1, S_2, S_3, and S_4, as shown in Figure 28. After turn on, while the device remains on the necessary steady state gate current $I_{G,steady}$ is supplied from source V_{CC} through R_G. Please refer to the article “A current-source concept for fast and efficient driving of silicon carbide transistors” by Dr. Jacek Rąbkowski for additional information on this driving topology.[4]

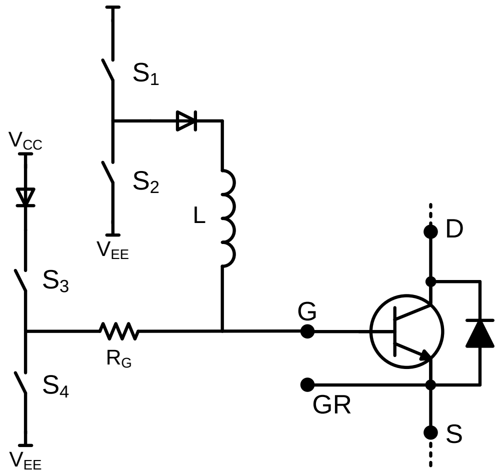

Figure 28: Simplified Inductive Pulsed Drive Topology

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[3] – $R_G = (1/RG1 + 1/RG2)^{-1}$. Driver is pre-installed with RG1 = 2.2 Ω, RG2 = 1.0 Ω

[4] – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/aee-2013-0026, June 2013

C: Proportional Gate Current Driving

For applications in which the GA100SICP12-227 will operate over a wide range of drain current conditions, it may be beneficial to drive the device using a proportional gate drive topology to optimize gate drive power consumption. A proportional gate driver relies on instantaneous drain current I_D feedback to vary the steady state gate current $I_{G,steady}$ supplied to the GA100SICP2-227

C:1: Voltage Controlled Proportional Driver

The voltage controlled proportional driver relies on a gate drive IC to detect the GA100SICP12-227 drain-source voltage V_{DS} during on-state to sense I_D. The gate drive IC will then increase or decrease $I_{G,steady}$ in response to I_D. This allows $I_{G,steady}$, and thus the gate drive power consumption, to be reduced while I_D is relatively low or for $I_{G,steady}$ to increase when is I_D higher. A high voltage diode connected between the drain and sense protects the IC from high-voltage when the driver and GA100SICP12-227 are in off-state. A simplified version of this topology is shown in Figure 29, additional information will be available in the future at http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/

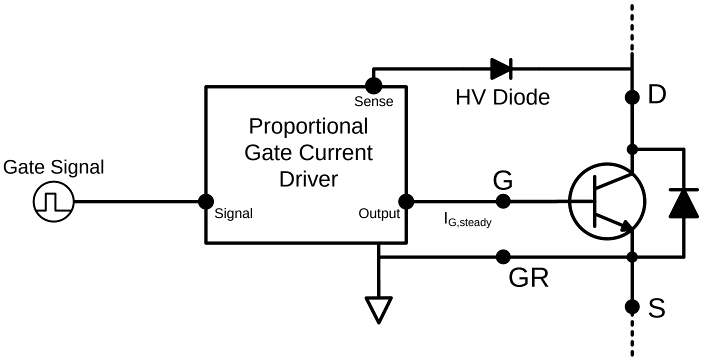


Figure 29: Simplified Voltage Controlled Proportional Driver

C:2: Current Controlled Proportional Driver

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback I_D of the GA100SICP12-227 during on-state to supply $I_{G,steady}$ into the device gate. $I_{G,steady}$ will then increase or decrease in response to I_D at a fixed forced current gain which is set be the turns ratio of the transformer, $h_{force} = I_D / I_G = N_2 / N_1$. GA100SICP12-227 is initially turned-on using a gate current pulse supplied into an RC drive circuit to allow I_D current to begin flowing. This topology allows $I_{G,steady}$, and thus the gate drive power consumption, to be reduced while I_D is relatively low or for $I_{G,steady}$ to increase when is I_D higher. A simplified version of this topology is shown in Figure 30, additional information will be available in the future at http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/.

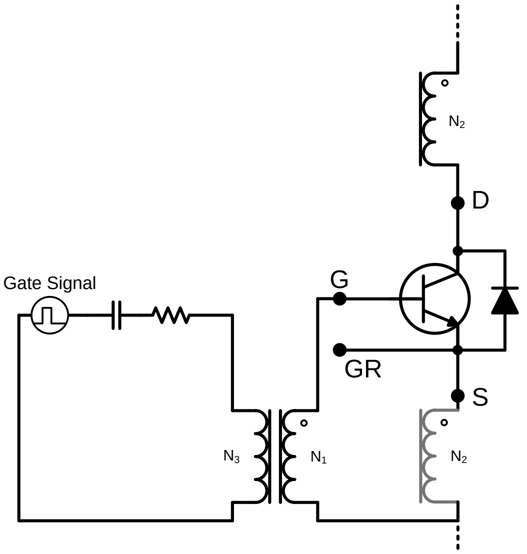
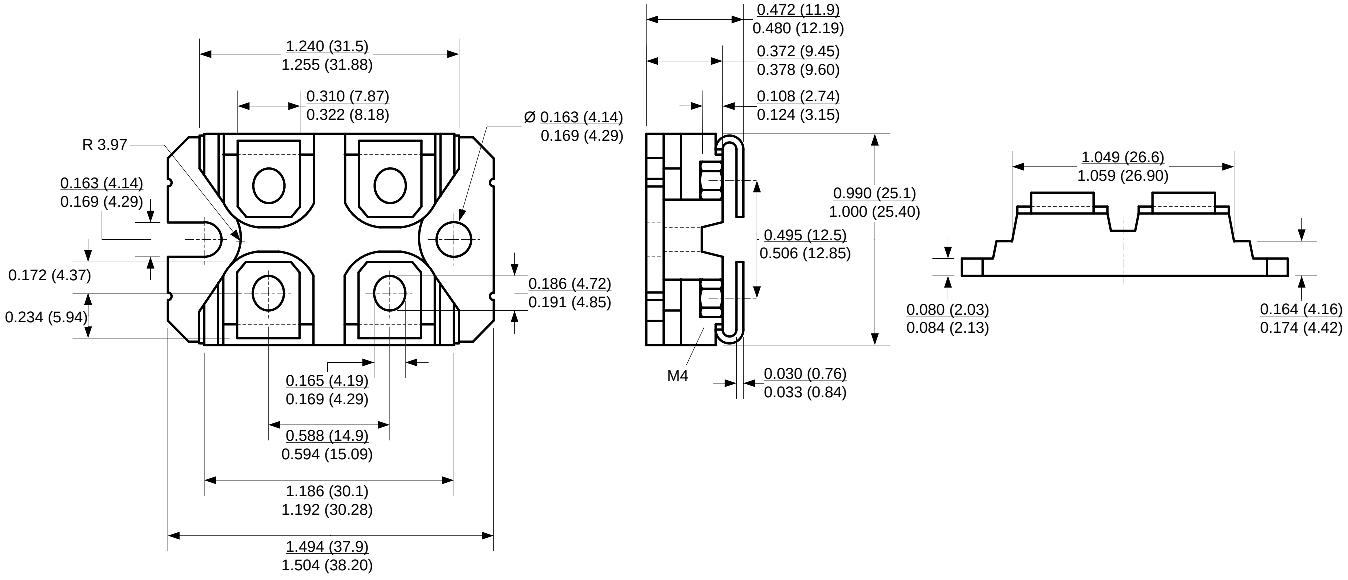


Figure 30: Simplified Current Controlled Proportional Driver

Section VI: Package Dimensions

SOT-227 PACKAGE OUTLINE



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2015/12/07	1	Updated Electrical Characteristics	
2015/03/30	0	Initial release	

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Section VII: SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/products_sic/igbt_copack/GA100SICP12-227_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA100SICP12-227.

```
*    MODEL OF GeneSiC Semiconductor Inc.
*    $Revision: 2.0              $
*    $Date:     07-DEC-2015      $
*
*    GeneSiC Semiconductor Inc.
*    43670 Trade Center Place Ste. 155
*    Dulles, VA 20166
*
*    COPYRIGHT (C) 2015 GeneSiC Semiconductor Inc.
*    ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
* Start of GA100SICP12-227 SPICE Model
.SUBCKT GA100SIPC12 DRAIN GATE SOURCE
QA1 DRAIN GATE SOURCE GA100SIPC12_Q
DA1 SOURCE DRAIN GA100SIPC12_D1
DA2 SOURCE DRAIN GA100SIPC12_D2
QB1 DRAIN GATE SOURCE GA100SIPC12_Q
DB1 SOURCE DRAIN GA100SIPC12_D1
DB2 SOURCE DRAIN GA100SIPC12_D2
.model GA100SIPC12_Q NPN
+ IS       9.833E-48       ISE        1.073E-26        EG         3.23
+ BF       89              BR         0.55             IKF        9000
+ NF       1               NE         2                RB         0.95
+ RE       0.004           RC         0.0125           CJC        2.398E-9
+ VJC      2.8346          MJC        0.4846           CJE        6.026E-09
+ VJE      3.1791          MJE        0.5295           XTI        3
+ XTB      -1.5            TRC1       9.0E-03          MFG   GeneSiC_Semi
+ IRB      0.005           RBM        0.073
.MODEL GA100SIPC12_D1 D
+ IS       1.99E-16        RS         0.015652965      N          1
+ IKF      1000            EG         1.2              XTI        3
+ TRS1     0.0042          TRS2       1.3E-05          CJO        3.86E-09
+ VJ       1.362328465     M          0.48198551       FC         0.5
+ TT       1.00E-10        IAVE       50
.MODEL GA100SIPC12_D2 D
+ IS       1.54E-19        RS         0.1              N          3.941
+ EG       3.23            TRS1       -0.004           IKF        19
+ XTI      0               FC         0.5              TT         0
.ENDS
* End of GA100SICP12-227 SPICE Model
```