

GB01SLT06-214

650V 1A SiC Schottky MPS™ Diode



Silicon Carbide Schottky Diode

V_{RRM}	=	650 V
$I_F (T_L \leq 150^\circ\text{C})$	=	1 A
Q_C	=	3 nC

Features

- Low V_F for High Temperature Operation
- Enhanced Surge and Avalanche Robustness
- Superior Figure of Merit Q_C/I_F
- Low Thermal Resistance
- Low Reverse Leakage Current
- Temperature Independent Fast Switching
- Positive Temperature Coefficient of V_F
- High dV/dt Ruggedness

Package



D0-214



Advantages

- Improved System Efficiency
- High System Reliability
- Optimal Price Performance
- Reduced Cooling Requirements
- Increased System Power Density
- Zero Reverse Recovery Current
- Easy to Parallel without Thermal Runaway
- Enables Extremely Fast Switching

Applications

- High Voltage Sensing
- Solar Inverters
- Electric Vehicles
- High Frequency Converters
- Battery Chargers
- Auxiliary Power Supplies
- Anti-Parallel / Free-Wheeling Diode
- LED and HID Lighting

Absolute Maximum Ratings (At $T_L = 25^\circ\text{C}$ Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Repetitive Peak Reverse Voltage	V_{RRM}		650	V	
Continuous Forward Current	I_F	$T_L \leq 150^\circ\text{C}$	1	A	
Non-Repetitive Peak Forward Surge Current, Half Sine Wave	I_{FSM}	$T_L = 25^\circ\text{C}, t_p = 10 \text{ ms}$	8	A	
		$T_L = 150^\circ\text{C}, t_p = 10 \text{ ms}$	7	A	
Repetitive Peak Forward Surge Current, Half Sine Wave	I_{FRM}	$T_L = 25^\circ\text{C}, t_p = 10 \text{ ms}$	5	A	
		$T_L = 150^\circ\text{C}, t_p = 10 \text{ ms}$	4	A	
Non-Repetitive Peak Forward Surge Current	I_{FMAX}	$T_L = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	40	A	
i^2t Value	$\int i^2 dt$	$T_L = 25^\circ\text{C}, t_p = 10 \text{ ms}$	0.32	A^2s	
Non-Repetitive Avalanche Energy	E_{AS}	$L = 33.6 \text{ mH}, I_{AS} = 1 \text{ A}$	17	mJ	
Diode Ruggedness	dV/dt	$V_R = 0 \sim 520 \text{ V}$	200	V/ns	
Power Dissipation	P_{TOT}	$T_L = 25^\circ\text{C}$	14	W	Fig. 3
Operating and Storage Temperature	T_j, T_{stg}		-55 to 175	$^\circ\text{C}$	

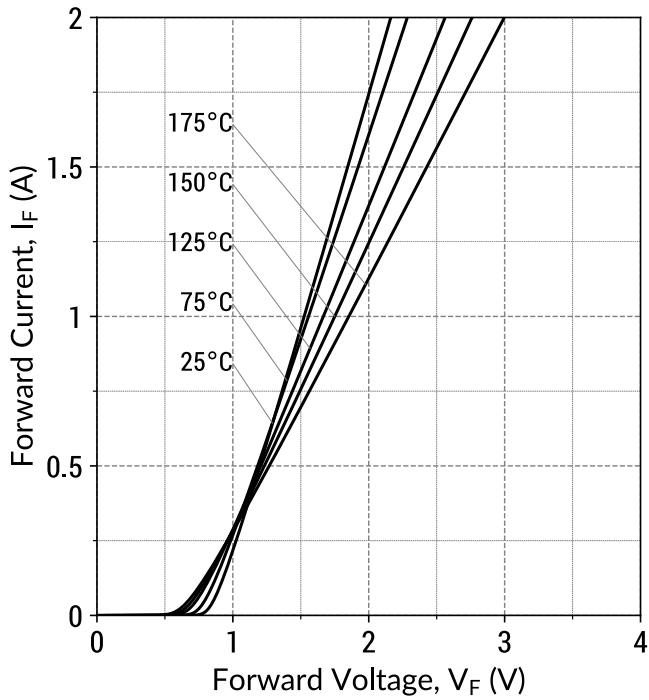
Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_F	$I_F = 1 \text{ A}, T_j = 25^\circ\text{C}$		1.5	1.8	V	Fig. 1
		$I_F = 1 \text{ A}, T_j = 175^\circ\text{C}$		1.8			
Reverse Current	I_R	$V_R = 650 \text{ V}, T_j = 25^\circ\text{C}$		1	5	μA	Fig. 2
		$V_R = 650 \text{ V}, T_j = 175^\circ\text{C}$		1			
Total Capacitive Charge	Q_C	$I_F \leq I_{F,MAX}$ $di_F/dt = 200 \text{ A}/\mu\text{s}$	$V_R = 200 \text{ V}$	2		nC	Fig. 5
			$V_R = 400 \text{ V}$	3			
Switching Time	t_s		$V_R = 200 \text{ V}$	< 10		ns	
Total Capacitance	C	$V_R = 1 \text{ V}, f = 1\text{MHz}$		45		pF	Fig. 4
		$V_R = 400 \text{ V}, f = 1\text{MHz}$		4			

Thermal/Package Characteristics

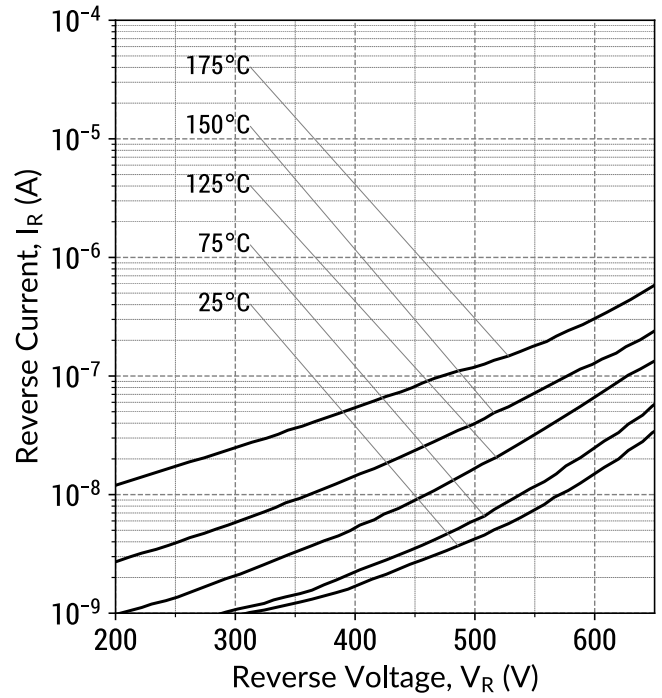
Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Thermal Resistance, Junction - Lead	R_{thJL}			10.54		$^\circ\text{C}/\text{W}$	
Weight	W_T			0.1		g	

Figure 1: Typical Forward Characteristics



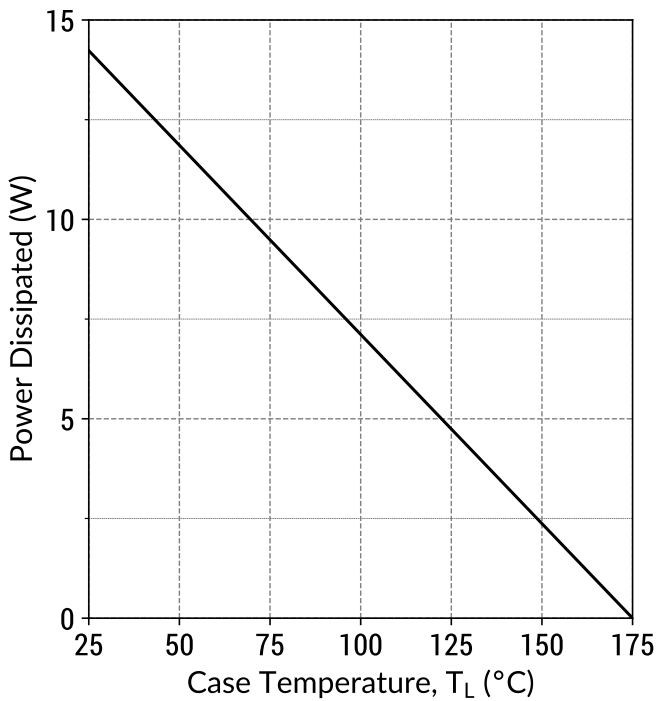
$$I_F = f(V_F, T_j); t_p = 250 \mu s$$

Figure 2: Typical Reverse Characteristics



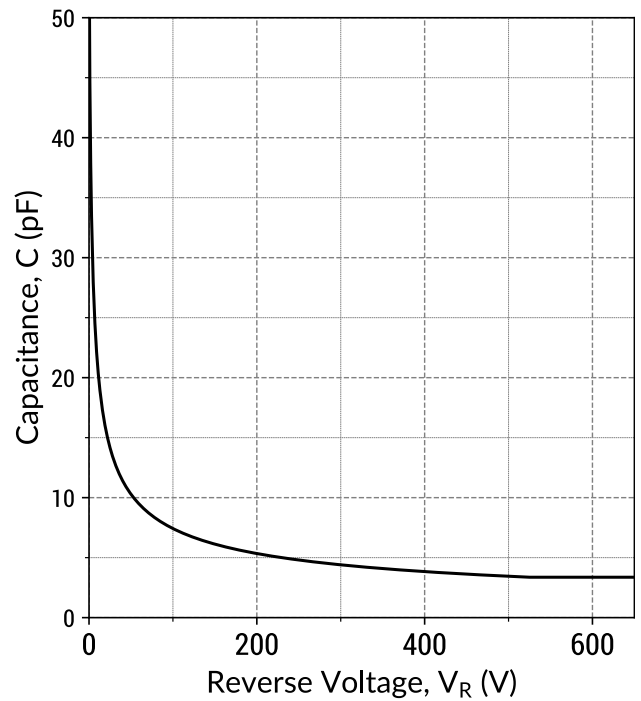
$$I_R = f(V_R, T_j)$$

Figure 3: Power Derating Curves



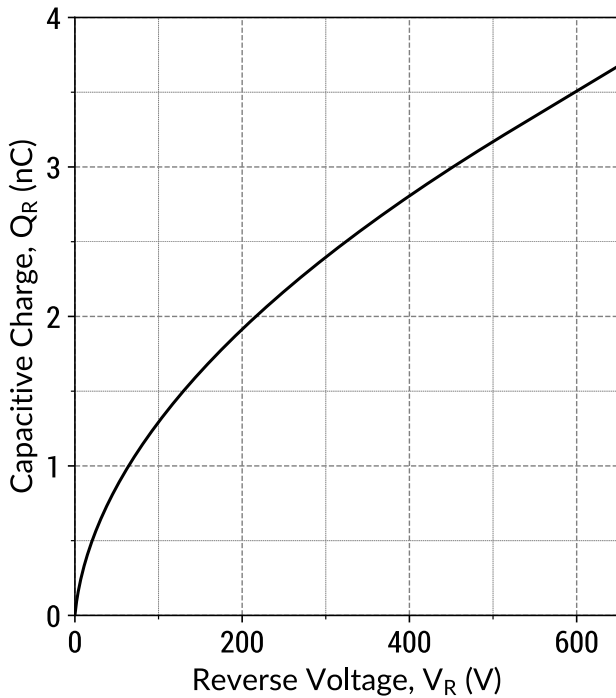
$$P_{TOT} = f(T_L); T_j = 175^\circ C$$

Figure 4: Typical Junction Capacitance vs Reverse Voltage Characteristics



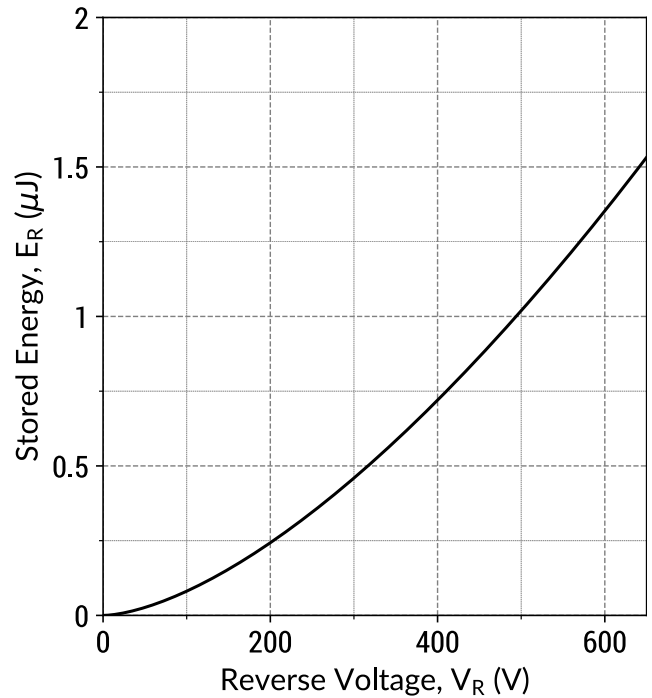
$$C = f(V_R); f = 1 \text{ MHz}$$

Figure 5: Typical Capacitive Charge vs Reverse Voltage Characteristics



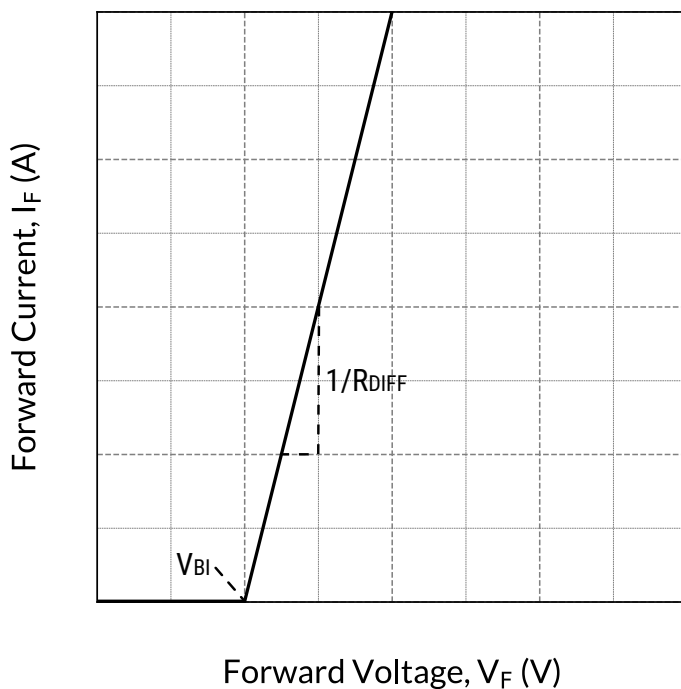
$$Q_C = f(V_R); f = 1\text{MHz}$$

Figure 6: Typical Capacitive Energy vs Reverse Voltage Characteristics



$$E_C = f(V_R); f = 1\text{MHz}$$

Figure 7: Forward Curve Model



$$I_F = f(V_F, T_j)$$

Forward Curve Model Equation:

$$I_F = (V_F - V_{BI})/R_{DIFF} \text{ (A)}$$

Built-In Voltage (V_{BI}):

$$V_{BI}(T_j) = m \times T_j + n \text{ (V)}$$

$$m = -0.0012 \text{ (V/°C)}$$

$$n = 0.916 \text{ (V)}$$

Differential Resistance (R_{DIFF}):

$$R_{DIFF}(T_j) = a \times T_j^2 + b \times T_j + c \text{ (Ω)}$$

$$a = 1.58e-05 \text{ (Ω/°C}^2\text{)}$$

$$b = 0.000228 \text{ (Ω/°C)}$$

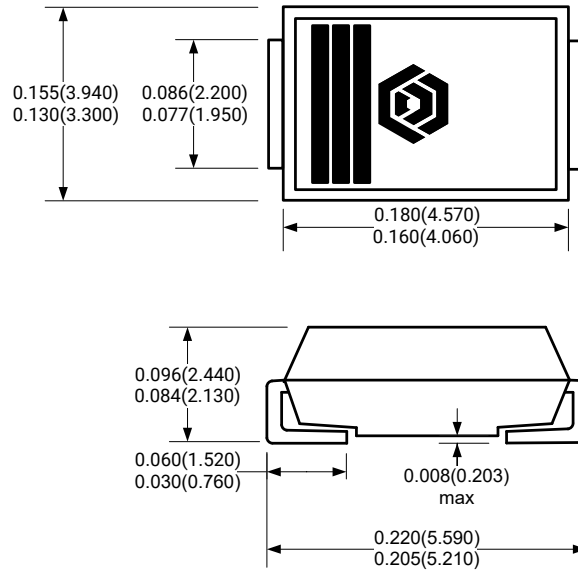
$$c = 0.624 \text{ (Ω)}$$

Forward Power Loss Equation:

$$P_{LOSS} = V_{BI}(T_j) \times I_{AVG} + R_{DIFF}(T_j) \times I_{RMS}^2$$

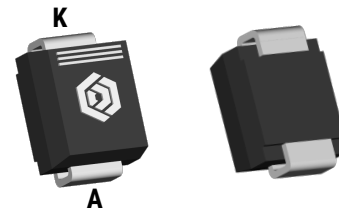
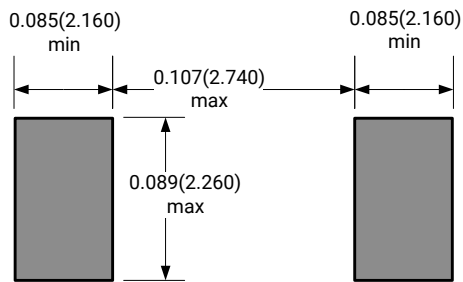
Package Dimensions

DO-214 Package Outline



Recommended Solder Pad Layout

Package View



NOTE

1. CONTROLLED DEIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

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