GigaDevice Semiconductor Inc.

GD32F150xx
ARM® Cortex®-M3 32-bit MCU

Datasheet

Table of Contents

List of Figures

List of Tables

1 General description

The GD32F150xx device belongs to the value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance ARM® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F150xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 72 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, one 12-bit DAC and two comparators, up to five general-purpose 16-bit timers, a general-purpose 32-bit timer, a basic timer, a PWM advanced-control timer, as well as standard and advanced communication interfaces: up to two SPIs, two I^2Cs, two USARTs, a I^2S, a HDMI-CEC a TSI and an USB 2.0 FS.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F150xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2 Device overview

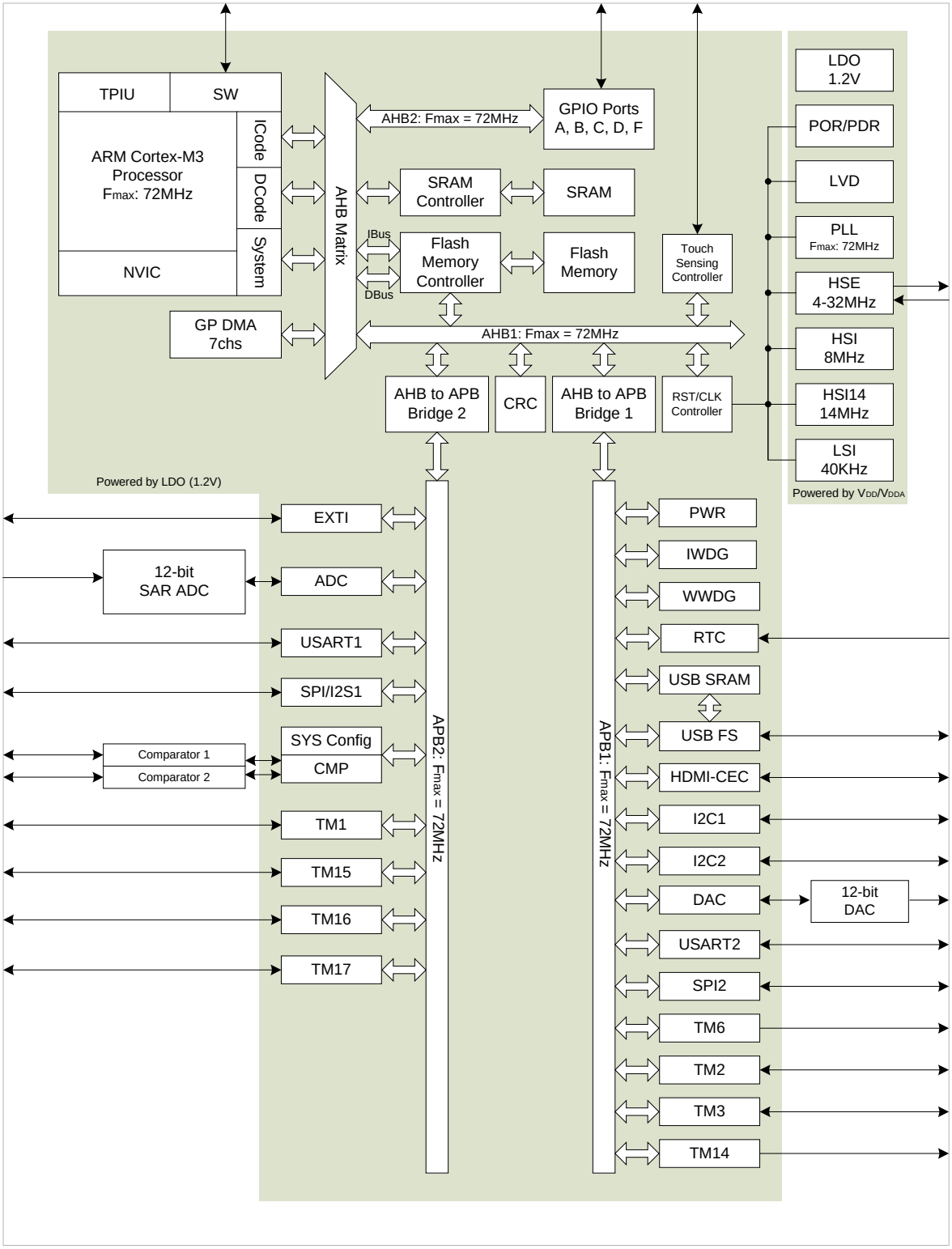
2.1 Device information

Table 1. GD32F150xx devices features and peripheral list

Part Number		GD32F150xx											
		G4	G6	G8	K4	K6	K8	C4	C6	C8	R4	R6	R8
Flash (KB)		16	32	64	16	32	64	16	32	64	16	32	64
SRAM (KB)		4	6	8	4	6	8	4	6	8	4	6	8
Timers	32-bit GP	1	1	1	1	1	1	1	1	1	1	1	1
	16-bit GP	5	5	5	5	5	5	5	5	5	5	5	5
	16-bit Adv.	1	1	1	1	1	1	1	1	1	1	1	1
	16-bit Basic	1	1	1	1	1	1	1	1	1	1	1	1
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	1	2	2	1	2	2	1	2	2	1	2	2
	I2C	1	1	2	1	1	2	1	1	2	1	1	2
	SPI	1	1	2	1	1	2	1	1	2	1	1	2
	I2S	1	1	1	1	1	1	1	1	1	1	1	1
	USB 2.0 FS	1	1	1	1	1	1	1	1	1	1	1	1
	HDMI CEC	1	1	1	1	1	1	1	1	1	1	1	1
GPIO		24	24	24	27	27	27	39	39	39	55	55	55
Capacitive Touch Channels		14	14	14	14	14	14	17	17	17	18	18	18
Analog Comparator		2	2	2	2	2	2	2	2	2	2	2	2
EXTI		16	16	16	16	16	16	16	16	16	16	16	16
ADC	Units	1	1	1	1	1	1	1	1	1	1	1	1
	Channels (Ext.)	10	10	10	10	10	10	10	10	10	16	16	16
	Channels (Int.)	3	3	3	3	3	3	3	3	3	3	3	3
DAC		1	1	1	1	1	1	1	1	1	1	1	1
Package		QFN28			QFN32			LQFP48			LQFP64		

2.2 Block diagram

Figure 1. GD32F150xx block diagram



2.3 Pinouts and pin assignment

Figure 2. GD32F150Rx LQFP64 pinouts

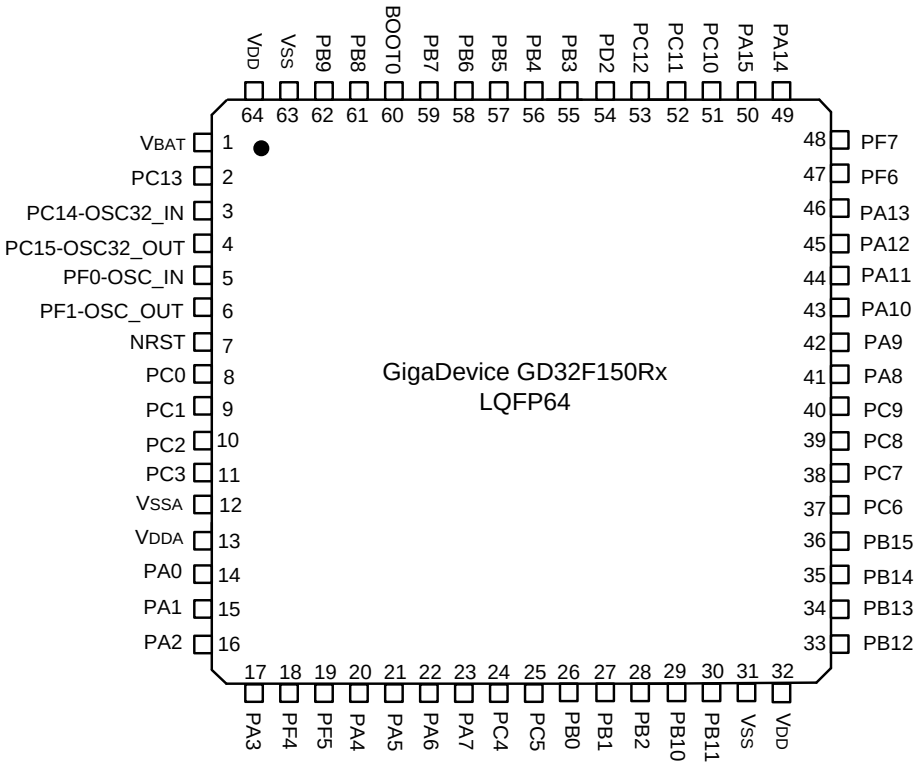


Figure 3. GD32F150Cx LQFP48 pinouts

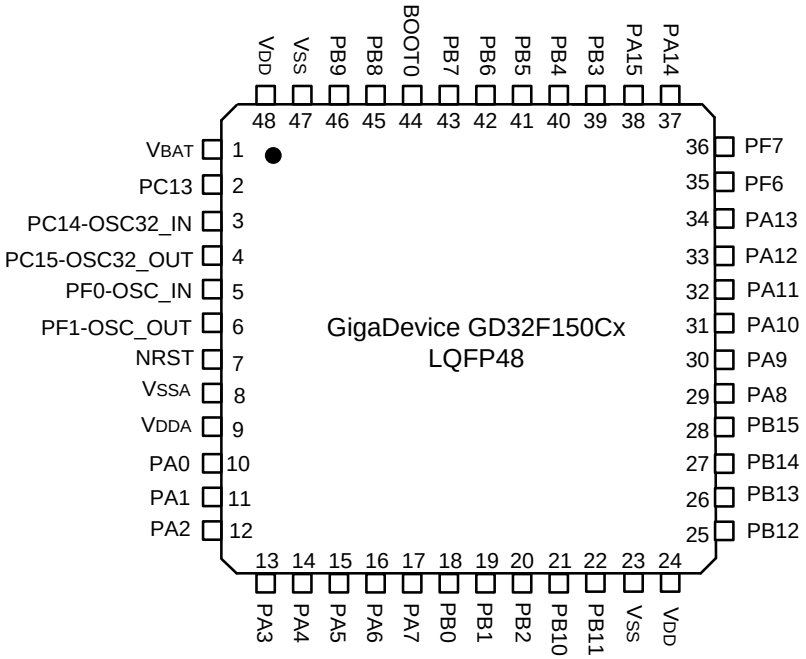


Figure 4. GD32F150Kx QFN32 pinouts

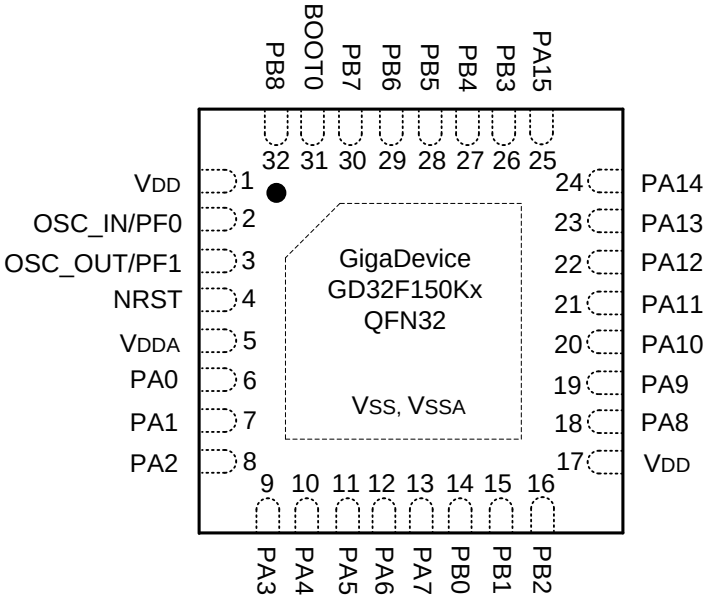
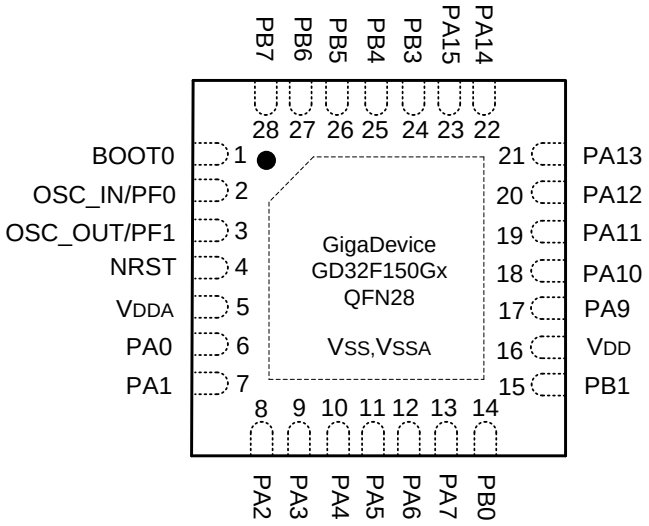
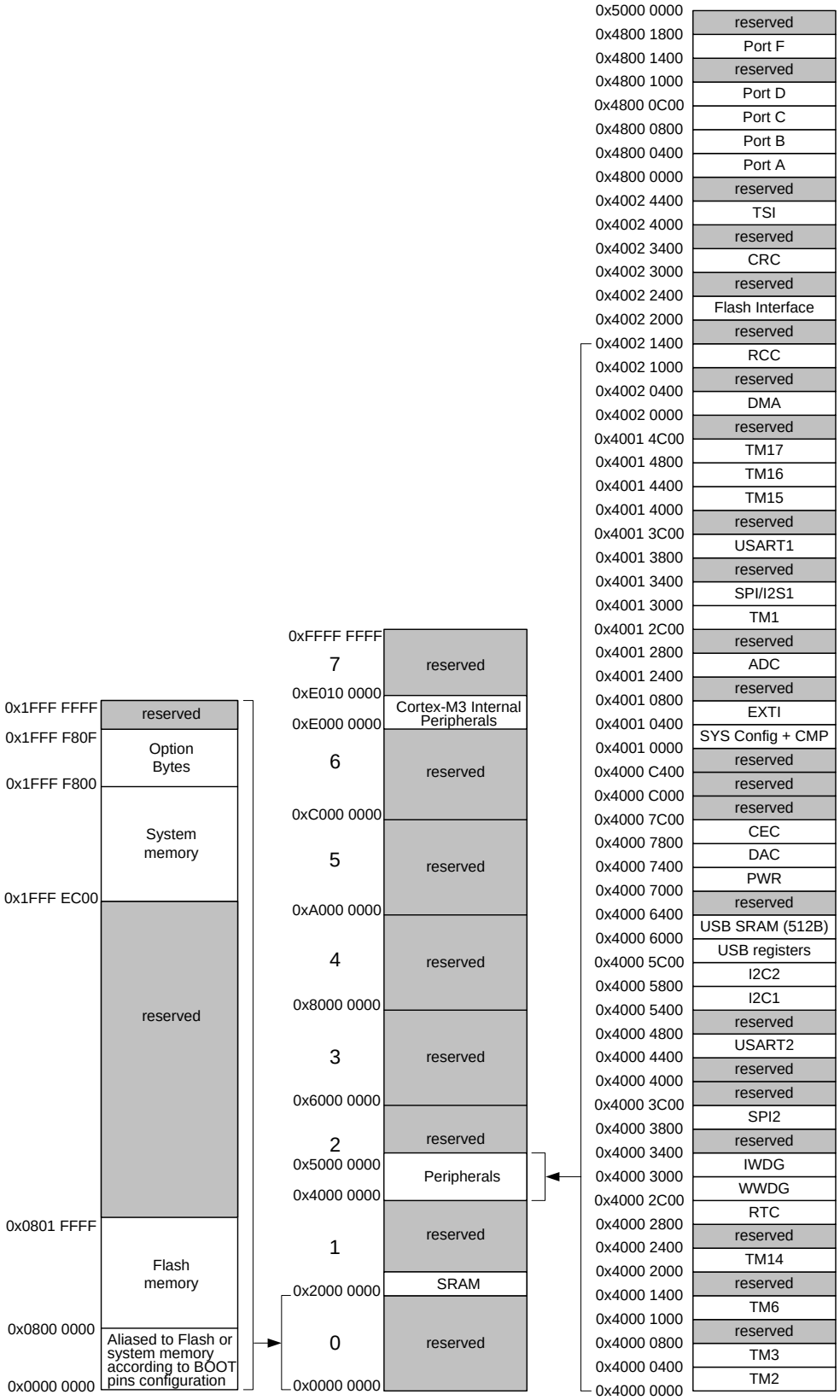


Figure 5. GD32F150Gx QFN28 pinouts



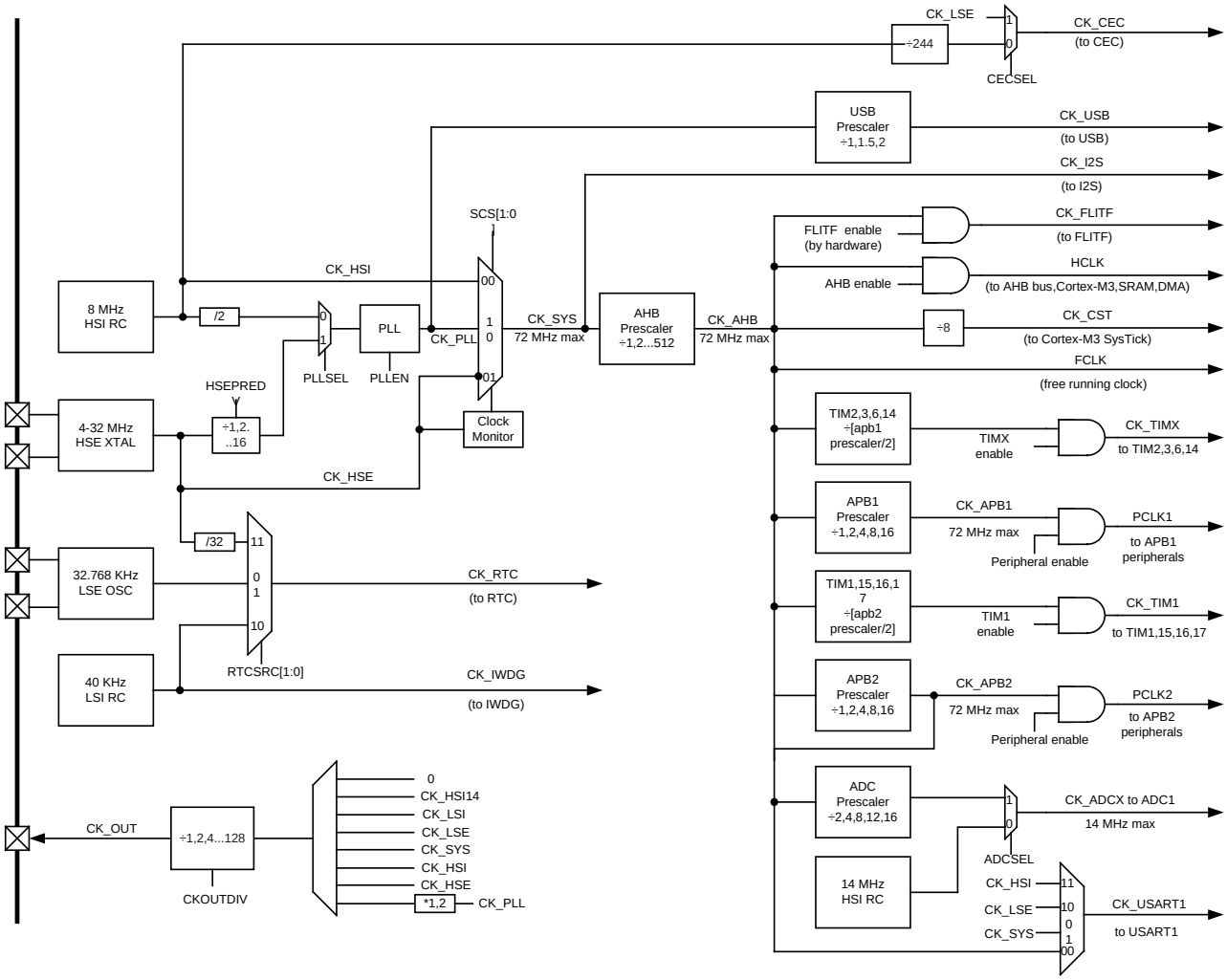
2.4 Memory map

Figure 6. GD32F150xx memory map



2.5 Clock tree

Figure 7. GD32F150xx clock tree



Legend:

HSE = High speed external clock

HSI = High speed internal clock

LSE = Low speed external clock

LSI = Low speed internal clock

2.6 Pin definitions

Table 2. GD32F150xx pin definitions

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
V_{BAT}	1	1	-	-	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	2	-	-	I/O		Default: PC13 Additional: RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
PC14-OSC32_IN	3	3	-	-	I/O		Default: PC14 Additional: OSC32_IN
PC15-OSC32_OUT	4	4	-	-	I/O		Default: PC15 Additional: OSC32_OUT
PF0-OSC_IN	5	5	2	2	I/O	5VT	Default: PF0 Additional: OSC_IN
PF1-OSC_OUT	6	6	3	3	I/O	5VT	Default: PF1 Additional: OSC_OUT
NRST	7	7	4	4	I/O		Default: NRST
PC0	8	-	-	-	I/O		Default: PC0 Alternate: EVENTOUT Additional: ADC_IN10
PC1	9	-	-	-	I/O		Default: PC1 Alternate: EVENTOUT Additional: ADC_IN11
PC2	10	-	-	-	I/O		Default: PC2 Alternate: EVENTOUT Additional: ADC_IN12
PC3	11	-	-	-	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC_IN13
V_{SSA}	12	8	0	0	P		Default: V_{SSA}
V_{DDA}	13	9	5	5	P		Default: V_{DDA}
PA0-WKUP	14	10	6	6	I/O		Default: PA0 Alternate: USART1_CTS(3), USART2_CTS(4), TM2_CH1_ETR, CMP1_OUT, TSI_G1_IO1, I2C2_SCL Additional: ADC_IN0, CMP1_INM6, RTC_TAMP2, WKUP1
PA1	15	11	7	7	I/O		Default: PA1 Alternate: USART1_RTS(3), USART2_RTS(4), TM2_CH2, TSI_G1_IO2, I2C2_SDA, EVENTOUT Additional: ADC_IN1, CMP1_INP
PA2	16	12	8	8	I/O		Default: PA2 Alternate: USART1_TX(3), USART2_TX(4), TM2_CH3, TM15_CH1 , CMP2_OUT,

Pin Name	Pins				Pin Type[1]	I/O[2] Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
							TSI_G1_IO3 Additional: ADC_IN2, CMP2_INM6
PA3	17	13	9	9	I/O		Default: PA3 Alternate: USART1_RX[3], USART2_RX[4], TM2_CH4, TM15_CH2, TSI_G1_IO4 Additional: ADC_IN3/CMP2_INP
PF4	18	-	-	-	I/O	5VT	Default: PF4 Alternate: SPI2_NSS, EVENTOUT
PF5	19	-	-	-	I/O	5VT	Default: PF5 Alternate: EVENTOUT
PA4	20	14	10	10	I/O		Default: PA4 Alternate: SPI1_NSS, I2S1_WS, USART1_RX[3], USART2_RX[4], TM14_CH1, TSI_G2_IO1, SPI2_NSS Additional: ADC_IN4, CMP1_INM4, CMP2_INM4, DAC1_OUT
PA5	21	15	11	11	I/O		Default: PA5 Alternate: SPI1_SCK, I2S1_CK, CEC, TM2_CH1_ETR, TSI_G2_IO2 Additional: ADC_IN5, CMP1_INM5, CMP2_INM5
PA6	22	16	12	12	I/O		Default: PA6 Alternate: SPI1_MISO, I2S1_MCK, TM3_CH1, TM1_BKIN, TM16_CH1, CMP1_OUT, TSI_G2_IO3, EVENTOUT Additional: ADC_IN6
PA7	23	17	13	13	I/O		Default: PA7 Alternate: SPI1_MOSI, I2S1_SD, TM3_CH2, TM14_CH1, TM1_CH1N, TM17_CH1, CMP2_OUT, TSI_G2_IO4, EVENTOUT Additional: ADC_IN7
PC4	24	-	-	-	I/O		Default: PC4 Alternate: EVENTOUT Additional: ADC_IN14
PC5	25	-	-	-	I/O		Default: PC5 Alternate: TSI_G3_IO1 Additional: ADC_IN15
PB0	26	18	14	14	I/O		Default: PB0 Alternate: TM3_CH3, TM1_CH2N, TSI_G3_IO2, USART2_RX, EVENTOUT Additional: ADC_IN8
PB1	27	19	15	15	I/O		Default: PB1 Alternate: TM3_CH4, TM14_CH1, TM1_CH3N, TSI_G3_IO3, SPI2_SCK Additional: ADC_IN9
PB2	28	20	16	-	I/O	5VT	Default: PB2 Alternate: TSI_G3_IO4
PB10	29	21	-	-	I/O	5VT	Default: PB10 Alternate: I2C2_SCL, CEC, TM2_CH3, TSI_SYNC
PB11	30	22	-	-	I/O	5VT	Default: PB11

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
							Alternate: I2C2_SDA, TM2_CH4, TSI_G6_IO1, EVENTOUT
V_{SS}	31	23	-	-	P		Default: V_{SS}
V_{DD}	32	24	17	16	P		Default: V_{DD}
PB12	33	25	-	-	I/O	5VT	Default: PB12 Alternate: SPI1_NSS(3), SPI2_NSS(4), TM1_BKIN, TSI_G6_IO2, I2C2_SMBA, EVENTOUT
PB13	34	26	-	-	I/O	5VT	Default: PB13 Alternate: SPI1_SCK(3), SPI2_SCK(4), TM1_CH1N, TSI_G6_IO3
PB14	35	27	-	-	I/O	5VT	Default: PB14 Alternate: SPI1_MISO(3), SPI2_MISO(4), TM1_CH2N, TM15_CH1, TSI_G6_IO4
PB15	36	28	-	-	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI(3), SPI2_MOSI(4), TIM1_CH3N, TM15_CH1N, TM15_CH2 Additional: RTC_REFIN
PC6	37	-	-	-	I/O	5VT	Default: PC6 Alternate: TM3_CH1
PC7	38	-	-	-	I/O	5VT	Default: PC7 Alternate: TM3_CH2
PC8	39	-	-	-	I/O	5VT	Default: PC8 Alternate: TM3_CH3
PC9	40	-	-	-	I/O	5VT	Default: PC9 Alternate: TM3_CH4
PA8	41	29	18	-	I/O	5VT	Default: PA8 Alternate: USART1_CK, TM1_CH1, MCO, USART2_TX, EVENTOUT
PA9	42	30	19	17	I/O	5VT	Default: PA9 Alternate: USART1_TX, TM1_CH2, TM15_BKIN, TSI_G4_IO1, I2C1_SCL
PA10	43	31	20	18	I/O	5VT	Default: PA10 Alternate: USART1_RX, TM1_CH3, TM17_BKIN, TSI_G4_IO2, I2C1_SDA
PA11	44	32	21	19	I/O	5VT	Default: PA11 Alternate: USART1_CTS, TM1_CH4, CMP1_OUT, TSI_G4_IO3, EVENTOUT Additional: USBDM
PA12	45	33	22	20	I/O	5VT	Default: PA12 Alternate: USART1_RTS, TM1_ETR, CMP2_OUT, TSI_G4_IO4, EVENTOUT Additional: USBDP
PA13	46	34	23	21	I/O	5VT	Default: PA13 Alternate: IR_OUT, SWDAT, SPI2_MISO
PF6	47	35	-	-	I/O	5VT	Default: I2C2_SCL
PF7	48	36	-	-	I/O	5VT	Default: I2C2_SDA
PA14	49	37	24	22	I/O	5VT	Default: PA14

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
							Alternate: USART1_TX(3), USART2_TX(4), SWCLK, SPI2_MOSI
PA15	50	38	25	23	I/O	5VT	Default: PA15 Alternate: SPI1_NSS, I2S1_WS, USART1_RX(3), USART2_RX(4), TM2_CH1_ETR, SPI2_NSS, EVENTOUT
PC10	51	-	-	-	I/O	5VT	Default: PC10
PC11	52	-	-	-	I/O	5VT	Default: PC11
PC12	53	-	-	-	I/O	5VT	Default: PC12
PD2	54	-	-	-	I/O	5VT	Default: PD2 Alternate: TM3_ETR
PB3	55	39	26	24	I/O	5VT	Default: PB3 Alternate: SPI1_SCK/I2S1_CK, TM2_CH2, TSI_G5_IO1, EVENTOUT
PB4	56	40	27	25	I/O	5VT	Default: PB4 Alternate: SPI1_MISO/I2S1_MCK, TM3_CH1, TSI_G5_IO2, EVENTOUT
PB5	57	41	28	26	I/O	5VT	Default: PB5 Alternate: SPI1_MOSI/I2S1_SD, I2C1_SMBA, TM16_BKIN, TM3_CH2
PB6	58	42	29	27	I/O	5VT	Default: PB6 Alternate: I2C1_SCL, USART1_TX, TM16_CH1N, TSI_G5_IO3
PB7	59	43	30	28	I/O	5VT	Default: PB7 Alternate: I2C1_SDA, USART1_RX, TM17_CH1N,TSI_G5_IO4
BOOT0	60	44	31	1	I		Default: BOOT0
PB8	61	45	32	-	I/O	5VT	Default: PB8 Alternate: I2C1_SCL, CEC, TM16_CH1, TSI_SYNC
PB9	62	46	-	-	I/O	5VT	Default: PB9 Alternate: I2C1_SDA, IR_OUT, TM17_CH1, EVENTOUT
V_{SS}	63	47	0	0	P		Default: V_{SS}
V_{DD}	64	48	1	-	P		Default: V_{DD}

Notes:

1. Type: I = input, O = output, P = power.
2. I/O Level: 5VT = 5 V tolerant.
3. This feature is available on GD32F150x4 devices only.
4. This feature is available on GD32F150x8 and GD32F150x6 devices only.

Table 3. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART1_CTS(1) USART2_CTS(2)	TM2_CH1_ ETR	TSI_G1_IO1	I2C2_SCL			CMP1_OUT
PA1	EVENTOUT	USART1_RTS(1) USART2_RTS(2)	TM2_CH2	TSI_G1_IO2	I2C2_SDA			
PA2	TM15_CH1	USART1_TX(1) USART2_TX(2)	TM2_CH3	TSI_G1_IO3				CMP2_OUT
PA3	TM15_CH2	USART1_RX(1) USART2_RX(2)	TM2_CH4	TSI_G1_IO4				
PA4	SPI1_NSS/ I2S1_WS	USART1_CK(1) USART2_CK(2)		TSI_G2_IO1	TM14_CH1		SPI2_NSS	
PA5	SPI1_SCK/ I2S1_CK	CEC	TM2_CH1_ ETR	TSI_G2_IO2				
PA6	SPI1_MISO/ I2S1_MCK	TM3_CH1	TM1_BKIN	TSI_G2_IO3		TM16_CH1	EVENTOUT	CMP1_OUT
PA7	SPI1_MOSI/ I2S1_SD	TM3_CH2	TM1_CH1N	TSI_G2_IO4	TM14_CH1	TM17_CH1	EVENTOUT	CMP2_OUT
PA8	MCO	USART1_CK	TM1_CH1	EVENTOUT	USART2_TX			
PA9	TM15_BKIN	USART1_TX	TM1_CH2	TSI_G4_IO1	I2C1_SCL			
PA10	TM17_BKIN	USART1_RX	TM1_CH3	TSI_G4_IO2	I2C1_SDA			
PA11	EVENTOUT	USART1_CTS	TM1_CH4	TSI_G4_IO3				CMP1_OUT
PA12	EVENTOUT	USART1_RTS	TM1_ETR	TSI_G4_IO4				CMP2_OUT
PA13	SWDAT	IR_OUT					SPI2_MISO	
PA14	SWCLK	USART1_TX(1) USART2_TX(2)					SPI2_MOSI	
PA15	SPI1_NSS/ I2S1_WS	USART1_RX(1) USART2_RX(2)	TM2_CH1_ ETR	EVENTOUT			SPI2_NSS	

1. This feature is available on GD32F150x4 devices only.
2. This feature is available on GD32F150x8 and GD32F150x6 devices only.

Table 4. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PB0	EVENTOUT	TM3_CH3	TM1_CH2N	TSI_G3_IO2	USART2_RX		
PB1	TM14_CH1	TM3_CH4	TM1_CH3N	TSI_G3_IO3			SPI2_SCK
PB2				TSI_G3_IO4			
PB3	SPI1_SCK / I2S1_CK	EVENTOUT	TM2_CH2	TSI_G5_IO1			
PB4	SPI1_MISO / I2S1_MCK	TM3_CH1	EVENTOUT	TSI_G5_IO2			
PB5	SPI1_MOSI / I2S1_SD	TM3_CH2	TM16_BKIN	I2C1_SMBA			
PB6	USART1_TX	I2C1_SCL	TM16_CH1N	TSI_G5_IO3			
PB7	USART1_RX	I2C1_SDA	TM17_CH1N	TSI_G5_IO4			
PB8	CEC	I2C1_SCL	TM16_CH1	TSI_SYNC			
PB9	IR_OUT	I2C1_SDA	TM17_CH1	EVENTOUT			
PB10	CEC	I2C2_SCL	TM2_CH3	TSI_SYNC			
PB11	EVENTOUT	I2C2_SDA	TM2_CH4	TSI_G6_IO1			
PB12	SPI1_NSS(1) SPI2_NSS(2)	EVENTOUT	TM1_BKIN	TSI_G6_IO2	I2C2_SMBA		
PB13	SPI1_SCK(1) SPI2_SCK(2)		TM1_CH1N	TSI_G6_IO3			
PB14	SPI1_MISO(1) SPI2_MISO(2)	TM15_CH1	TM1_CH2N	TSI_G6_IO4			
PB15	SPI1_MOSI(1) SPI2_MOSI(2)	TM15_CH2	TM1_CH3N	TM15_CH1N			

1. This feature is available on GD32F150x4 devices only.
2. This feature is available on GD32F150x8 and GD32F150x6 devices only.

3 Functional description

3.1 ARM® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex®-M3 processor core
- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2 On-chip memory

- Up to 64 Kbytes of Flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

The ARM® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 64 Kbytes of inner Flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The Figure 7. GD32F150xx memory map shows the memory map of the GD32F150xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 72 MHz. See Figure 9 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART1 in device mode.

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (HSI, HSE) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the HSI is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of HSI, HSE and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the IWDG reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC engine with up to 1 MSPS conversion rate
- Conversion range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

One 12-bit 1 μs multi-channel ADC is integrated in the device. It is a total of up to 16 multiplexed external channels and 3 internal channels for temperature sensor, voltage reference, V_{BAT} voltage measurement. The conversion range is between 2.6 V < V_{DDA} < 3.6 V. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages. The ADC can be triggered from the events generated by the general-purpose timers (TMx) and the advanced-control timers (TM1) with internal connection.

The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

3.7 Digital to analog converter (DAC)

- 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DAC is designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V_{REF+}.

3.8 DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I^2Cs, USARTs, DAC and I^2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9 General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F150xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10 Timers and PWM generation

- One 16-bit advanced-control timer (TM1), one 32-bit general-purpose timer (TM2), five 16-bit general-purpose timers (TM3, TM14 ~ TM17), and one 16-bit basic timer (TM6)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Independent watchdog and window watchdog)

The advanced-control timer (TM1) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM) can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TM14 ~ TM17 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TM6, is mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F150xx have two watchdog peripherals, Independent watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The independent watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It

features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11 Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

3.12 Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 kHz of standard mode or 400 kHz of the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13 Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14 Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 9 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART1, USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.15 Inter-IC sound (I2S)

- One I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz, multiplexed with SPI1
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F150xx contain a I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 kHz to 192 kHz is supported with less than 0.5% accuracy error.

3.16 HDMI CEC

- Hardware support Consumer Electronics Control (CEC) protocol (HDMI standard rev1.4)

The CEC protocol provides high-level control functions between the audiovisual products linked with HDMI cables. GD32F150xx contain a HDMI-CEC controller which has an independent clock domain and can wake up the MCU from deep-sleep mode on data reception.

3.17 Universal serial bus full-speed (USB 2.0 FS)

- One full-speed USB Interface with frequency up to 12 Mbit/s
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between one or more devices. Full-speed peripheral is compliant with the USB 2.0 specification. The device controller enables 12 Mbit/s data exchange with a USB Host controller. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator) and the operating frequency divided from APB1 should be 12 MHz above.

3.18 Touch sensing interface (TSI)

- Supports up to 18 external electrodes by the sensing channels distributed over 6 analog I/O groups
- Programmable charging frequency and I/O pins
- Capability to wake up the MCU from power saving modes

Capacitive sensing technology can be used for the detection of a finger (or any conductive object) presence near an electrode. The capacitive variation of the electrode introduced by the finger can be measured by charging and detecting the voltage across the sampling capacitor. GD32F150xx contain a hardware touch sensing interface (TSI) and only requires few external components to operate. The sensing channels are distributed over 6 analog I/O groups including: Group1 (PA0 ~ PA3), Group2 (PA4 ~ PA7), Group3 (PC5, PB0 ~ PB2), Group4 (PA9 ~ PA12), Group5 (PB3,PB4, PB6,PA7) and Group6 (PB11 ~ PB14),

3.19 Comparators (CMP)

- Two fast rail-to-rail low-power comparators with software configurable
- Programmable reference voltage (internal, external I/O or DAC output pin)

Two Comparators (CMP) are implemented within the devices. Both comparators can wake up from deep-sleep mode to generate interrupts and breaks for the timers and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.20 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.21 Package and operation temperature

- LQFP64 (GD32F150Rx), LQFP48 (GD32F150Cx), QFN32 (GD32F150Kx) and QFN28 (GD32F150Gx)
- Operation temperature range: -40°C to +85°C (industrial level)

4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2 Recommended DC characteristics

Table 6. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 7. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{DDA}=3.3V, HSE=8MHz, System clock=72 MHz, All peripherals enabled	—	26.10	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, System clock =72 MHz, All peripherals disabled	—	17.69	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, System clock =48 MHz, All peripherals enabled	-—	17.81	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, System Clock =48 MHz, All peripherals disabled	—	12.21	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{DDA}=3.3V, HSE=8MHz, CPU clock off, System clock =72 MHz, All peripherals enabled	—	14.86	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, CPU clock off, System clock =72 MHz, All peripherals disabled	—	5.19	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{DDA}=3.3V, Regulator in run mode, LSI on, RTC on, All GPIOs analog mode	—	172.49	—	µA
		V_{DD}=V_{DDA}=3.3V, Regulator in low power mode, LSI on, RTC on, All GPIOs analog mode	—	160.84	—	µA
	Supply current (Standby mode)	V_{DD}=V_{DDA}=3.3V, LSE off, LSI on, RTC on	—	7.39	—	µA
		V_{DD}=V_{DDA}=3.3V, LSE off, LSI on, RTC off	—	6.93	—	µA
		V_{DD}=V_{DDA}=3.3V, LSE off, LSI off, RTC off	—	5.72	—	µA
I_{BAT}	Battery supply current	V_{DD} not available, V_{BAT}=3.6 V, LSE on with external crystal, RTC on, Higher driving	—	3.12	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LSE on with external crystal, RTC on, Higher driving	—	2.80	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LSE on with external crystal, RTC on, Higher driving	—	2.16	—	µA
		V_{DD} not available, V_{BAT}=3.6 V, LSE on with external crystal, RTC on, Lower driving	—	1.40	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LSE on with external crystal, RTC on, Lower driving	—	1.29	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LSE on with external crystal, RTC on, Lower driving	—	1.10	—	µA

4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the following table, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 8. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in the following table, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 9. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions		Unit
				48M	72M	
S_{EMI}	Peak level	VDD = 3.3 V, TA = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	dBµV
			2 to 30 MHz	-3.7	-2.8	
			30 to 130 MHz	-6.5	-8	
			130 MHz to 1GHz	-7	-7	

4.5 Power supply supervisor characteristics

Table 10 Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	PDR_S=0	2.32	2.40	2.48	V
V_{PDR}	Power down reset threshold		2.27	2.35	2.43	V
V_{HYST}	PDR hysteresis		—	0.05	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms
V_{POR}	Power on reset threshold	PDR_S=1	2.32	2.40	2.48	V
V_{PDR}	Power down reset threshold		1.72	1.80	1.88	V
V_{HYST}	PDR hysteresis		—	0.6	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms

4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 11. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	500	V

Table 12. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±100	mA
	V_{supply} over voltage		—	—	5.4	V

4.7 External clock characteristics

Table 13. High speed external clock (HSE) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High Speed External oscillator (HSE) frequency	V_{DD}=3.3V	4	8	32	MHz
C_{HSE}	Recommended load capacitance on OSC_IN and OSC_OUT	—	—	20	30	pF
R_{FHSE}	Recommended external feedback resistor between XTALIN and XTALOUT	—	—	200	—	KΩ
D_{HSE}	HSE oscillator duty cycle	—	48	50	52	%
I_{DDHSE}	HSE oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	1.4	—	μA
t_{SUHSE}	HSE oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

Table 14. Low speed external clock (LSE) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low Speed External oscillator (LSE) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	1000	KHz
C_{LSE}	Recommended load capacitance on OSC32_IN and OSC32_OUT	—	—	—	15	pF
D_{LSE}	LSE oscillator duty cycle	—	48	50	52	%
I_{DDLSE}	LSE oscillator operating current	V_{DD}=V_{BAT}=3.3V	—	1.4	—	µA
t_{SULSE}	LSE oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	3	—	s

4.8 Internal clock characteristics

Table 15. High speed internal clock (HSI) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	High Speed Internal Oscillator (HSI) frequency	V_{DD}=3.3V	—	8	—	MHz
ACC_{HSI}	HSI oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-2.5	—	+1.5	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-1.2	—	+1.2	%
		V_{DD}=3.3V, T_A=25°C	-1	—	+1	%
D_{HSI}	HSI oscillator duty cycle	V_{DD}=3.3V, f_{HSI}=8MHz	48	50	52	%
I_{DDHSI}	HSI oscillator operating current	V_{DD}=3.3V, f_{HSI}=8MHz	—	80	100	µA
t_{SUHSI}	HSI oscillator startup time	V_{DD}=3.3V, f_{HSI}=8MHz	1	—	2	us

Table 16. Low speed internal clock (LSI) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal oscillator (LSI) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	30	40	60	KHz
I_{DDLSI}	LSI oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	1	2	µA
t_{SULSI}	LSI oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	—	80	µs

4.9 PLL characteristics

Table 17. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency		1	8	25	MHz
f_{PLL}	PLL output clock frequency		16	—	72	MHz
t_{LOCK}	PLL lock time		—		200	μs
$Jitter_{PLL}$	Cycle to cycle Jitter				300	ps

4.10 Memory characteristics

Table 18. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

4.11 GPIO characteristics

Table 19. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.95	V
	5V-tolerant IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.9	V
V_{IH}	Standard IO High level input voltage	V_{DD}=2.6V	1.2	—	4.0	V
	5V-tolerant IO High level input voltage	V_{DD}=2.6V	1.5	—	5.5	V
V_{OL}	Low level output voltage	V_{DD}=2.6V	—	—	0.2	V
V_{OH}	High level output voltage	V_{DD}=2.6V	2.3	—	—	V
R_{PU}	Internal pull-up resistor	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Internal pull-down resistor	V_{IN}=V_{DD}	30	40	50	kΩ

4.12 ADC characteristics

Table 20. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{ADCIN}	ADC input voltage range		0	—	V_{REF+}	V
f_{ADC}	ADC clock		0.6	—	14	MHz
f_S	Sampling rate		—	—	1	MHz
$f_{ADCCONV}$	ADC conversion time	f_{ADC}=14MHz	1	—	18	µs
R_{ADC}	Input sampling switch resistance		—	—	0.2	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	32	—	pF
t_{SU}	Startup time		—	—	1	µs

4.13 DAC characteristics

Table 21. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{DACIN}	DAC input voltage range		0	—	V_{REF+}	V
R_{LOAD}	Load resistance	Resistive load vs. V_{SSA} with buffer ON	5	—	—	kΩ
C_{LOAD}	Load capacitance	No pin/pad capacitance included	—	—	50	pF
DNE	Differential non-linearity error	DAC in 12-bit	—	—	±3	LSB
INL	Integral non-linearity	DAC in 12-bit	—	—	±4	LSB
Offset	Offset error	DAC in 12-bit, V_{REF+} = 3.6 V	—	—	±12	LSB
GE	Gain error	DAC in 12-bit	—	—	±0.5	%

4.14 I2C characteristics

Table 22. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	KHz
$t_{SCL(H)}$	SCL clock high time		4.0	—	0.6	—	ns
$t_{SCL(L)}$	SCL clock low time		4.7	—	1.3	—	ns

4.15 SPI characteristics

Table 23. SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency		—	—	18	MHz
$t_{SCK(H)}$	SCK clock high time		19	—	—	ns
$t_{SCK(L)}$	SCK clock low time		19	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time		—	—	25	ns
$t_{H(MO)}$	Data output hold time		2	—	—	ns
$t_{SU(MI)}$	Data input setup time		5	—	—	ns
$t_{H(MI)}$	Data input hold time		5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time		3	—	10	ns
$t_{V(SO)}$	Data output valid time		—	—	25	ns
$t_{H(SO)}$	Data output hold time		15	—	—	ns
$t_{SU(SI)}$	Data input setup time		5	—	—	ns
$t_{H(SI)}$	Data input hold time		4	—	—	ns

5 Package information

5.1 QFN package outline dimensions

Figure 8. QFN package outline

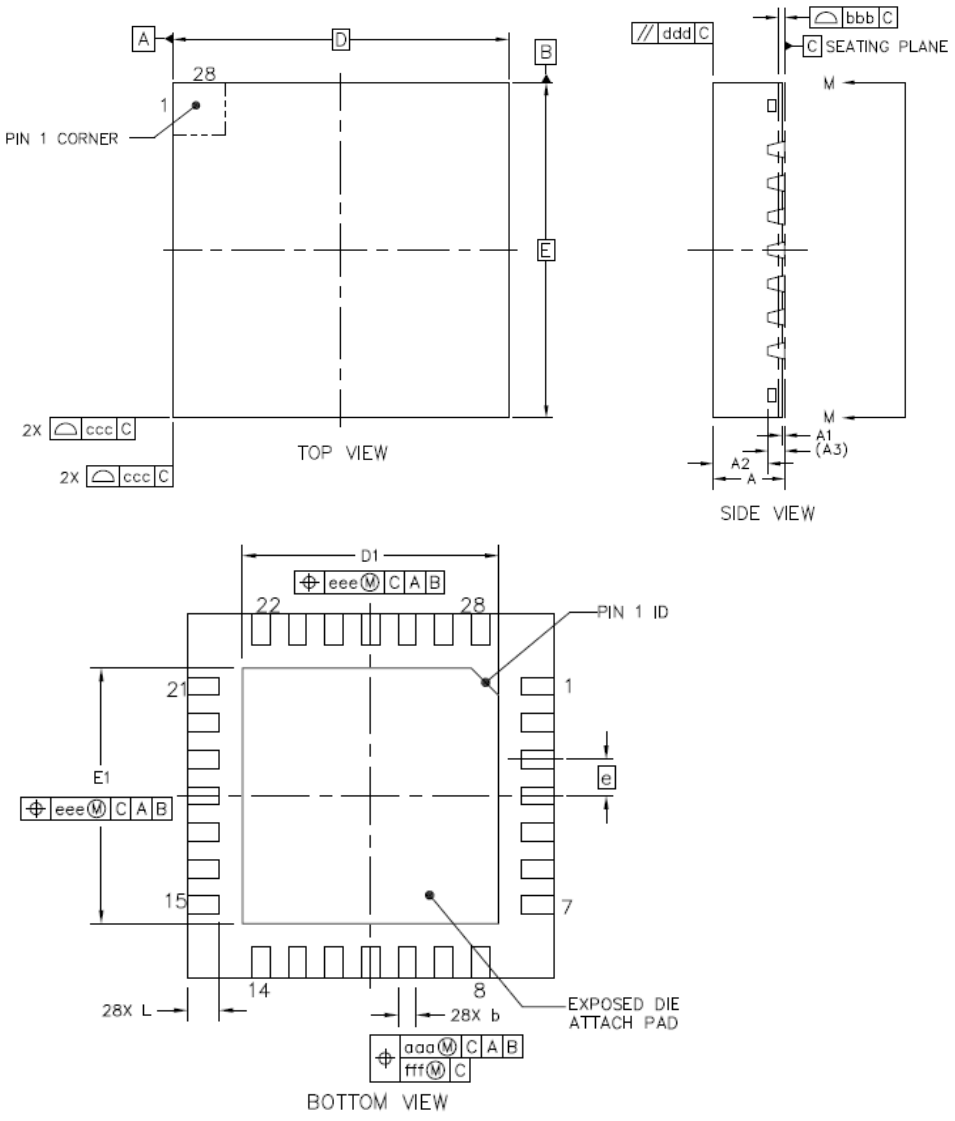


Table 24. QFN package dimensions

Symbol	QFN28		
	Min	Typ	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	-	0.65	0.67
A3	-	0.203	-
D	-	4.0	-
E	-	4.0	-
D1	2.7	2.8	2.9
E1	2.7	2.8	2.9
L	0.25	0.35	0.45
e	0.4		
b	0.15	0.2	0.25

Symbol	QFN32		
	Min	Typ	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	-	0.65	0.67
A3	-	0.203	-
D	-	5.0	-
E	-	5.0	-
D1	3.4	3.5	3.6
E1	3.4	3.5	3.6
L	0.3	0.4	0.5
e	0.5		
b	0.2	0.25	0.3

(Original dimensions are in millimeters)

5.3 LQFP package outline dimensions

Figure 9. LQFP package outline

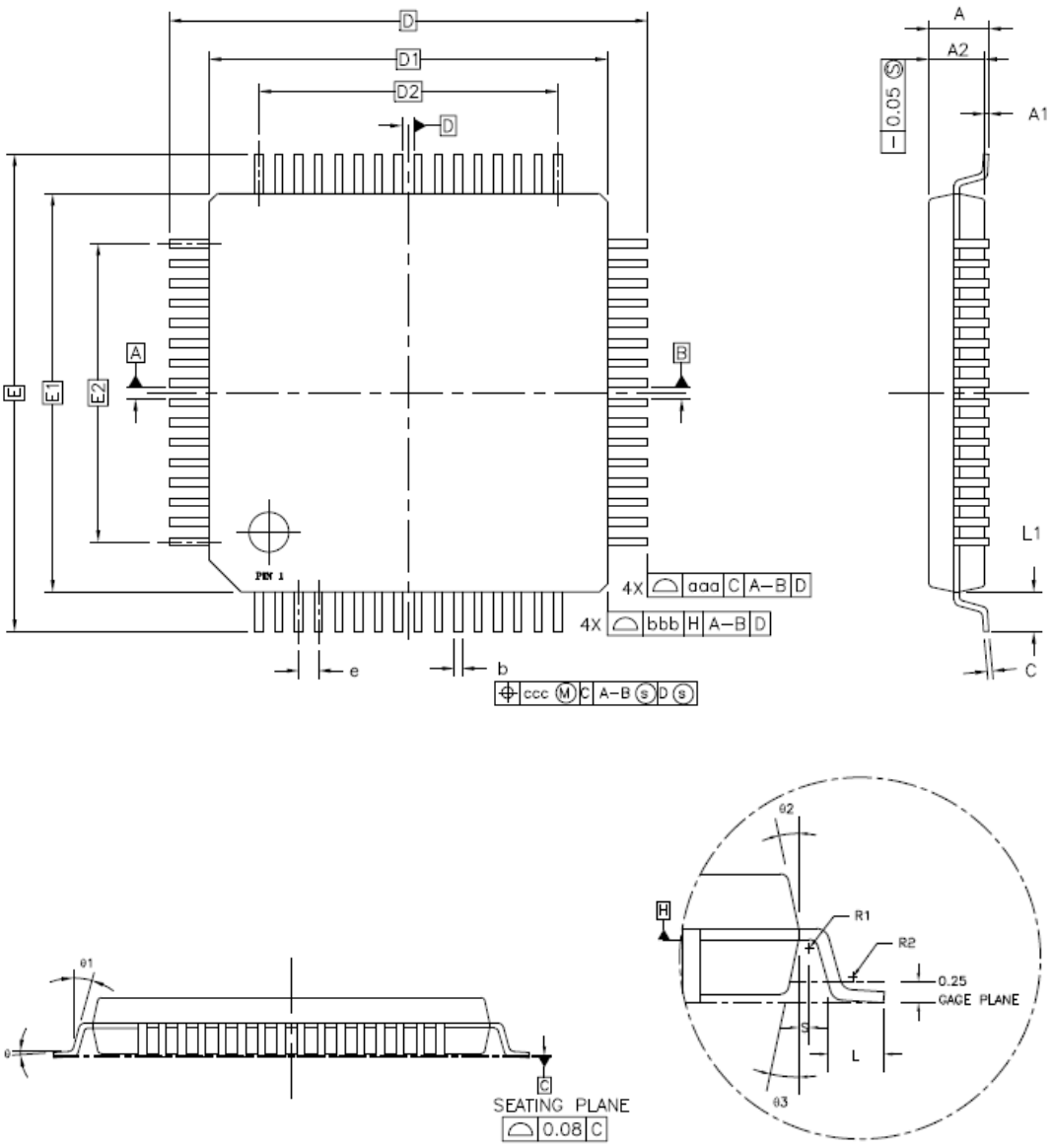


Table 25. LQFP package dimensions

Symbol	LQFP48		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
D	-	9.00	-
D1	-	7.00	-
E	-	9.00	-
E1	-	7.00	-
R1	0.08	-	-
R2	0.08	-	0.20
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	-	1.00	-
S	0.20	-	-
b	0.17	0.22	0.27
e	-	0.50	-
D2	-	5.50	-
E2	-	5.50	-
aaa	0.20		
bbb	0.20		
ccc	0.08		

Symbol	LQFP64		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	-	12.00	-
D1	-	10.00	-
E	-	12.00	-
E1	-	10.00	-
R1	0.08	-	-
R2	0.08	-	0.20
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	-	1.00	-
S	0.20	-	-
b	0.17	0.20	0.27
e	-	0.50	-
D2	-	7.50	-
E2	-	7.50	-
aaa	0.20		
bbb	0.20		
ccc	0.08		

(Original dimensions are in millimeters)

6 Ordering Information

Table 26. Part ordering code for GD32F150xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F150G4U6	16	QFN28	Green	Industrial -40°C to +85°C
GD32F150G6U6	32	QFN28	Green	Industrial -40°C to +85°C
GD32F150G8U6	64	QFN28	Green	Industrial -40°C to +85°C
GD32F150K4U6	16	QFN32	Green	Industrial -40°C to +85°C
GD32F150K6U6	32	QFN32	Green	Industrial -40°C to +85°C
GD32F150K8U6	64	QFN32	Green	Industrial -40°C to +85°C
GD32F150C4T6	16	LQFP48	Green	Industrial -40°C to +85°C
GD32F150C6T6	32	LQFP48	Green	Industrial -40°C to +85°C
GD32F150C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32F150R4T6	16	LQFP64	Green	Industrial -40°C to +85°C
GD32F150R6T6	32	LQFP64	Green	Industrial -40°C to +85°C
GD32F150R8T6	64	LQFP64	Green	Industrial -40°C to +85°C

7 Revision History

Table 27. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.8, 2014
1.1	Package data updated in ***Table 25. QFN package dimensions*** and ***Table 27. Part ordering code for GD32F150xx devices***	Jun.18, 2014
2.1	Characteristics values updated in ***Table 7. Power consumption characteristics***	Oct.20, 2014

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