GD5F1GQ4xExIS

DATASHEET

Contents

1 FEATURE

- 1Gb SLC NAND Flash
- Page Size
  - 2048 bytes + 128 bytes with ECC disabled
  - 2048 bytes + 64 bytes with ECC enabled
- Standard, Dual, Quad SPI
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
- High Speed Clock Frequency
  - 120MHz for fast read with 30PF load
  - Quad I/O Data transfer up to 480Mbits/s
- Software/Hardware Protection
  - Write protect all/portion of memory via software
  - Register protection with WP# Pin
  - Top or Bottom, Block selection combination
- Advanced security Features
  - 8K-Byte OTP Region
- Single Power Supply Voltage
  - Full voltage range for 1.8V: 1.7V ~ 2.0V
  - Full voltage range for 3.3V: 2.7V ~ 3.6V
- Program/Erase/Read Speed
  - Page Program time: 400us typical
  - Block Erase time: 3ms typical
  - Page read time: 80us maximum(w/I ECC)
- Reliability
  - Endurance: 100K program/erase cycles
  - Data retention: 10 Years
- Low Power Consumption
  - 40mA maximum active current
  - 90uA(1) maximum standby current
- Enhanced access performance
  - 2kbyte cache for fast random read
  - Cache read and cache program
- Advanced Feature for NAND
  - Internal ECC option, per 528bytes
  - Internal data move by page with ECC
- The first block(Block0) is guaranteed to be a valid block at the time of shipment.

Note 1: When Temperature is 105℃, the maximum standby current is 200uA

2 GENERAL DESCRIPTION

SPI (Serial Peripheral Interface) NAND Flash provides an ultra cost-effective while high density non-volatile memory storage solution for embedded systems, based on an industry-standard NAND Flash memory core. It is an attractive alternative to SPI-NOR and standard parallel NAND Flash, with advanced features:

- Total pin count is 8, including VCC and GND
- Density is 1G bit
- Superior write performance and cost per bit over SPI-NOR
- Significant low cost than parallel NAND

This low-pin-count NAND Flash memory follows the industry-standard serial peripheral interface, and always remains the same pin-out from one density to another. The command sets resemble common SPI-NOR command sets, modified to handle NAND specific functions and added new features. GigaDevice SPI NAND is an easy-to-integrate NAND Flash memory, with specified designed features to ease host management:

- **User-selectable internal ECC**. ECC code is generated internally during a page program operation. When a page is read to the cache register, the ECC code is detect and correct the errors when necessary. The 64-bytes spare area is available even when internal ECC enabled. The device outputs corrected data and returns an ECC error status.
- **Internal data move or copy back with internal ECC**. The device can be easily refreshed and manage garbage collection task, without need of shift in and out of data.
- **Power on Read with internal ECC**. The device will automatically read first page of fist block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correctly by internal ECC.

It is programmed and read in page-based operations, and erased in block-based operations. Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation. The cache register functions as the buffer memory to enable page and random data READ/WRITE and copy back operations. These devices also use a SPI status register that reports the status of device operation.

2.1 Product List

Product Number	Density	Voltage	Package Type	Temperature	**Page Size**
GD5F1GQ4REFIS	1Gbit	1.7V to 2.0V	SOP16 300mil	-40℃ to 85℃	2Kbytes + 128bytes
GD5F1GQ4REFJS				-40℃ to 105℃	
GD5F1GQ4REFFS				-40℃ to 85℃	
GD5F1GQ4REZIS			TFBGA24(6*4 Ball Array)	-40℃ to 85℃	
GD5F1GQ4REZJS				-40℃ to 105℃	
GD5F1GQ4REZFS				-40℃ to 85℃	
GD5F1GQ4RE9IS			LGA8(6*8mm)	-40℃ to 85℃	
GD5F1GQ4RE9JS				-40℃ to 105℃	
GD5F1GQ4RE9FS				-40℃ to 85℃	
GD5F1GQ4UEYIS		2.7V to 3.6V	WSON8(8*6mm)	-40℃ to 85℃	
GD5F1GQ4UEYJS				-40℃ to 105℃	
GD5F1GQ4UEYFS				-40℃ to 85℃	
GD5F1GQ4UEFIS			SOP16 300mil	-40℃ to 85℃	
GD5F1GQ4UEFJS				-40℃ to 105℃	
GD5F1GQ4UEFFS				-40℃ to 85℃	
GD5F1GQ4UEZIS			TFBGA24(6*4 Ball Array)	-40℃ to 85℃	
GD5F1GQ4UEZJS				-40℃ to 105℃	
GD5F1GQ4UEZFS				-40℃ to 85℃	

2.2 Connection Diagram

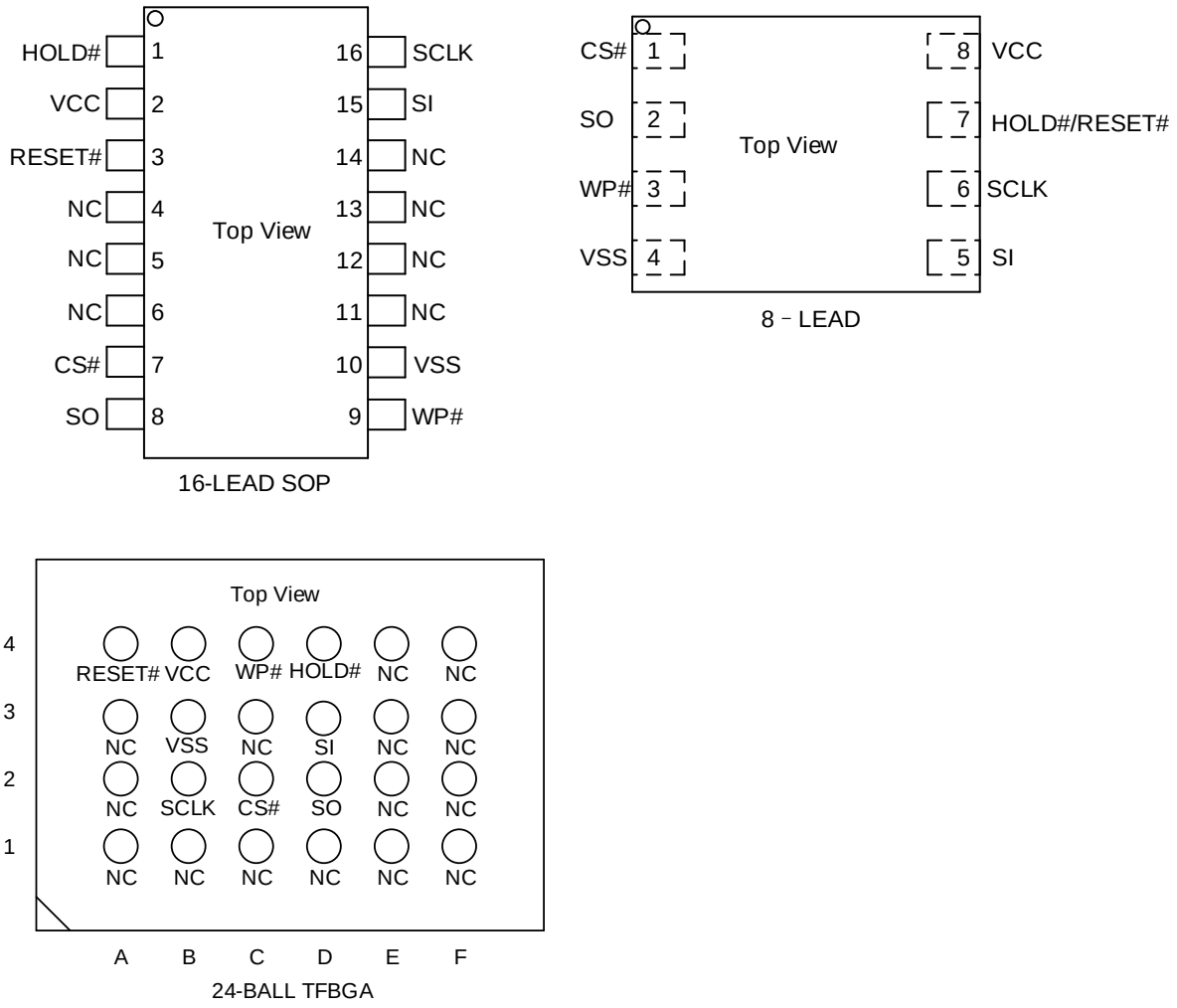


Figure 2-1 Connect Diagram

2.3 Pin Description

Pin Name	I/O	Description
CS#	**I**	Chip Select input, active low
SO/SIO1	**I/O**	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	**I/O**	Write Protect, active low / Serial Data Input Output 2
VSS	**Ground**	Ground
SI/SIO0	**I/O**	Serial Data Input / Serial Data Input Output 0
SCLK	**I**	Serial Clock input
HOLD#/RESET#/SIO3	**I/O**	Hold input, active low / Reset input, active low / Serial Data Input Output3
VCC	**Supply**	Power Supply

2.4 Block Diagram

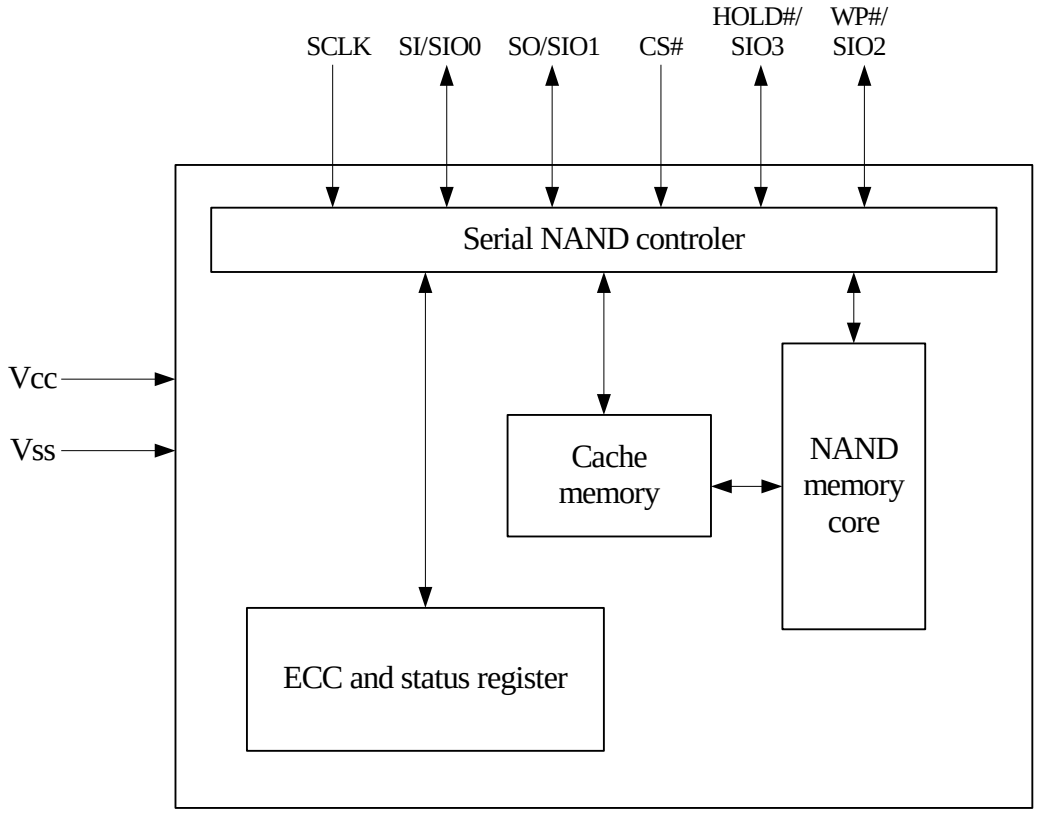
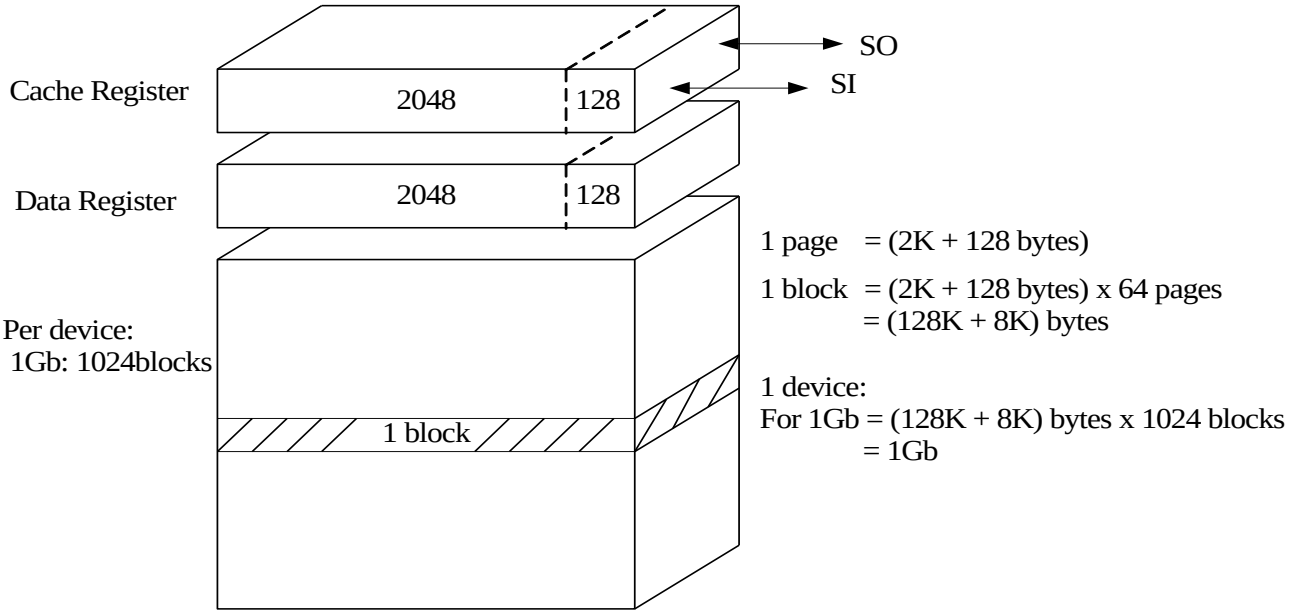


Figure 2-2 Block Diagram

3 ARRAY ORGANIZATION

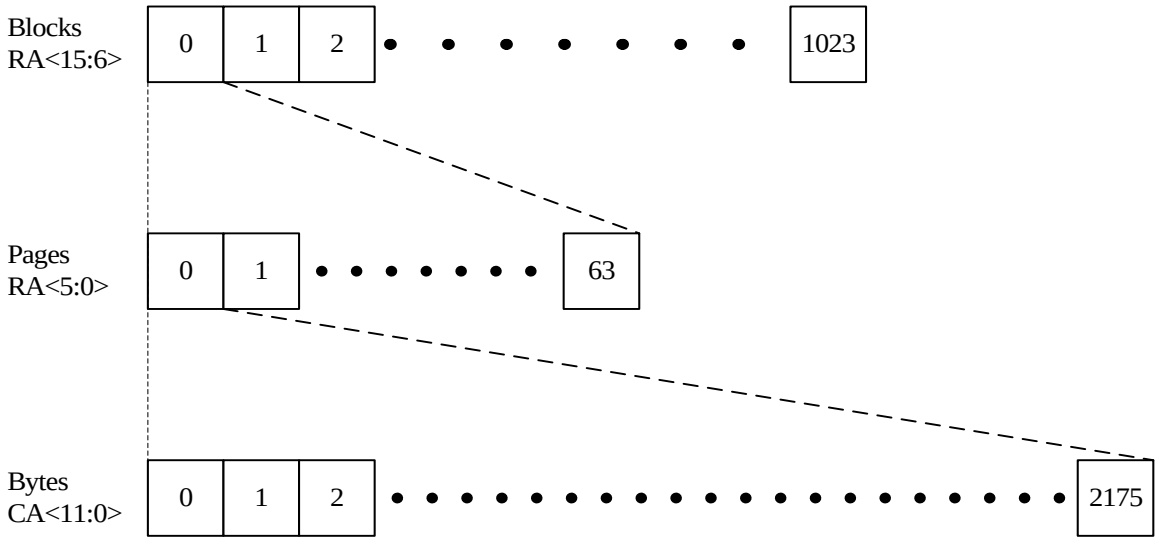
Each block has	Each page has	
128K+8K	2K+128	bytes
64	-	pages
-	-	blocks

Figure3-1. Array Organization



3.1 Memory Mapping

FOR 1G:



Note:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<15:6> selects a block.

4 DEVICE OPERATION

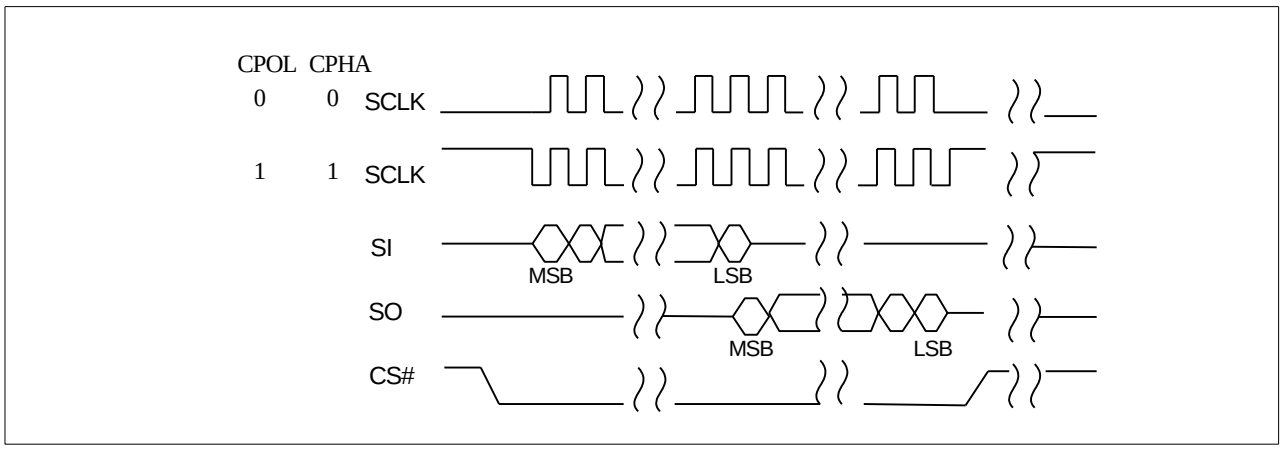
4.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes. All timing diagrams shown in this data sheet are mode 0. See Figure4-1 for more details.

Figure4-1. SPI Modes Sequence Diagram



Note: While CS# is HIGH, keep SCLK at VCC or GND (determined by mode 0 or mode 3).

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD#/RESET# pins become SIO2 and SIO3.

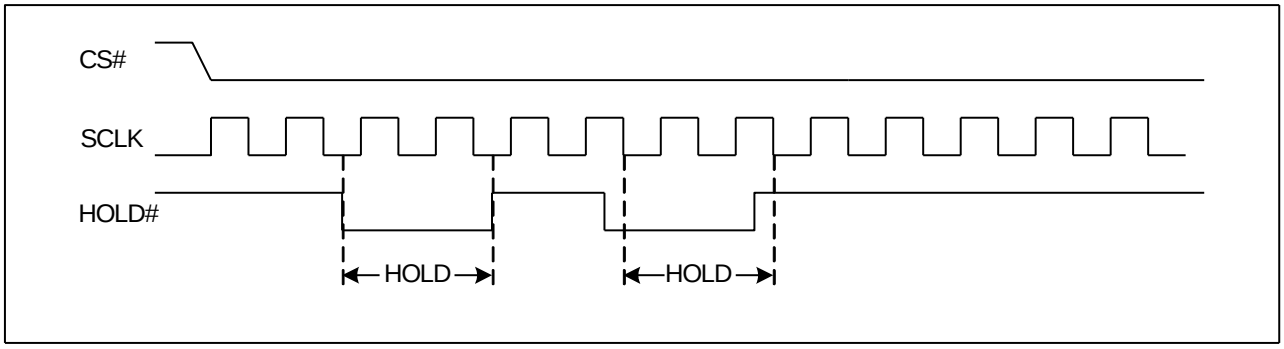
4.2 HOLD Mode

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure4-2. Hold Condition



4.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

5 COMMANDS DESCRIPTION

Table5-1. Commands Set

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte N
Write Enable	06H					
Write Disable	04H					
Read UID	EDH	00H				
Read CID	13H	A23-A16	A15-A8	A7-A0		
Read parameter page	13H	A23-A16	A15-A8	A7-A0		
Get Features	0FH	A7-A0	(D7-D0)			Wrap
Set Feature	1FH	A7-A0	(D7-D0)	dummy(1)		
Page Read (to cache)	13H	A23-A16	A15-A8	A7-A0		
Read From Cache	03H/0BH	A15-A8(4)	A7-A0	dummy(2)	(D7-D0)	
Read From Cache x 2	3BH	A15-A8(4)	A7-A0	dummy(2)	(D7-D0)x2	
Read From Cache x 4	6BH	A15-A8(4)	A7-A0	dummy(2)	(D7-D0)x4	
Read From Cache Dual IO	BBH	A15-A0(4)	dummy(3)	(D7-D0)x2		
Read From Cache Quad IO	EBH	A15-A0(5)	(D7-D0)x4			
Read ID(8)	9FH	A7-A0	MID	DID		Wrap
Program Load	02H	A15-A8(6)	A7-A0	(D7-D0)	Next byte	Byte N
Program Load x4	32H	A15-A8(6)	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Execute	10H	A23-A16	A15-A8	A7-A0		
Program Load Random Data	84H(10)	A15-A8(6)	A7-A0	(D7-D0)	Next byte	Byte N
Program Load Random Data x4	C4H/34H(10)	A15-A8(6)	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Load Random Data Quad IO	72H	A15-A0(7)	(D7-D0)x4	Next byte		Byte N
Block Erase(128K)	D8H	A23-A16	A15-A8	A7-A0		
Reset(9)	FFH					

Notes:

1. The dummy byte can be inputted or not.
2. The x8 clock = dummy<7:0>.
3. The x8 clock = dummy<7:0>, D7-D0.
4. The x8 clock = dummy<3-0>, A11-A8 or dummy<3-0>, A11-A0.
5. The x8 clock = dummy<3-0>, A11-A0, dummy<7:0>, D7-D0.
6. The x8 clock = dummy<3:0>, A<11:8>.
7. The x8 clock = dummy<3:0>, A<11:0>, D7-D0, D7-D0.
8. MID is Manufacture ID (C8h for GigaDevice), DID is Device ID
   When A7-A0 is 00h, read MID and DID.
9. Reset command:
   - During busy, Reset will reset PAGE READ/PROGRAM/ERASE operation.
   - During idle, Reset will reset status register bits P_FAIL/E_FAIL/ECCS bits.
10. Those commands are only available in Internal Data Move operation.
11. Read UID/CID/parameter page all are same as page read to cache.

6 WRITE OPERATIONS

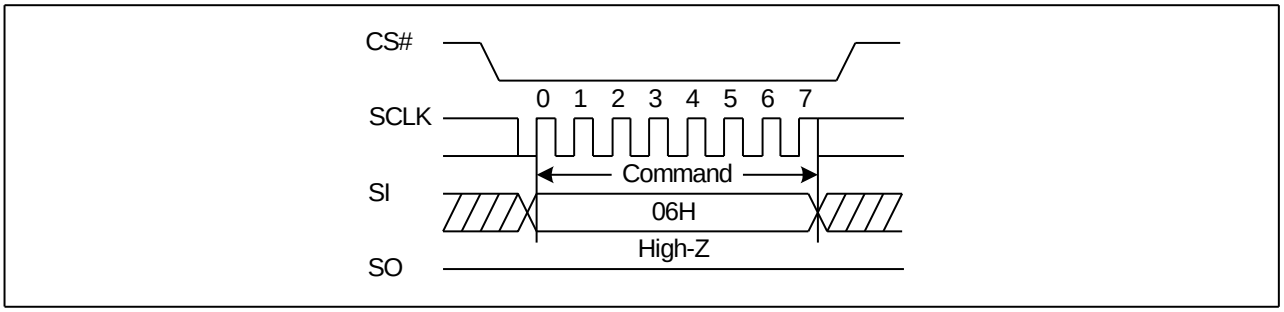
6.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

The WEL bit can be cleared after a reset command.

Figure6-1. Write Enable Sequence Diagram

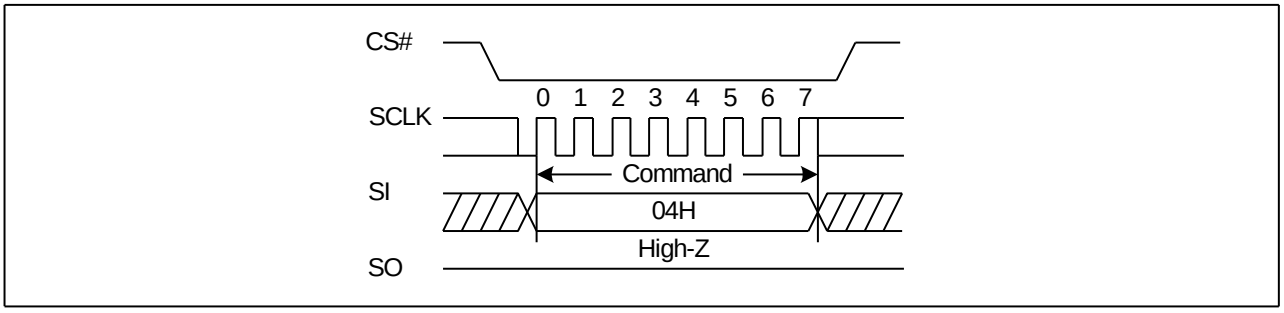


6.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is also reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase

Figure6-2. Write Disable Sequence Diagram



7 FEATURE OPERATIONS

7.1 Get Features (0FH) and Set Features (1FH)

The GET FEATURES (0FH) and SET FEATURES (1FH) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific feature bits (shown in the following table). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06H) command. When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFH) command is issued.

Table7-1. Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0H	HOLDB/RST	DS_S1	DS_S0	Reserved	Reserved	Reserved	Reserved	Reserved
Status	F0H	Reserved	Reserved	ECCSE1	ECCSE0	Reserved	Reserved	Reserved	Reserved

Note: If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

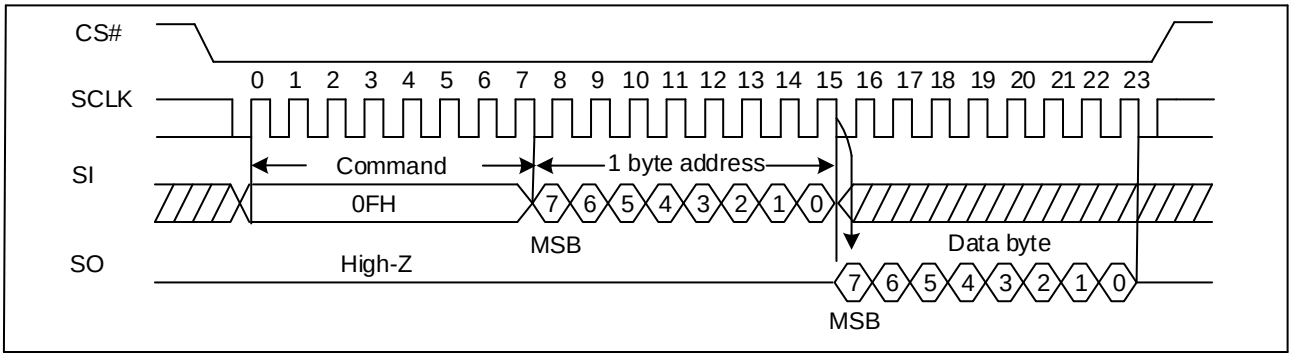
If QE is enabled, the quad IO operations can be executed.

All the reserved bits must be held low when the feature is set.

00h is the default data byte value for Output Driver Register after power-up.

HOLDB/RST is for WSON8 Package only. By default HOLDB/RST registers is 0 after power-on-reset or hardware reset, and this bit default is HOLD function.

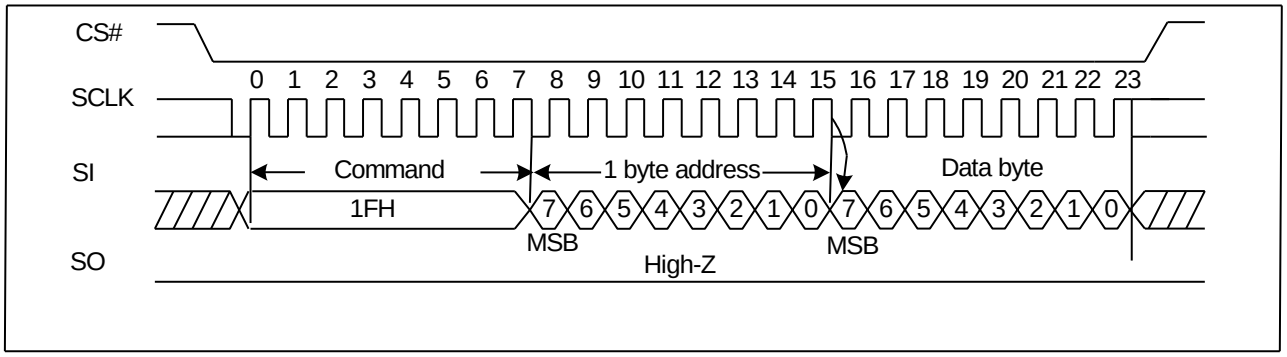
Figure7-1. Get Features Sequence Diagram



Note: The output would be updated by real-time, until CS# is driven high.

The set features command supports a dummy byte mode after the data byte as well. The features in the feature byte B0H are all volatile except OTP_PRT bit.

Figure7-2. Set Features Sequence Diagram



8 READ OPERATIONS

8.1 Page Read

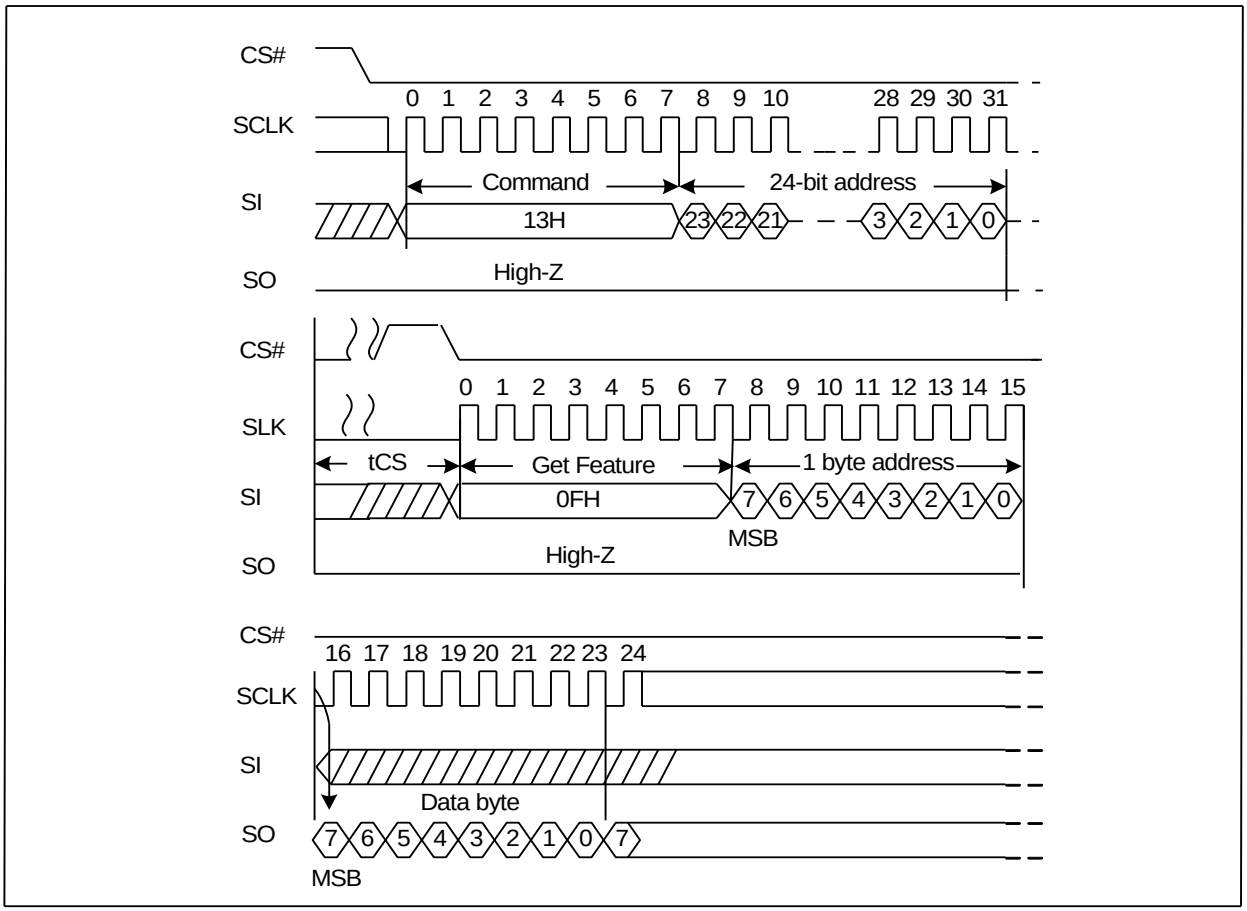
The PAGE READ (13H) command transfers the data from the NAND Flash array to the cache register. The command sequence is as follows:

- 13H (PAGE READ to cache)
- 0FH (GET FEATURES command to read the status)
- 03H or 0BH (Read from cache)/3BH (Read from cache x2)/6BH (Read from cache x4)/BBH (Read from cache dual IO)/EBH (Read from cache quad IO)

The PAGE READ command requires a 24-bit address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for t_{RD} time. During this time, the GET FEATURE (0FH) command can be issued to monitor the status. Followed the page read operation, the RANDOM DATA READ (03H/0BH/3BH/6BH/BBH/EBH) command must be issued in order to read out the data from cache. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 2176-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate this operation. Refer waveforms to view the entire READ operation.

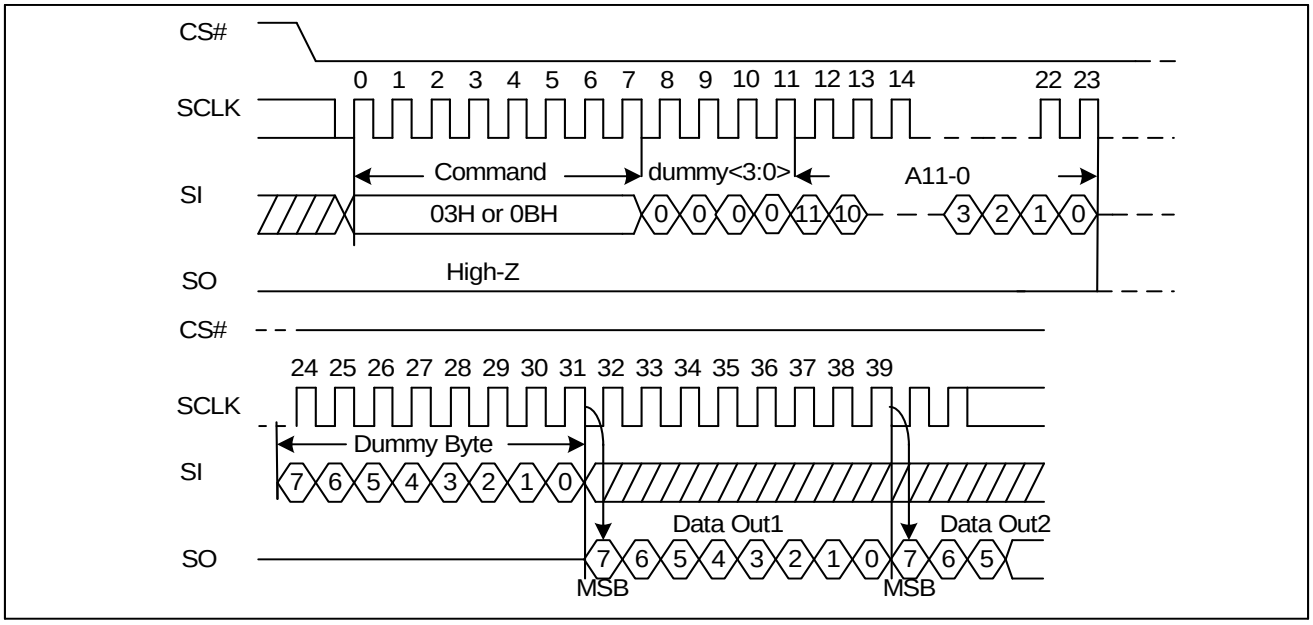
8.2 Page Read to Cache (13H)

Figure8-1. Page Read to cache Sequence Diagram



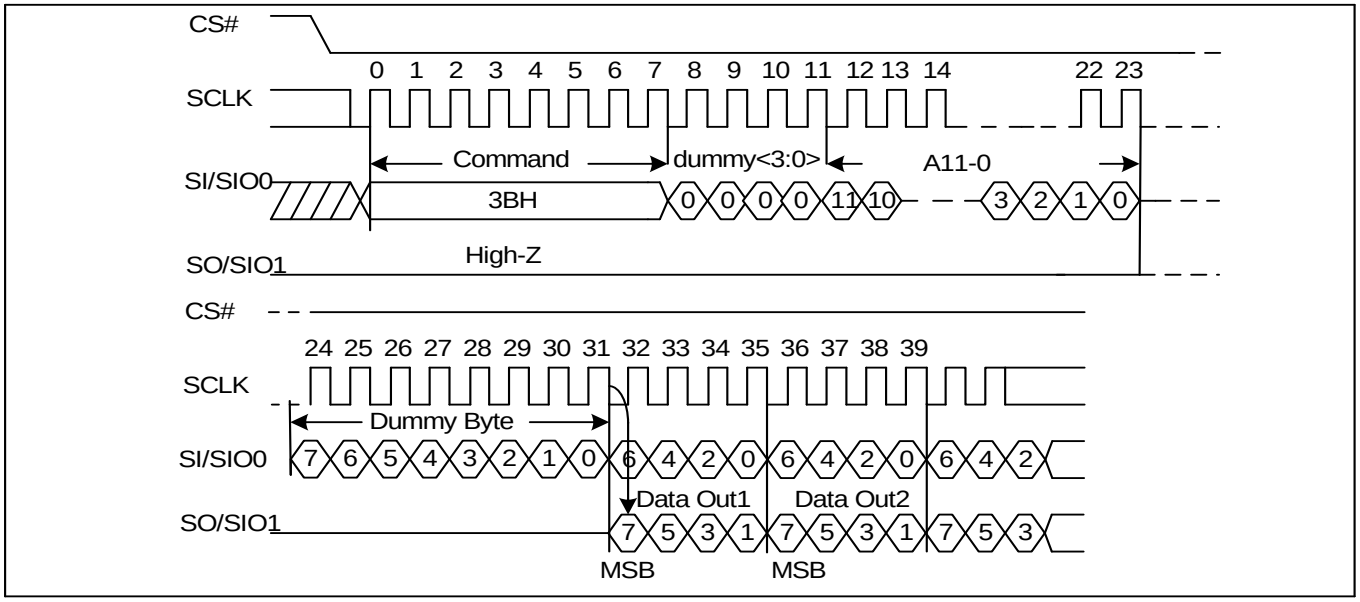
8.3 Read From Cache (03H or 0BH)

Figure8-2. Read From Cache Sequence Diagram



8.4 Read From Cache x2 (3BH)

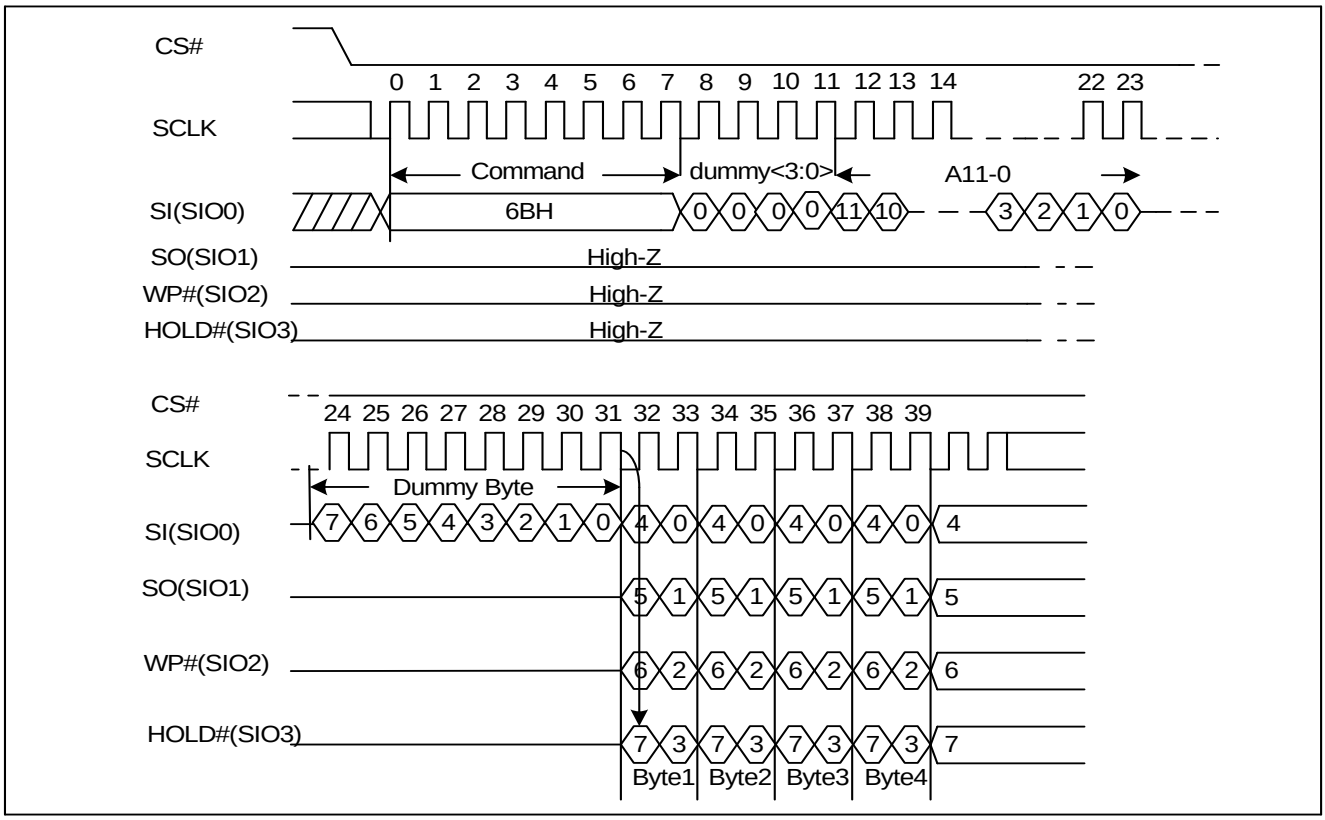
Figure8-3. Read From Cache x2 Sequence Diagram



8.5 Read From Cache x4 (6BH)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command.

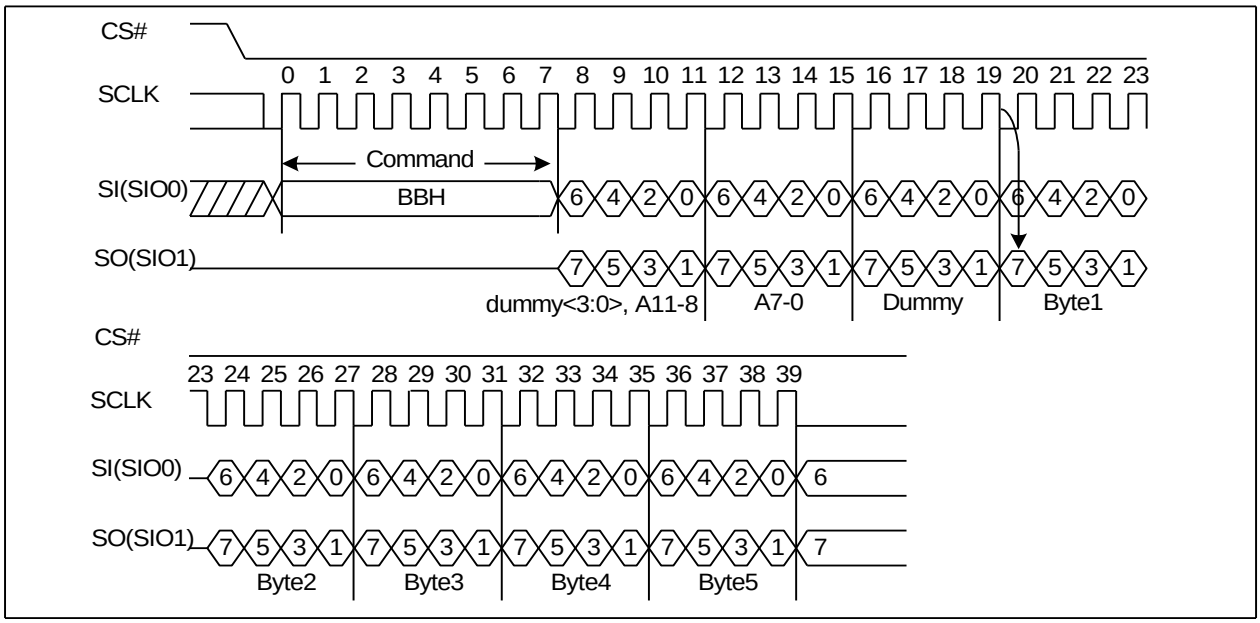
Figure8-4. Read From Cache x4 Sequence Diagram



8.6 Read From Cache Dual IO (BBH)

The Read from Cache Dual I/O command (BBH) is similar to the Read form Cache x2 command (3BH) but with the capability to input the 4 Dummy bits, followed by a 12-bit column address for the starting byte address and a dummy byte by SIO0 and SIO1, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 2-bit per clock cycle from SIO0 and SIO1. The first address byte can be at any location. The address increments automatically to the next higher address after each byte of data shifted out until the boundary wrap bit.

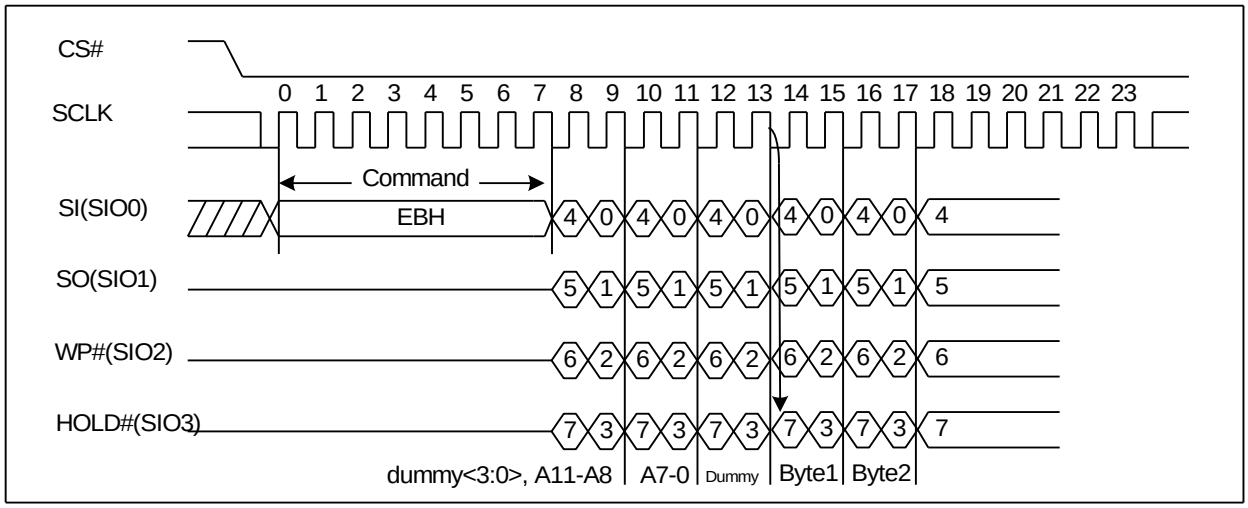
Figure8-5. Read From Cache Dual IO Sequence Diagram



8.7 Read From Cache Quad IO (EBH)

The Read from Cache Quad IO command is similar to the Read from Cache x4 command but with the capability to input the 4 dummy bits, followed a 12-bit column address for the starting byte address and a dummy byte by SIO0, SIO1, SIO3, SIO4, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 4-bit per clock cycle from SIO0, SIO1, SIO2, SIO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out until the boundary wrap bit. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache quad IO command.

Figure8-6. Read From Cache Quad IO Sequence Diagram



9 Read ID

9.1 Read ID (9FH)

The READ ID command is used to identify the NAND Flash device.

• With address 00H~01H, the READ ID command outputs the Manufacturer ID and the device ID. See Table 4 for details.

Figure9-1_1. Read ID Sequence Diagram(Address 00h)

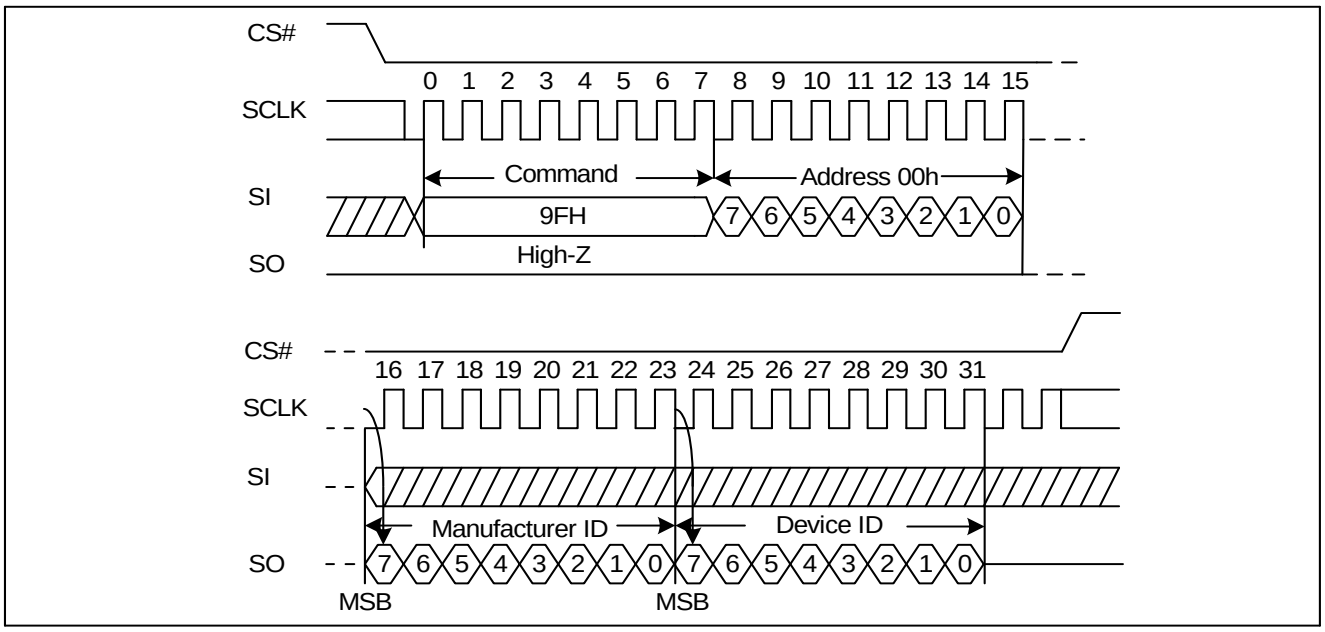


Figure9-1_2. Read ID Sequence Diagram(Address 01h)

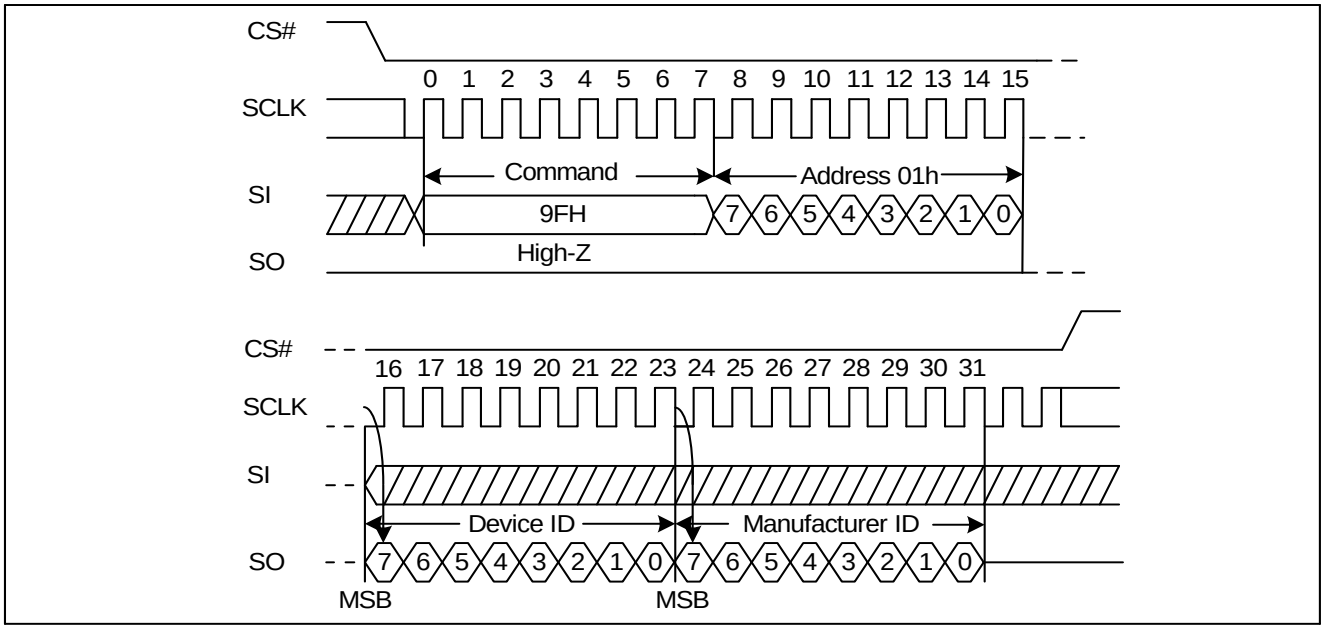


Table4. READ ID Table

Address	Part No	Value	Page Size	Description
00H	GD5F1GQ4U	C8h	2Kbyte + 128Byte	Manufacture ID (GigaDevice)
	GD5F1GQ4R			
01H	GD5F1GQ4U	D3h		Device ID (SPI NAND 1Gbit 3.3V)
	GD5F1GQ4R	C3h		Device ID (SPI NAND 1Gbit 1.8V)

9.2 Read UID

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement shall be stored by the target. For example, reading bytes 32-63 returns to the host another copy of the UID and its complement.

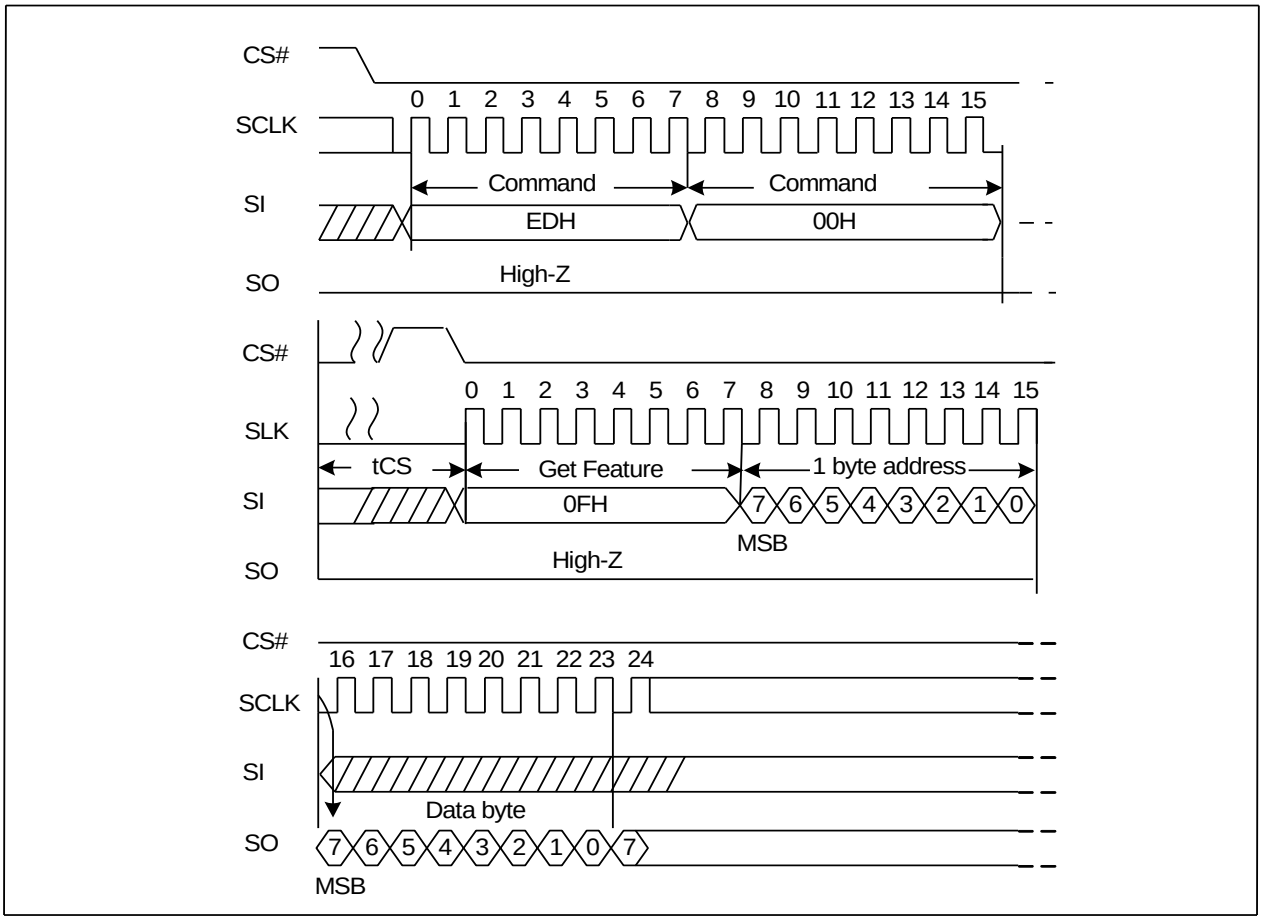
Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

The Read UID command sequence is as follows:

1. Use EDh+00h read UID from array to cache.
2. Use 0FH (GET FEATURES command) read the status
3. User can use Read from cache command (03H/0BH/3BH/6BH/BBH/EBH), read UID from cache.

Read UID to Cache (EDH+00H) + Get Feature (0FH)

Figure9-2. Read UID to cache and Get Feature command Sequence Diagram



9.3 Read CID

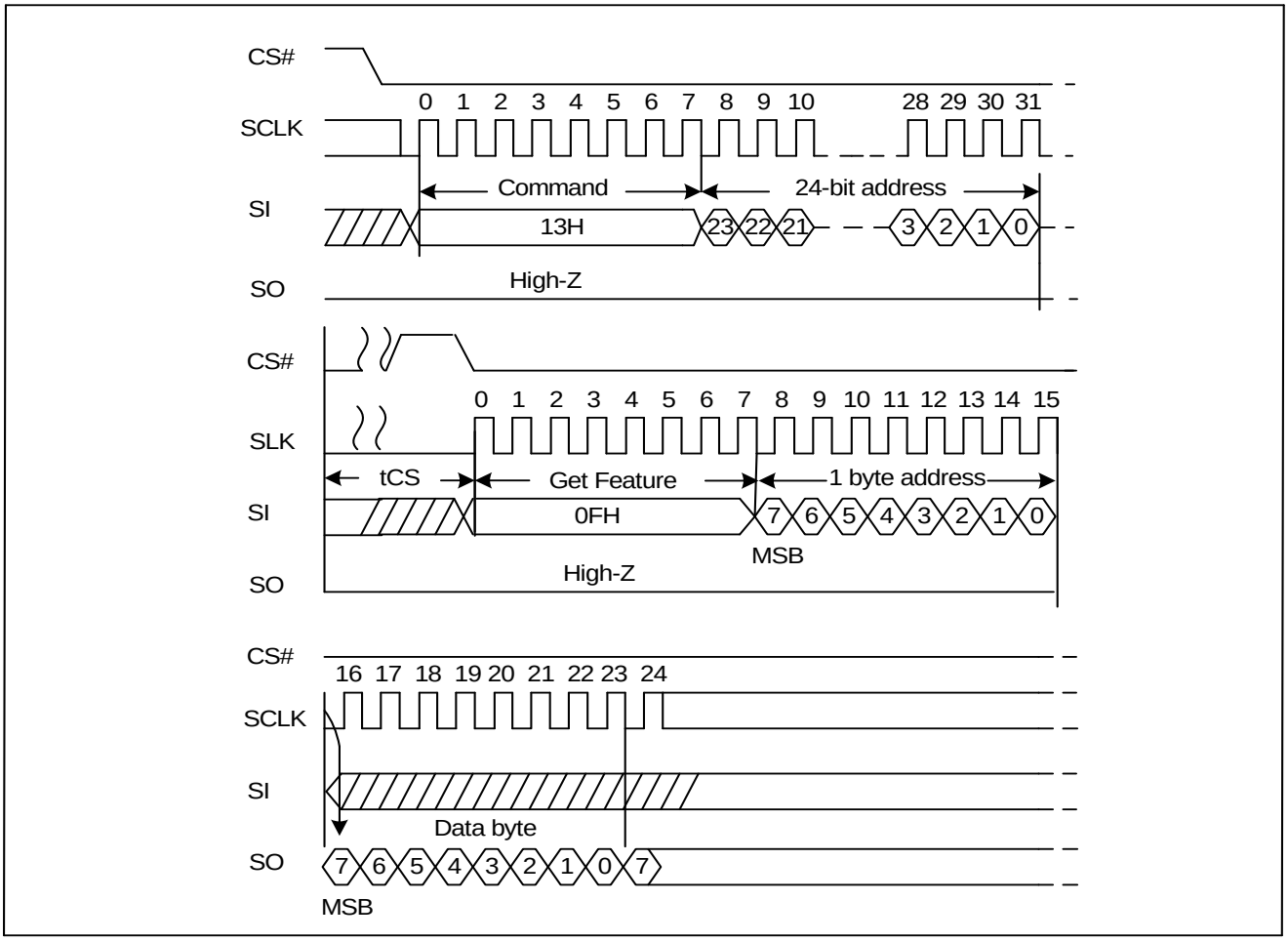
CID is customer ID, one custom for one ID, which is used for special demand for customer

User can read CID with follow step. The command sequence is as follows:

1. Use set_feature set data 0x50 to B0 register, to enable OTP_EN.
2. Use get_feature get data from B0 register and check if the data is 0x50.
3. Use page read to cache (13h) command with address 24'h000005h, read data from array to cache.
4. Use 0FH (GET FEATURES command) read the status
5. User can use Read from cache command (03H/0BH), read 2 bytes CID from cache.

Register	Addr.	7	6	5	4	3	2	1	0
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE

Figure9-3. Read CID to cache and Get Feature command Sequence Diagram



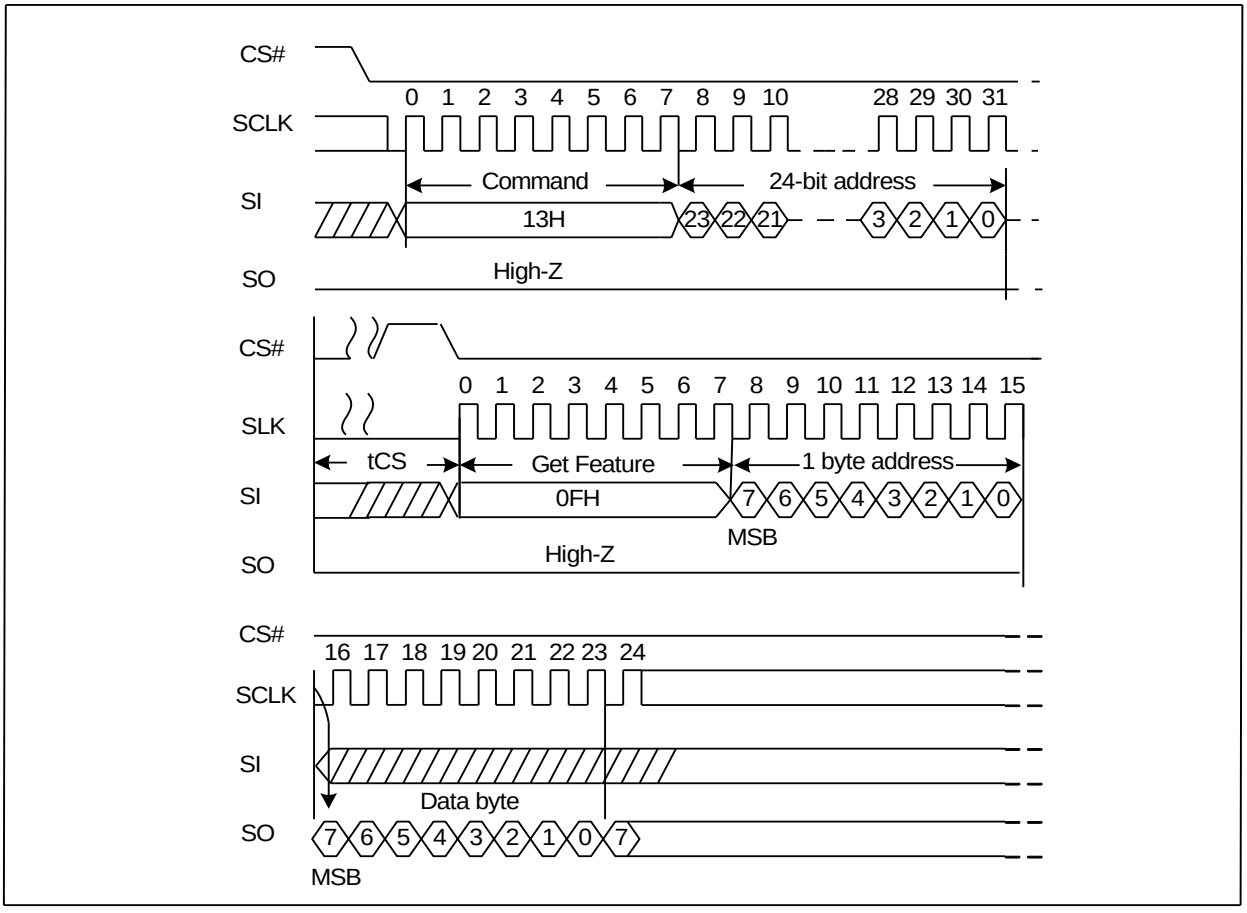
9.4 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing-sand other behavioral parameters. This data structure enables the host processor to automatically recognize the SPI-NAND Flash configuration of a device. The whole data structure is repeated at least three times. The Random Data Read command (05H-E0H) can be issued during execution of the read parameter page to read specific portion-soft the parameter page.

The Read parameter page command sequence is as follows

1) Set "OTP_EN=1", Use set_feature set data 0x50 to B0 register, to enable OTP_EN.
2) Send 13h command with address 24'h000004. Load parameter page from array to cache.
3) Use 0FH (GET FEATURES command) read the status
4) User can use Read from cache command (03H/0BH/3BH/6BH/BBH/EBH), read parameter page from cache.

Figure9-4. Read parameter page to cache and Get Feature command Sequence Diagram



Parameter page table as follow

<table>
<tr><th>Byte</th><th>O/M</th><th>Description</th><th></th></tr>
<tr><td>0-3</td><td>M</td><td>Parameter page signature
Byte 0: 4FH, “O”
Byte 1: 4EH, “N”
Byte 2: 46H, “F”
Byte 3: 49H, “I”</td><td>4FH
4EH
46H
49H</td></tr>
<tr><td>4-5</td><td>M</td><td>Revision number
0-15 Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>6-7</td><td>M</td><td>Features supported
0-15 Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>8-9</td><td>M</td><td>Reserved (0)</td><td>00H
00H</td></tr>
<tr><td>10-31</td><td></td><td>Reserved (0)</td><td>00H
…
00H</td></tr>
<tr><td></td><td></td><td>Manufacturer Information block</td><td></td></tr>
<tr><td>32-43</td><td>M</td><td>Device manufacturer (12 ASCII characters)“GIGADEVICE ”</td><td>47H
49H
47H
41H
44H
45H
56H
49H
43H
45H
20H
20H</td></tr>
<tr><td>44-63</td><td>M</td><td>Device model (20 ASCII characters)
<table>
<tr><th>Device Model</th><th>ORGANIZATION</th><th>VCC RANGE</th></tr>
<tr><td>“GD5F1GQ4U”</td><td>X4</td><td>2.7v ~ 3.6v</td></tr>
<tr><td>“GD5F1GQ4R”</td><td>X4</td><td>1.7v ~ 1.95v</td></tr>
</table></td><td>47H
44H
35H
46H
31H
47H
51H
34H
55H/52H
20H
20H
20H
20H
20H</td></tr>
</table>

			20H 20H 20H 20H 20H 20H
64	M	JEDEC manufacturer ID“C8”	C8H
65-66	O	Date code	00H 00H
67-79		Reserved	00H 00H 00H
		Memory organization block	
80-83	M	Number of data bytes per page	00H 08H 00H 00H
84-85	M	Number of spare bytes per page	80H 00H
86-89	M	Number of data bytes per partial page	00H 02H 00H 00H
90-91	M	Number of spare bytes per partial page	20H 00H
92-95	M	Number of pages per block	40H 00H 00H 00H
96-99	M	Number of blocks per logical unit (LUN)	00H 04H 00H 00H
100	M	Number of logical units (LUNs)	01H
101	M	Reserved	00H
102	M	Number of bits per cell	01H
103-104	M	Bad blocks maximum per LUN	14H 00H
105-106	M	Block endurance	01H 05H
107	M	Guaranteed valid blocks at beginning of target	01H

108-109	M	Block endurance for guaranteed valid blocks	01H 05H
110	M	Number of programs per page	04H
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00H
112	M	Number of bits ECC correctability	08H
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	00H
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00H
115-127		Reserved	00H … 00H
		Electrical parameters block	
128	M	I/O capacitance	06H
129-130	M	IO clock support 3-1 5 Reserved (0) 2 1 = supports 80MHz 1 1 = supports 104MHz 0 1 = supports 120MHz	01H 00H
131-132	O	Reserved (0)	00H 00H
133-134	M	tPROG Maximum page program time (us)	BCH 02H
135-136	M	tBERS Maximum block erase time (us)	88H 13H
137-138	M	tR Maximum page read time (us)	50H 00H
139-140	M	Reserved	00H 00H
141-163		Reserved	00H
		Vendor block	
164-165	M	Vendor specific Revision number	00H
166-253		Vendor specific	00H

254-255	M	Integrity CRC	Set on test
		Redundant parameter pages	
256-511	M	Value of bytes 0-255	
512-767	M	Value of bytes 0-255	
768+	O	Additional redundant parameter pages	

Notes:

1. “O” Stands for Optional, “M” for Mandatory
2. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details.

   The CRC shall be calculated using the following 16-bit generator polynomial: *G(X) = X16 + X15 +X2 + 1*， This polynomial in hex may be represented as 8005h.

3. The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Device Model	**ORGANIZATION**	**VCC RANGE**	**CRC value B254/B255**
“GD5F1GQ4U”	X4	2.7v ~ 3.6v	D9H/B9H
“GD5F1GQ4R”	X4	1.7v ~ 1.95v	01H/74H

10 PROGRAM OPERATIONS

10.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to 2176 bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

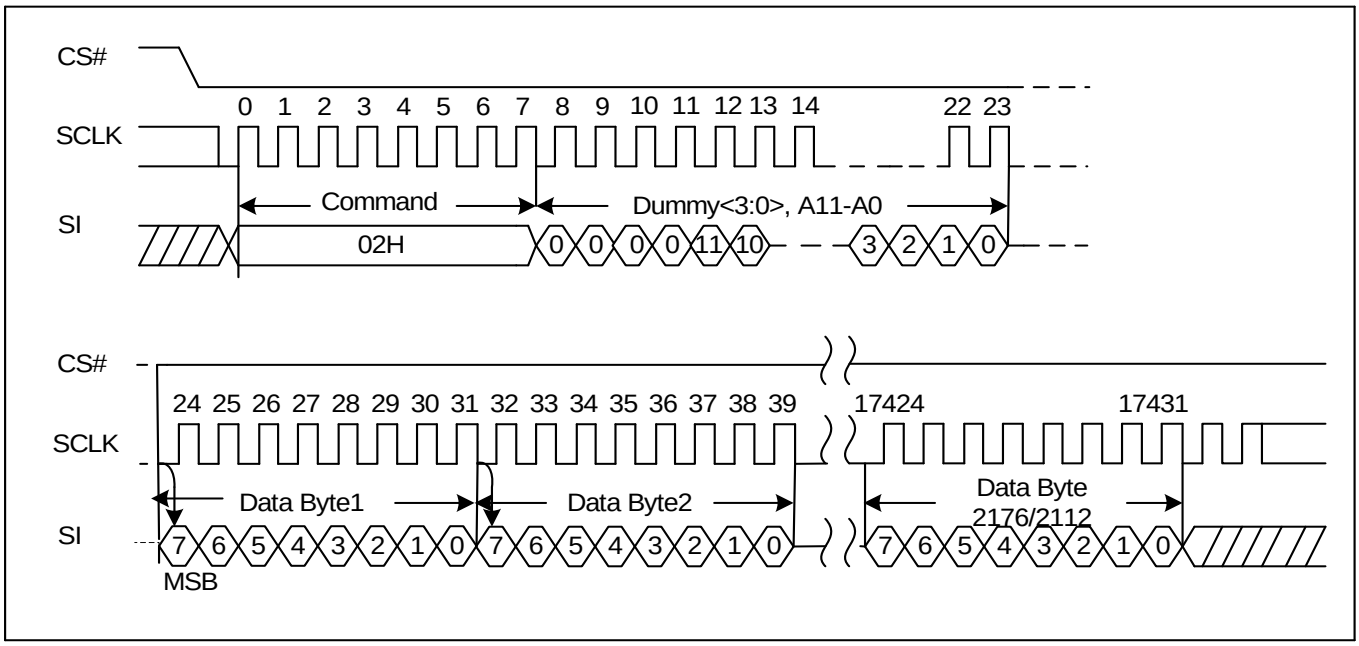
Firstly, a PROGRAM LOAD (02H/32H) command is issued. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register that is 2176 bytes long. If more than 2176 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure10-1 shows the PROGRAM LOAD operation. Secondly, prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

Note:

1. The contents of Cache Register doesn't reset when Program Load (02h) command, Program Random Load (84h) command and RESET (FFh) command.
2. When Program Execute (10h) command was issued just after Program Load (02h) command, SPI-NAND controller outputs 0xFF data to the NAND for the address that data was not loaded by Program Load (02h) command.
3. When Program Execute (10h) command was issued just after Program Load Random Data (84h) command, SPI-NAND controller outputs contents of Cache Register to the NAND.
4. The addressing should be done in sequential order in a block.

10.2 Program Load (PL) (02H)

Figure10-1. Program Load Sequence Diagram

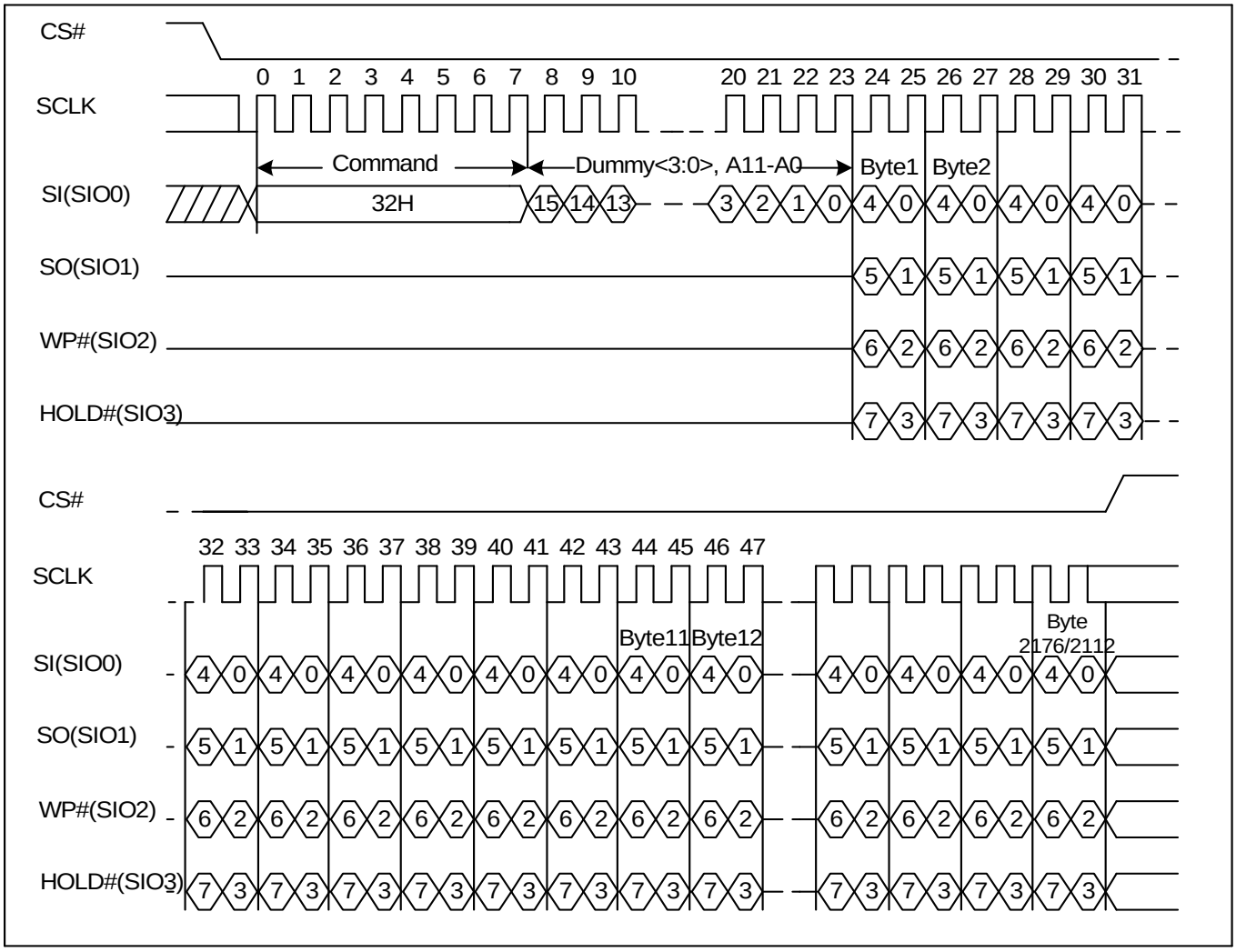


Note: when internal ECC disabled the Data Byte is 2176, when internal ECC enabled the Data Byte is 2112.

10.3 Program Load x4 (PL x4) (32H)

The Program Load x4 command (32H) is similar to the Program Load command (02H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the program load x4 command.

Figure10-2. Program Load x4 Sequence Diagram

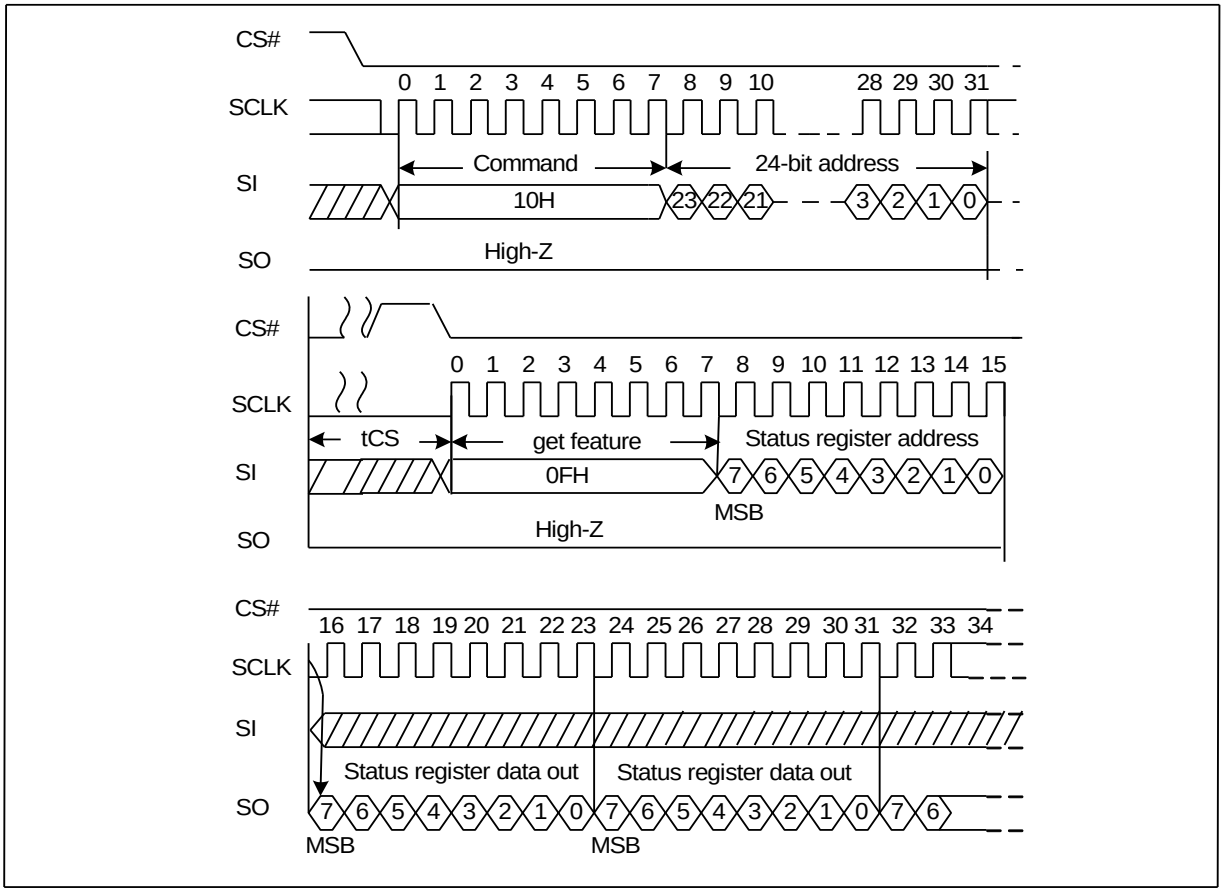


Note: when internal ECC disabled the Byte is 2176, when internal ECC enabled the Byte is 2112.

10.4 Program Execute (PE) (10H)

After the data is loaded, a PROGRAM EXECUTE (10H) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address. After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation is shown in Figure10-3. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Figure10-3. Program Execute Sequence Diagram



10.5 Internal Data Move

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

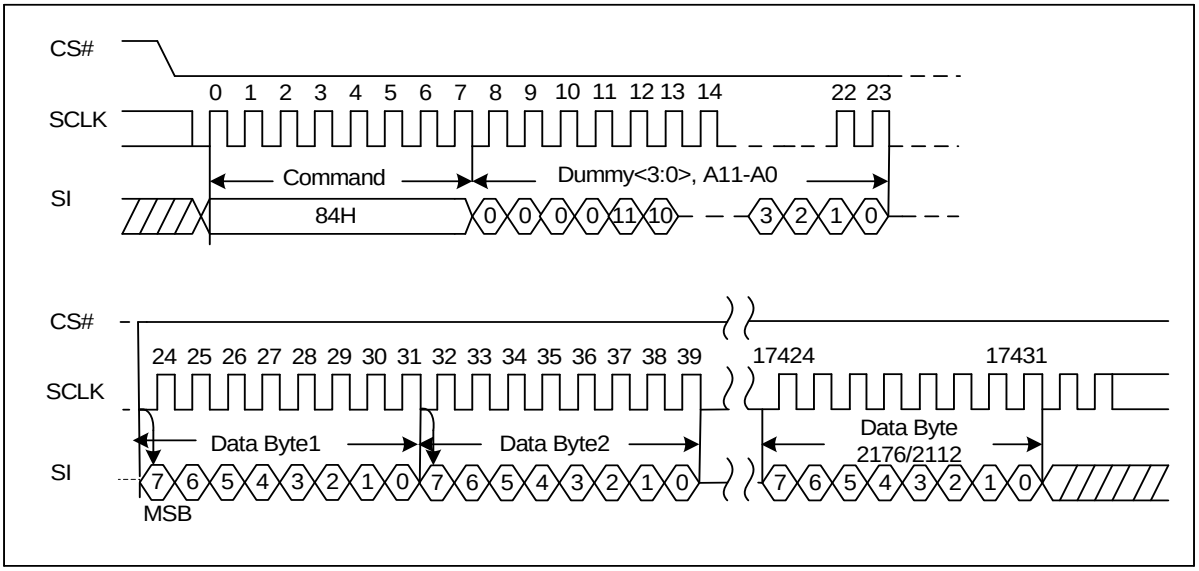
- 13H (PAGE READ to cache)
- Optional 84H/C4H/34H(PROGRAM LOAD RANDOM DATA)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/C4H/72H) command can be issued, if user wants to update bytes of data in the page. New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84H/C4H/72H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and then a PROGRAM EXECUTE (10H) command can be issued to start the programming operation.

10.6 Program Load Random Data (84H)

This command consists of an 8-bit Op code, followed by 4 dummy bits, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84H) command must be issued with a new column address, see Figure10-4 for details. This command is only available during internal data move sequence.

Figure10-4. Program Load Random Data Sequence Diagram

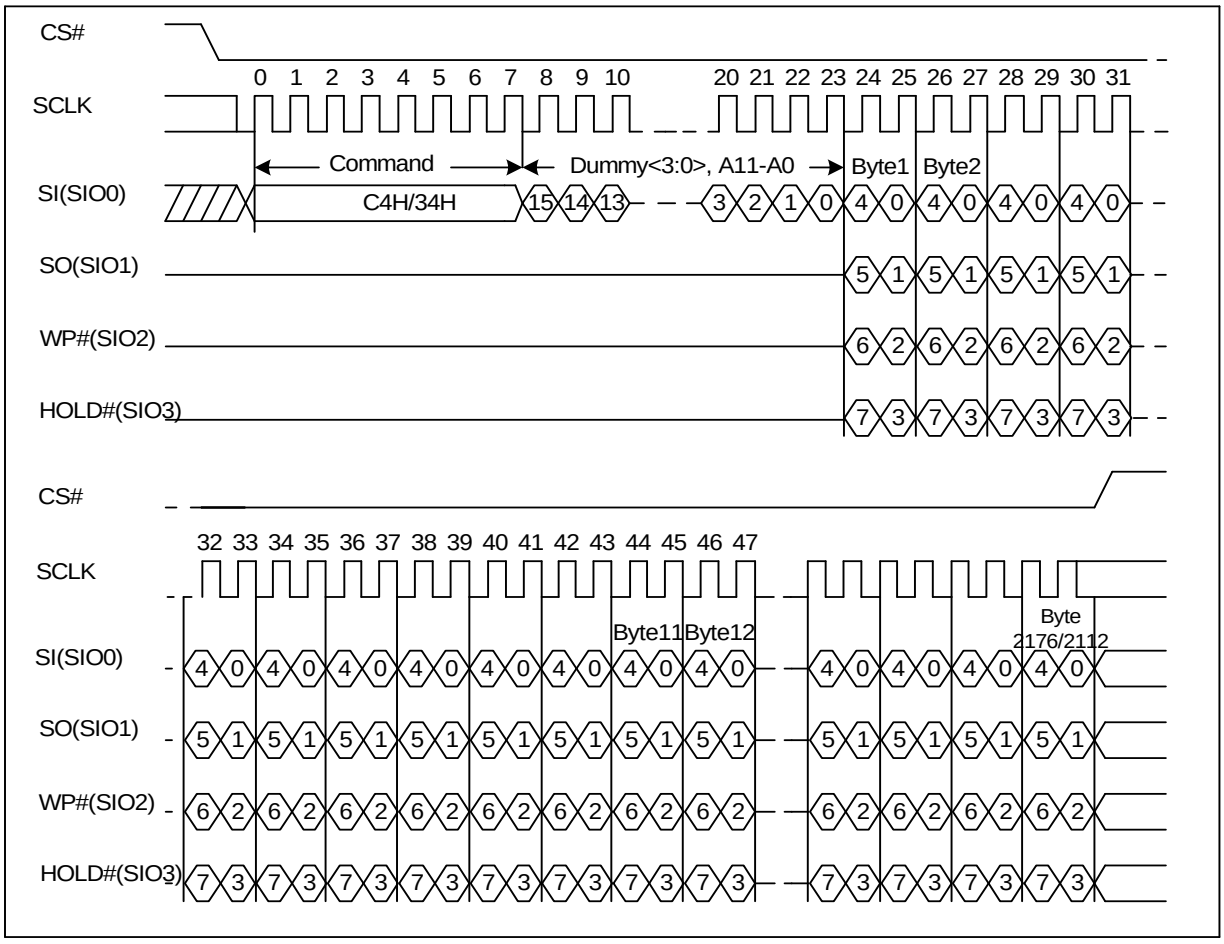


Note: when internal ECC disabled the Data Byte is 2176, when internal ECC enabled the Data Byte is 2112.

10.7 Program Load Random Data x4 (C4H/34H)

The Program Load Random Data x4 command (C4H/34H) is similar to the Program Load Random Data command (84H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable for the program load random data x4 command. See Figure10-5 for details. Those two commands are only available during internal data move sequence.

Figure10-5. Program Load Random Data x4 Sequence Diagram

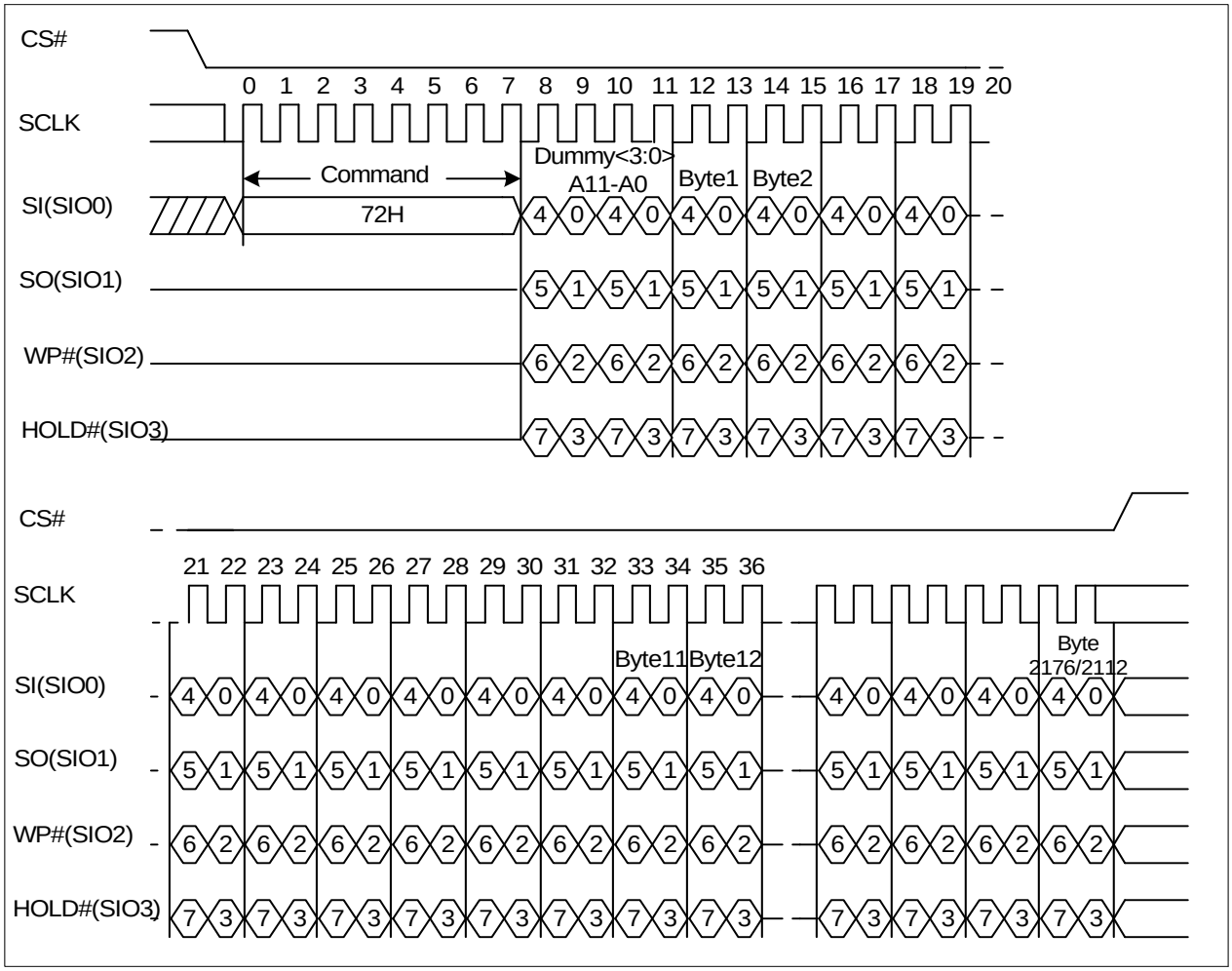


Note: when internal ECC disabled the Data is 2176, when internal ECC enabled the Data is 2112.

10.8 Program Load Random Data Quad IO (72H)

The Program Load Random Data Quad IO command (72H) is similar to the Program Load Random Data x4 command (C4H) but with the capability to input the 4 dummy bits, and a 12-bit column address by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable for the program load random data x4 command. See Figure10-6 for details. This command is only available during internal data move sequence.

Figure10-6. Program Load Random Data Quad IO Sequence Diagram

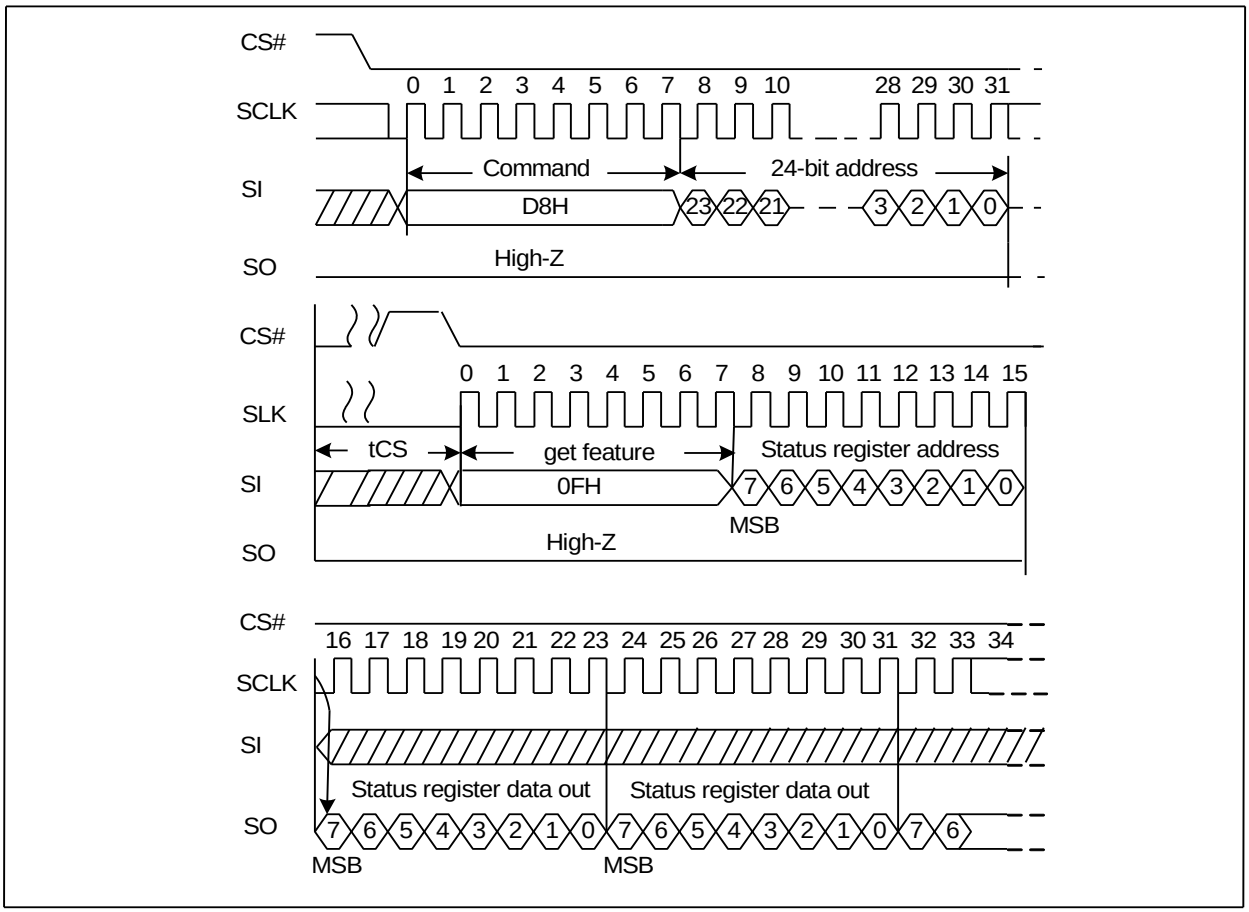


Note: when internal ECC disabled the Data is 2176, when internal ECC enabled the Data Byte is 2112.

11 ERASE OPERATIONS

11.1 Block Erase (D8H)

Figure11-1. Block Erase Sequence Diagram



The BLOCK ERASE (D8H) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2176 bytes per page (2048 + 128 bytes). Each block is 136 Kbytes. The BLOCK ERASE command (D8H) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06H (WRITE ENBALE command)
- D8H (BLOCK ERASE command)
- 0FH (GET FEATURES command to read the status register)

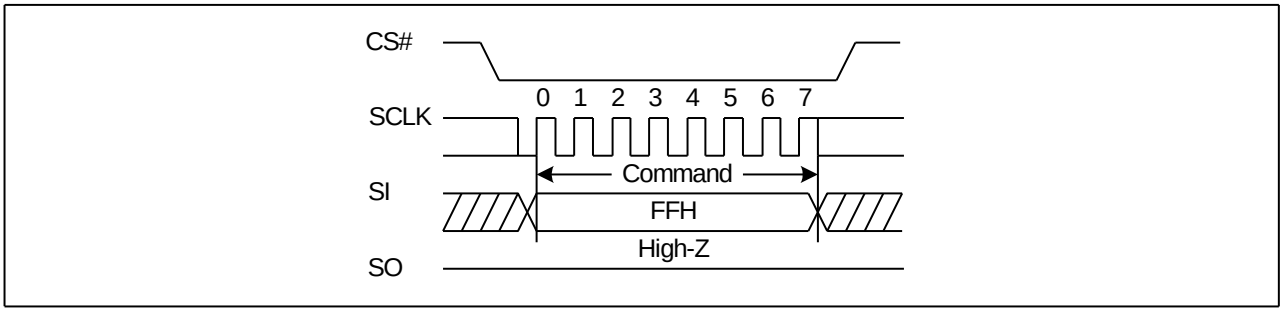
Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8H) command. This command requires a 24-bit address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for t_{ERS} time during the BLOCK ERASE operation. The GET FEATURES (0FH) command can be used to monitor the status of the operation.

When a block erase operation is in progress, user can issue normal read from cache commands (03H/0BH/3BH/6BH/BBH/EBH) to read the data in the cache.

12 RESET OPERATIONS

12.1 Soft Reset (FFH)

Figure12-1. Reset Sequence Diagram



The RESET (FFH) command stops all operations. For example, in case of a program or erase or read operation, the reset command can make the device enter the wait state. The device will automatically read first page of fist block to cache after RESET (FFH)

During a cache program or cache read, a reset can also stops the previous operation and the pending operation. The OIP status can be read from 300ns after the reset command is sent.

12.2 Hardware RESET

12.2.1 Hardware RESET Function

The RESET# pin allows the device to be reset by the host controller or system reset timer like watchdog for re-boot without a power off and on sequence.

For the WSON8/LGA8 package, pin7 can be configured as a RESET# pin depending on the status register setting, QE=0 and HOLD/RST=1(see Section Hardware RESET Setting). On the SOP16/BGA24 package, a dedicated RESET# pin is provided and it is independent of QE bit setting (see Section Hardware RESET Setting).

The RESET# pin goes low for a period of tRLRH or longer will reset the flash memory. After a reset cycle, the flash is at the following states:

-In standby mode

-All the volatile bits return to the default value as after power-on-reset.

-Data of page0/block0 is read out to the cache, user can issue read from cache command (03/0B/3B/6B/BB/EB) for data.

Please note that No command is accepted during the reset cycle (tRB1 or tRB2).

Figure12-2. Hardware RESET Timing

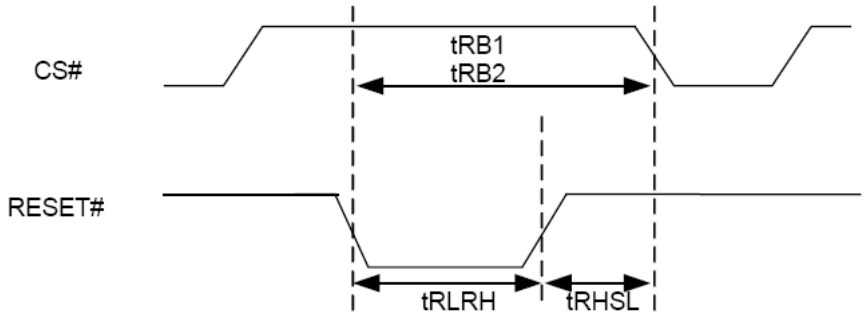


Table12-1. Hardware RESET Timing

Symbol	Parameter	Setup	Speed	Unit.
tRLRH	Reset pulse width	MIN	500	us
tRHSL	Reset high time before read	MIN	50	ns
tRB1	Reset recovery time (For NOT busy mode)	MAX	500	us
tRB2	Reset recovery time (For busy mode)	MAX	1	ms

12.2.2 Hardware RESET Setting

a) WSON8/LGA8 package

For the WSON8/LGA8 package, RESET#, HOLD# and data IO3 share the same pin7. The pin7 can be configured as any of the three functions depending on the status register setting. When QE=0, HOLDB/RST=1, the pin7 acts as a RESET# pin. When QE=1 or QE=0 HOLDB/RST=0, the pin7 will be configured as the other functions and Hardware Reset function can't be used.

QE and HOLDB/RST registers can be set by Set Feature command (see table12-2). QE can be set by Set Feature command when address is B0H and HOLDB/RST can be set by Set Feature command when address is D0H. Both of them can be read out by Get Feature command with related address. Through reading the status registers, users could know the value and infer which function is supported on the pin7.

By default QE and HOLDB/RST registers are both 0 after power-on-reset or hardware reset.

Table12-2. Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0H	HOLDB/RST	DS_S1	DS_S0	Reserved	Reserved	Reserved	Reserved	Reserved
Status	F0H	Reserved	Reserved	ECCSE1	ECCSE0	Reserved	Reserved	Reserved	Reserved

b) SOP16/BGA24 package

For SOP16/BGA24 package (see Figure2-1), a dedicated RESET# pin is provided and it is independent of QE bit setting. At the same time, HOLDB/RST register is not existed in SOP16, and the corresponding bit in command Set/Get Feature with address D0H is reserved.

Table12-3. Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0H	Reserved	DS_S1	DS_S0	Reserved	Reserved	Reserved	Reserved	Reserved
Status	F0H	Reserved	Reserved	ECCSE1	ECCSE0	Reserved	Reserved	Reserved	Reserved

13 ADVANCED FEATURES

13.1OTP REGON

The serial device offers a protected, One-Time Programmable NAND Flash memory area. 4 full pages (2176 bytes per page) are available on the device. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, pages 00h–03H can be programmed in sequential order by PROGRAM LOAD (02H) and PROGRAM EXECUTE (10H) commands (when not yet protected), and read out by PAGE READ (13H) command and output data by READ from CACHE(03H/0BH/3BH/6BH/BBH/EBH).

Table13-1. OTP States

OTP_PRT	OTP_EN	State
x	0	Normal operation
0	1	Access OTP region, read and program data.
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10H) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data.

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

Access to OTP data

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

Protect OTP region

Only when the following steps are completed, the OTP_PRT will be set and users can get this feature out with 0FH command.

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN and OTP_PRT
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command.

13.2 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1and BP2 are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, status bit OIP remains 0. When an ERASE command is issued to a locked block, the erase failure, 04H, is returned. When a PROGRAM command is issued to a locked block, program failure, 08h, is returned.

Table13-2. Block Lock Register Block Protect Bits

CMP	INV	BP2	BP1	BP0	Protect Rows	Protect Rows
					1G	
x	x	0	0	0	NONE	None—all unlocked
0	0	0	0	1	FC00h ~ FFFFh	Upper 1/64 locked
0	0	0	1	0	F800h ~ FFFFh	Upper 1/32 locked
0	0	0	1	1	F000h ~ FFFFh	Upper 1/16 locked
0	0	1	0	0	E000h ~ FFFFh	Upper 1/8 locked
0	0	1	0	1	C000h ~ FFFFh	Upper 1/4 locked
0	0	1	1	0	8000h ~ FFFFh	Upper 1/2 locked
x	x	1	1	1	0000h ~ FFFFh	All locked (default)
0	1	0	0	1	0000h ~ 03FFh	Lower 1/64 locked
0	1	0	1	0	0000h ~ 07FFh	Lower 1/32 locked
0	1	0	1	1	0000h ~ 0FFFh	Lower 1/16 locked
0	1	1	0	0	0000h ~ 1FFFh	Lower 1/8 locked
0	1	1	0	1	0000h ~ 3FFFh	Lower 1/4 locked
0	1	1	1	0	0000h ~ 7FFFh	Lower 1/2 locked
1	0	0	0	1	0000h ~ FBFFh	Lower 63/64 locked
1	0	0	1	0	0000h ~ F7FFh	Lower 31/32 locked
1	0	0	1	1	0000h ~ EFFFh	Lower 15/16 locked
1	0	1	0	0	0000h ~ DFFFh	Lower 7/8 locked
1	0	1	0	1	0000h ~ BFFFh	Lower 3/4 locked
1	0	1	1	0	0000h ~ 003Fh	Block0
1	1	0	0	1	0400h ~ FFFFh	Upper 63/64 locked
1	1	0	1	0	0800h ~ FFFFh	Upper 31/32 locked
1	1	0	1	1	1000h ~ FFFFh	Upper 15/16 locked
1	1	1	0	0	2000h ~ FFFFh	Upper 7/8 locked
1	1	1	0	1	4000h ~ FFFFh	Upper 3/4 locked
1	1	1	1	0	0000h ~ 003Fh	Block0

When WP# is not LOW, user can issue bellows commands to alter the protection states as want.

- Issue SET FEATURES register write (1FH)
- Issue the feature bit address (A0h) and the feature bits combination as the table

13.3 Status Register and Driver Register

The NAND Flash device has an 8-bit status register that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0FH) command, followed by the feature address C0h or F0h (see FEATURE OPERATION). The Output Driver Register can be set and read by issuing the SET FEATURE (0FH) and GET FEATURE command followed by the feature address D0h (see FEATURE OPERATION).

Table13-3. Status Register Bit Descriptions

Bit	Bit Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred (E_FAIL set to 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
ECCS1, ECCS0 ECCSE1 ECCSE0	ECC Status	ECCS provides ECC status as the following table. ECCS and ECCSE are set to 00b either following a RESET, or at the beginning of the READ. They are then updated after the device completes a valid READ operation. ECCS and ECCSE are invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN to 0). After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.

Table13-4. ECC Error Bits Descriptions

ECCS1	ECCS0	ECCSE1	ECCSE0	Description
0	0	x	x	No bit errors were detected during the previous read algorithm.
0	1	0	0	Bit errors(≤4) were detected and corrected.
0	1	0	1	Bit errors(=5) were detected and corrected.
0	1	1	0	Bit errors(=6) were detected and corrected.
0	1	1	1	Bit errors(=7) were detected and corrected.
1	0	x	x	Bit errors greater than ECC capability(8 bits) and not corrected
1	1	x	x	Bit errors reach ECC capability(8 bits) and corrected

Table13-5. Driver Register Bits Descriptions

DS_S1	DS_S0	Driver Strength
0	0	50%
0	1	25%
1	0	75%
1	1	100%

13.4 Assistant Bad Block Management

As a NAND Flash, the device may have blocks that are invalid when shipped from the factory, and a minimum number of valid blocks (N_{VB}) of the total available blocks are specified. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below N_{VB} during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms, which ensure data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFH data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

To simplify the system requirement and guard the data integration, GigaDevice SPI NAND provides assistant Management options as below.

Table13-6. Bad Block Mark information

Description	Density	Requirement
Minimum number of valid blocks (N_{VB})	1G	1004
Total available blocks per die	1G	1024
First spare area location		Byte 2048
Bad-block mark		00h(use non FFH to check)

13.5 Internal ECC

The serial device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the “active” state. To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1FH).
- Set the feature bit ECC_EN as you want:
  1. To enable ECC, Set ECC_EN to 1.
  2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

- Spare area definitions provided in the ECC Protection table below. User meta data I is not protected by internal ECC and User meta data II is protected by internal ECC.
- ECC can protect main data and spare areas data. Any data wrote to the ECC area are ignored.

Table13-7. ECC Protection and Spare Area

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFH	000H	Yes	Main 0	User data 0
3FFH	200H	Yes	Main 1	User data 1
5FFH	400H	Yes	Main 2	User data 2
7FFH	600H	Yes	Main 3	User data 3
803H	800H	No	Spare 0	User meta 0 data I(1)
80FH	804H	Yes	Spare 0	User meta 0 data II
813H	810H	No	Spare 1	User meta 1 data I
81FH	814H	Yes	Spare 1	User meta 1 data II
823H	820H	No	Spare 2	User meta 2 data I
82FH	824H	Yes	Spare 2	User meta 2 data II
833H	830H	No	Spare 3	User meta 3 data I
83FH	834H	Yes	Spare 3	User meta 3 data II
87FH	840H	Yes	Spare area	Internal ECC parity data

Note1: 800H is reserved for initial bad block mark

14 POWER ON TIMING

Figure14-1. Power on Timing Sequence

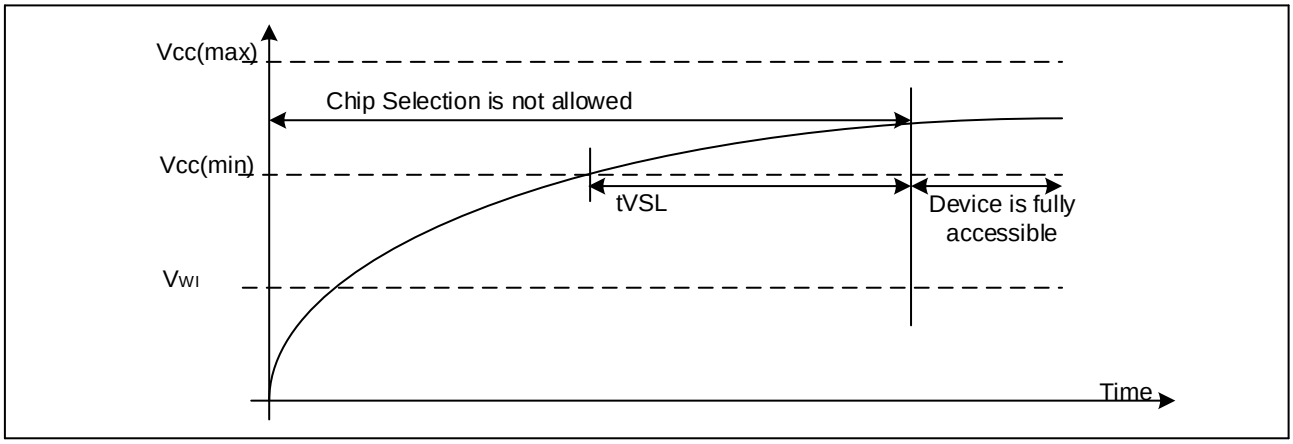


Table14-1. Power-On Timing and Write Inhibit Threshold for 1.8V/3.3V

Symbol	Parameter		Min	Max	Unit
tVSL	VCC(min) To CS# Low		5		ms
VWI	Write Inhibit Voltage	1.8V		1.7	V
		3.3V		2.5	

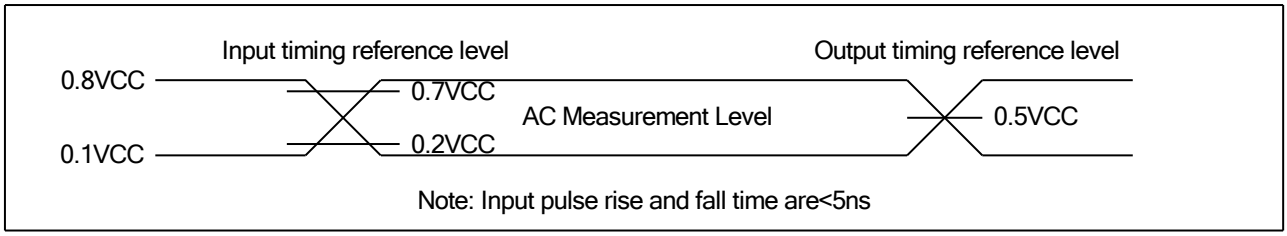
15 ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 105	℃
Storage Temperature	-55 to 125	℃
Applied Input/Output Voltage	-0.6 to Vcc+0.4	V
VCC	-0.6 to Vcc+0.4	V

16 CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure16-1. Input Test Waveform and Measurement Level



17 DC CHARACTERISTIC

(T= -40℃~105℃, VCC=1.7~2.0V/2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS			90 (1)	μA
ICC2	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 108MHz, Q=Open(*1,*2,*4 I/O)			40	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)			30	mA
I_{CC3}	Operation Current (PP)	CS#=VCC			40	mA
I_{CC4}	Operation Current (BE)	CS#=VCC			40	mA
V_{IL}	Input Low Voltage				0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC			V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note: 1. When Temperature is 105℃, the maximum standby current is 200uA

18 AC CHARACTERISTICS

(T= -40℃~105℃, VCC=1.7~2.0V/2.7~3.6V, C_L=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
F_C	Serial Clock Frequency For: all command	DC.		120	MHz
t_{CH}	Serial Clock High Time	4			ns
t_{CL}	Serial Clock Low Time	4			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}/t_{CS}	CS# High Time	20			ns
t_{SHQZ}	Output Disable Time			20	ns
t_{CLQX}	Output Hold Time	2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	Hold# Low Setup Time (relative to Clock)	5			ns
t_{HHCH}	Hold# High Setup Time (relative to Clock)	5			ns
t_{CHHL}	Hold# High Hold Time (relative to Clock)	5			ns
t_{CHHH}	Hold# Low Hold Time (relative to Clock)	5			ns
t_{HLQZ}	Hold# Low To High-Z Output			15	ns
t_{HHQX}	Hold# High To Low-Z Output			15	ns
t_{CLQV}	Clock Low To Output Valid			8	ns
t_{WHSL}	WP# Setup Time Before CS# Low	20			ns
t_{SHWL}	WP# Hold Time After CS# High	100			ns

19 PERFORMANCE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit.
T_{RST}	CS# High To Next Command After Reset(FFh)			500	us
t_{RD}	Read From Array			80	us
t_{PROG}	Page Programming Time		0.4	0.7	ms
t_{BERS}	Block Erase Time		3	5	ms

Figure19-1. Serial Input Timing

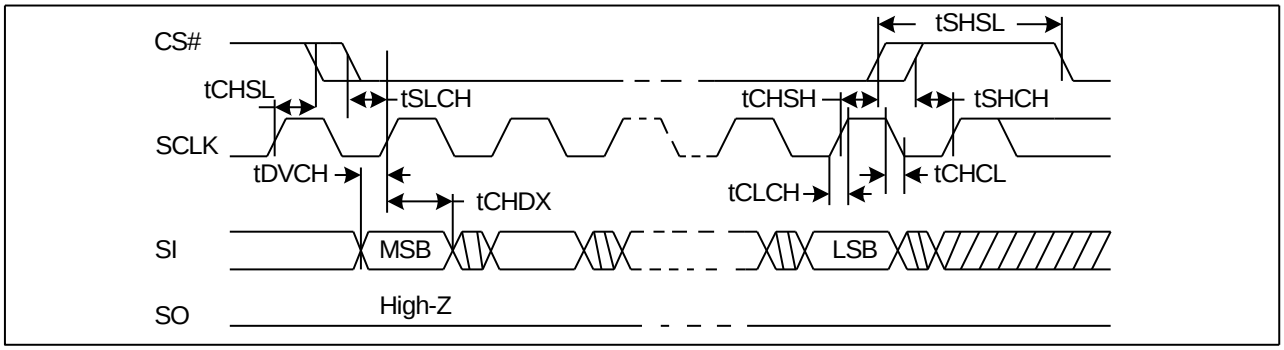


Figure19-2. Output Timing

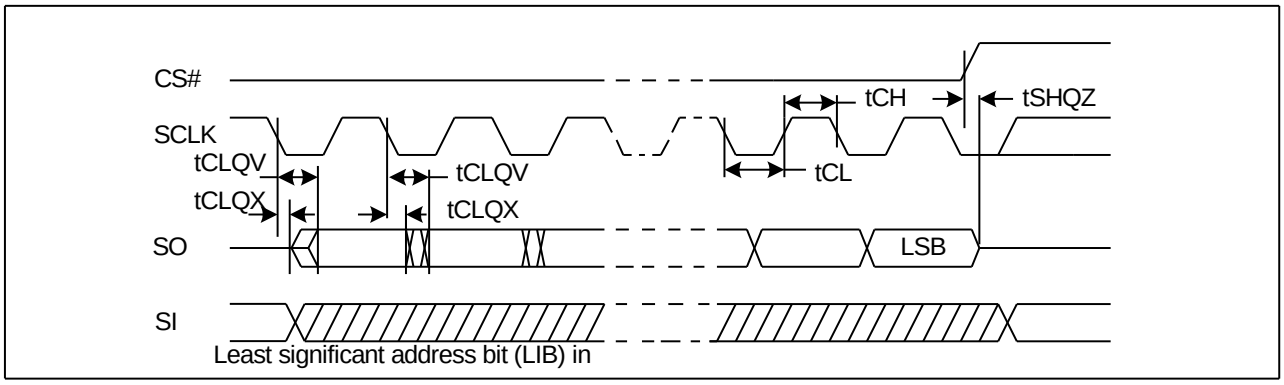


Figure19-3. Hold Timing

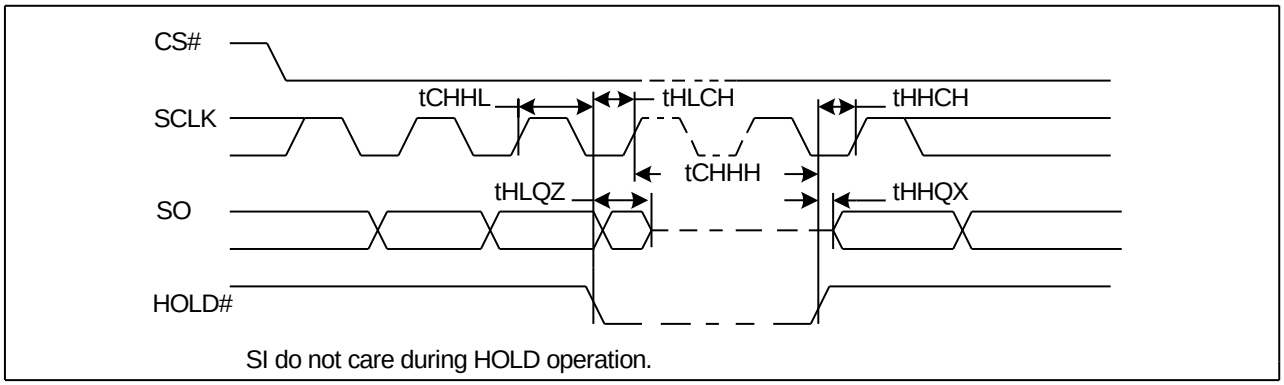
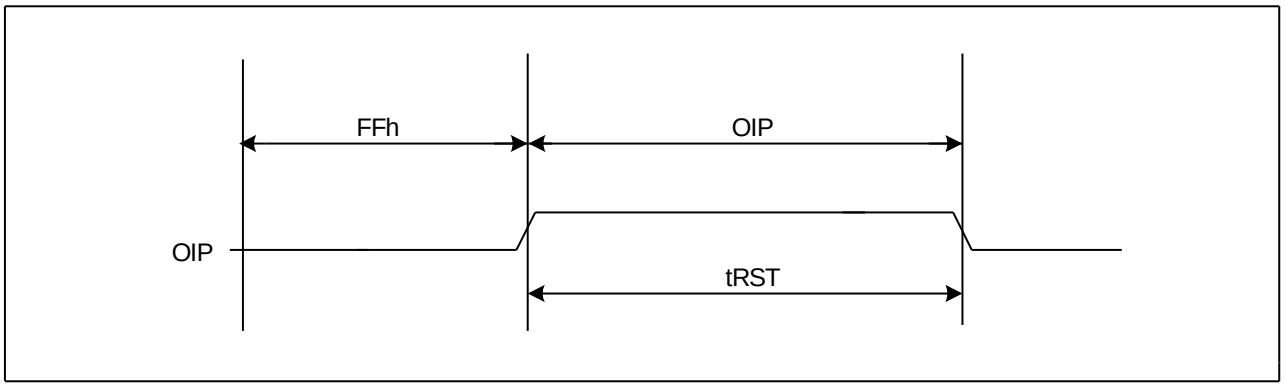


Figure19-4. Reset Timing



Note: The maximum tRST depends on different operations.

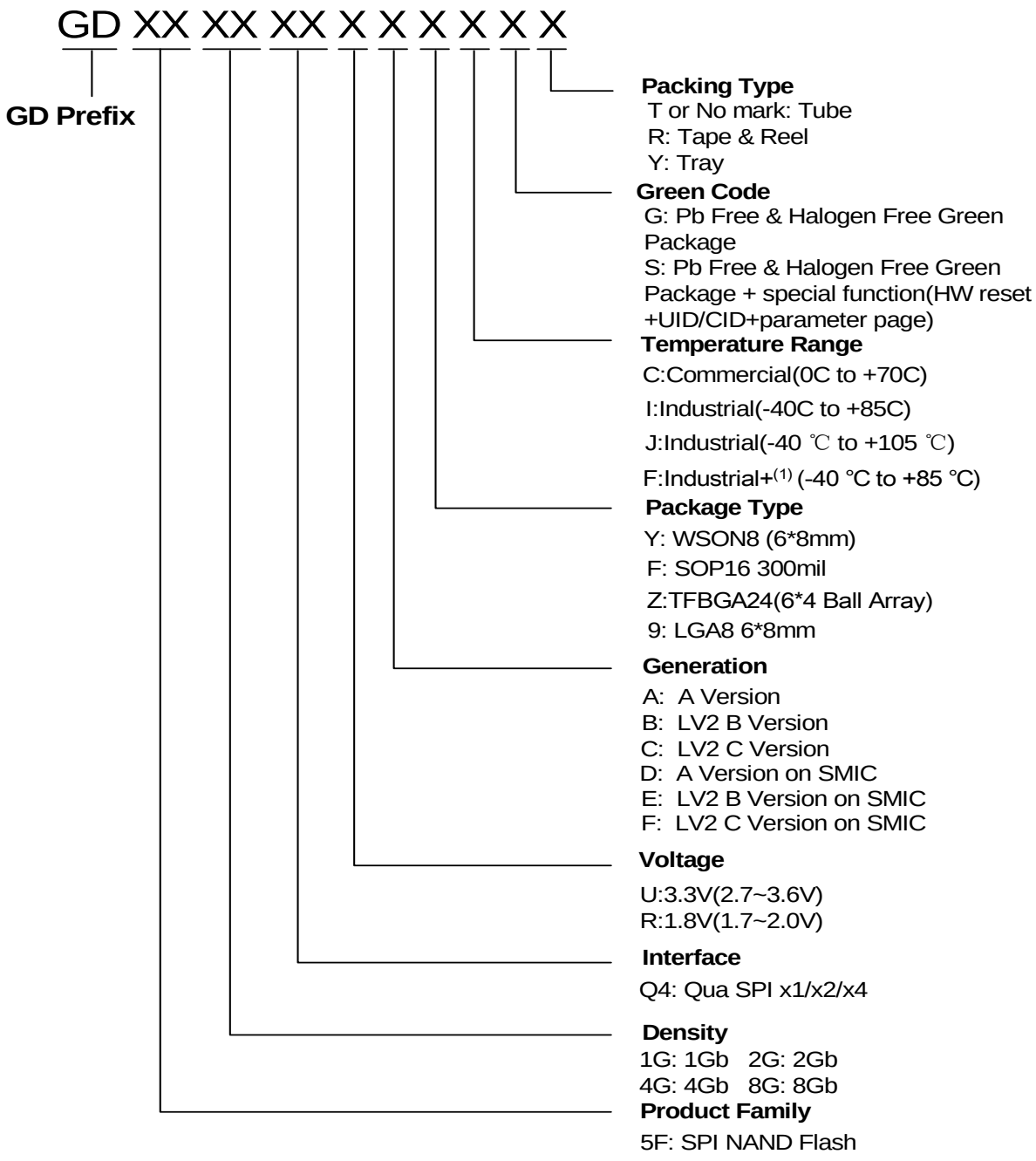
Idle: maximum tRST = 5us;

Read: maximum tRST = 5us;

Program: maximum tRST = 10us;

Erase: maximum tRST = 500us;

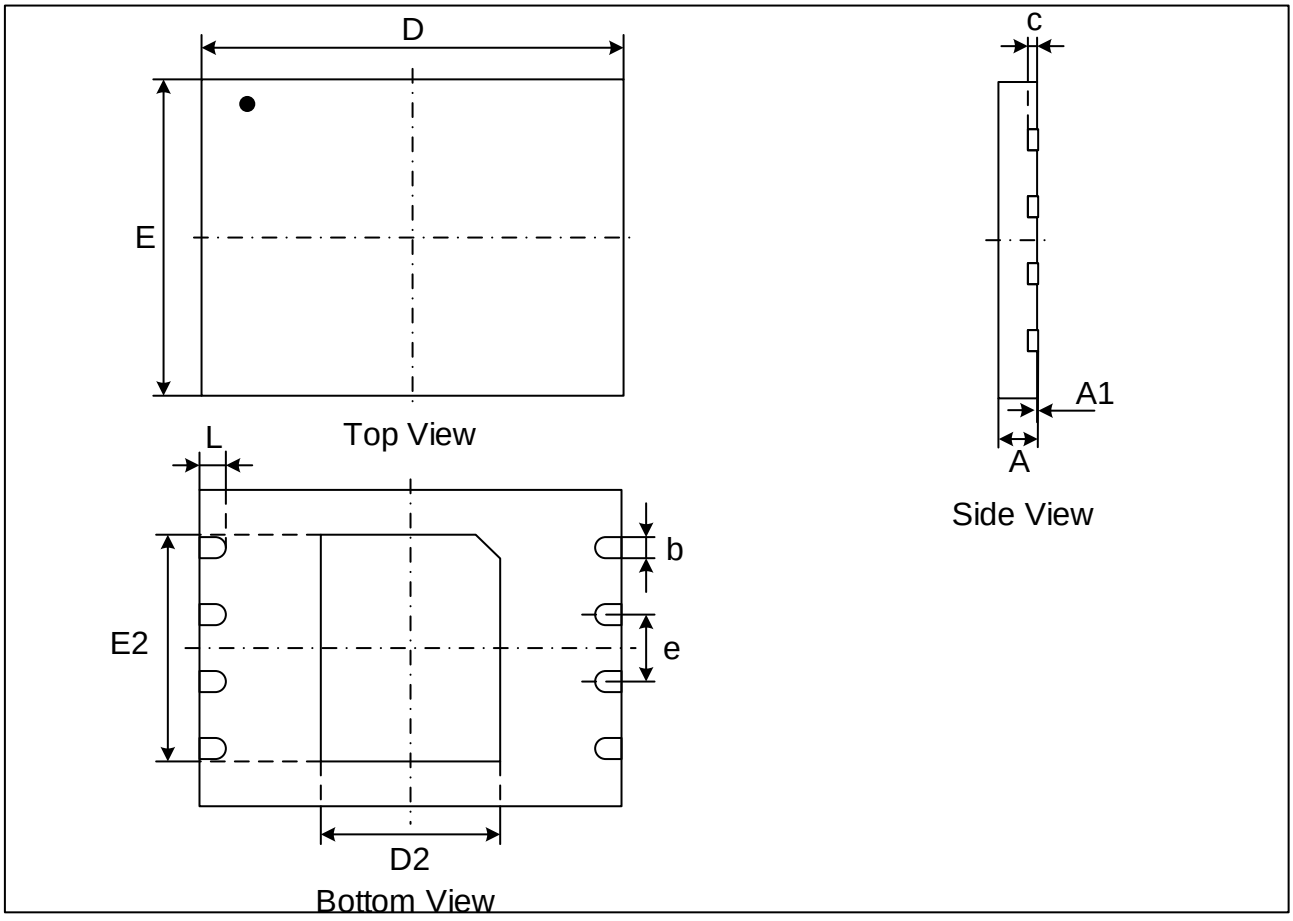
20 ORDERING INFORMATION



Note: (1) Industrial+: Full Function Test for Automotive application and no AECQ.

21 PACKAGE INFORMATION

Figure21-1. WSON8 (6*8mm)



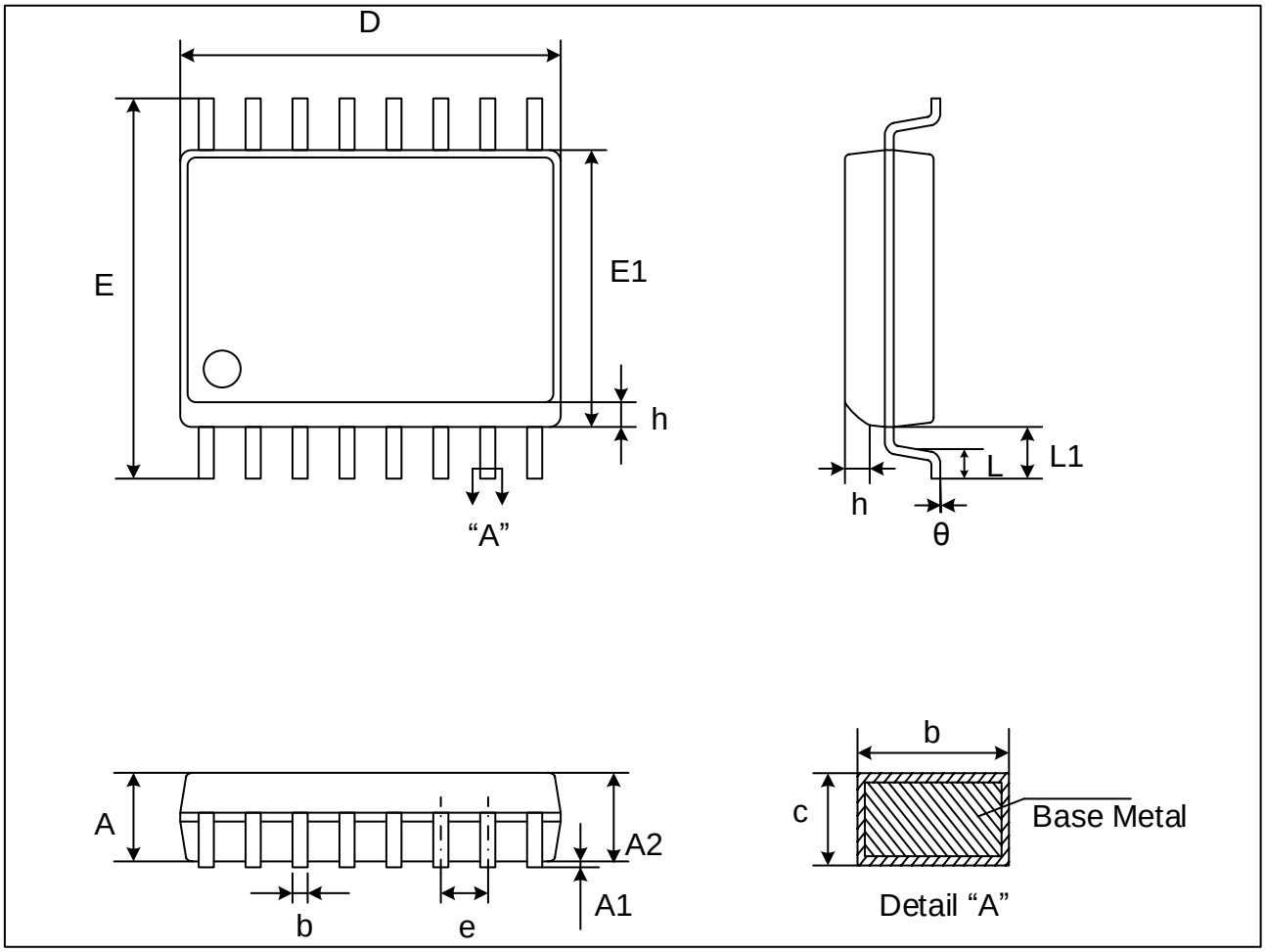
Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.05	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.238	0.173		0.022

Note:

1. Both the package length and width do not include the mold flash.
2. The exposed metal pad area on the bottom of the package is floating.
3. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
4. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

Figure21-2. SOP16 300MIL



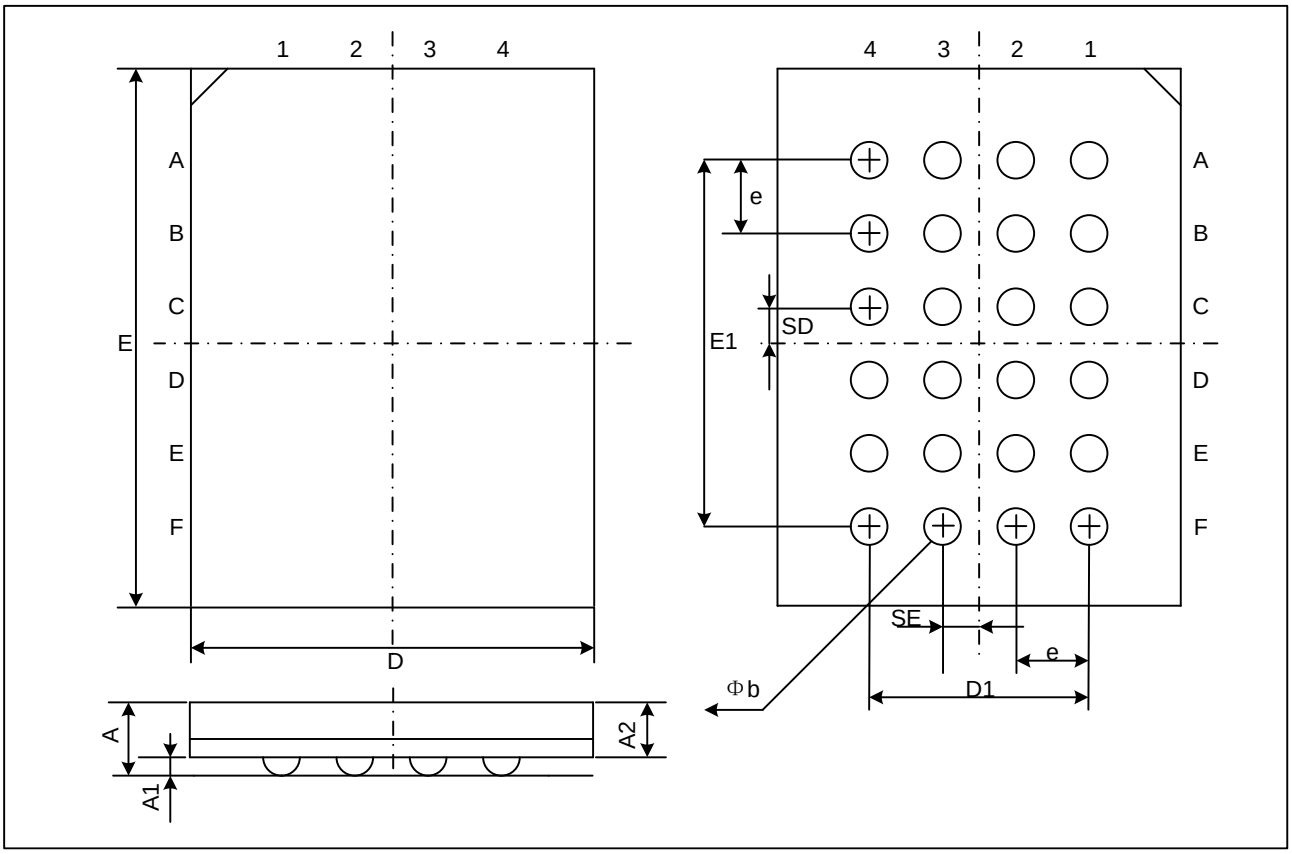
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	-	0.10	2.05	0.31	0.10	10.20	10.10	7.40	1.27	0.40	1.40	0.25	0
	Nom	-	0.20	-	0.41	0.25	10.30	10.30	7.50		-		-	5
	Max	2.65	0.30	2.55	0.51	0.33	10.40	10.50	7.60		1.27		0.75	8
Inch	Min	-	0.004	0.081	0.012	0.004	0.402	0.398	0.291	0.05	0.016	0.055	0.010	0
	Nom	-	0.008	-	0.016	0.010	0.406	0.406	0.295				-	0.197
	Max	0.104	0.012	0.100	0.020	0.013	0.409	0.413	0.299		0.05		0.030	0.315

Note:

1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.

Figure21-3. TFBGA-24BALL (6*4 ball array)

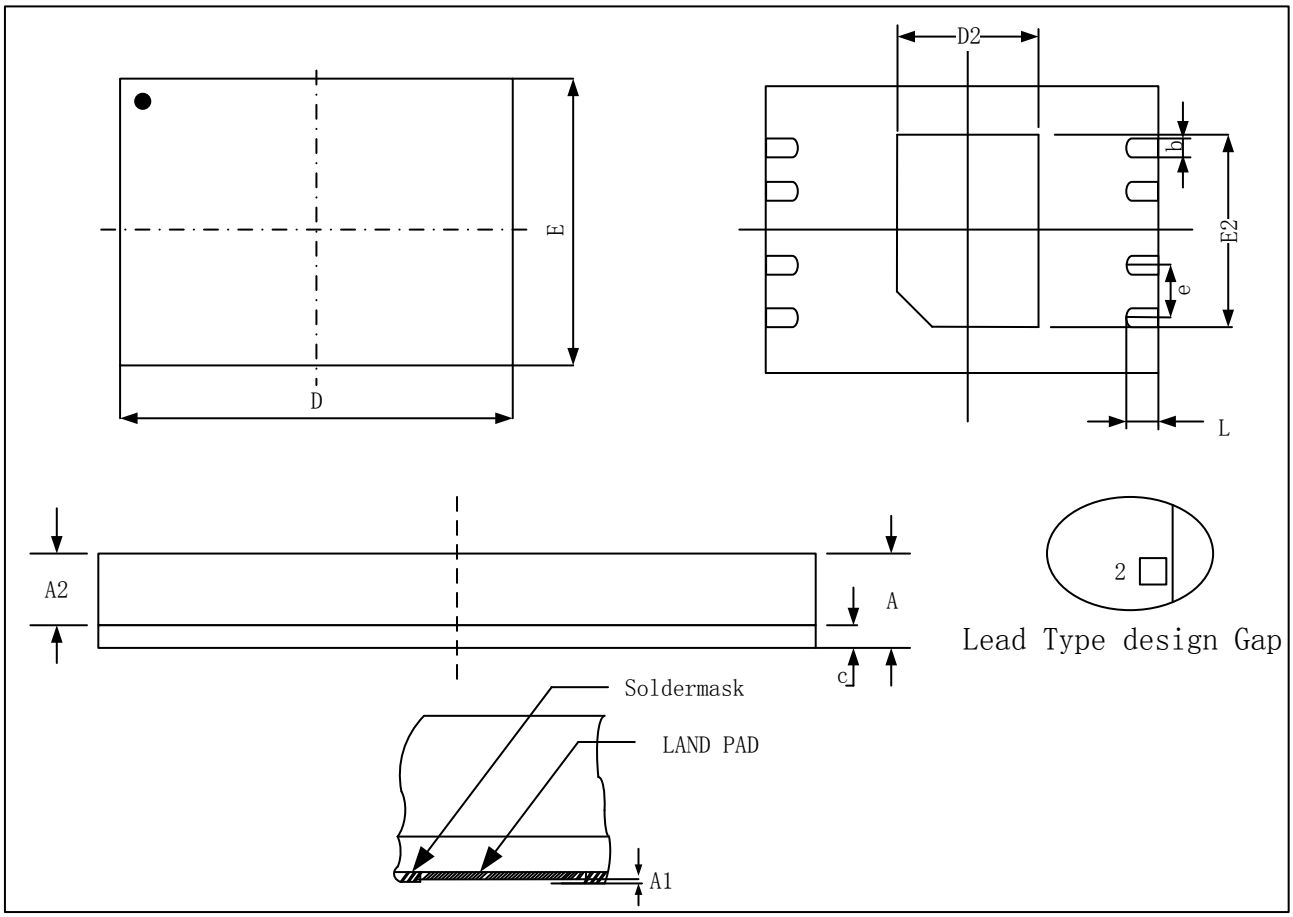


Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	SE	SD
mm	Min		0.25	0.70	0.35	5.90	3.00 BSC	7.90	5.00 BSC	1.00 BSC	0.50 TYP	0.50 TYP
	Nom		0.30	0.80	0.40	6.00		8.00				
	Max	1.20	0.35	0.85	0.45	6.10		8.10				
Inch	Min		0.010	0.028	0.014	0.232	0.118 BSC	0.311	0.197 BSC	0.039 BSC	0.020 TYP	0.020 TYP
	Nom		0.012	0.031	0.016	0.236		0.315				
	Max	0.047	0.014	0.034	0.018	0.240		0.319				

Note: Both the package length and width do not include the mold flash.

Figure21-4. LGA8 GD Type1 (6*8 mm)



Dimensions

Symbol		A		A1	A2		c	b	D	D2	E	E2	e	L
Unit		GD Type1	GD Type2		GD Type1	GD Type2								
mm	Min	0.70	0.80	0.02	0.53	0.70	0.15	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom						0.18	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.95				0.21	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0.031	0.001	0.021	0.028	0.006	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom						0.007	0.016	0.315	0.134	0.236	0.169		0,020
	Max	0.031	0.037				0.008	0.018	0.319	0.138	0.240	0.173		0.022

22 REVISION HISTORY

Version No	Description	Date
1.0	1. Initial Release 2. Add RESET function description with ch12.2 3. Add RESET# pin on Connection Diagram ch2.2 4. Add/Update read ID/UID/CID/parameter page on ch9.	2017-06-14
1.1	Add parameter page CRC value	2017-07-14
1.2	Modify Package WSON8 (6*8mm)	2017-07-20
1.3	Modify the Number of Figure and Table Modify some typo of Read Operation Sequence Diagram Modify Package 'R' description Reduce the size of parameter page device model table Modify Read CID command sequence description Add automatically read first page of fist block to cache after RESET (FFH)	2017-09-01
1.4	Add the Note article 4 of Page Program	2017-10-23
1.5	Add the chapter of Valid Part Numbers	2017-11-03
1.6	Add the description of 1Gb SLC NAND Flash Add the description of Reliability Delete Valid Part Number of GD5FQ4UE9IG Modify the Figure of Program Load Sequence Diagram typo Modify the package of LGA8	2017-12-11
1.7	Modify the package of WSON8,SOP16 300mil,TFBGA24 Modify the typo of LGA8 Add a note for Figure7-1	2017-12-27
1.8	Add LGA8 package description for hardware reset section	2018-1-16
1.9	Modify some typo Add Temperature Range J:Industrial(-40 ℃ to 105℃) and related description Change Memory Mapping CA from <12:0> to <11:0>,RA from <17:6> to <16:6> Add a figure to description Read ID sequence Add page size 2048bytes + 64bytes with ECC enabled Modify figure 10-1,10-2,10-4,10-5,10-6 Byte from 4352 or 2176 to 2176/2112, and add a note to explain Change Parameter page table Byte 105-106 and 108-109,and change CRC Value Merge chapters 2.1 and 20.1 Change the description of protection with WP# Pin	2018-2-13
2.0	Add Temperature Range F:Industrial$^+$ (-40℃ to 85℃)	Mar.12.2018

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