Ultra Low Output Voltage Linear N-FET Controller

Features

- **0.5V±1.5% Reference Voltage**
- **Adjustable Output Voltage Down to 0.5V**
- **MLCC and POSCAP Stable**
- **Enable Control**
- **Power Good Signal Output**
- **Under Voltage Short Circuit Protection**
- **Drive N-Channel MOSFETs**
- **TSOT-23-6 Package**

Applications

- **Notebook or Desknote Computers**
- **Motherboards**
- **Graphic Cards**
- **Ultra-Low-Dropout Voltage Regulators**

General Description

The G9336 series are ultra low output voltage linear N-FET controllers designed to simplify power management for notebook computers. Both voltage adjustable (G9336-ADJ) version available for TSOT-23-6 package. The output voltage can be adjusted from 0.5V to 2.5V for G9336-ADJ.

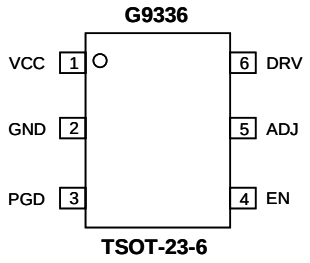
A 0.5V reference voltage with ±1.5% accuracy providing tight regulation of the output voltage, enable control, open drain power good signal, under-voltage protection and soft start.

Ordering Information

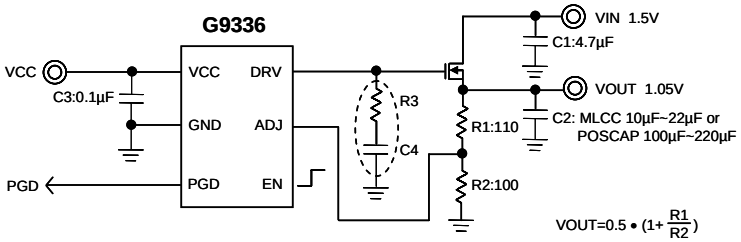
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G9336ADJTP1U	9336x	-40°C to 85°C	TSOT-23-6

Note:TP:TSOT-23-6
1: Bonding Code
U : Tape & Reel

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

VCC, EN, PGD, ADJ, VOUT to GND. . . . .-0.3V to +7V
DRV to GND . . . . . .-0.3V to VCC+0.3V
Thermal Resistance Junction to Ambient, (θ_{JA})*
TSOT-23-6 . . . . . .250°C/W
Continuous Power Dissipation (T_A = +25°C)*
TSOT-23-6 . . . . . .0.5W

Thermal Resistance Junction to Ambient, (θ_{JC})
TSOT-23-6 . . . . . 60°C/W
Operating Temperature Range . . . . . .-40°C to +85°C
Junction Temperature. . . . . .125°C
Storage Temperature . . . . . -65°C to +150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C

*Please refer to Minimum Footprint PCB Layout Section.

Stress beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device.

Electrical Characteristics

V_{CC}= V_{EN}=5V, T_A=25°C.

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{CC}	4.5	---	5.5	V
Quiescent Current	$I_{Q(STANDBY)}$	---	350	500	µA
Shutdown Current	$I_{Q(OFF)}$, V_{EN} = 0V	-1	---	+1	µA
Input Voltage UVLO Threshold	V_{UVLO}, V_{CC} rising	---	3.75	---	V
Input Voltage UVLO Hysteresis	V_{HYST}, V_{CC} falling	---	0.25	---	V
EN Pin Input Voltage High	V_{IH}	1.3	---	---	V
EN Pin Input Voltage Low	V_{IL}	---	---	0.7	V
EN Pin Input Current	I_{EN}	-1	---	+1	µA
ADJ Pin Reference Voltage	V_{ADJ}	-1.5%	0.5	+1.5%	V
ADJ Pin Input Current	I_{ADJ}, V_{ADJ} = 0.5V	-100	---	+100	nA
DRV Pin Output Current	$I_{DRV(SS)}$, sourcing, V_{ADJ} = 0V (startup)	10	20	30	µA
	$I_{DRV(SRC)}$, sourcing, V_{ADJ} = 0.48V (normal)	1.3	1.95	2.6	mA
	$I_{DRV(SINK)}$, sinking, V_{ADJ} = 0.52V	6	9.5	13	mA
DRV Pin Output Voltage	V_{DRV}, V_{CC} = 5V, V_{ADJ} = 0.48V, no load	4.9	---	5	V
Output Voltage UVLO Threshold	$V_{TH(UV)}$, measured at ADJ pin	40	50	60	%V_{ADJ}
Power Good Threshold	$V_{TH(PGD)}$, measured at ADJ pin	85	88	91	%V_{ADJ}
PGD Pin Output Low Voltage	I_{PGD} = 1mA	---	---	0.4	V
PGD Pin Leakage Current	I_{PGD}, V_{ADJ} = 0.5V, V_{PGD} = 6V	-1	---	+1	µA

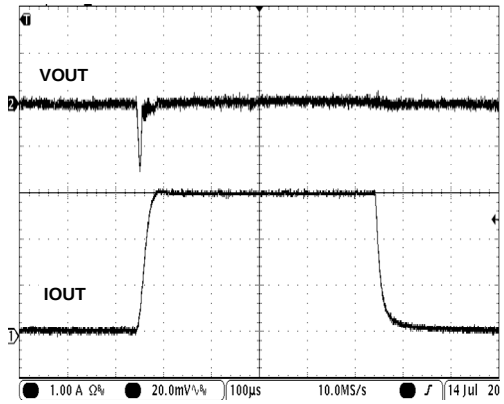
Notes:

1. If $V_{TH(UV)}$ is exceeded for longer than 50µs (TYP.) the protection circuitry will shut down the output.
2. During startup only, $V_{TH(PGD)}$ is 94%(TYP.), then switches to 88% (TYP.).

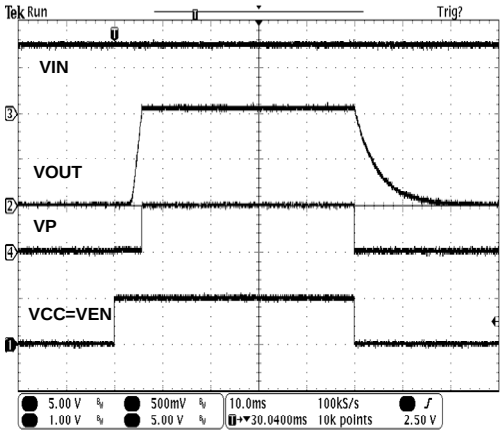
Typical Performance Characteristics

VCC=5V; VIN=1.5V; CVCC=0.1μF; CVIN=4.7μF; CVOUT=22μF; T_A=25°C

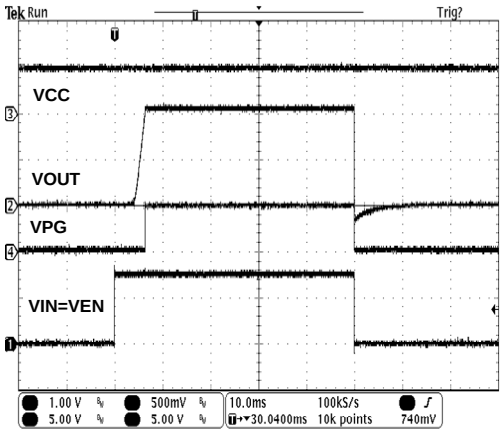
Load Transient



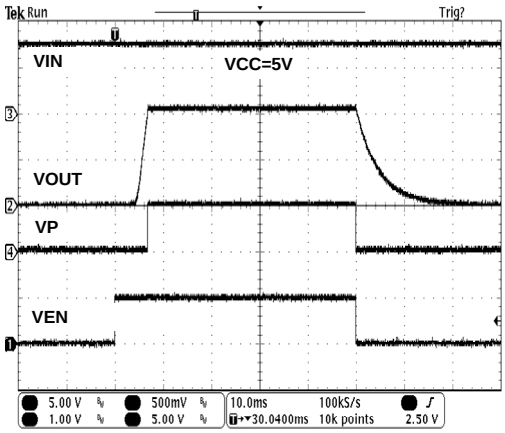
Power On Sequencing with V_{CC}



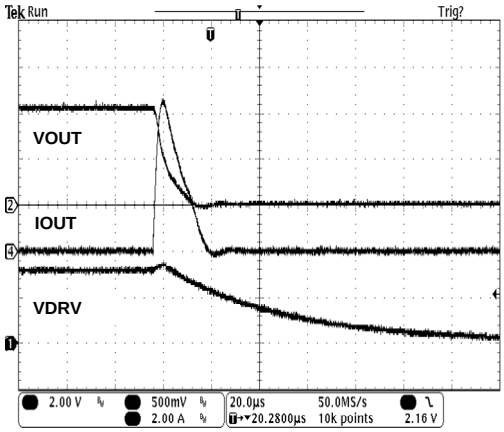
Power On Sequencing with V_{IN}



Enable On Sequencing

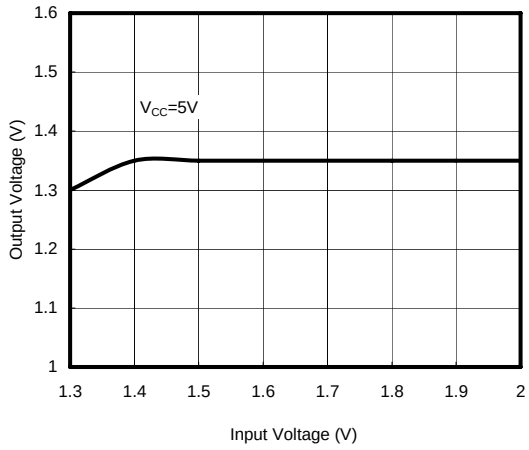


Short Circuit Protection

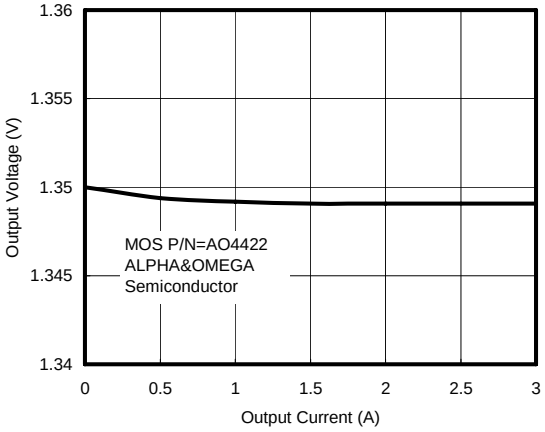


Typical Performance Characteristics (continued)

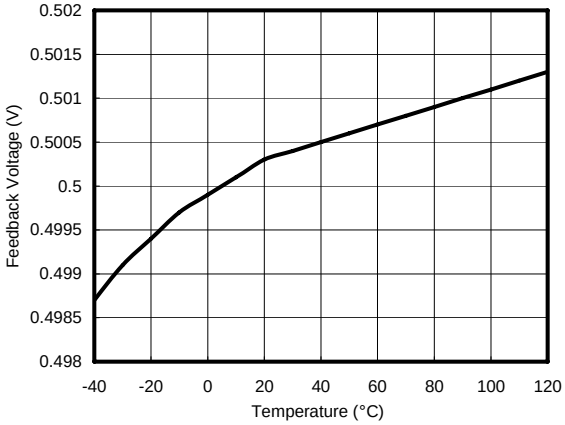
Output Voltage vs Input Voltage



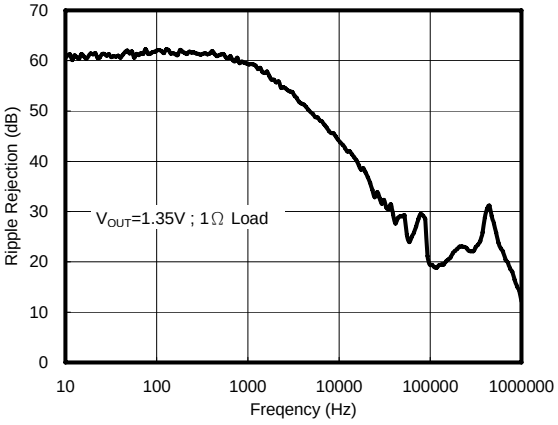
Output Voltage vs Output Current



Feedback Voltage vs Temperature

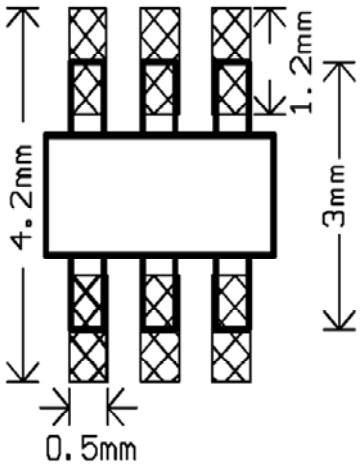


PSRR vs Frequency



Minimum Footprint PCB Layout Section

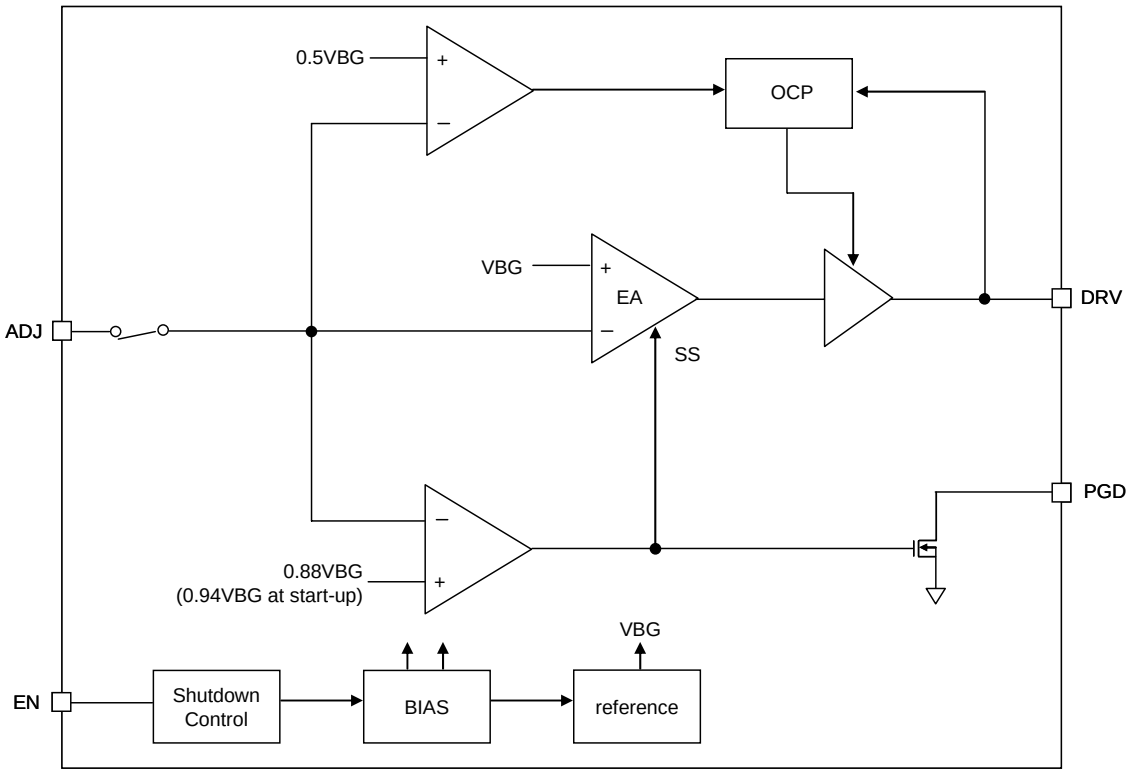
TSOT-23-6



Pin Descriptions

PIN	NAME	FUNCTION
1	VCC	Power supply
2	GND	Ground.
3	PGD	Open drained power good signal output.
4	EN	Active high enable control.
5	ADJ	Sense input used for adjust output voltage.
6	DRV	Gate drive to N-FET.

Block Diagram



Function Description

Normal Operation

The G9336 controls an N-channel MOSFET to produce a tightly regulated output voltage from a higher supply voltage. It takes 5V power supply and draws typically 350μA while operating.

To set the output voltage, feedback the conjunction of a resistor voltage divider from output node to ground for the G9336-ADJ.

The feedback voltage is regulated to compare with the internal 0.5V reference voltage. Depending upon the input voltage used for the device, the DRV pin can pull up to 4.9V. Thus the device can be used to regulate a large range of output voltages by careful selection of the external MOSFETs.

An active high enable control (EN pin) is used to turn on the G9336. If this pin is pulled low, the DRV pin is pulled low, tuning off the N-channel MOSFET. If this pin is pulled higher than 1.3V, the DRV pin is enabled. The EN pin should not be allowed to float.

The G9336 contains a power good output pin (PGD pin) which is an open drain output that pulled low if the output is below the power good threshold (typically 88% of the programmed output voltage, or 94% at the start up). The power good detection is active if the device is enabled, regardless of the state of the over current latch. The power good detector is not active if the output is disabled.

Also included is an over current protection circuit that monitors the output voltage. If the output voltage drops below 50% (typical) of nominal, as would occur during over current or short condition, the device will pull the DRV pin low and latch off. The device will need to have the power supply or EN pin toggled to reset the latch condition.

Drive Output and Stability Design

The drive output (DRV pin) is sink/source capable. The sink current is typically 9.5mA while the source current is typically 1.8mA in normal operating. At start-up, the source current is limited to 20μA (typical) until the power good threshold (94%) is reached. At this point the full drive capability is enabled.

This drive output is also used for stabilize the loop of the system using different type of output capacitor. For the use of the POSCAPs, the output pole is often designed as a dominant pole of the system. The maximum loading determines the highest frequency of this pole. To cancel the ESR zero of the POSCAPs, add a capacitor from drive output to ground. It makes a pole-zero cancellation. For the use of ceramic capacitors, 10μF~22μF is enough for most of the application. The output pole is often at the higher frequency compare to the POSCAPs. It is not suitable to be arranged as a dominant pole. A resistor-capacitor series should be added from drive pin to ground that creates a pole-zero pair. The pole created at drive pin is designed as the dominant pole of the system, and the zero is to cancel the ceramic capacitors output pole. The components listed in the table below are use for most applications.

	MLCC	POSCAP
C2	22μF/X5R	220μF
R3	47Ω	0Ω
C4	33nF	22nF
R2	100Ω	10kΩ

The start-up source current and the loop compensation capacitor (C4) also determine the soft start time T_{SS}.

$T_{SS} = \frac{C4 \cdot (0.94 \cdot VOUT + Vgs)}{20\mu A}$, where Vgs is depend on N-channel MOSFETs

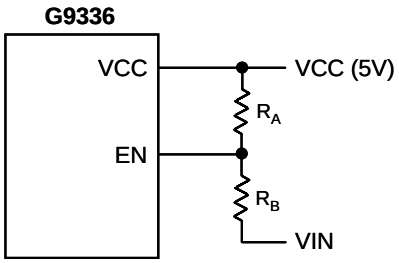
OCP

The G9336 has output under voltage protection that look at its output to see if it is:

(a) less than 50% (typical) of its nominal value and
(b) V_{DRV} is within 1V (typical) of its maximum.

If both of these criteria are met, the output is shut down by means of the V_{DRV} pulled to ground immediately. This provides inherent immunity to under voltage shut down at start up since V_{DRV} has a very slow rate of rising.

If the 5V VCC input is coming prior to the VIN, it could accidentally meet the OCP fault protection. To avoid entering OCP latch off, using enable control (EN pin) to turn the system on whenever all the power supplies are ready. Alternatively, use a voltage divider (from VCC to VIN) controls enable input, as shown below.



$\frac{VCC-0.7}{R_A}=\frac{0.7-(VOUT/2)}{R_B}$, which VOUT is the target output voltage.

For example, if VCC=5V, VIN=1.2V (later arrival) and the VOUT is to be 1.05V, the equation is reduced to R_A/R_B=24.6. By choosing correct R_A/R_B ratio, the G9336 will be turned on when VIN is greater than 50% of the target VOUT. It will avoid the OCP fault protection when starting up. If the VOUT is designed greater than 1.4V, the EN pin can be shorted to VIN that will also not meet the OCP fault protection.

Component Selection

Output Capacitor

Low ESR capacitors such as Sanyo POSCAPs or ceramic capacitors are recommended for bulk capacitance.

Input Capacitor

Low ESR capacitors such as Sanyo POSCAPs or ceramic capacitors will help to hold up the power supply during fast load transients. If V_{DRAIN} is located at the bulk capacitors of the upstream voltage regulator, additional capacitance may not be required. In this case a 0.1µF ceramic capacitor will suffice. The input supply (VCC) to the G9336 should be bypassed with a 0.1µF ceramic capacitor.

MOSFETs

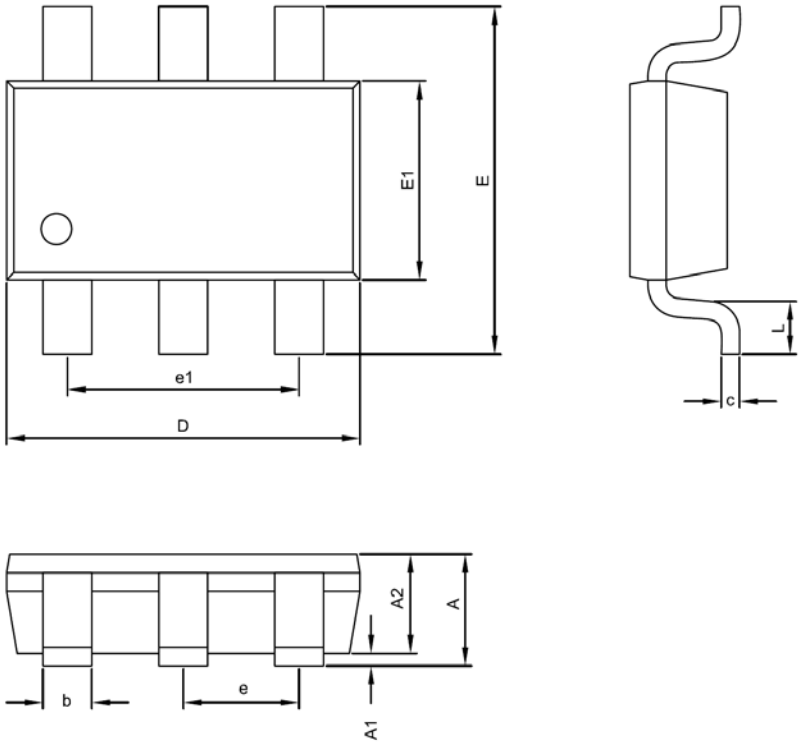
Very low or low threshold N-channel MOSFETs are required. For the device to work under all operating conditions, a maximum $R_{DS(ON)}$ must be met to ensure that the output will never go into dropout:

$$R_{DS(ON)(MAX)}=\frac{VIN_{(MIN)}-VOUT_{(MAX)}}{IOUT_{(PEAK)}}$$

Note that $R_{DS(ON)}$ must be met at all temperatures.

Power consumptions of the N-channel MOSFETs should be taken into consideration for the selection of various package type.

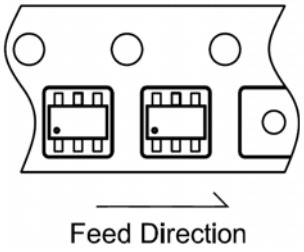
Package Information



TSOT-23-6 (TP) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	- - -	- - -	1.00	- - -	- - -	0.039
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70	0.80	0.90	0.028	0.031	0.035
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
c	0.08	0.15	0.25	0.003	0.006	0.010
b	0.30	0.40	0.50	0.012	0.016	0.020
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024

Taping Specification



PACKAGE	Q'TY/REEL
TSOT-23-6	3,000 ea

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