G2034A

120mA, Current Sinking, 10-bit I2C DAC for VCM Driver

Features

- **VCM driver for auto-focus**
- **10bit resolution current sinking of 120mA for VCM**
- **VCM slew rate control (SRC) – Linear slope control, Dual level control**
- **Supply voltage range (VDD) : 2.3V to 3.6V**
- **Fast mode I2C interface (1.8V interface available)**
- **Power on reset (POR)**
- **TDFN2X2-6 and WLCSP2X3-6 package**

Applications

- **Digital camera**
- **Cell phone**
- **Lens auto focus**
- **Web camera**

General Description

The G2034A is single 10bit DAC with 120mA output current sink capability. Designed for linear control of voice coil motors, the G2034A is capable of operating voltage to 3.6V. The DAC is controlled via a I2C serial interface that operates DAC by clock rates up to 400kHz.

The G2034A incorporates with a power-on reset circuit, power-down function, and exactly matched sense resistor. Power-on reset circuit ensure when supply power up, DAC output is to 0V Until valid write-bit value takes place. It has a power down features that reduces the current consumption of the device to 1μA maximum.

The G2034A is designed for auto focus and optical zoom camera phones, digital still cameras, and camcorders applications. The I2C address for the G2034A is 0x18.

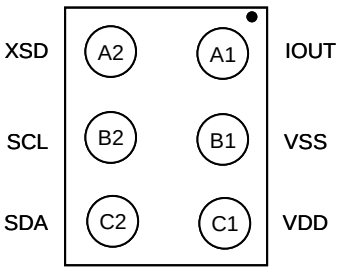
Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2034ARB1U	234A	0°C to +85°C	TDFN2X2-6
G2034AG21U	24A x	0°C to +85°C	WLCSP2X3-6 (Ball Size: 0.025 MM)
G2034AG22U	24A Bx	0°C to +85°C	WLCSP2X3-6 (Ball Size: 0.055 MM)

Note: RB: TDFN2X2-6 1: Bonding Code
G2: WLCSP2X3-6 1 & 2: Ball Size
U: Tape & Reel
Green: Lead Free / Halogen Free.

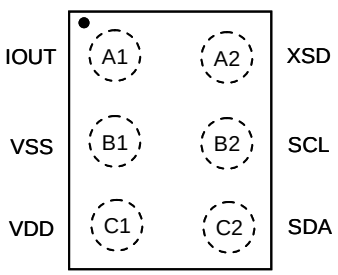
Pin Configuration

6 Bump WLCSP



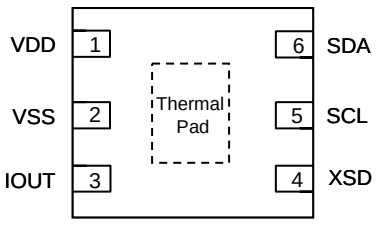
Bottom View
WCSP2X3-6

6 Bump WLCSP



Top View
WCSP2X3-6

G2034A



TDFN2X2-6

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings*1

Power supply voltage (VDD) . . . . . -0.3V to 4.5V
Control input voltage (VIN) . . . . . .-0.3 to VDD+0.3V
Thermal Resistance of Junction to Ambient (θ_{JA})*
TDFN2X2-6. . . . . .225°C/W
WLCSP2X3-6. . . . . TBD
Continuous Power Dissipation (T_A = +25°C)
TDFN2X2-6. . . . . 550mW
WLCSP2X3-6. . . . . TBD
Operating Temperature range. . . . . -40 to 85°C
Junction Temperature . . . . . 150°C
Reflow Temperature (soldering, 10sec). . . . . .260°C
ESD Susceptibility*2
Human body model(Vhbm). 2kV
Machine model (Vmm) 200V

Recommended Operating Conditions

Power supply voltage (VDD) . . . . . 2.3V to 3.6V
Control input voltage (VIN) . . . . . 1.8 to VDD
I2C bus transmission rate (SCL). 400kHz

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
3. Using X5R or X7R input capacitors.

Electrical Characteristics

(VDD= 2.3V to 3.6V, VIN=1.8V to VDD,T_A=+25°C.)

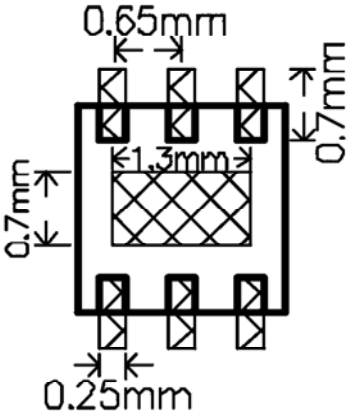
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Overall						
Power Voltage	VDD		2.3	---	3.6	V
VDD Current	I_{SD}	Shutdown mode	-1	---	+1	µA
	I_{PD}	Power down mode	-1	---	+1	µA
	I_Q	Quiescent mode	0.24	---	0.35	mA
Logic input/output (XSD)						
Input Current			-1	---	+1	µA
Low Level Input Voltage	V_{IL}		---	---	0.54	V
High Level Input Voltage	V_{IH}		1.26	---	---	V
Logic input/output (SCL, SDA)						
Input Current			-1	---	+1	µA
Low Level Input Voltage	V_{IL}		---	---	0.54	V
High Level Input Voltage	V_{IH}	LIN=3mA(SDA)	1.26	---	---	V
Low Level Output Voltage	V_{OL}		---	---	0.4	V
Glitch rejection			---	50	---	ns
VCM driver						
Current resolution		117.3µA/LSB	---	10	---	bit
INL	INL		-4	---	+4	LSB
DNL	DNL		-1	---	+1	LSB
Zero code error	ZCE	Zero data loaded to DAC	-1	---	+1	mA
IOUT compliance voltage (1)		Output current=100mA	150	---	---	mV
Maximum output current	I_{MAX}		115	120 (3)	125	mA
Power on time (2)	T_{PON}		---	12	---	ms

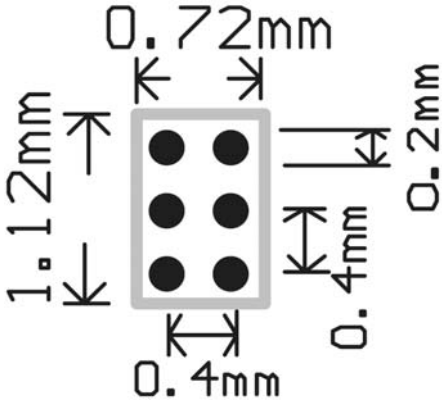
1. The output compliance voltage is guaranteed by design and characterization, not mass production test.
2. G2034A requires waiting time of 12ms after power on. During this waiting time, the offset calibration of internal amplifier is operating for minimization of output offset current.
3. Maximum output current can be set 60mA to 130mA.

Minimum Footprint PCB Layout Section

TDFN2X2-6



WLCSP2X3-6



Pin Description

PIN		NAME	I/O	FUNCTION
TDFN2X2-6	WSCSP2X3-6			
1	C1	VDD	-	Power supply
2	B1	VSS	-	Ground
3	A1	IOUT	O	Output current sink
4	A2	XSD(1)	I	Shutdown mode (active low)
5	B2	SCL	I	I2C Interface Input/Output (Clock)
6	C2	SDA	I/O	I2C interface Input (Data)

(1) XSD: Shutdown mode (active low)
1: Normal operation mode
0: Shutdown mode

Block Diagram

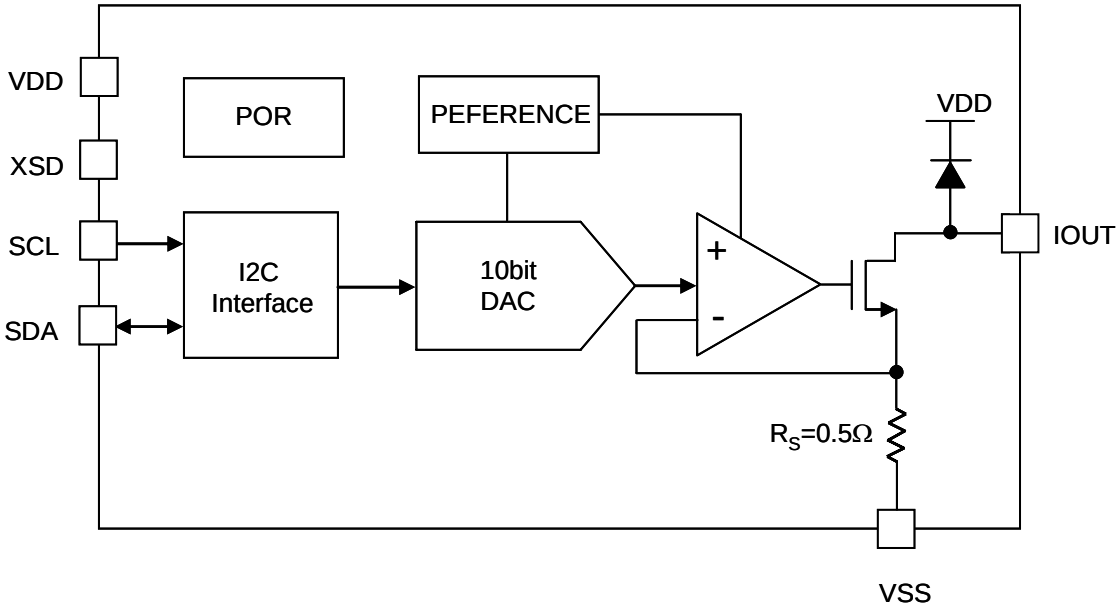
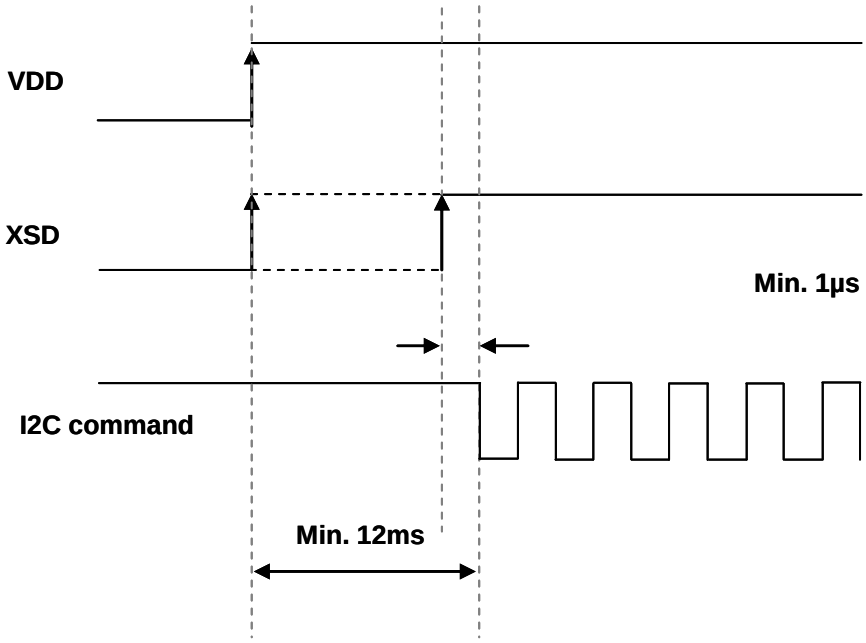


Figure 1: Block Diagram of G2034A

Power on sequence

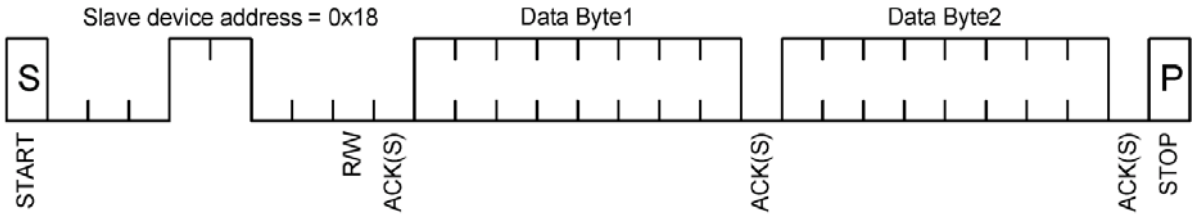


∗ G2034A required waiting time of 12ms after power on.
∗ XSD have only to be set “high” before I2C command.
∗ XSD can be connect to VDD.

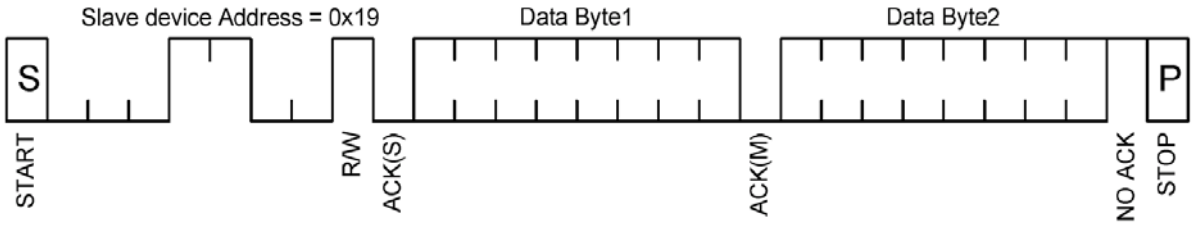
Register

I2C format

Write Operation



Read Operation



Register Format

Byte1								Tyte2							
PD	FLAG	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S3	S2	S1	S0

PD: Power down mode
1: Power down mode (active high)
0: Normal operation mode

FLAG: FLAG must keep “L” at writing operation.

D[9:0]: Data input
Output current=(D[9:0]/1023)X120mA

S[3:2]: Codes per step for “Linear slope control”

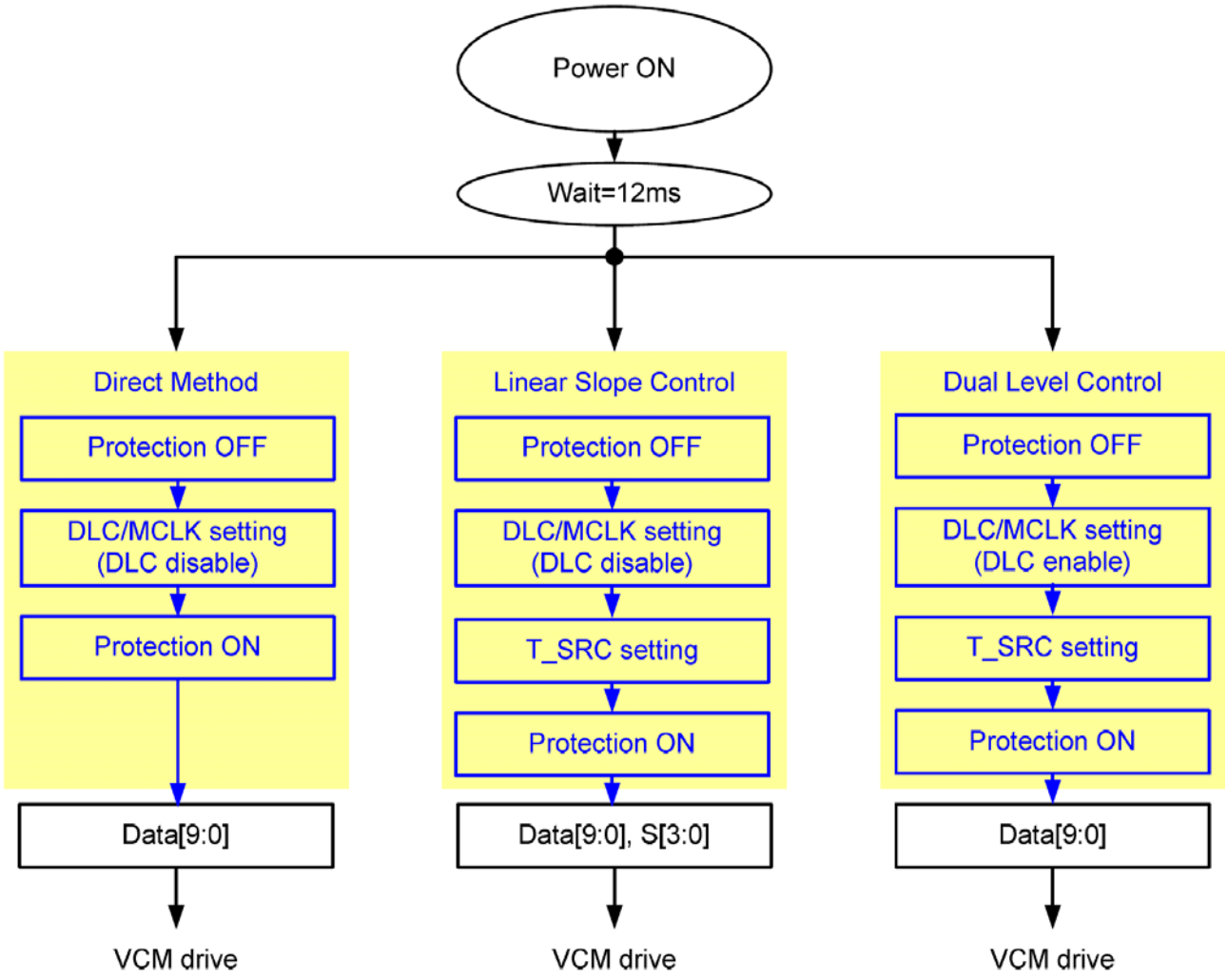
S[3:2]	Codes per step
00	0(no SRC)-direct driving
01	1
10	2
11	4

S[1:0]: Step period is determined by S[1:0] and T_SRC[4:0] for “Linear slope control”

S[1:0]	Period [us]
00	Refer “Linear slop control”
01	Refer “Linear slop control”
10	Refer “Linear slop control”
11	Refer “Linear slop control”

Slew Rate Control Set up Method

Driving mode-Direct, Linear Slope Control, Dual Level Control



※ When you use direct mode after power on, you don't need register set. Because, DLC disable is default.

Direct mode Control set up method

Protection off

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

DLC and MCLK[1:0] setting

Byte1 (0xA1)								Byte2 (*)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC=0	1	MCLK1	MCLK0

※(*)default:0x05

DLC: Dual-level control mode

1: Dual-level control mode (active high)

0: Direct and linear slope control

T_SRC[4:0] setting

Byte1 (0xF2)								Byte2 (*)							
1	1	1	1	0	0	1	0	T_SRC4	T_SRC4	T_SRC4	T_SRC4	T_SRC4	0	0	0

Protection on

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

∗When you use direct mode after power on, you don’t need register set. Because, DLC disable is default.

Linear Slope Control set up method

Protection off

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

DLC and MCLK[1:0] setting

Byte1 (0xA1)								Byte2 (*)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC=0	1	MCLK1	MCLK0

※(*)default:0x05

DLC: Dual-level control mode

1: Dual-level control mode (active high)

0: Direct and linear slope control

T_SRC[4:0] setting

Byte1 (0xF2)								Byte2 (*)							
1	1	1	1	0	0	1	0	T_SRC4	T_SRC4	T_SRC4	T_SRC4	T_SRC4	0	0	0

Protection on

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

Linear Slope Control – T_SRC[4:0] selection table

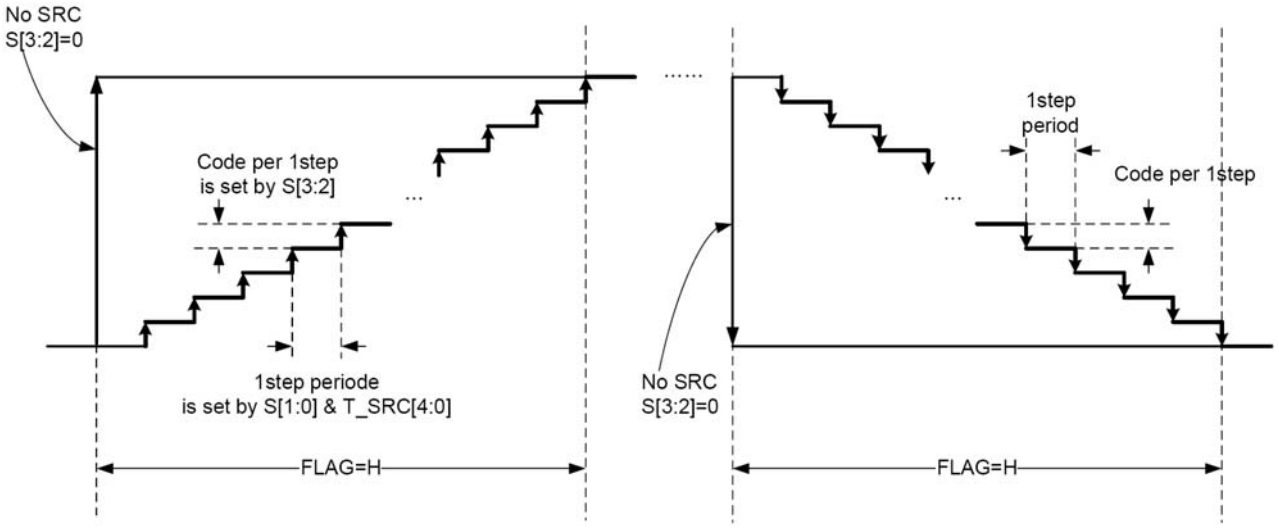
Linear Slope Control step period is set by S[1:0] and T_SRC[4:0]
T_SRC[4:0] = 00000(default),(*)MCLK[1:0] = 01(default)

Unit = μs

1 Step period				
T_SRC[4:0]	S[[1:0]			
	00	01	10	11
10000	136.0	272.0	544.0	1088.0
10001	130.0	260.0	520.0	1040.0
10010	125.0	250.0	500.0	1000.0
10011	120.0	240.0	480.0	960.0
10100	116.0	232.0	464.0	928.0
10101	112.0	224.0	448.0	896.0
10110	108.0	216.0	432.0	864.0
10111	104.0	208.0	416.0	832.0
11000	101.0	202.0	404.0	808.0
11001	98.0	196.0	392.0	784.0
11010	95.0	190.0	380.0	760.0
11011	92.0	184.0	368.0	736.0
11100	89.0	178.0	356.0	712.0
11101	87.0	174.0	348.0	696.0
11110	85.0	170.0	340.0	680.0
11111	83.0	166.0	332.0	664.0
00000 (default)	81.0	162.0	324.0	648.0
00001	79.0	158.0	316.0	632.0
00010	77.5	155.0	310.0	620.0
00011	76.0	152.0	304.0	608.0
00100	74.5	149.0	298.0	596.0
00101	73.0	146.0	292.0	584.0
00110	71.5	143.0	286.0	572.0
00111	70.0	140.0	280.0	560.0
01000	69.0	138.0	276.0	552.0
01001	68.0	136.0	272.0	544.0
01010	67.0	134.0	268.0	536.0
01011	66.0	132.0	264.0	528.0
01100	65.5	131.0	262.0	524.0
01101	65.0	130.0	260.0	520.0
01110	64.5	129.0	258.0	516.0
01111	64.0	128.0	256.0	512.0

※ (*) MCLK[1:0] = 00 : double 01 :X1 (default) 10 : half 11 : quarter

Linear slope control scheme



Dual Level Control set up method

Protection off

Byte1 (0xEC)								Byte2 (0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

DLC and MCLK[1:0] setting

Byte1 (0xA1)								Byte2 (*)							
1	0	1	0	0	0	0	1	0	0	0	0	DLC=0	1	MCLK1	MCLK0

※(*)default:0x05

DLC: Dual-level control mode

1: Dual-level control mode (active high)

0: Normal operation mode

T_SRC[4:0] setting

Byte1 (0xF2)								Byte2 (*)							
1	1	1	1	0	0	1	0	T_SRC4	T_SRC4	T_SRC4	T_SRC4	T_SRC4	0	0	0

Protection on

Byte1 (0xDC)								Byte2 (0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

Dual Level Control (DLC) – T_SRC[4:0] & MCLK[1:0] selection table

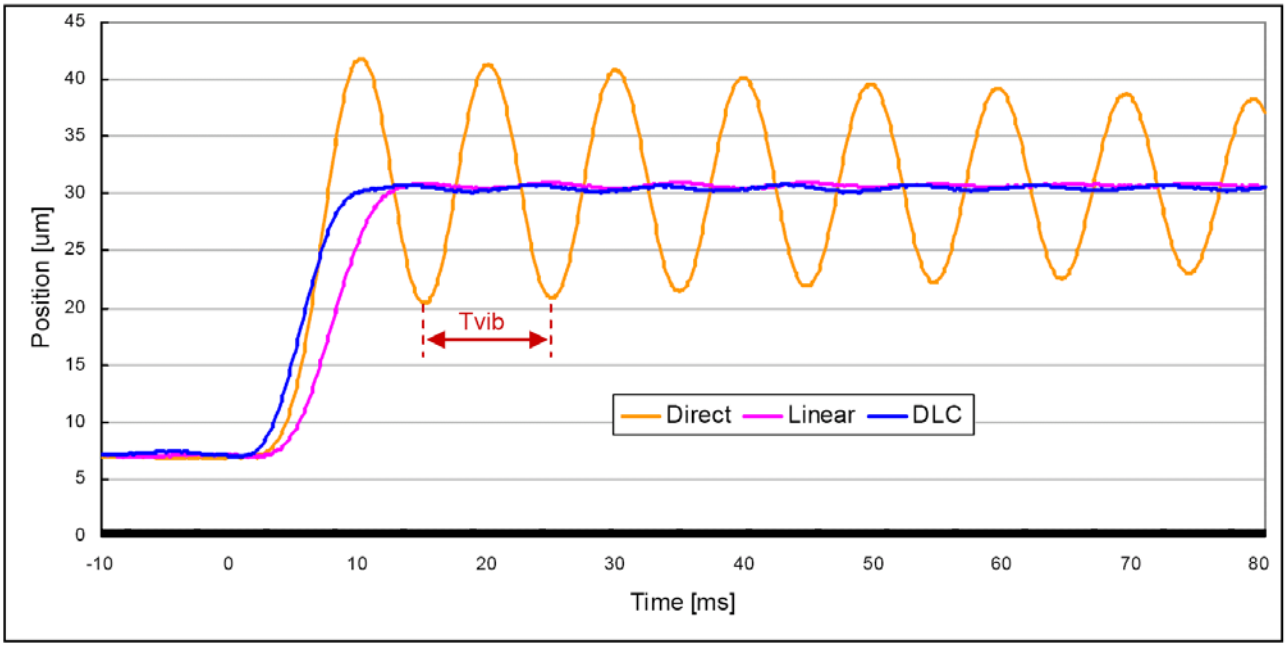
DLC step period is set by MCLK[1:0] and T_SRC[4:0],
MCLK[1:0] default value is 2'b=01 and T_SRC[4:0] default value is 5'b=00000.
Recommended that DLC step period is set Tvib/2 (Tvib=VCM vibration period)

Unit = ms

Tvib/2				
T_SRC[4:0]	MCLK[1:0]			
	00	01	10	11
10000	21.25	10.63	5.31	2.66
10001	20.31	10.16	5.08	2.54
10010	19.53	9.77	4.88	2.44
10011	18.75	9.38	4.69	2.34
10100	18.13	9.06	4.53	2.27
10101	17.50	8.75	4.38	2.19
10110	16.88	8.44	4.22	2.11
10111	16.25	8.13	4.06	2.03
11000	15.78	7.89	3.95	1.97
11001	15.31	7.66	3.83	1.91
11010	14.84	7.42	3.71	1.86
11011	14.38	7.19	3.59	1.80
11100	13.91	6.95	3.48	1.74
11101	13.59	6.80	3.40	1.70
11110	13.28	6.64	3.32	1.66
11111	12.97	6.48	3.24	1.62
00000 (default)	12.66	6.33	3.16	1.58
00001	12.34	6.17	3.09	1.54
00010	12.11	6.05	3.03	1.51
00011	11.88	5.94	2.97	1.48
00100	11.64	5.82	2.91	1.46
00101	11.41	5.70	2.85	1.43
00110	11.17	5.59	2.79	1.40
00111	10.94	5.47	2.73	1.37
01000	10.78	5.39	2.70	1.35
01001	10.63	5.31	2.66	1.33
01010	10.47	5.23	2.62	1.31
01011	10.31	5.16	2.58	1.29
01100	10.23	5.12	2.56	1.28
01101	10.16	5.08	2.54	1.27
01110	10.08	5.04	2.52	1.26
01111	10.00	5.00	2.50	1.25

※ (*) MCLK[1:0] = 00 : double 01 :X1 (default) 10 : half 11 : quarter

SRC Test Results-Comparison of Direct, Linear slope control, and Dual level control

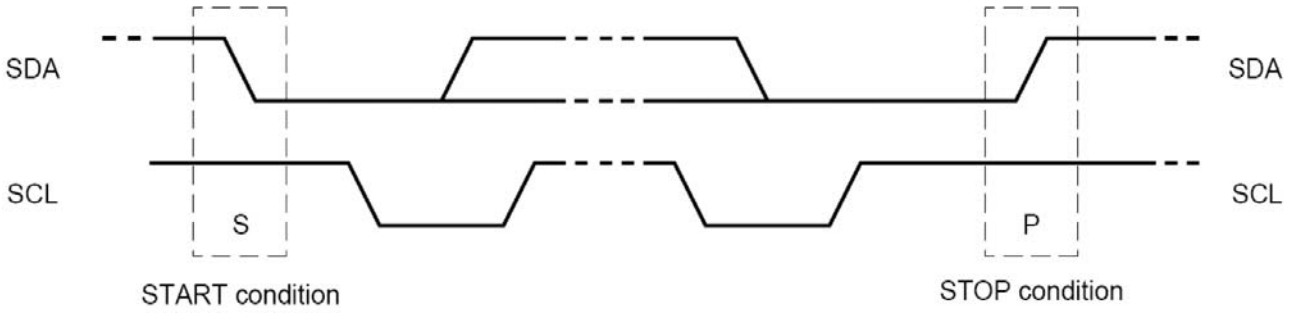


※ Tvib: Vibration period of the VCM

DLC rising time=Tvib/2
Linear rising time=Tvib

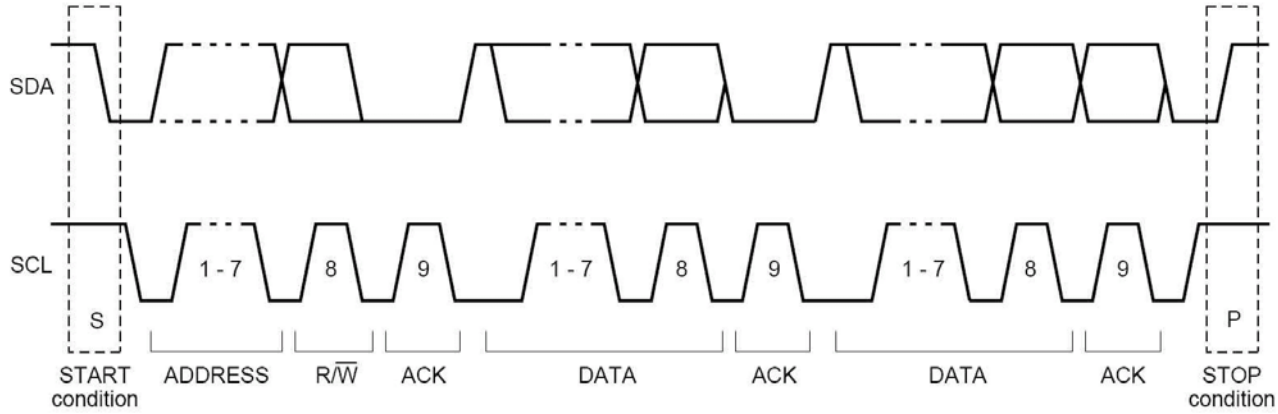
I2C Protocol

Start and Stop condition



Within the procedure of the I2C-bus, unique situations arise which are defined as START (S) and STOP (P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

Complete I2C Data Transfer



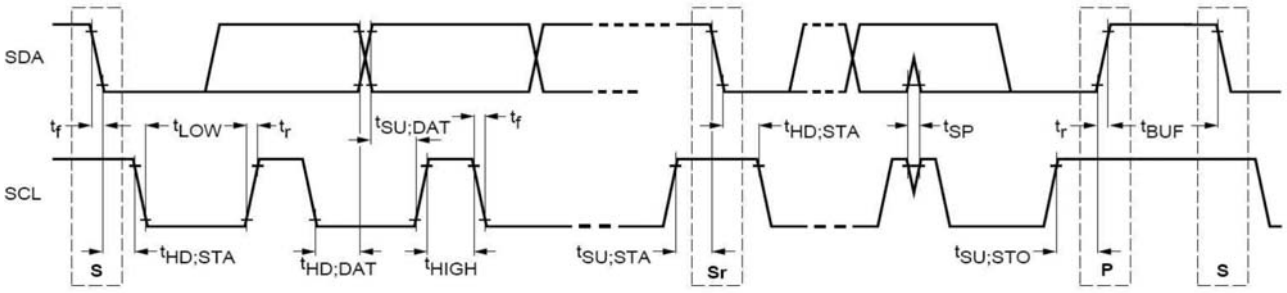
Data transfers follow the format. After the START condition (S), a slave address is sent. A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated.

I²C Timing

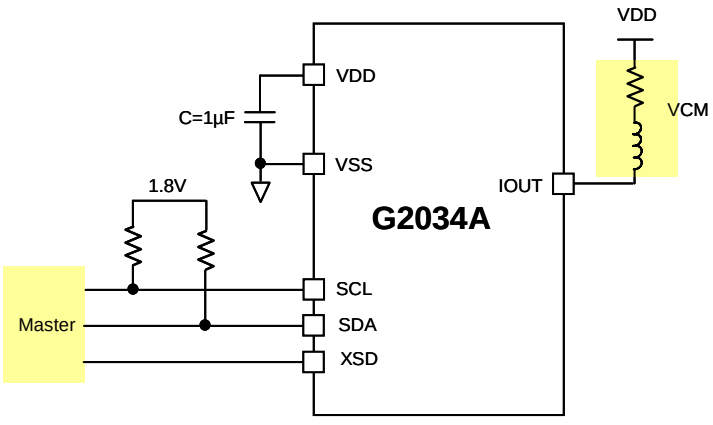
PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition.	$t_{HD;STA}$	0.6	---	µs
Low period of the SCL clock	t_{LOW}	1.3	---	µs
High period of the SCL clock	t_{HIGH}	0.6	---	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	---	µs
Data hold time	$t_{HD;DAT}$(1)	---	0.9	µs
Data set-up time	$t_{SU;DA}T$	100	---	ns
Rise time of both SDA and SCL signals	t_r	$20+0.1C_b$(2)	300	ns
Fall time of both SDA and SCL signals	t_f	$20+0.1C_b$(2)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	---	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	---	µs
Capacitive load for each bus line	C_b	---	400	pF
Pulse width of spike suppress	t_{SP}	0	50	ns

(1) A master device must provide a hold time of at least 100ns for the SDA signal to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

(2) C_b is the total capacitance of one bus line in pF, tr and tf are measured between $0.3V_{DD}$ to $0.7V_{DD}$.

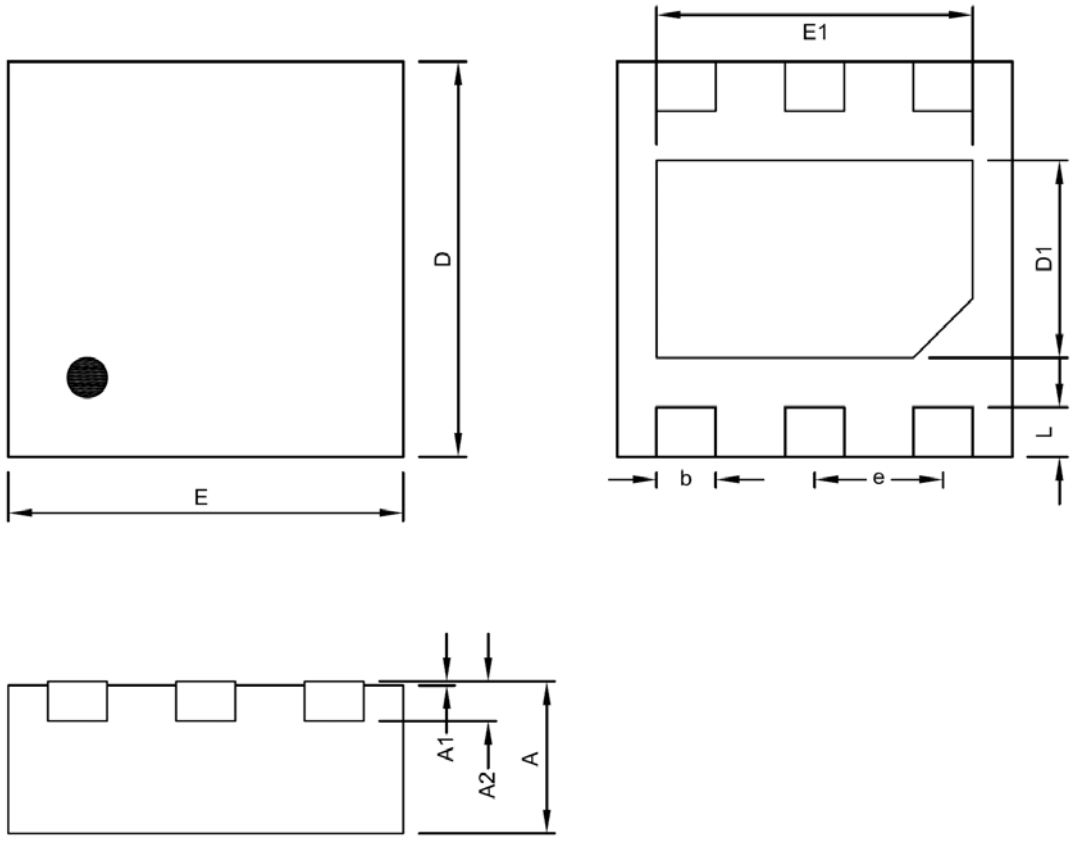


Typical Application Circuit



※ XSD can be connected to VDD

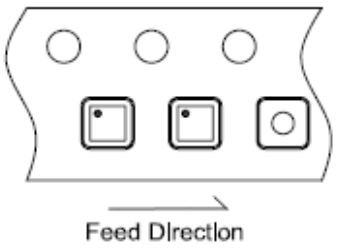
Package Information



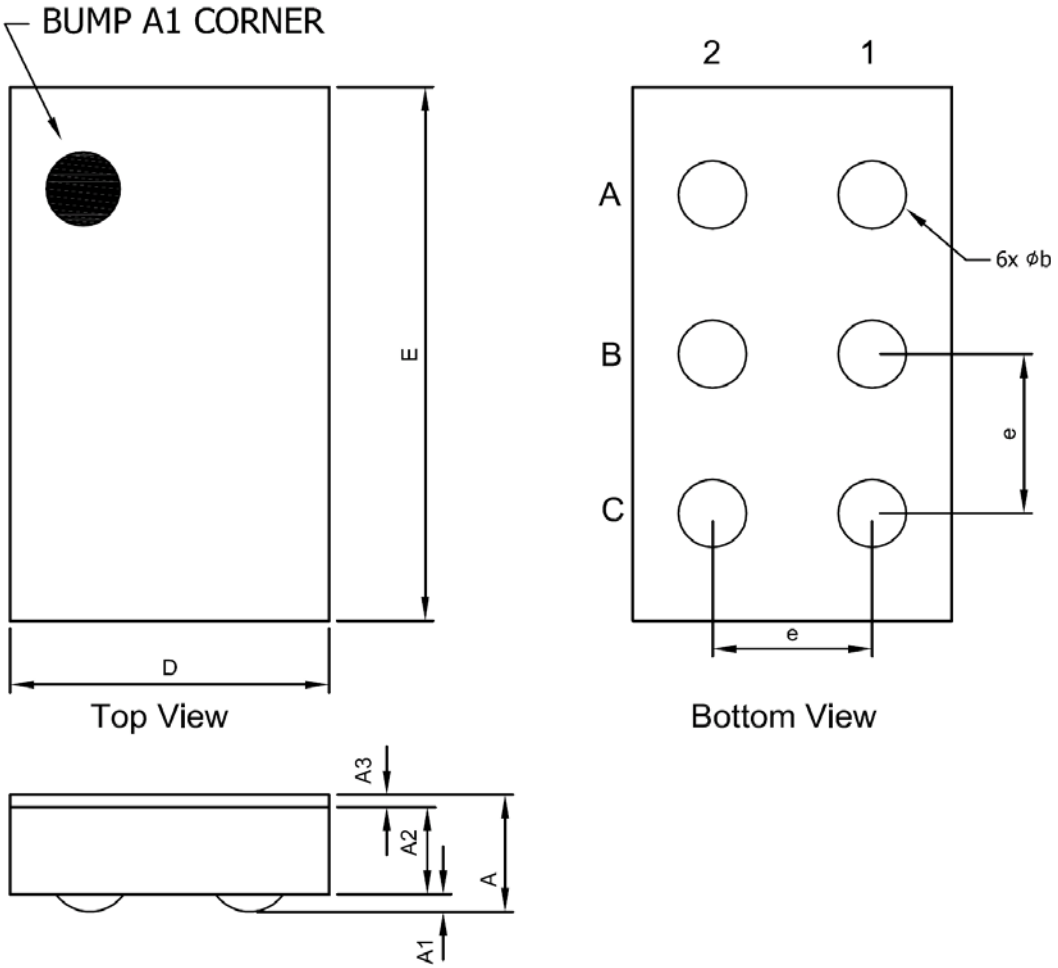
TDFN2X2-6 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D1	0.90	1.00	1.10	0.0354	0.0394	0.0433
E1	1.50	1.60	1.65	0.0591	0.0630	0.0650
b	0.25	0.30	0.35	0.0098	0.0118	0.0138
e	0.65 BSC			0.0256 BSC		
L	0.20	0.25	0.30	0.0079	0.0098	0.0118

Taping Specification



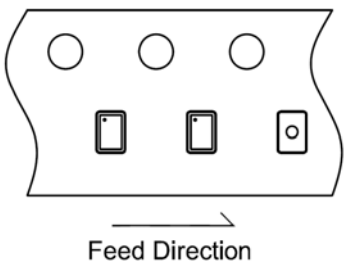
PACKAGE	Q'TY/REEL
TDFN2X2-6	3,000 ea



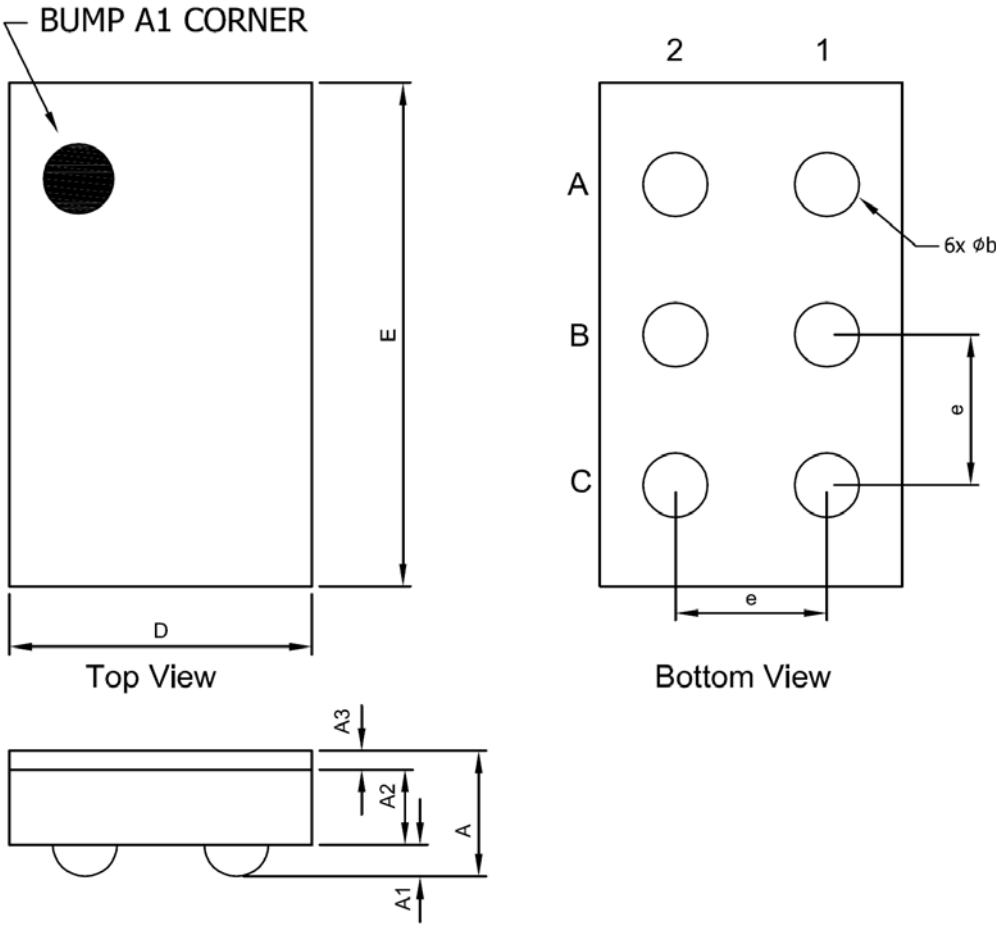
WLCSP2X3-6 (G21) Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.270	0.300	0.330	0.0106	0.0118	0.0130
A1	0.020	0.025	0.030	0.0008	0.0010	0.0012
A2	0.230	0.250	0.270	0.0091	0.0098	0.0106
A3	0.020	0.025	0.030	0.0008	0.0010	0.0012
D	0.720	0.760	0.800	0.0283	0.0299	0.0315
E	1.120	1.160	1.200	0.0441	0.0457	0.0472
b	0.185	0.200	0.215	0.0073	0.0079	0.0085
e	0.40 BSC			0.0157 BSC		

Taping Specification



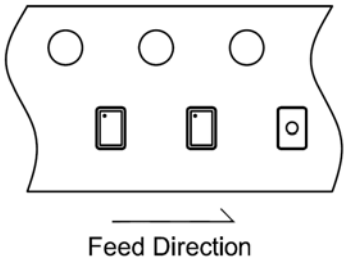
PACKAGE	Q'TY/REEL
WLCSP2X3-6	3,000 ea



WLCSP2X3-6 Package (G22)

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.270	0.300	0.330	0.0106	0.0118	0.0130
A1	0.045	0.055	0.065	0.0018	0.0022	0.0026
A2	0.205	0.220	0.235	0.0080	0.0087	0.0093
A3	0.020	0.025	0.030	0.0008	0.0010	0.0012
D	0.720	0.760	0.800	0.0283	0.0299	0.0315
E	1.120	1.160	1.200	0.0441	0.0457	0.0472
b	0.185	0.200	0.215	0.0073	0.0079	0.0085
e	0.40 BSC			0.0157 BSC		

Taping Specification



PACKAGE	Q'TY/REEL
WLCSP2X3-6	3,000 ea

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