DESCRIPTION

The 11N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

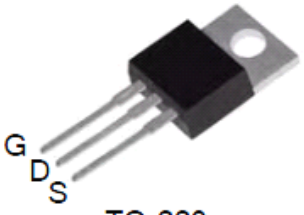
V_{DSS}	$R_{DS(ON)}$	I_D
100V	7.8mΩ	110A

GENERAL FEATURES

- VDS =100V,ID =110A

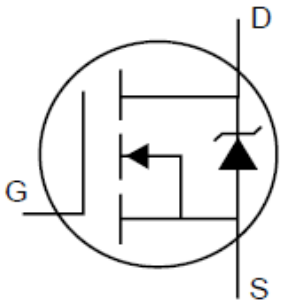
  RDS(ON) < 9mΩ @ VGS=10V

- High density cell design for ultra low Rdson.
- Fully characterized avalanche voltage and current.
- Good stability and uniformity with high EAS .
- Excellent package for good heat dissipation .
- Special process technology for high ESD capability



TO-220
Not to Scale

G06NP06DS2



Applications

- Power switching application.
- Hard switched and high frequency circuits.
- Uninterruptible power supply.

Ordering Information

PART NUMBER	PACKAGE	BRAND
11N10	TO-220	0GFD

Absolute Maximum Ratings (TC=25℃, unless otherwise noted)

Symbol	Parameter	11N10	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current	110	A
ID (100℃)	Drain Current-Continuous(TC=100℃)	78	
I_{DM}	Pulsed Drain Current@VG=10V	440	
P_D	Power Dissipation	220	W
	Derating Factor above 25℃	1.47	W/℃
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single PulseAvalanche Energy	1100	mJ
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 175	℃

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	--	--	0.68	℃/W	Water cooled heatsink, PD adjusted for a peak junction temperature of +175℃.
$R_{\theta JA}$	Junction-to-Ambient	--	--	--		1 cubic foot chamber, free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
B_{VDSS}	Drain-to-Source Breakdown Voltage	100	113	--	V	V_{GS}=0, I_D=250uA
I_{GSS}	Gate-to-Source Forward Leakage	--	--	±100	nA	V_{DS}=0V, V_{GS}=±20V
I_{DSS}	Zero Gate Voltage Drain Current	--	--	1	uA	V_{DS}=100V, V_{GS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	7.8	9	mΩ	V_{GS}=10V,I_D=40A
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	2	3	4	V	V_{DS}=10V, I_D=250uA
G_{fs}	Forward Transconductance	90	---	--	S	V_{DS}=25V, I_D=57A

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	6500	--	pF	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ
C_{oss}	Output Capacitance	--	380	--		
C_{rss}	Reverse Transfer Capacitance	--	330	--		
Q_g	Total Gate Charge	--	163	--	nC	V_{DS}=30V, V_{GS}=10V, I_D=30A
Q_{gs}	Gate-to-Source Charge	--	31	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	64	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$T_{d(ON)}$	Turn-on Delay Time		26		ns	VDD=30V,ID=2A RL=15Ω VGS=10V,RG=2.5Ω
T_{rise}	Rise Time		24			
$T_{d(OFF)}$	Turn-Off Delay Time		91			
T_{fall}	Fall Time		39			

Drain-Source Diode Characteristics

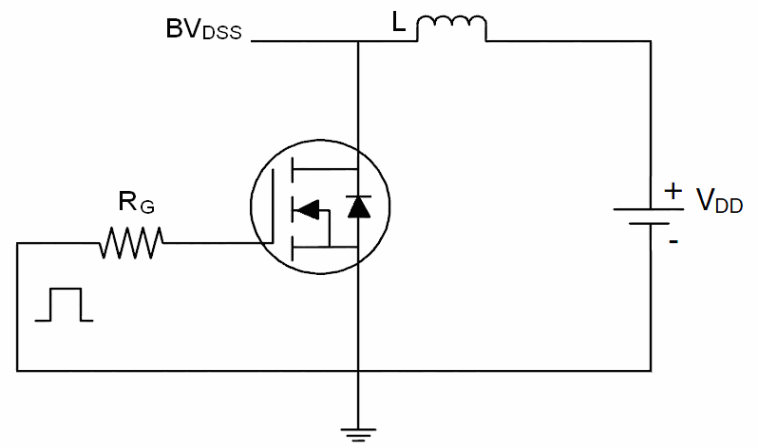
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=40A	--	--	1.2	V	
Diode Forward Current	I_S	--	--	--	110	A	
Reverse Recovery Time	t_{rr}	TJ=25℃,IF=40A Di/dt = 100 A/μs	--	42	--	nS	
Reverse Recovery Charge	Q_{rr}		--	66	--	nC	
Forword Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD					

Notes:

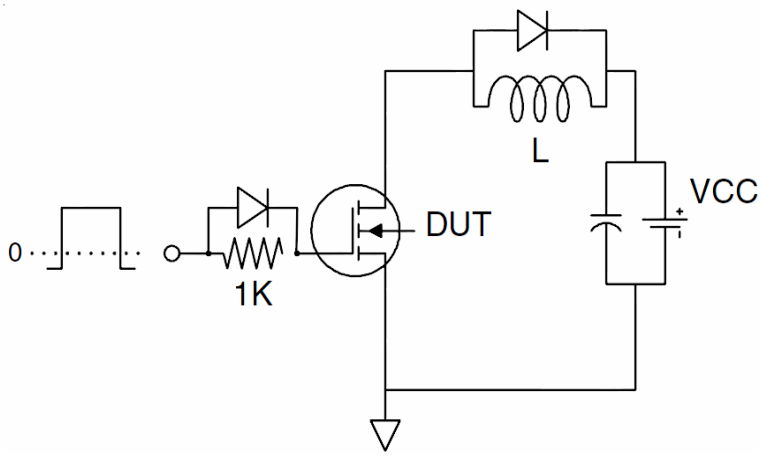
1. Repetitive Rating:Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤10 sec.
3. Pulse Test:Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production.
5. EAS condition：Tj=25℃,VDD=50V,VG=10V,L=0.5mH,Rg=25Ω

Test circuit

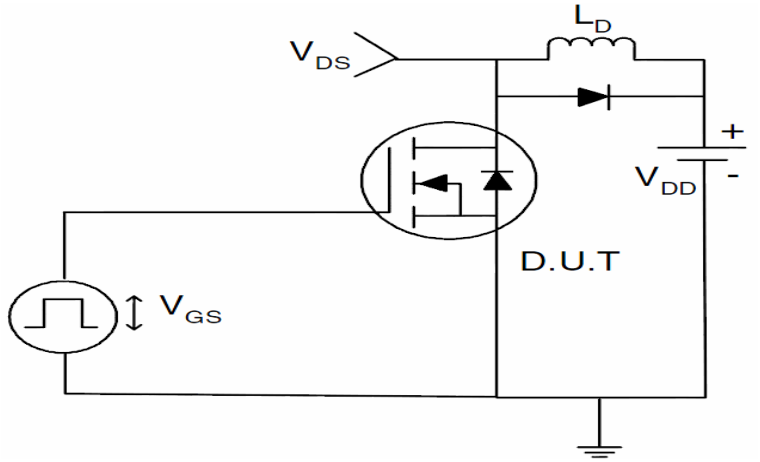
1）E_{AS} test Circuits



2）Gate charge test Circuit:



3）Switch Time Test Circuit：



Typical Electrical and Thermal Characteristics

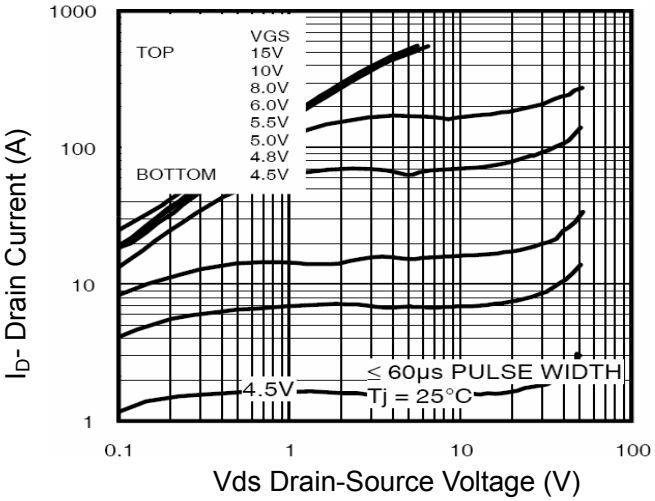


Figure 1 Output Characteristics

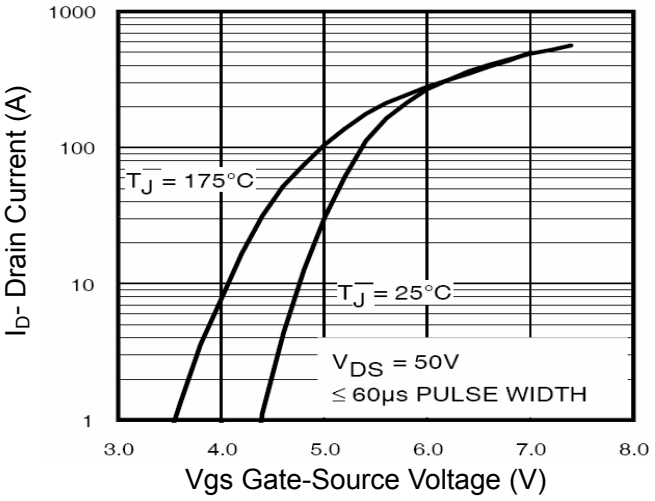


Figure 2 Transfer Characteristics

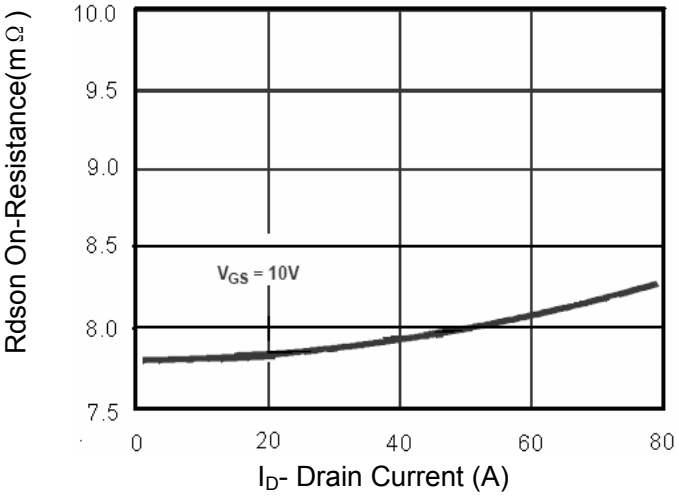


Figure 3 Rdson- Drain Current

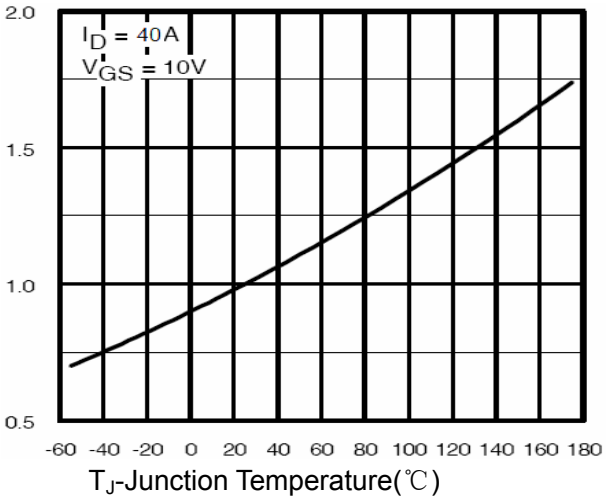


Figure 4 Rdson-JunctionTemperature

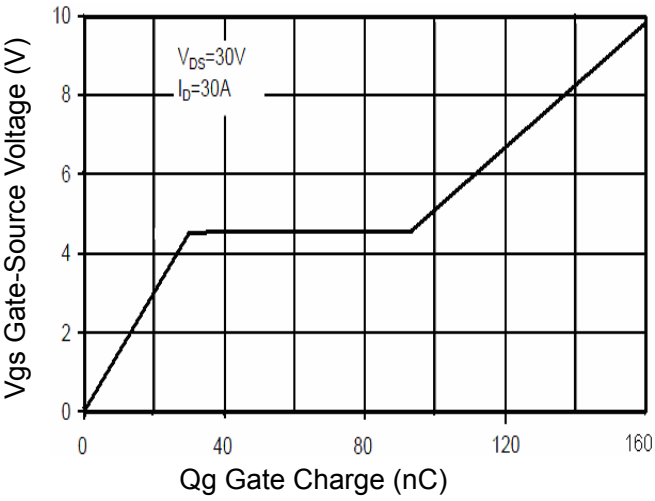


Figure 5 Gate Charge

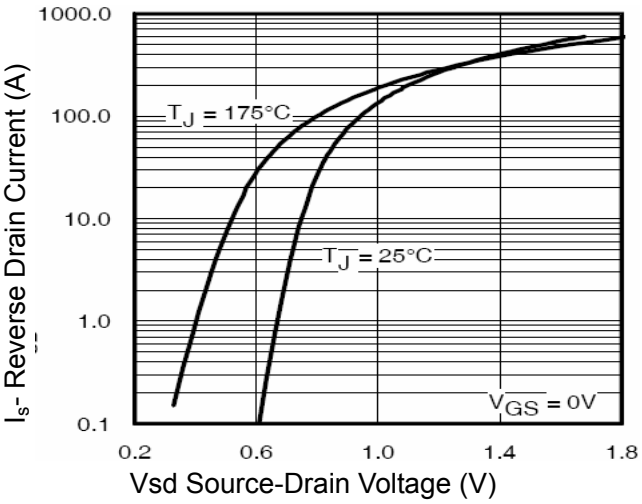


Figure 6 Source- Drain Diode Forward

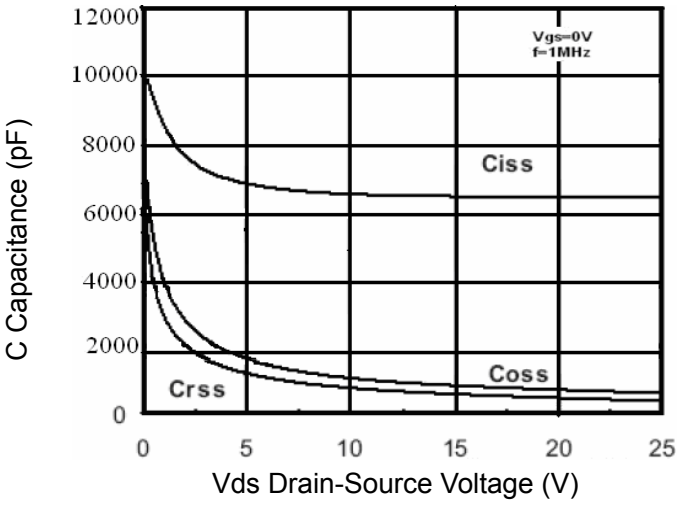


Figure 7 Capacitance vs Vds

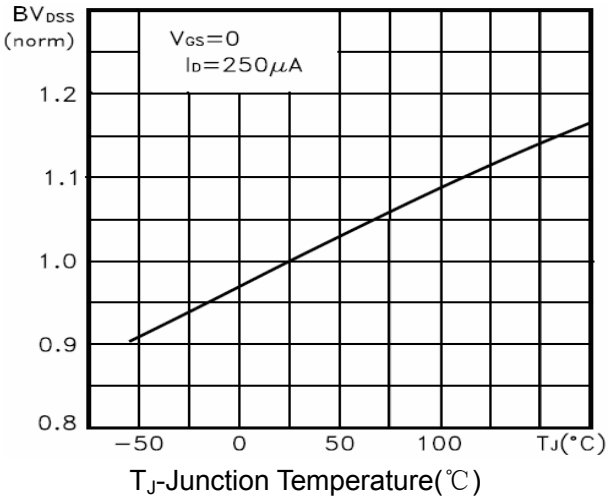


Figure 9 BV_{DSS} vs Junction Temperature

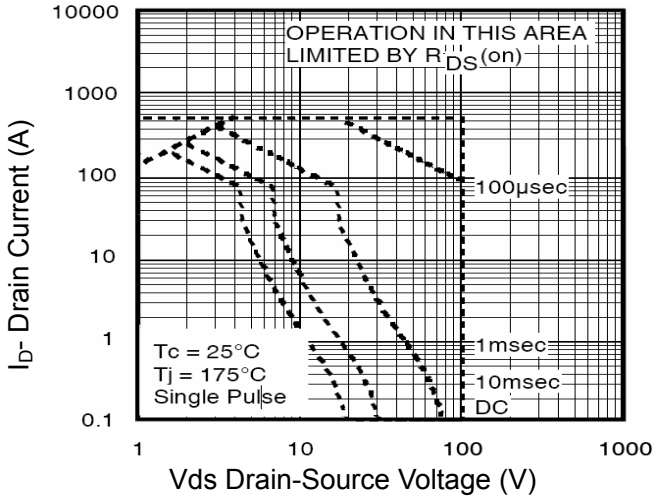


Figure 8 Safe Operation Area

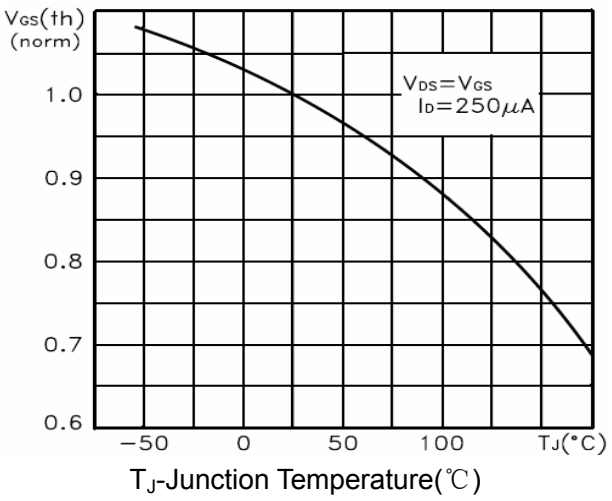


Figure 10 $V_{GS(th)}$ vs Junction Temperature

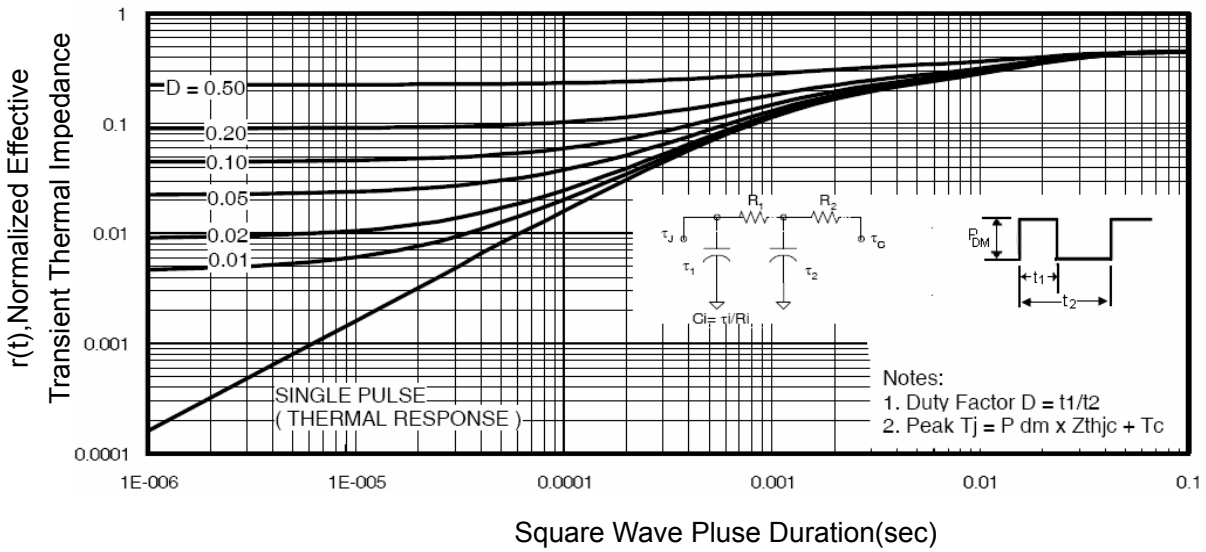


Figure 11 Normalized Maximum Transient Thermal Impedance

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