

Description

The 4402 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

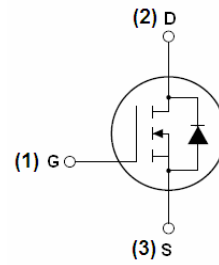
General Features

- | | | | |
|-----------|-----------------------------|-----------------------------|-------|
| V_{DSS} | $R_{DS(ON)}$
@ 4.5V(Typ) | $R_{DS(ON)}$
@ 2.5V(Typ) | I_D |
| 20V | 6.8m Ω | 8 m Ω | 30A |

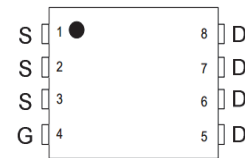
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

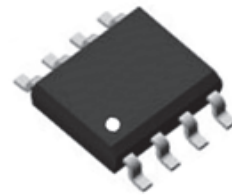
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic diagram



Marking and pin Assignment



SOP-8 top view

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	21	A
Pulsed Drain Current	I_{DM}	80	A
Maximum Power Dissipation	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	50	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

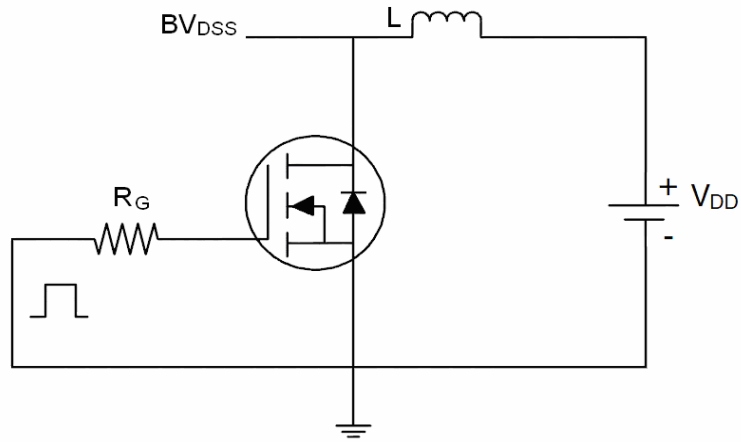
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	500	nA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.64	1	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=8A$	-	6.8	16	m Ω
		$V_{GS}=2.5V, I_D=6A$	-	8	25	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	26	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	938	-	PF
Output Capacitance	C_{oss}		-	142	-	PF
Reverse Transfer Capacitance	C_{rss}		-	99	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V, R_L=0.75\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	5	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	19	-	nS
Turn-Off Fall Time	t_f		-	6	-	nS
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=20A,$ $V_{GS}=10V$	-	17.5	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	nC
Gate-Drain Charge	Q_{gd}		-	4.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=1A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	30	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 20A$ $di/dt = 100A/\mu\text{s}$ ^(Note 3)	-	19	-	nS
Reverse Recovery Charge	Q_{rr}		-	10	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

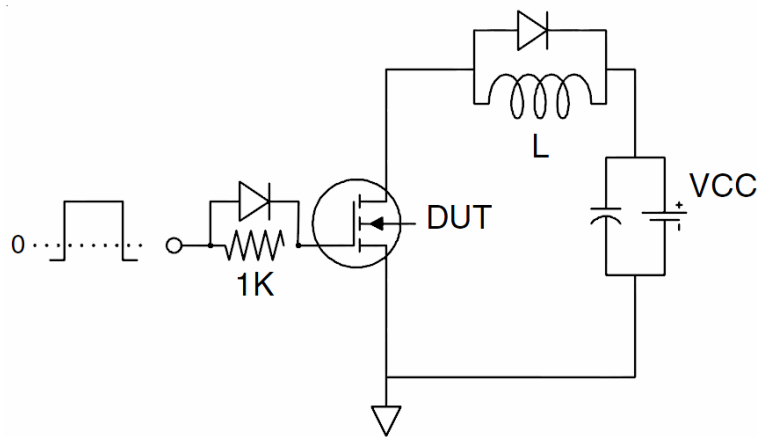
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test circuit

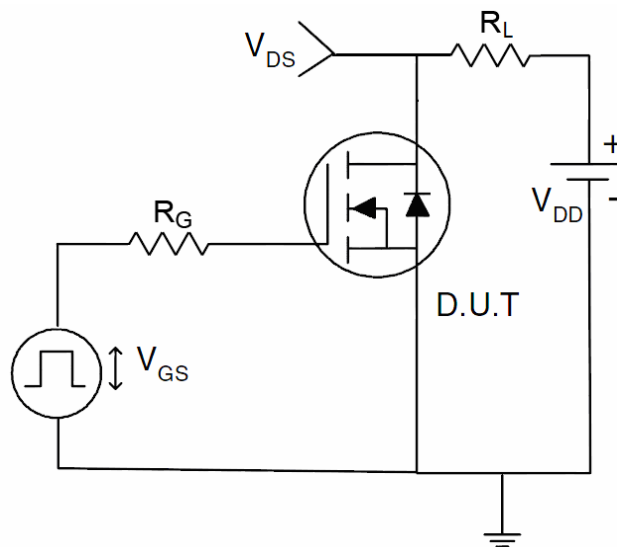
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

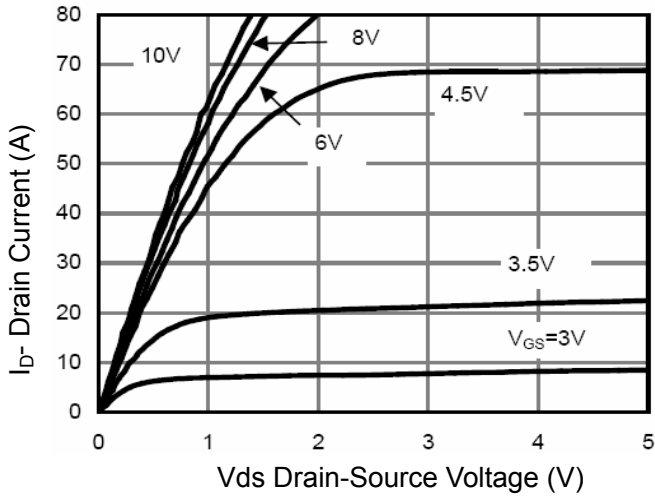


Figure 1 Output Characteristics

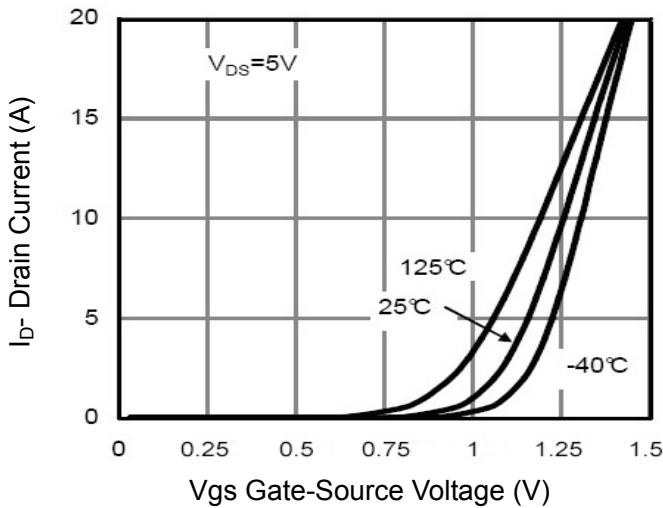


Figure 2 Transfer Characteristics

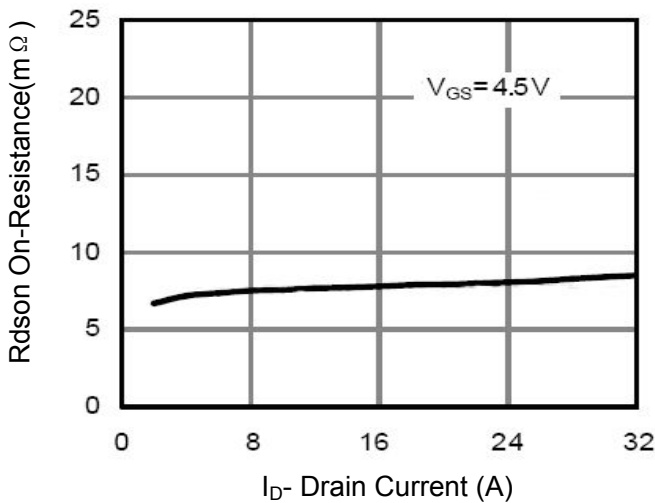


Figure 3 Rdson- Drain Current

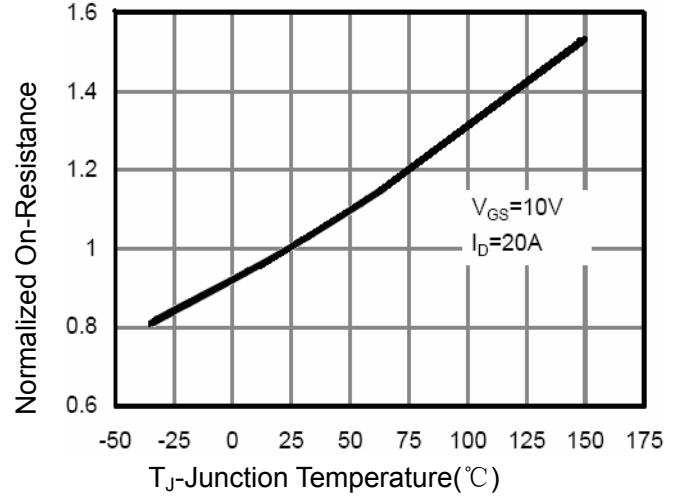


Figure 4 Rdson-Junction Temperature

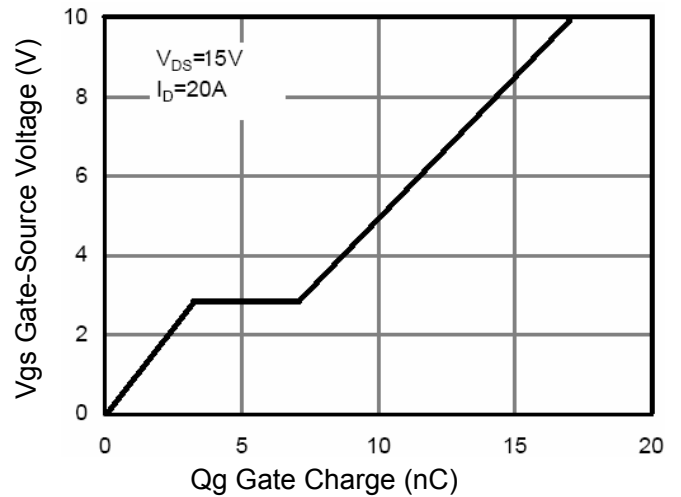


Figure 5 Gate Charge

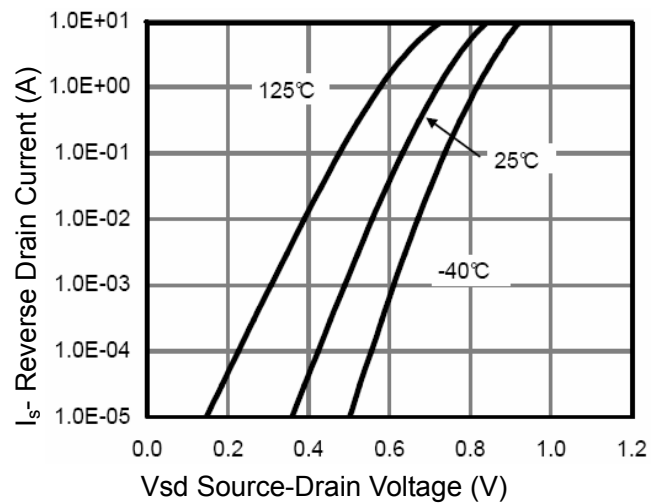


Figure 6 Source- Drain Diode Forward

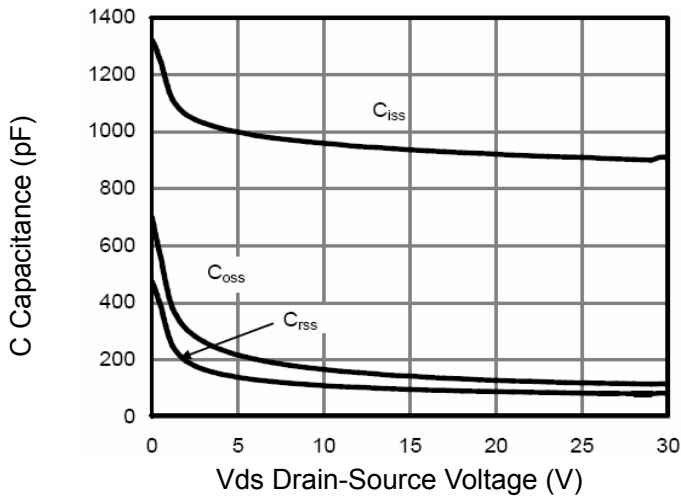


Figure 7 Capacitance vs Vds

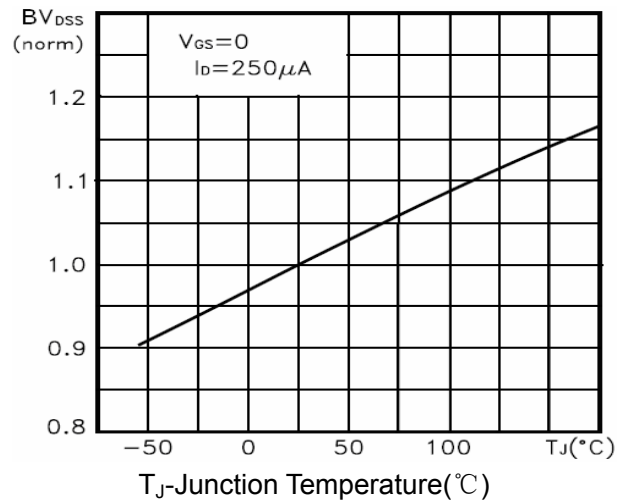


Figure 9 BV_{DSS} vs Junction Temperature

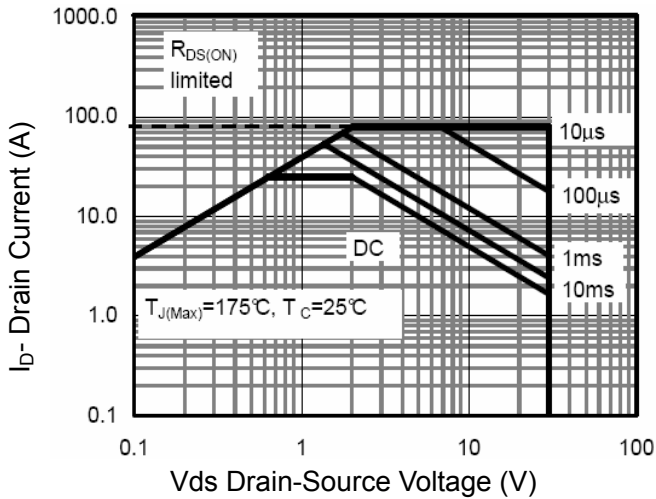


Figure 8 Safe Operation Area

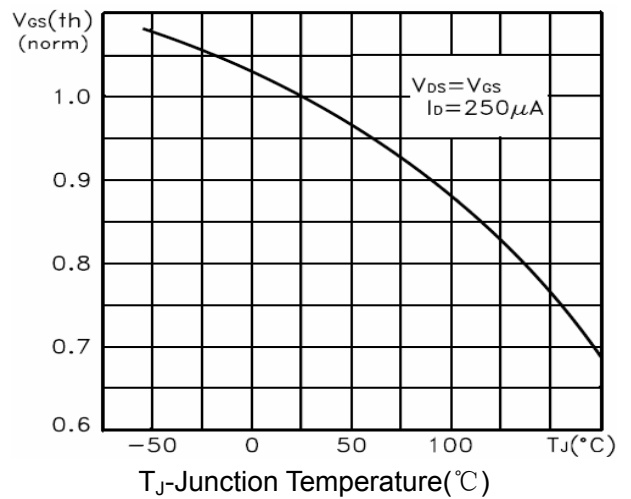


Figure 10 $V_{GS(th)}$ vs Junction Temperature

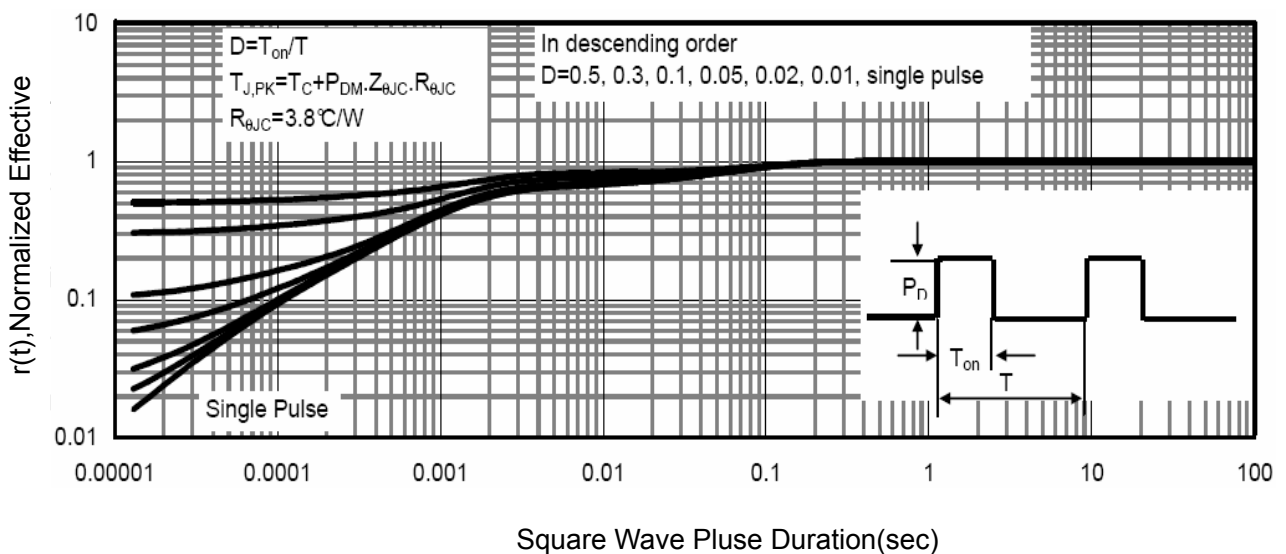
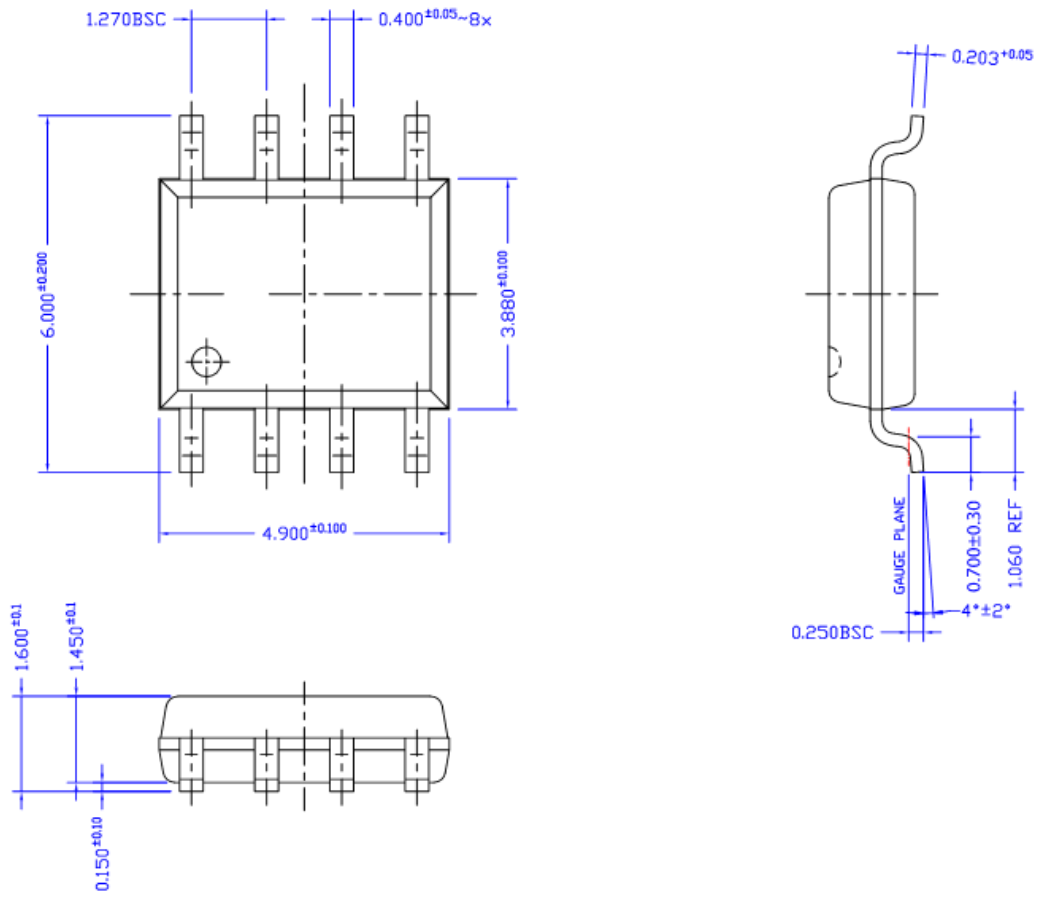


Figure 11 Normalized Maximum Transient Thermal Impedance



subject to real sample

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