

General Description

The 8680A is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching especially for E-Bike controller applications.

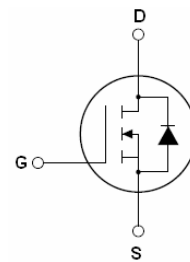
Features

VDSS	RDS(ON) @10V (typ)	ID
80V	6.6 mΩ	92A

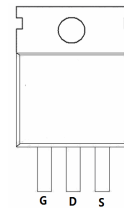
- Special Designed for E-Bike Controller Application
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- 64V E-Bike Controller Applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic Diagram



Marking and pin assignment



To-220 Top View

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
8680A	8680A	TO-220	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	80	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	±25	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	92	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	64.4	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	368	A
dv/dt	Peak Diode Recovery Voltage	30	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	139	W
	Derating Factor	0.93	W/°C
EAS	Single Pulse Avalanche Energy (Note 2)	625	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=40V, V_G=10V, R_G=25\Omega$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	1.08	°C/W

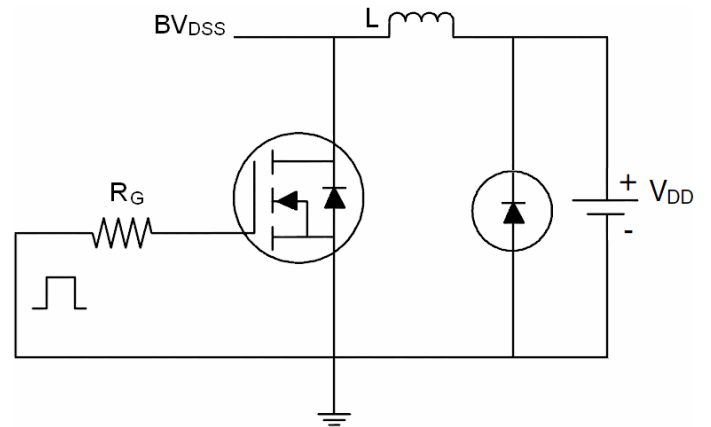
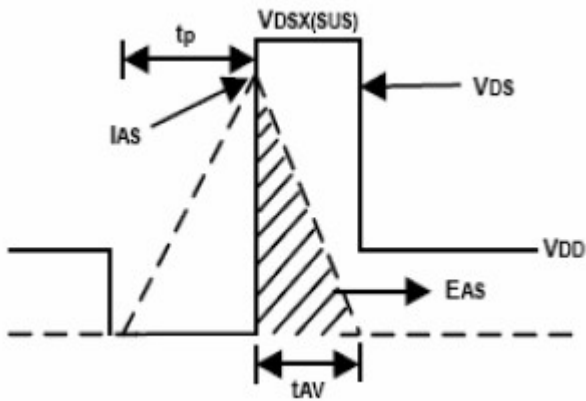
Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	82			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25°C)	V _{DS} =82V, V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=125°C)	V _{DS} =82V, V _{GS} =0V			10	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2	2.8	4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		6.6	7.8	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =15A	20			S
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		5053		PF
C _{oss}	Output Capacitance			442		PF
C _{rss}	Reverse Transfer Capacitance			145		PF
Q _g	Total Gate Charge	V _{DS} =50V, I _D =40A, V _{GS} =10V		106		nC
Q _{gs}	Gate-Source Charge			19		nC
Q _{gd}	Gate-Drain Charge			47.9		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =40A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω		15		nS
t _r	Turn-on Rise Time			18		nS
t _{d(off)}	Turn-Off Delay Time			31		nS
t _f	Turn-Off Fall Time			38		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-drain Current(Body Diode)			92		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			368		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25°C, I _{SD} =40A, V _{GS} =0V		0.78	0.95	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25°C, I _F =75A di/dt=100A/μs		56		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			113		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

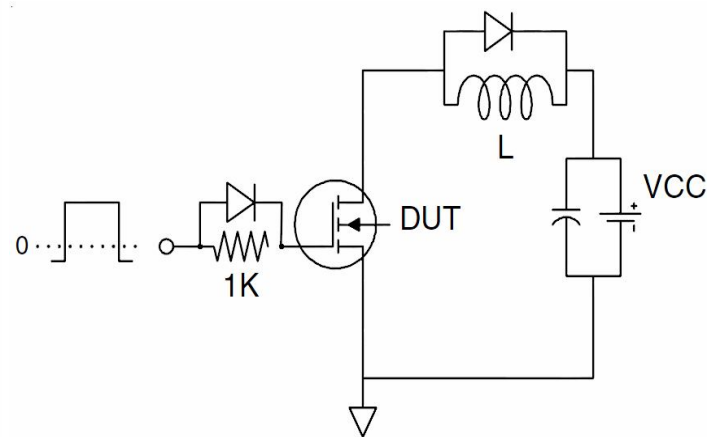
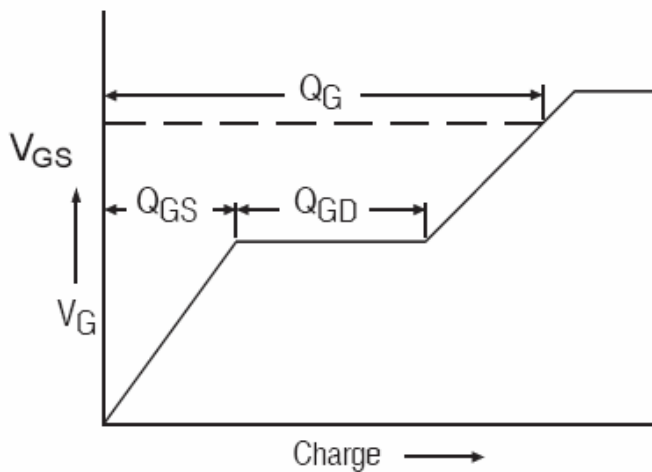
Notes 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting T_J=25°C

Test Circuit

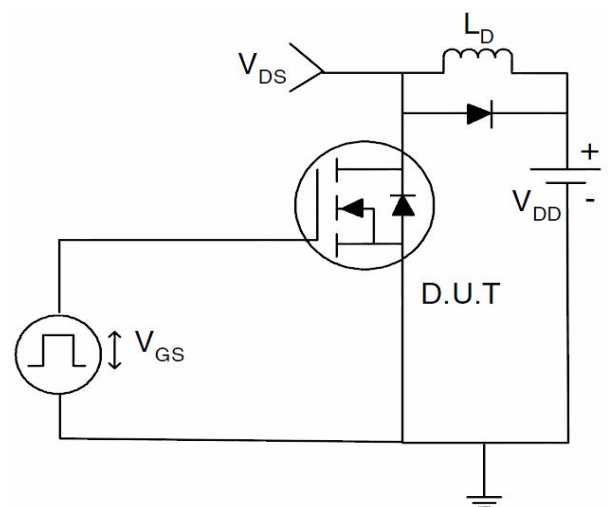
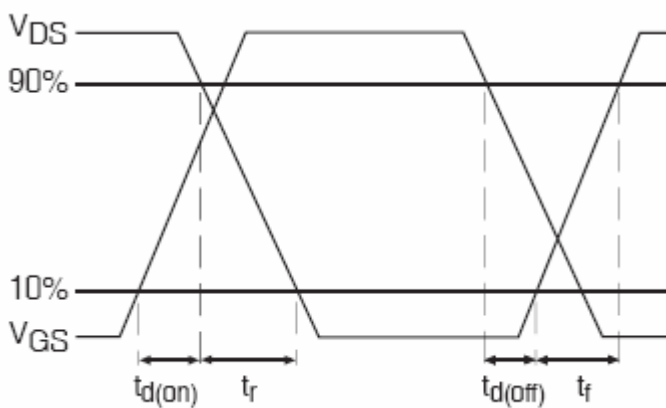
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

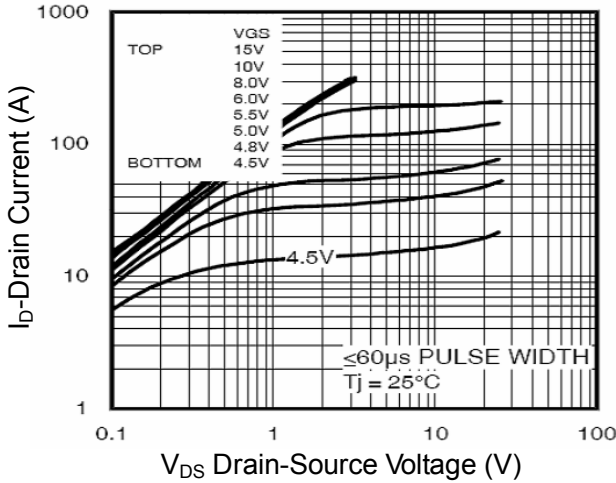


Figure2. Transfer Characteristics

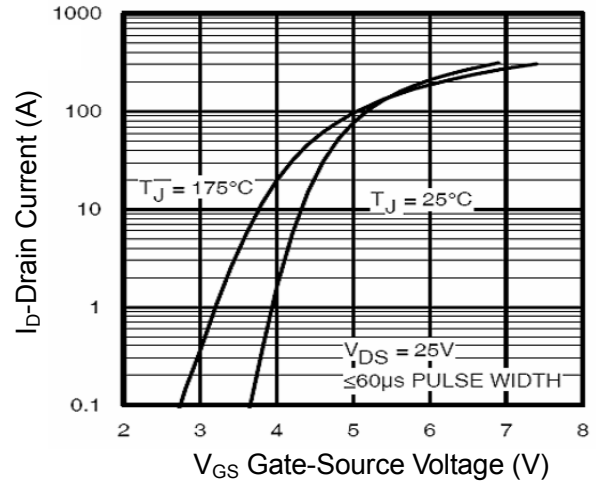


Figure3. Rdson Vs Drain Current

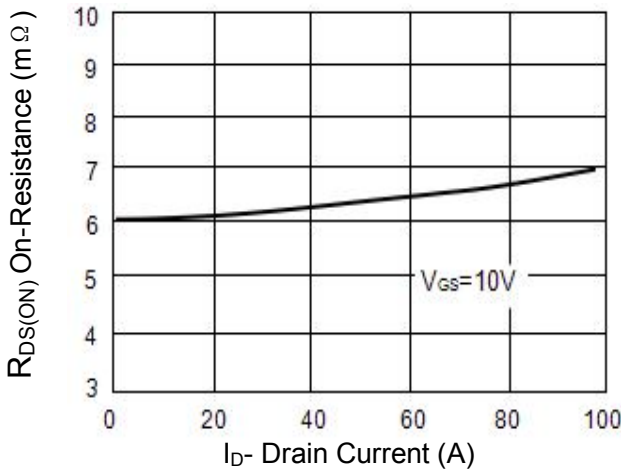


Figure4. Rdson Vs Junction Temperature

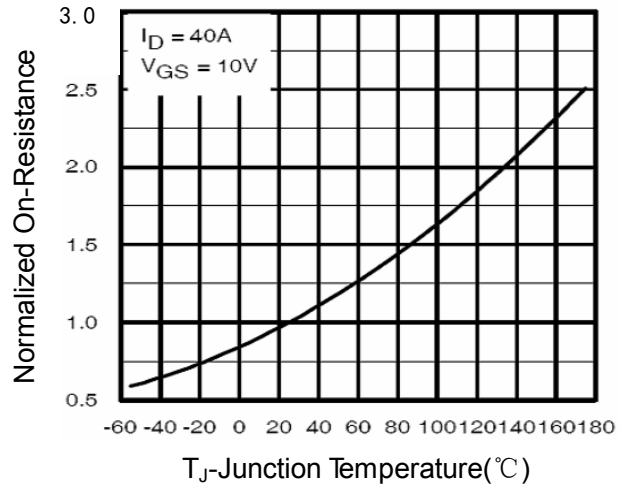


Figure5. Gate Charge

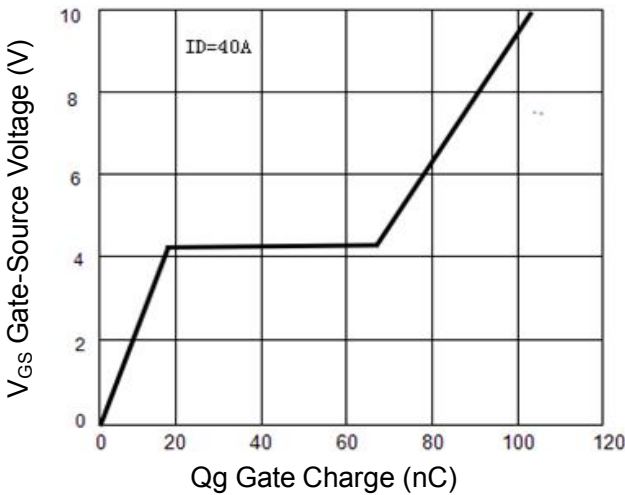


Figure6. Source- Drain Diode Forward

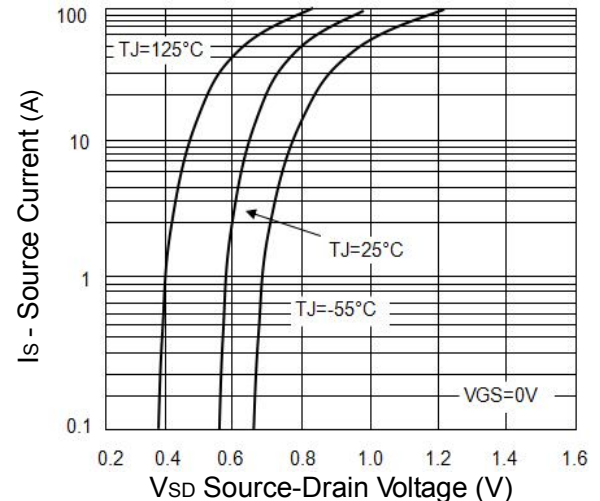


Figure7. Capacitance vs Vds

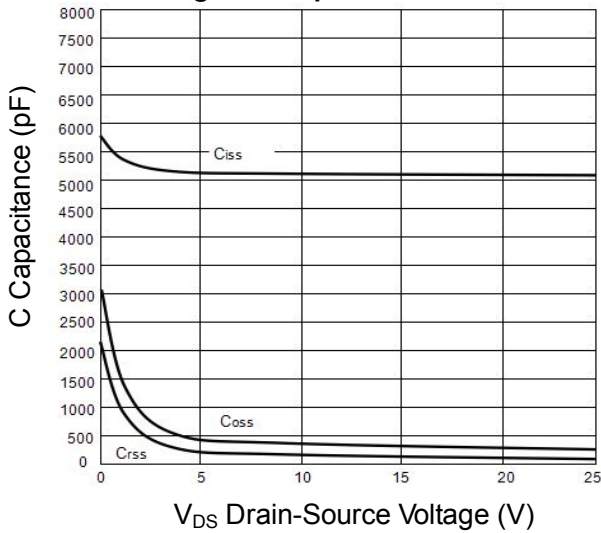


Figure8. Safe Operation Area

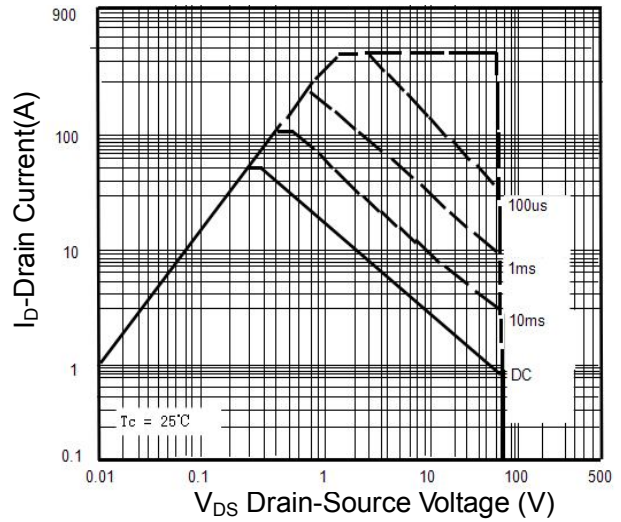


Figure9. BV DSS vs Junction Temperature

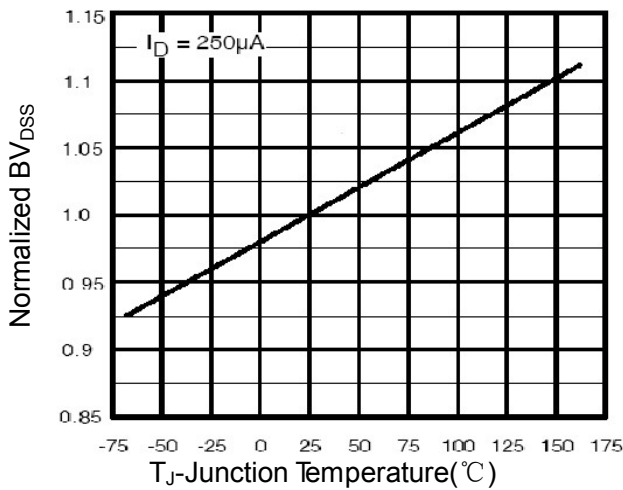


Figure10. VGS(th) vs Junction Temperature

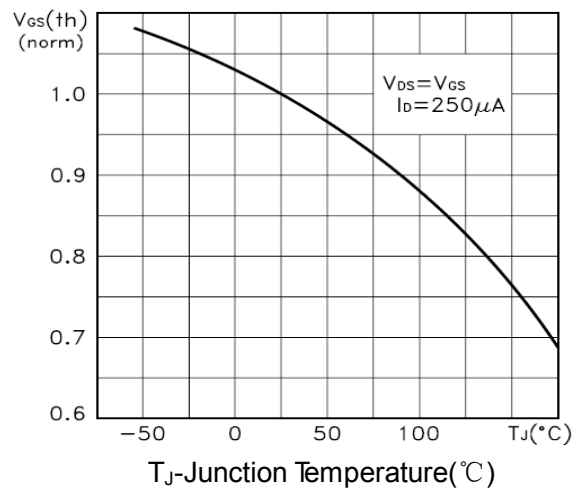
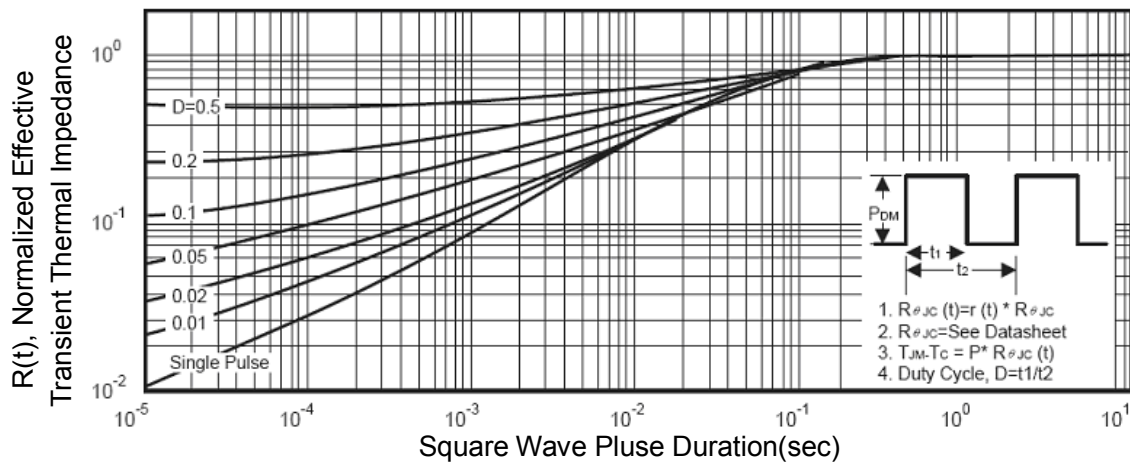


Figure11. Normalized Maximum Transient Thermal Impedance



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