

P-Channel Enhancement Mode Power MOSFET

Description

The G10P03 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

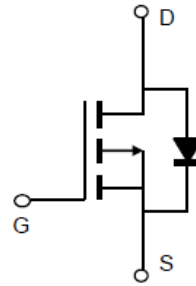
General Features

V_{DSS}	$R_{DS(ON)}$ @ -4.5V(Typ)	$R_{DS(ON)}$ @ -2.5V(Typ)	I_D
-30V	20 m Ω	28 m Ω	-10A

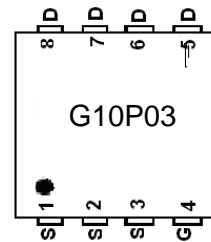
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability
- RoHS Compliant

Application

- SMPS and general purpose applications
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



DFN3X3-8L

Ordering Information

Part Number	Marking	Case	Packaging
G10P03	G10P03	DFN3*3-8L	3000pcs/Reel

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	-10	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	-7.5	A
Pulsed Drain Current	I_{DM}	-40	A
Maximum Power Dissipation	P_D	20	W
Derating factor		0.16	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	75	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	6.1	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

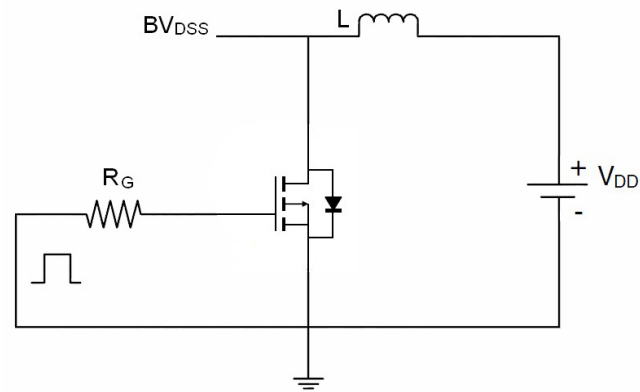
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.6	-0.9	-1.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-10A$	-	20	26	$m\Omega$
		$V_{GS}=-2.5V, I_D=-5A$	-	28	38	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=-15V, I_D=-10A$	10	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{ISS}	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0MHz$	-	1550	-	PF
Output Capacitance	C_{OSS}		-	260	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	190	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-1A,$ $V_{GS}=-4.5V, R_{GEN}=6\Omega$	-	10	-	nS
Turn-on Rise Time	t_r		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	110	-	nS
Turn-Off Fall Time	t_f		-	70	-	nS
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-10A$ $V_{GS}=-4.5V$	-	27	-	nC
Gate-Source Charge	Q_{gs}		-	6	-	nC
Gate-Drain Charge	Q_{gd}		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=-10A$	-	-0.87	-0.99	V
Diode Forward Current ^(Note 2)	I_S		-	-	-10	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = -10A$ $di/dt = 100A/\mu s$ (Note3)	-	23	33	nS
Reverse Recovery Charge	Q_{rr}		-	12	20	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

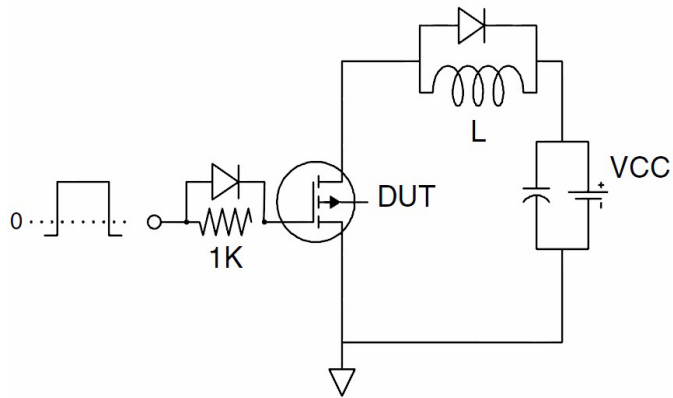
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ\text{C}, V_{DD}=-15V, V_G=-4.5V, L=0.5mH, R_g=25\Omega$

Test Circuit

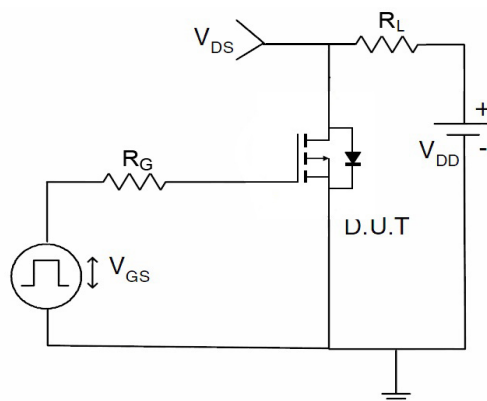
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

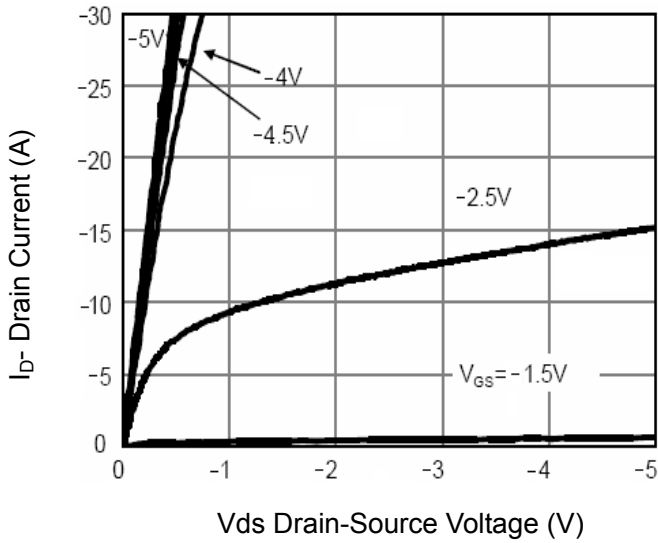


Figure 1 Output Characteristics

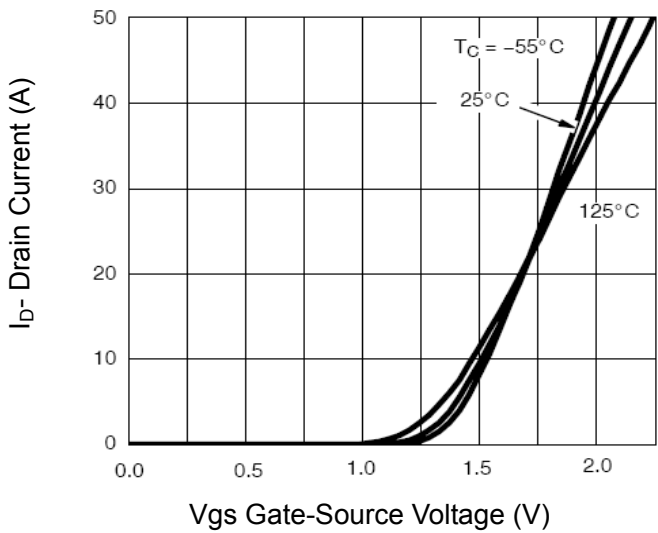


Figure 2 Transfer Characteristics

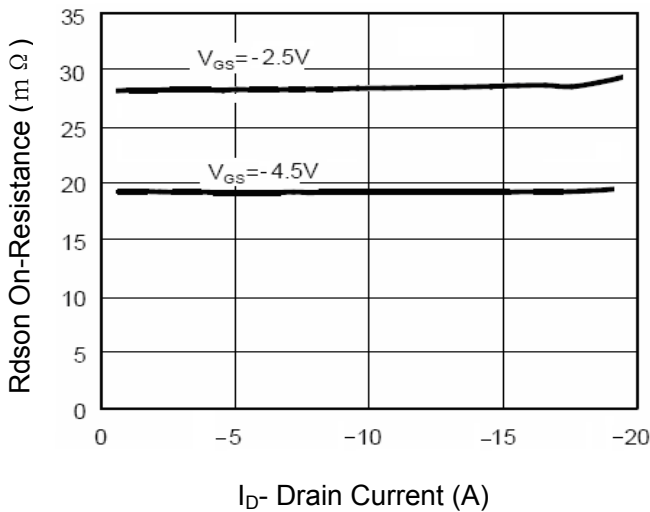


Figure 3 Rdson- Drain Current

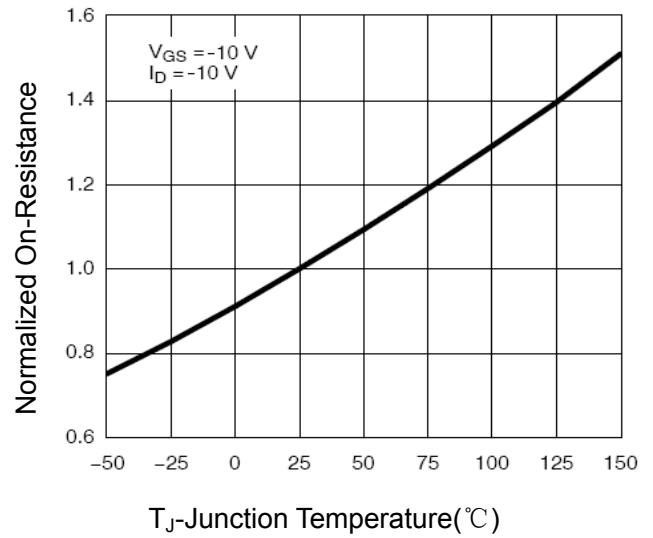


Figure 4 Rdson-Junction Temperature

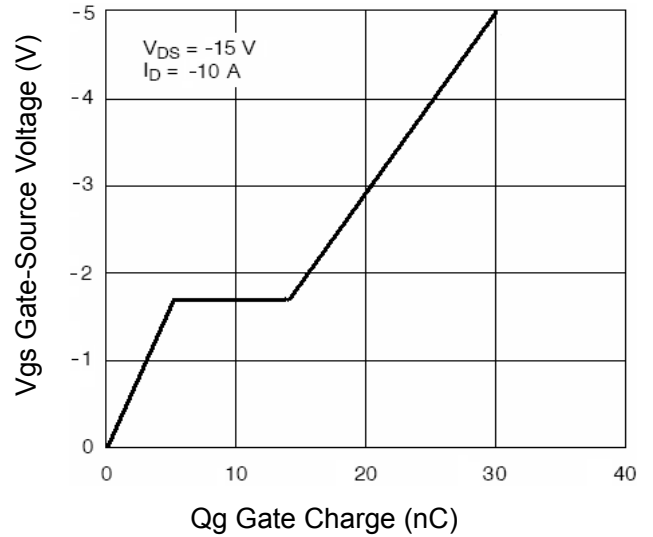


Figure 5 Gate Charge

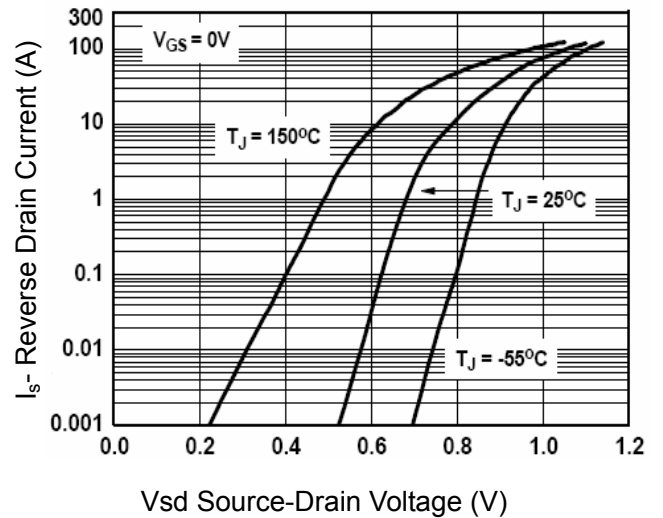


Figure 6 Source- Drain Diode Forward

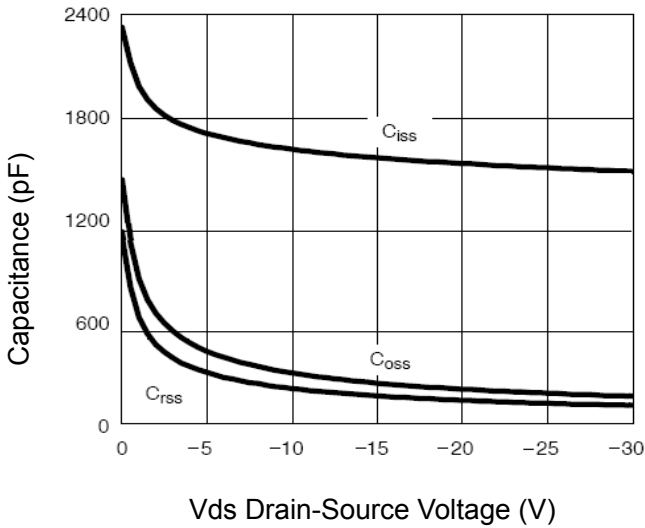


Figure 7 Capacitance vs Vds

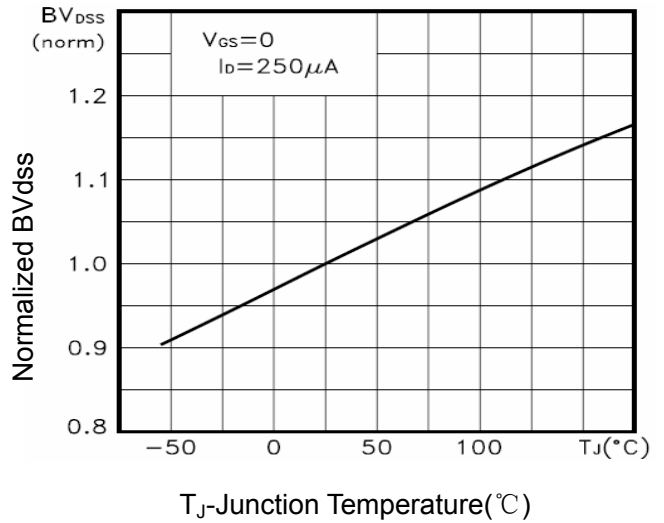


Figure 9 BV_{DSS} vs Junction Temperature

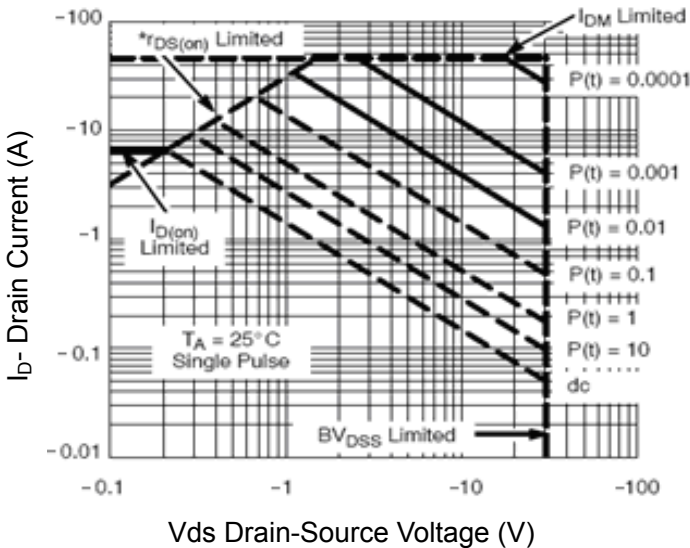


Figure 8 Safe Operation Area

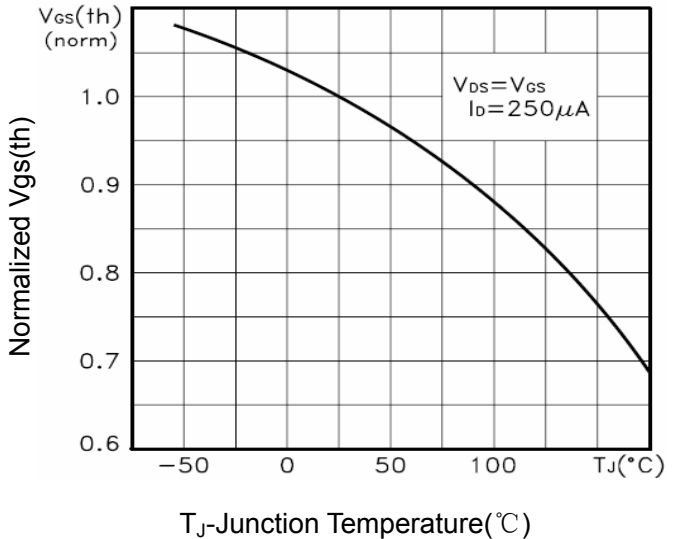


Figure 10 $V_{GS(th)}$ vs Junction Temperature

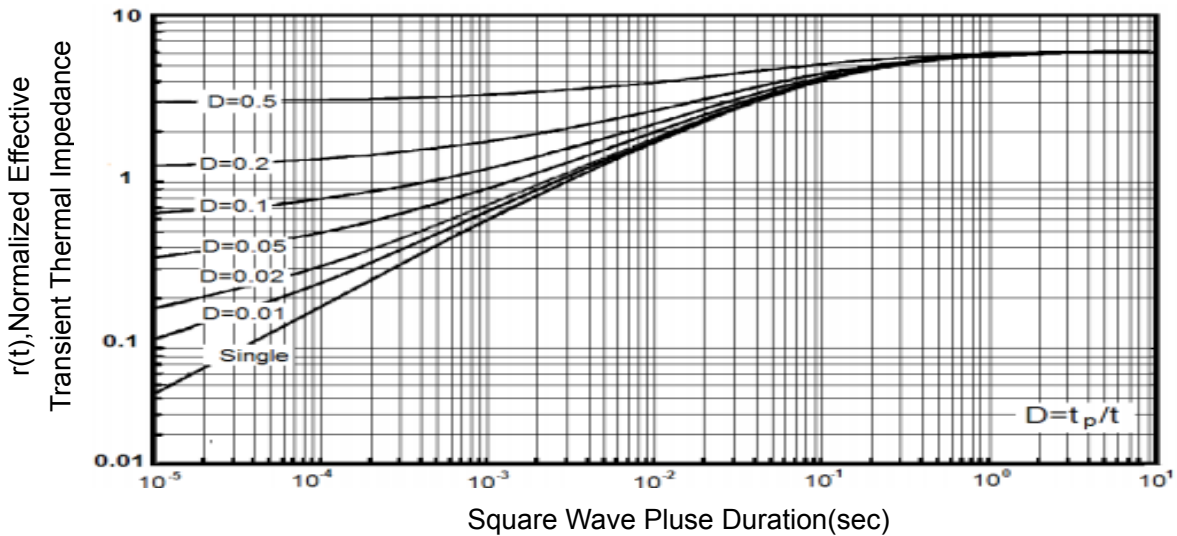
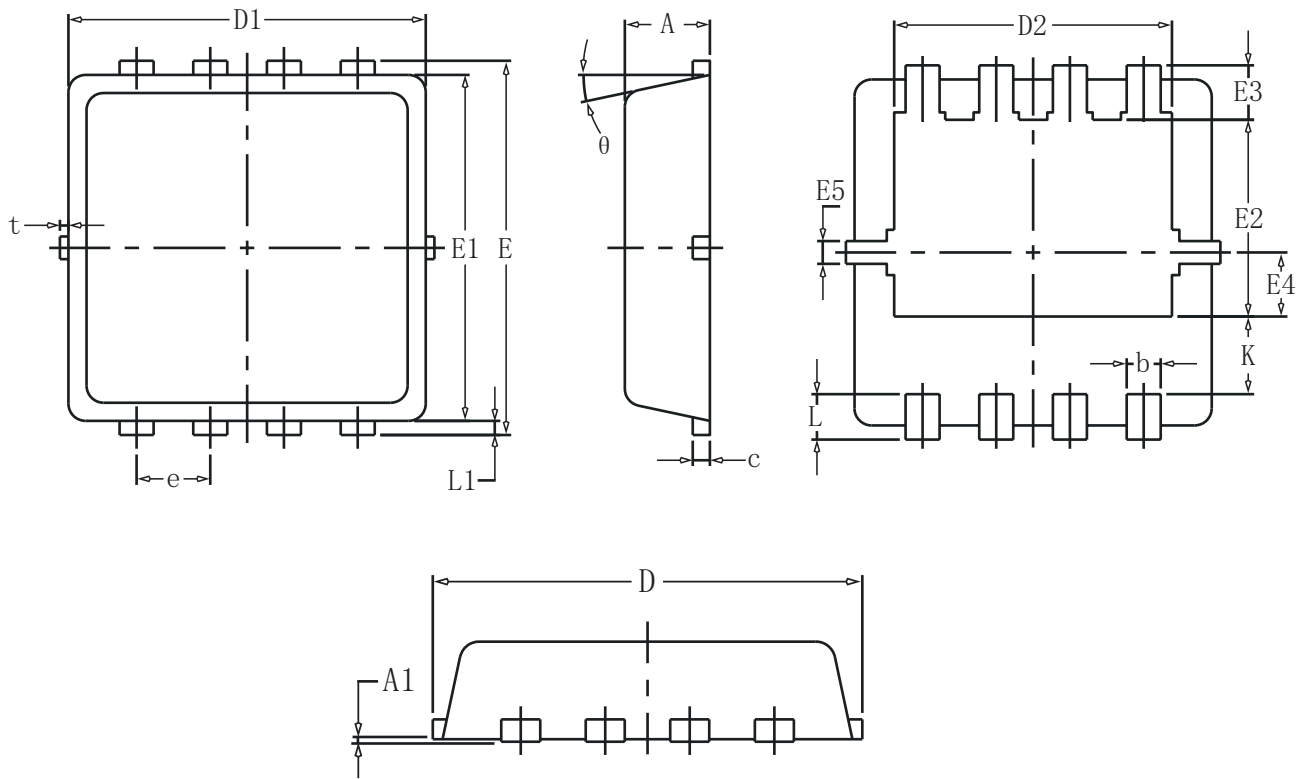


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3X3-8L Package information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	-	-	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°

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