

N and P Channel Enhancement Mode Power MOSFET

Description

The G1NP02LLE uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

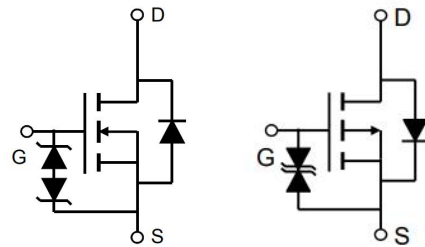
General Features

- NMOS
- V_{DS} 20V
- I_D (at $V_{GS} = 10V$) 1.3A
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 210m Ω
- $R_{DS(ON)}$ (at $V_{GS} = 2.5V$) < 270m Ω
- $R_{DS(ON)}$ (at $V_{GS} = 1.8V$) < 360m Ω
- 100% Avalanche Tested
- RoHS Compliant
- ESD (HBM)>2.0KV

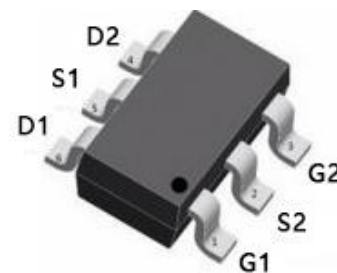
- PMOS
- V_{DS} -20V
- I_D (at $V_{GS} = -10V$) -1.1A
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 460m Ω
- $R_{DS(ON)}$ (at $V_{GS} = -2.5V$) < 580m Ω
- $R_{DS(ON)}$ (at $V_{GS} = -1.8V$) < 760m Ω
- 100% Avalanche Tested
- RoHS Compliant
- ESD (HBM)>2.0KV

Application

- Power switch
- DC/DC converters



Schematic diagram



SOT-23-6L

Ordering Information

Device	Package	Marking	Packaging
G1NP02LLE	SOT-23-6L	G1NP02E	3000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Continuous Drain Current	I_D	1.3	1.1	A
Pulsed Drain Current (note1)	I_{DM}	5.2	4.4	A
Gate-Source Voltage	V_{GS}	± 10	± 10	V
Power Dissipation	P_D	1.25	1.25	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	$^\circ C$

Thermal Resistance

Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	100	100	$^\circ C/W$

NMOS Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10V$	--	--	± 10	μA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.35	0.55	1	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 0.65A$	--	170	210	m Ω
		$V_{GS} = 2.5V, I_D = 0.55A$	--	220	270	
		$V_{GS} = 1.8V, I_D = 0.45A$	--	300	360	
Forward Transconductance	g_{FS}	$V_{GS} = 5V, I_D = 0.55A$	--	1.3	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 10V,$ $f = 1.0MHz$	--	146	--	pF
Output Capacitance	C_{oss}		--	108	--	
Reverse Transfer Capacitance	C_{rss}		--	52	--	
Total Gate Charge	Q_g	$V_{DD} = 10V,$ $I_D = 0.65A,$ $V_{GS} = 4.5V$	--	1	--	nC
Gate-Source Charge	Q_{gs}		--	0.27	--	
Gate-Drain Charge	Q_{gd}		--	0.21	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 10V,$ $I_D = 0.65A,$ $R_G = 10\Omega$	--	17.5	--	ns
Turn-on Rise Time	t_r		--	2.1	--	
Turn-off Delay Time	$t_{d(off)}$		--	9.5	--	
Turn-off Fall Time	t_f		--	22	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	1.3	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 0.65A, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = 0.65A, V_{GS} = 0V$ $di/dt = 20A/\mu s$	--	0.39	--	nC
Reverse Recovery Time	T_{rr}		--	14	--	ns

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

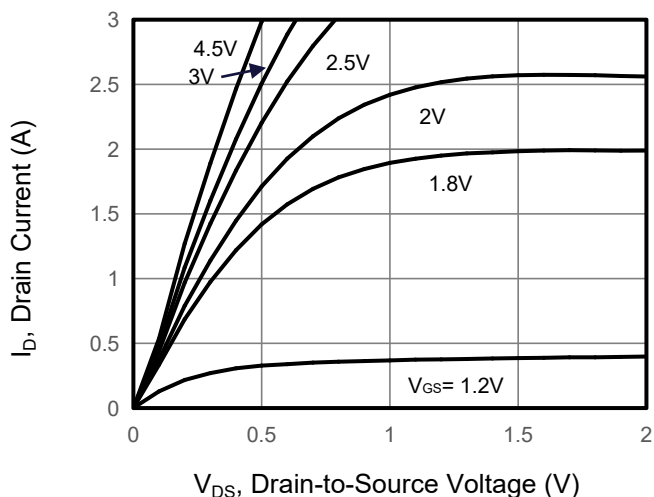


Figure 2. Transfer Characteristics

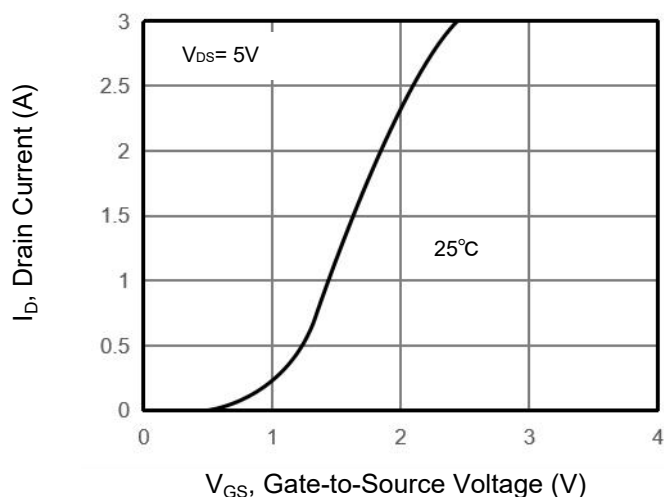


Figure 3. Drain Source On Resistance

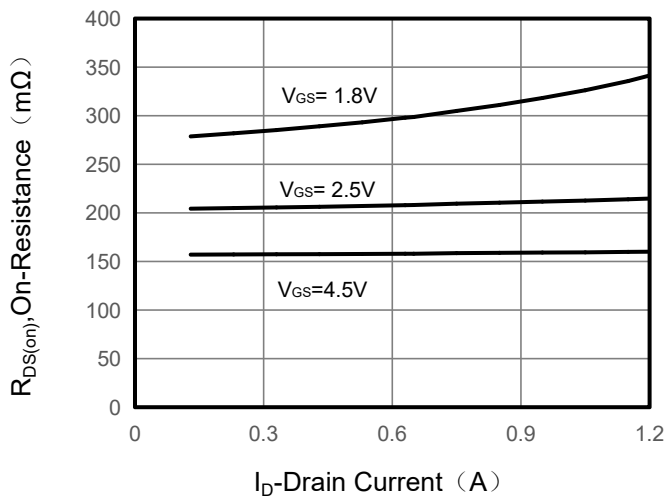


Figure 4. Gate Charge

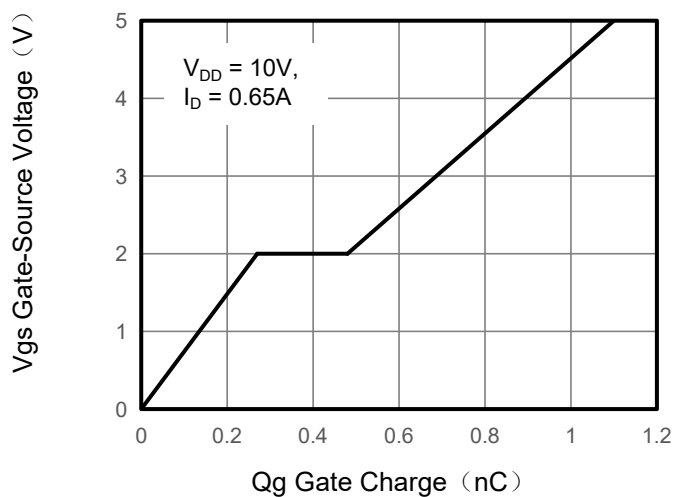


Figure 5. Capacitance

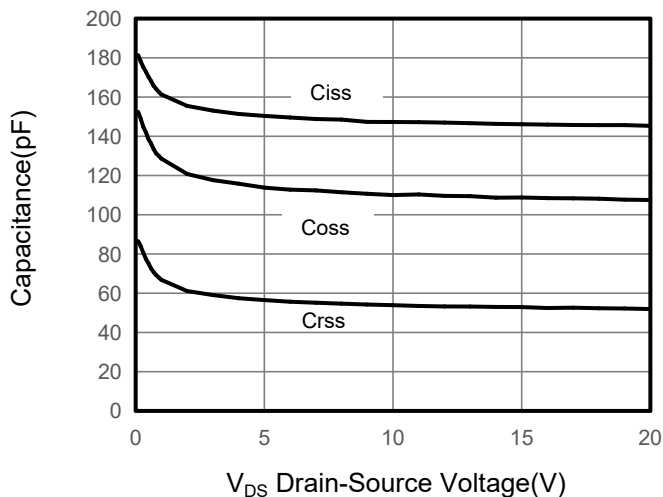
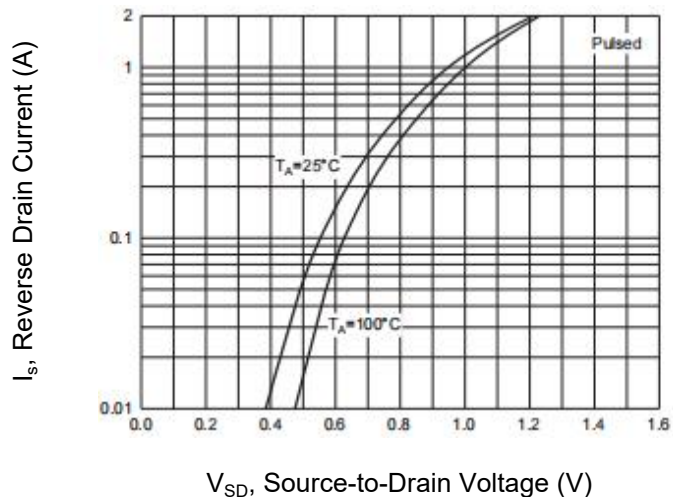


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

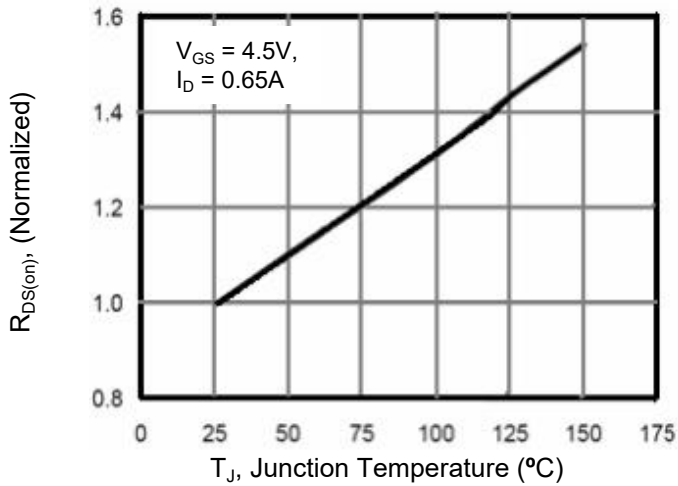


Figure 8. Safe Operation Area

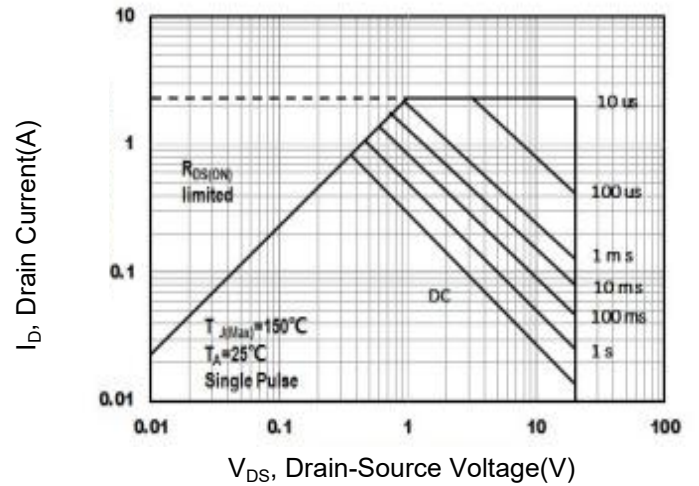
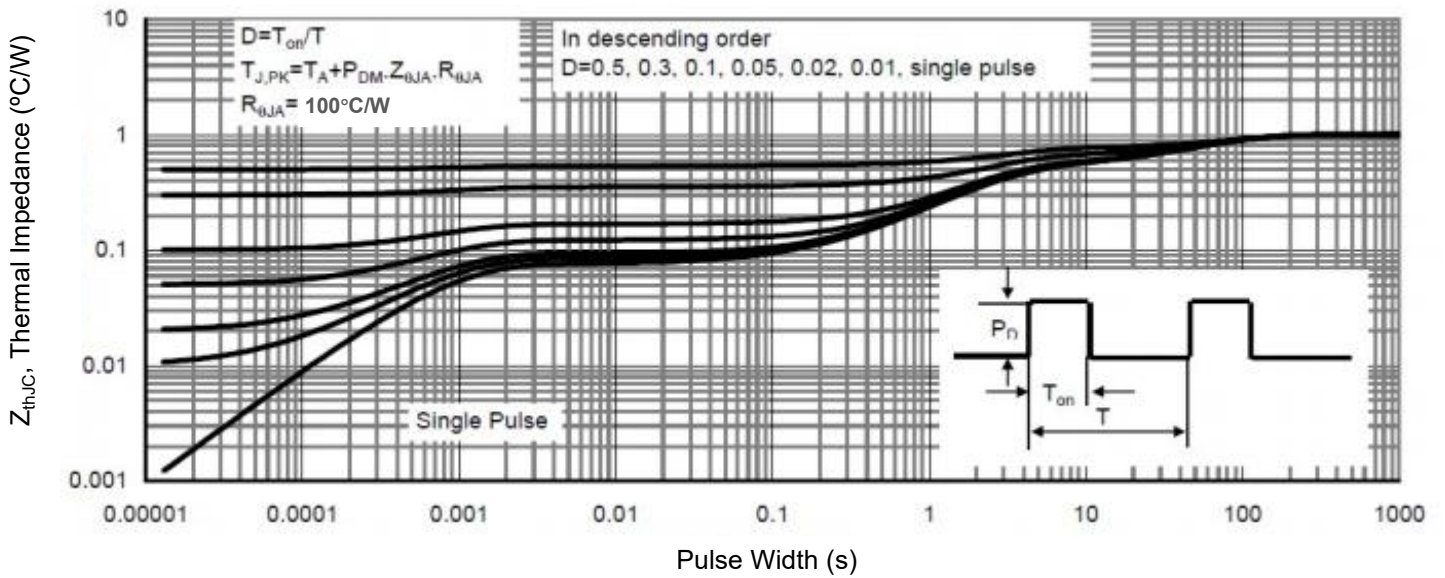


Figure 9. Normalized Maximum Transient Thermal Impedance

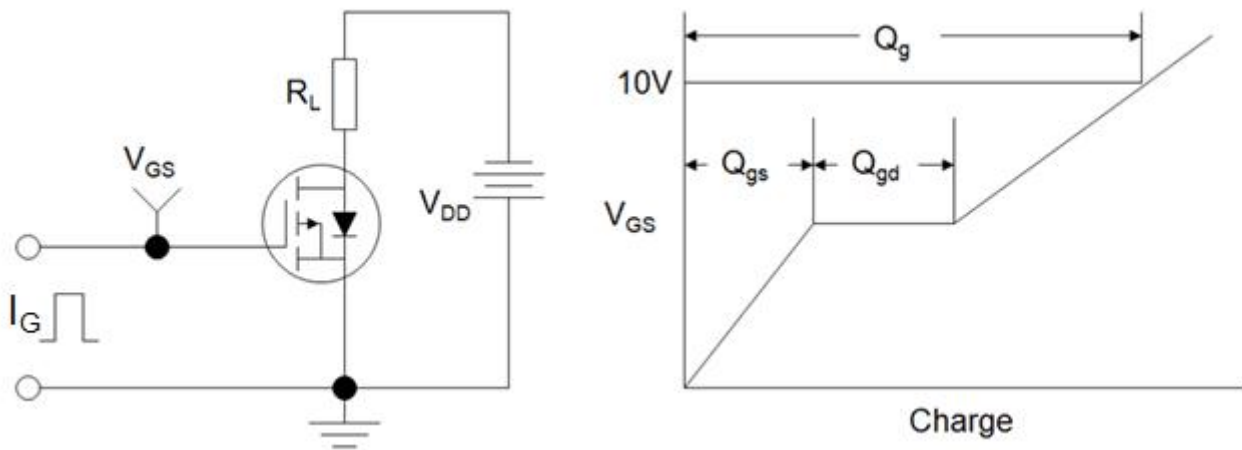


PMOS Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10V$	--	--	± 10	μA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.35	-0.55	-0.8	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -0.5A$	--	380	460	m Ω
		$V_{GS} = -2.5V, I_D = -0.5A$	--	480	580	
		$V_{GS} = -1.8V, I_D = -0.5A$	--	630	760	
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_D = -0.5A$	--	1.3	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = -10V,$ $f = 1.0MHz$	--	177	--	pF
Output Capacitance	C_{oss}		--	109	--	
Reverse Transfer Capacitance	C_{rss}		--	51	--	
Total Gate Charge	Q_g	$V_{DD} = -10V,$ $I_D = -0.5A,$ $V_{GS} = -4.5V$	--	1.22	--	nC
Gate-Source Charge	Q_{gs}		--	0.36	--	
Gate-Drain Charge	Q_{gd}		--	0.26	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -10V,$ $I_D = -0.5A,$ $R_G = 3\Omega$	--	18	--	ns
Turn-on Rise Time	t_r		--	4.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	23	--	
Turn-off Fall Time	t_f		--	15	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-1.1	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = -0.5A, V_{GS} = 0V$	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = -0.5A, V_{GS} = 0V$ $di/dt = -20A/\mu s$	--	0.95	--	nC
Reverse Recovery Time	T_{rr}		--	24	--	ns

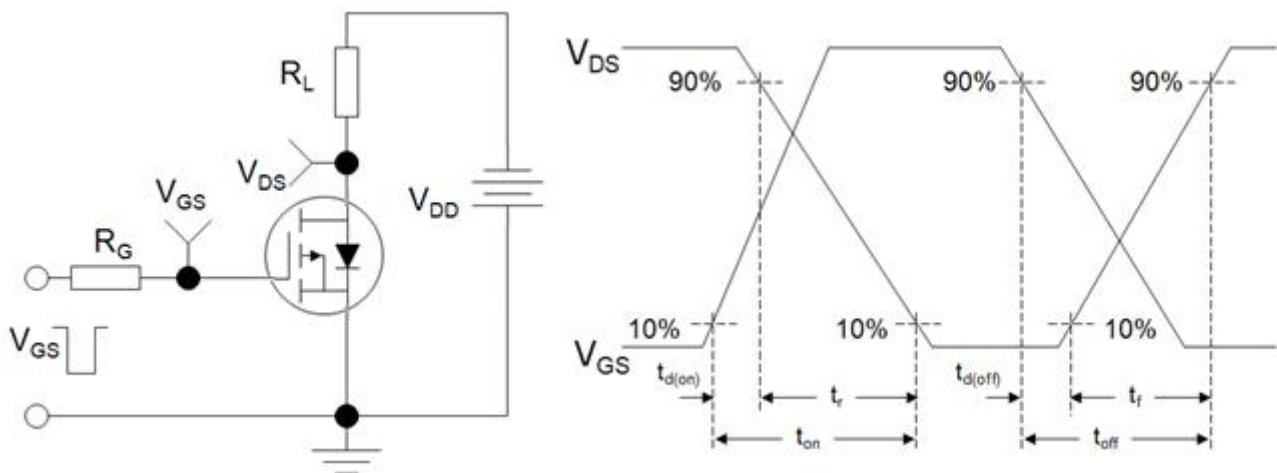
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J = 25^\circ\text{C}, V_{DD} = -20V, V_{GS} = -10V, L = 0.5mH, R_G = 25\Omega$
3. Identical low side and high side switch with identical R_G

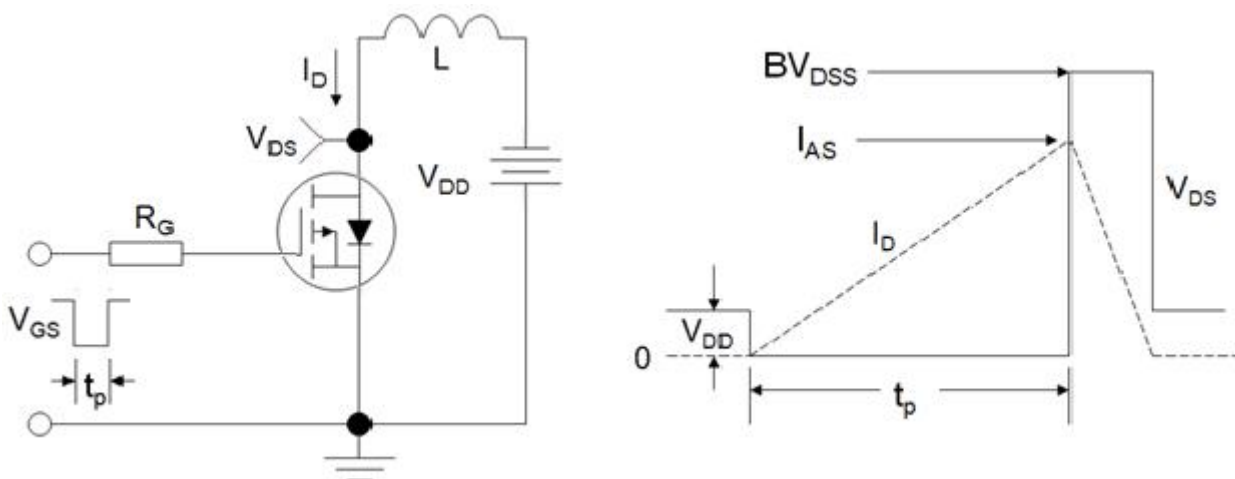
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

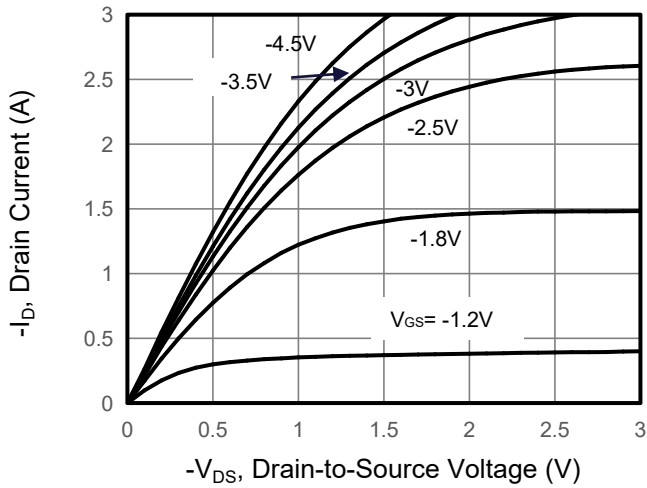


Figure 2. Transfer Characteristics

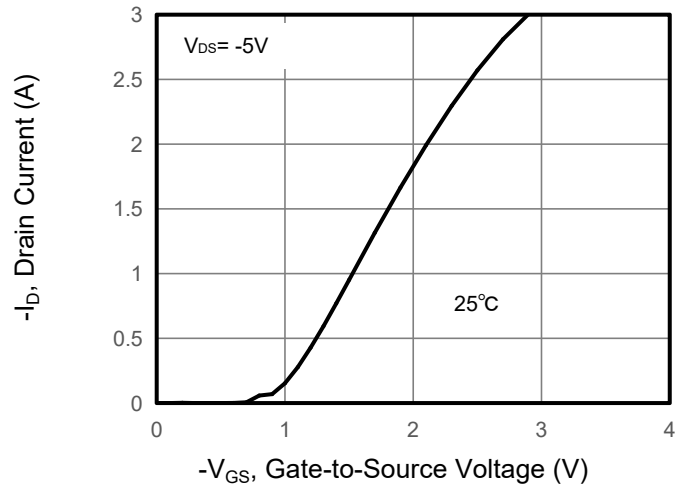


Figure 3. Drain Source On Resistance

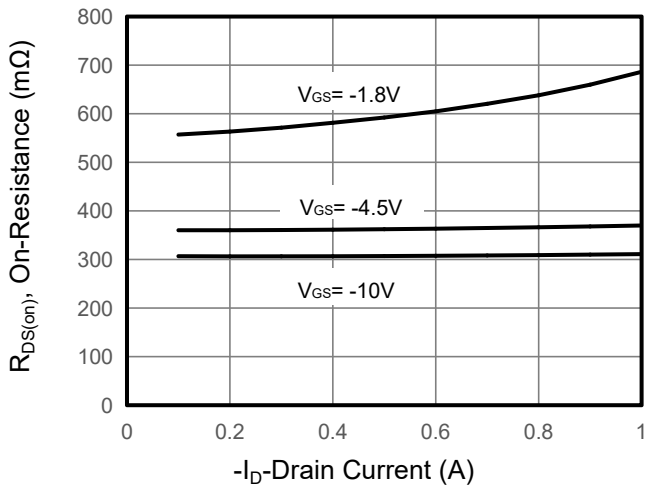


Figure 4. Gate Charge

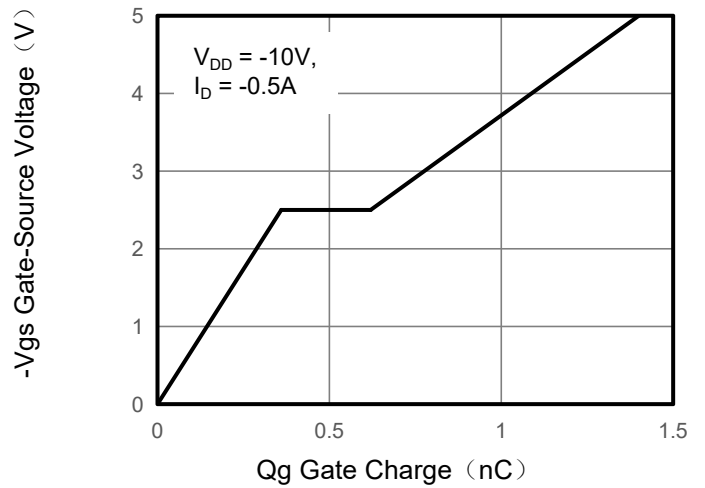


Figure 5. Capacitance

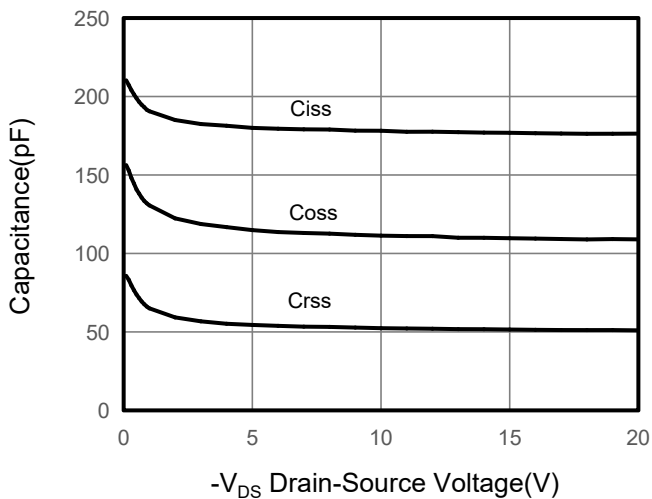
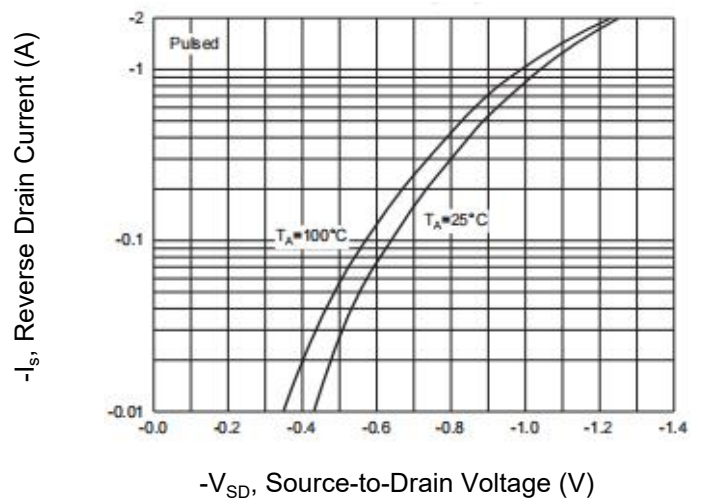


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

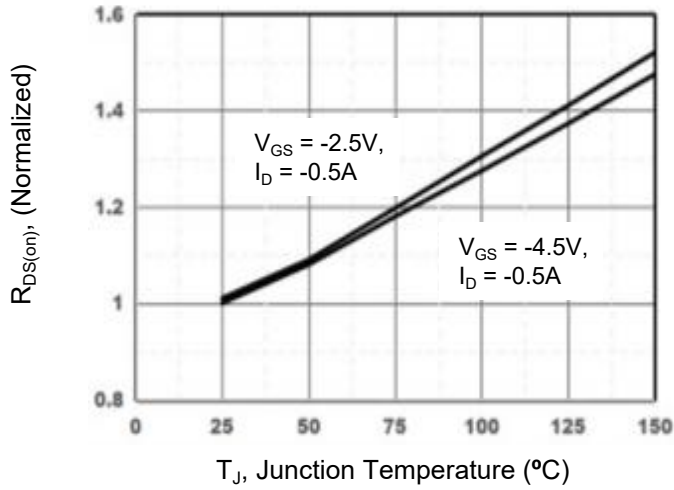


Figure 10. Safe Operation Area

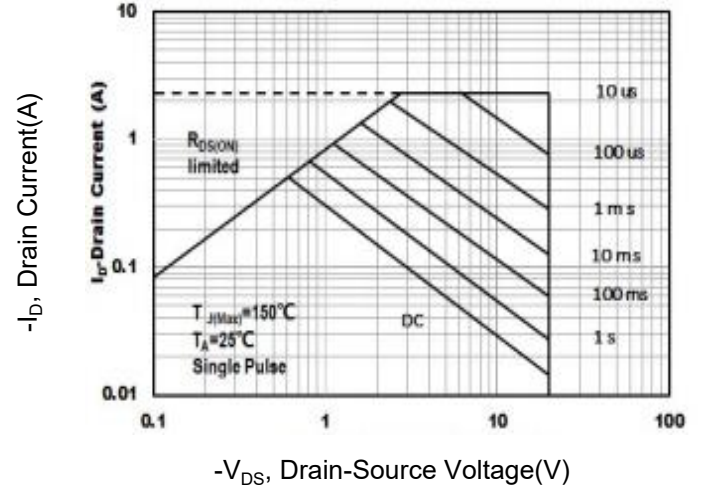
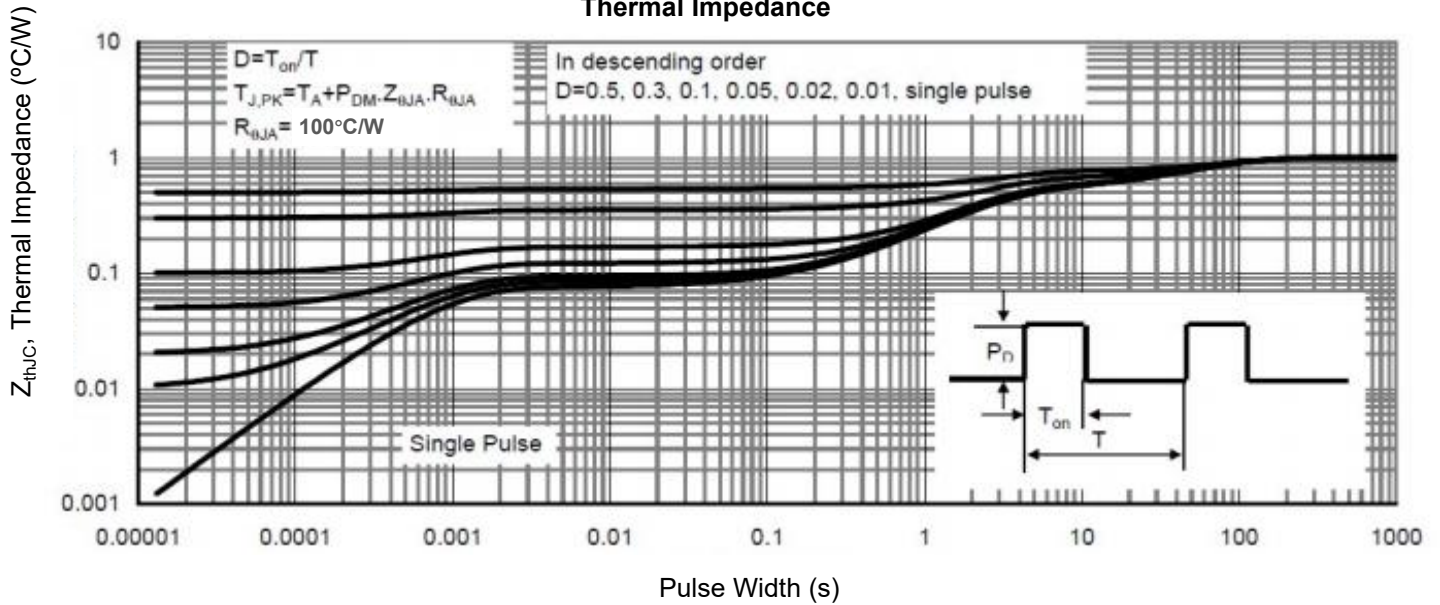
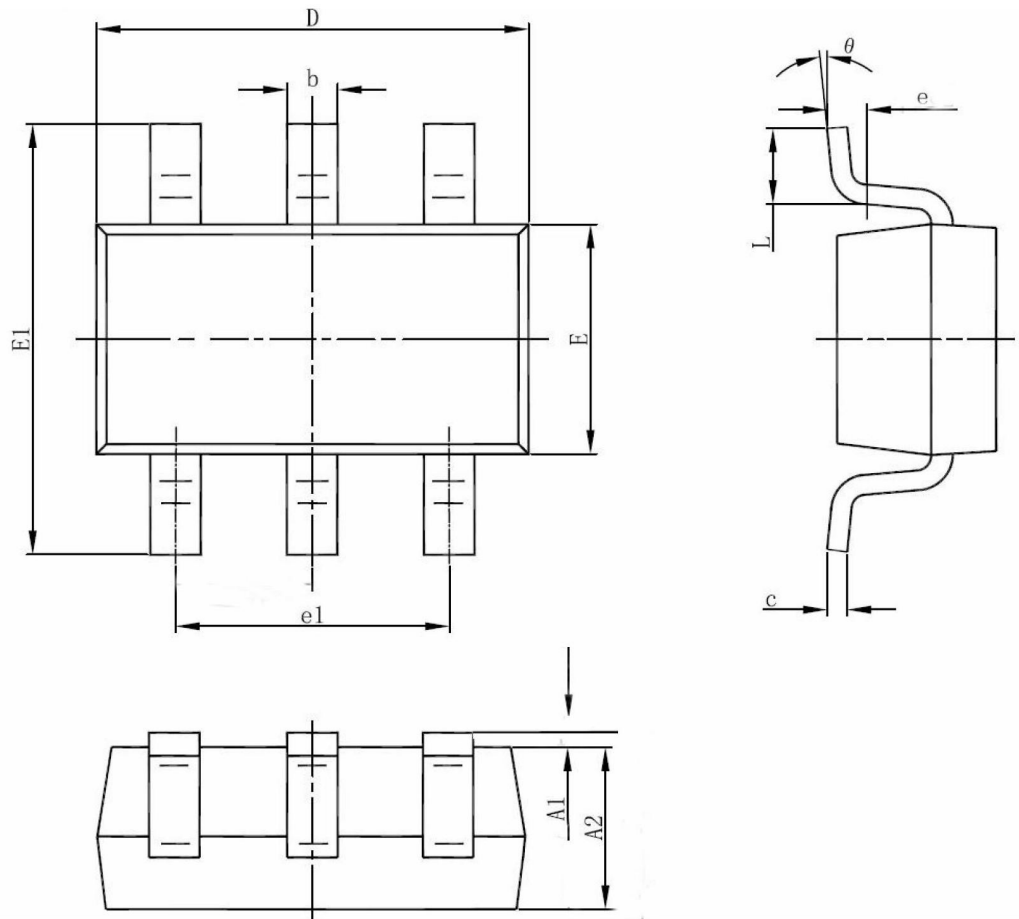


Figure 9. Normalized Maximum Transient Thermal Impedance



SOT-23-6L Package Information



DIM	MIN	NOM	MAX
A1	0.00	-	0.10
A2	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.10	0.15	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
E1	2.60	2.80	3.00
e	0.2GAUGE PLANE		
e1	-	1.90	-
L	0.30	0.45	0.60
θ	0°	-	8°
All Dimensions in mm			

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