

**DESCRIPTION**

The G20N06D52 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

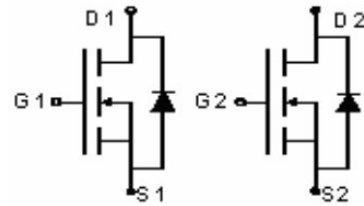
**GENERAL FEATURES**

- High density cell design for ultra low  $R_{dson}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- RoHS Compliant

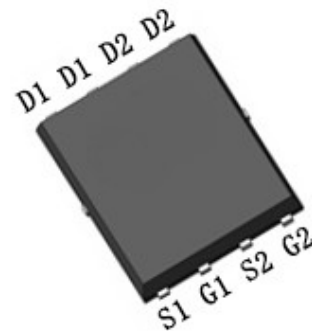
$V_{DSS}$	$R_{DS(ON)}$ @ 10V (typ)	$I_D$
60V	24m $\Omega$	20 A

**Application**

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic diagram



DFN5\*6-8L

**Ordering Information**

Part Number	Marking	Case	Packaging
G20N06D52	G20N06	DFN5*6-8L	2500pcs/Reel

**Absolute Maximum Ratings (TA=25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	20	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	15	A
Pulsed Drain Current	$I_{DM}$	63	A
Maximum Power Dissipation	$P_D$	45	W
Single pulse avalanche energy (Note 5)	$E_{AS}$	89	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	4.33	$^\circ C/W$
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## Electrical Characteristics (TA=25°C unless otherwise noted)

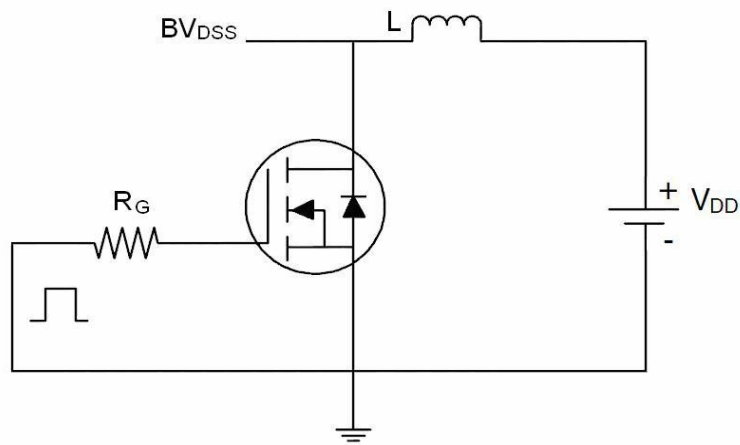
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	24	30	m $\Omega$
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=10A$	-	30	40	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=4.5A$	11	-	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	1220	-	PF
Output Capacitance	$C_{oss}$		-	102	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	92	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=6.7\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	6	-	nS
Turn-on Rise Time	$t_r$		-	2.9	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	16.8	-	nS
Turn-Off Fall Time	$t_f$		-	2.9	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=48V, I_D=10A,$ $V_{GS}=10V$	-	25	-	nC
Gate-Source Charge	$Q_{gs}$		-	4	-	nC
Gate-Drain Charge	$Q_{gd}$		-	8	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	21	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ C, I_F = 10A$	-	38	-	nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100A/\mu s$ (Note3)	-	55	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

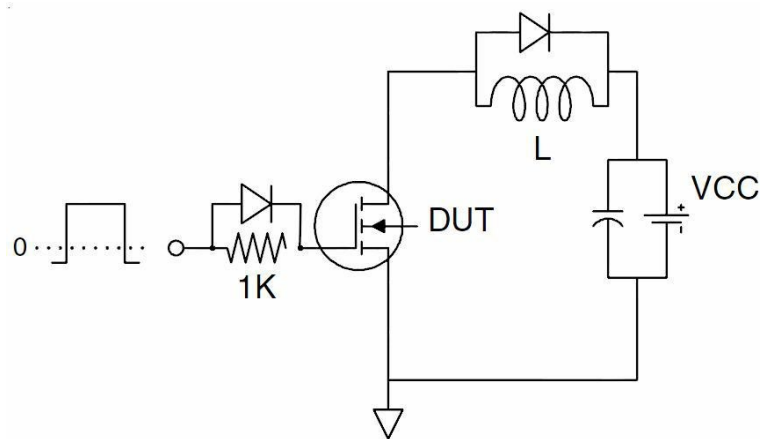
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ C, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

**Test circuit**

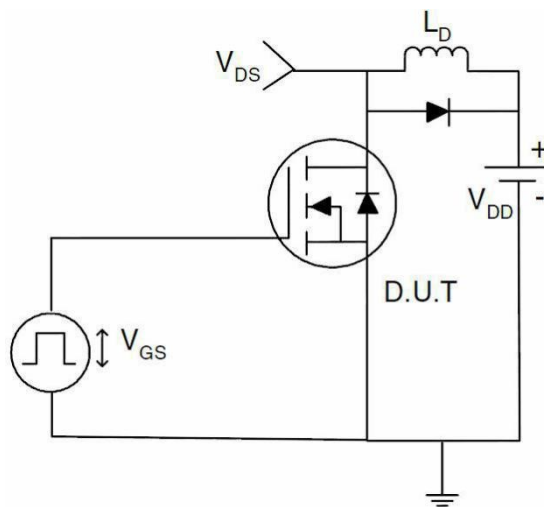
**1) EAS test Circuits**



**2) Gate charge test Circuit:**



**3) Switch Time Test Circuit:**



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

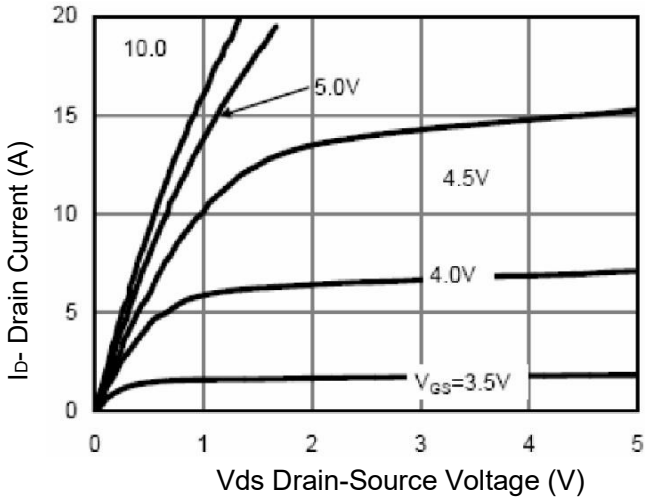


Figure 1 Output Characteristics

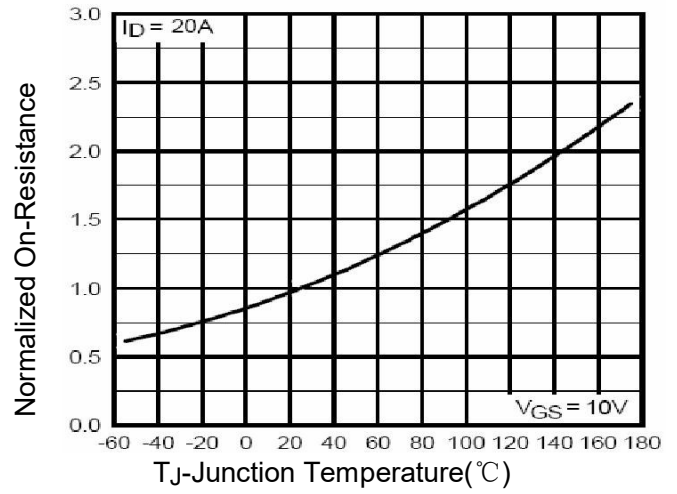


Figure 4 Rdson-Junction Temperature

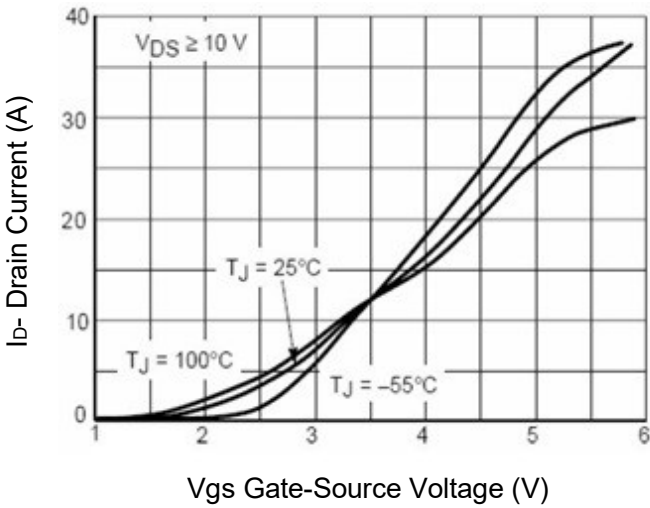


Figure 2 Transfer Characteristics

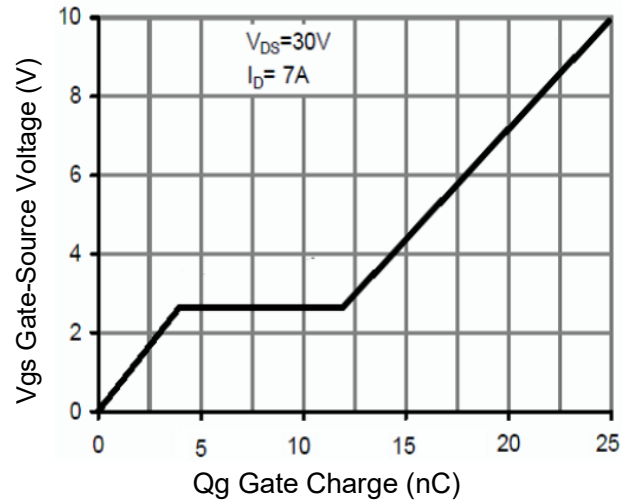


Figure 5 Gate Charge

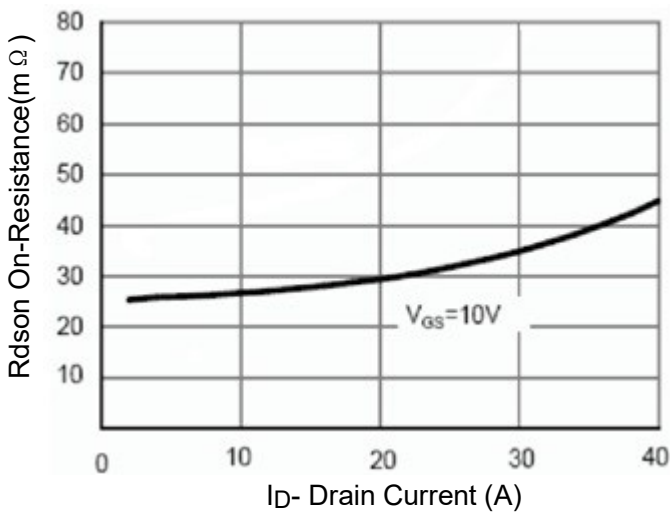


Figure 3 Rdson- Drain Current

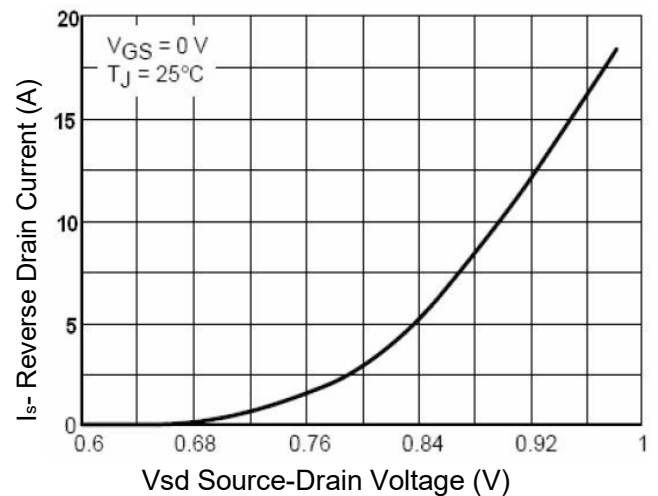


Figure 6 Source- Drain Diode Forward

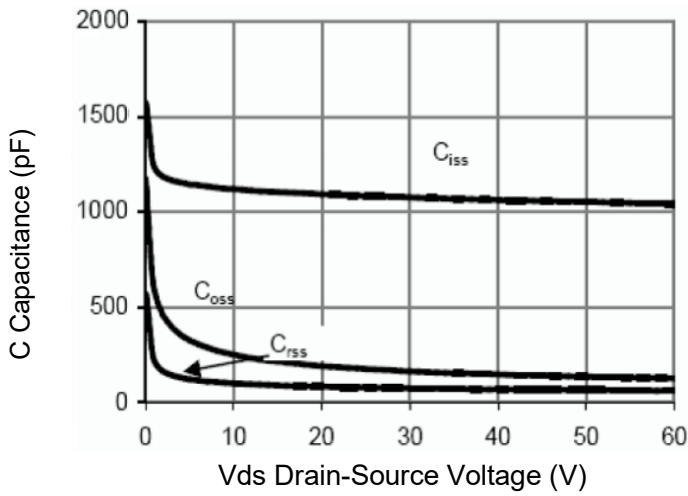


Figure 7 Capacitance vs Vds

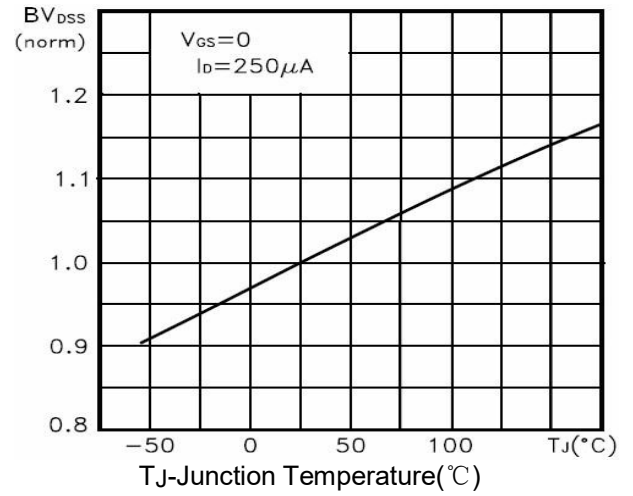


Figure 9  $BV_{DSS}$  vs Junction Temperature

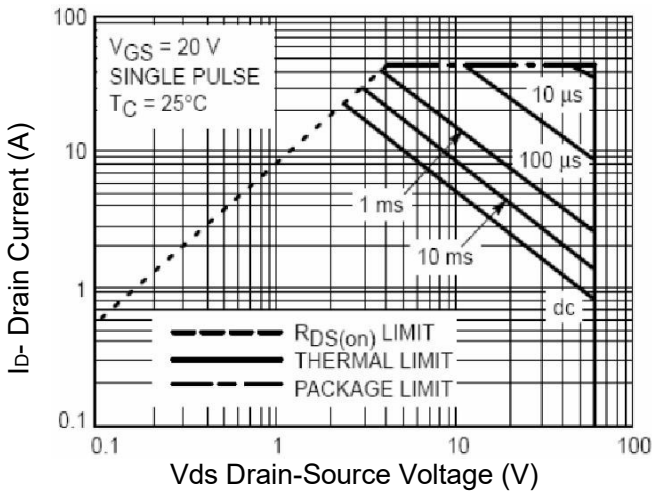


Figure 8 Safe Operation Area

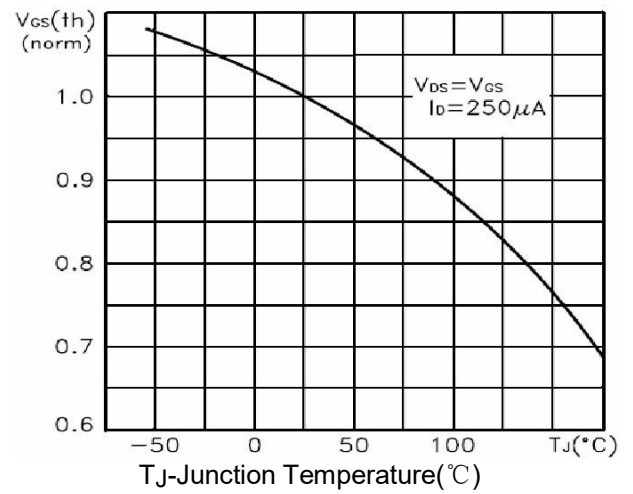


Figure 10  $V_{GS(th)}$  vs Junction Temperature

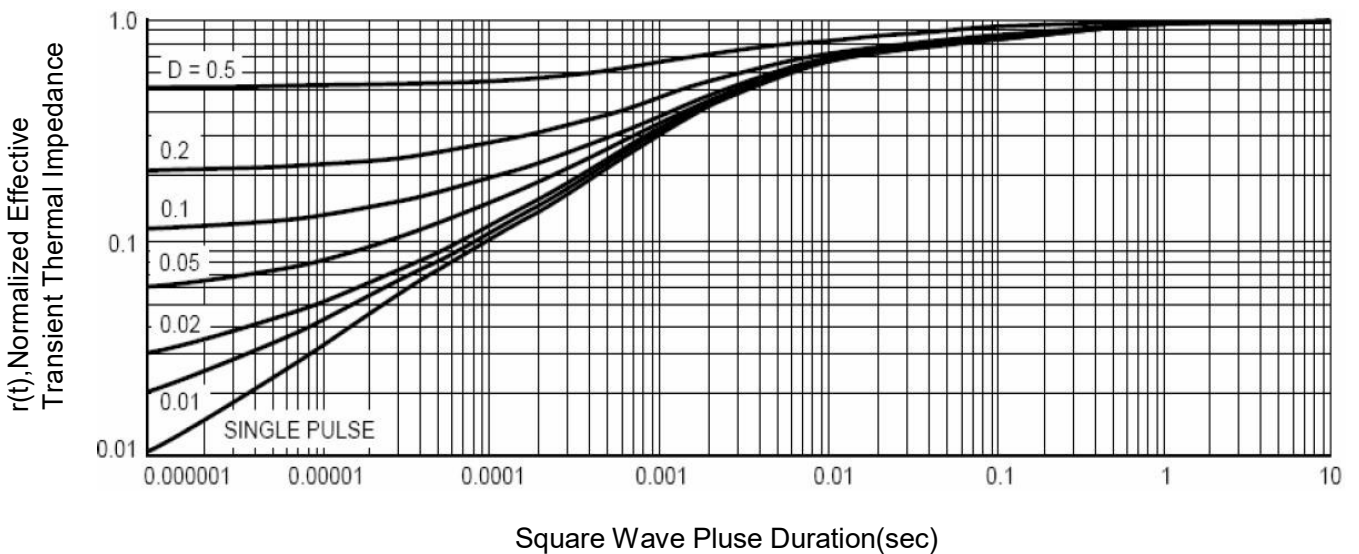
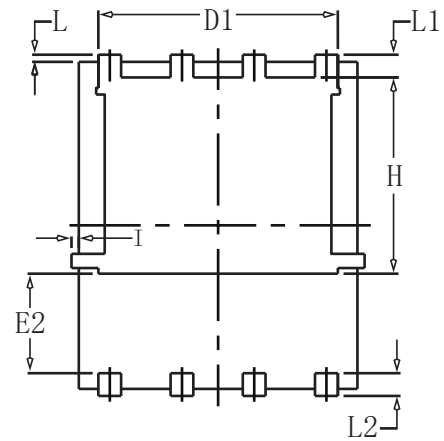
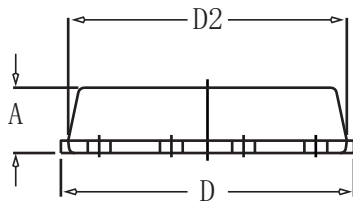
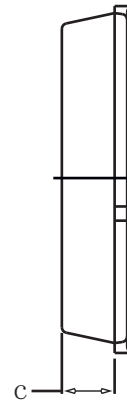
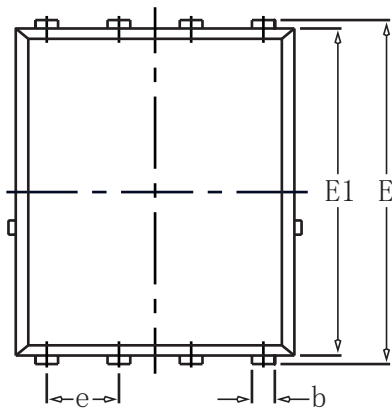


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package information



SYMBOL	COMMON			
	MM		INCH	
	MIN	MAX	MIN	MAX
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.59	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	-	0.0630	-
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	-	0.18	-	0.0070

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