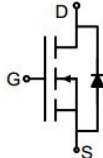
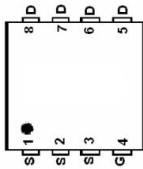
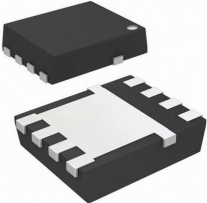


## N-Channel Enhancement Mode Power MOSFET

<p><b>Description</b></p> <p>The GT100N04D3 uses advanced trench technology to provide excellent <math>R_{DS(ON)}</math>, low gate charge. It can be used in a wide variety of applications.</p> <p><b>General Features</b></p> <ul style="list-style-type: none"> <li>● <math>V_{DS}</math> 40V</li> <li>● <math>I_D</math> (at <math>V_{GS} = 10V</math>) 13A</li> <li>● <math>R_{DS(ON)}</math> (at <math>V_{GS} = 10V</math>) &lt; 10m<math>\Omega</math></li> <li>● <math>R_{DS(ON)}</math> (at <math>V_{GS} = 4.5V</math>) &lt; 16m<math>\Omega</math></li> <li>● 100% Avalanche Tested</li> <li>● RoHS Compliant</li> </ul> <p><b>Application</b></p> <ul style="list-style-type: none"> <li>● Power switch</li> <li>● DC/DC converters</li> </ul>	 <p>Schematic diagram</p>  <p>pin assignment</p>  <p>DFN3X3-8L</p>
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### Ordering Information

Device	Package	Marking	Packaging
GT100N04D3	DFN3X3-8L	GT100N04	5000psc/Reel

### Absolute Maximum Ratings $T_C = 25^\circ C$ , unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Continuous Drain Current	$I_D$	13	A
Pulsed Drain Current (note1)	$I_{DM}$	52	A
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation	$P_D$	23	W
Single pulse avalanche energy (note2)	$E_{AS}$	14	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 To 150	$^\circ C$

### Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	70	$^\circ C/W$
Maximum Junction-to-Case	$R_{thJC}$	5.3	$^\circ C/W$

Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static Parameters</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40V, V_{GS} = 0V$	--	--	1	$\mu A$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 5A$	--	7	10	m $\Omega$
		$V_{GS} = 4.5V, I_D = 5A$	--	11	16	
Forward Transconductance	$g_{FS}$	$V_{GS} = 5V, I_D = 5A$	--	22	--	S
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = 20V,$ $f = 1.0\text{MHz}$	--	642	--	pF
Output Capacitance	$C_{oss}$		--	117	--	
Reverse Transfer Capacitance	$C_{rss}$		--	115	--	
Total Gate Charge	$Q_g$	$V_{DD} = 20V,$ $I_D = 20A,$ $V_{GS} = 10V$	--	32	--	nC
Gate-Source Charge	$Q_{gs}$		--	7	--	
Gate-Drain Charge	$Q_{gd}$		--	3	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 20V,$ $I_D = 20A,$ $R_G = 1.6\Omega$	--	6.5	--	ns
Turn-on Rise Time	$t_r$		--	3	--	
Turn-off Delay Time	$t_{d(off)}$		--	21	--	
Turn-off Fall Time	$t_f$		--	3	--	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	13	A
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = 5, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Charge	$Q_{rr}$	$I_F = 20A, V_{GS} = 0V$ $di/dt=100A/us$	--	16	--	nC
Reverse Recovery Time	$T_{rr}$		--	28	--	ns

### Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition :  $T_J=25^\circ\text{C}$  , $V_{DD}= 40V, V_{GS}=10V, L=0.5\text{mH}, R_G=25\Omega$
3. Identical low side and high side switch with identical  $R_G$

### Gate Charge Test Circuit



### Switch Time Test Circuit

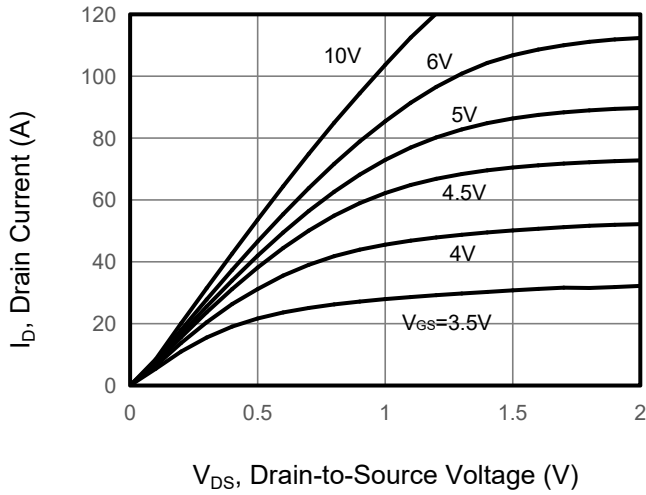


### EAS Test Circuit

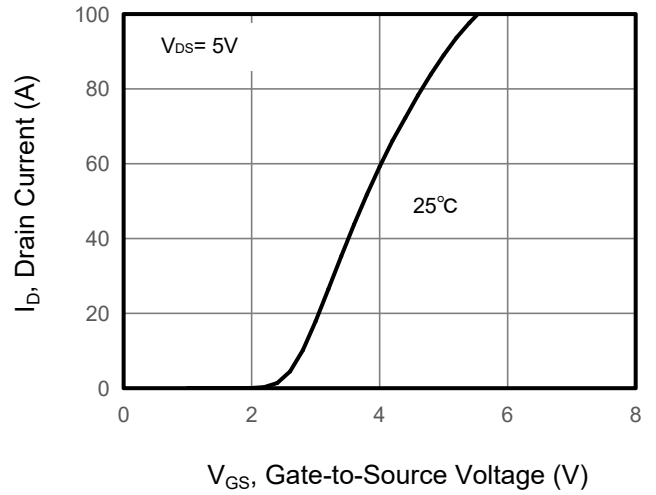


Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

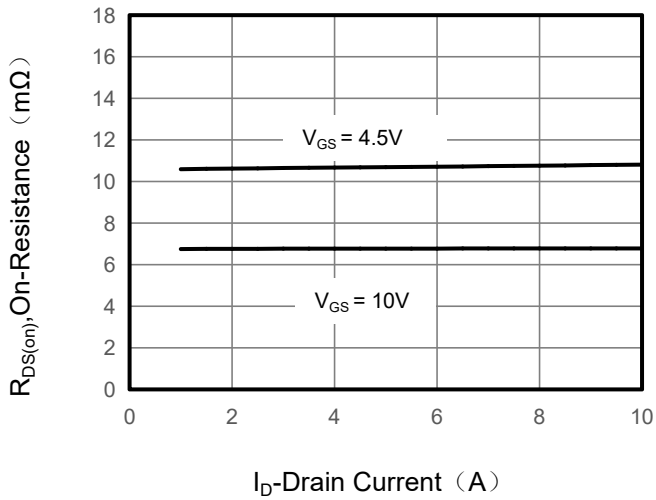
**Figure 1. Output Characteristics**



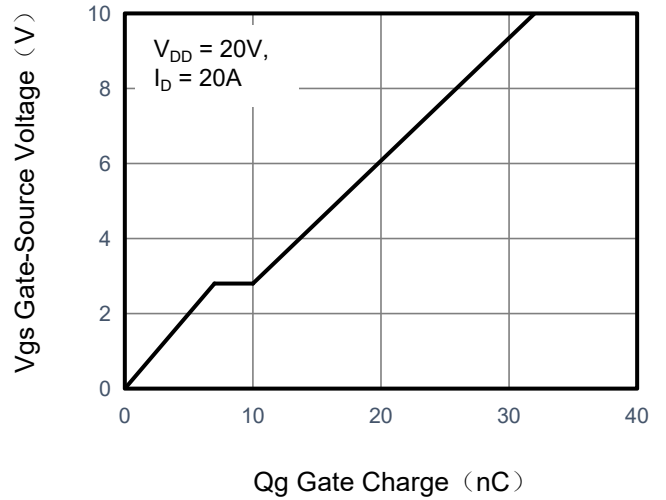
**Figure 2. Transfer Characteristics**



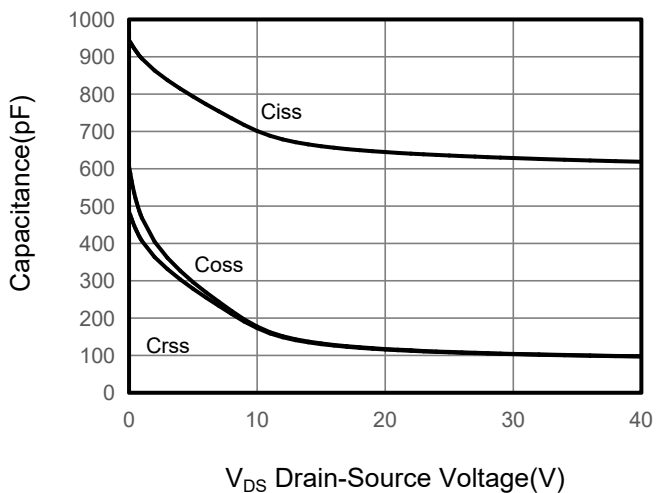
**Figure 3. Drain Source On Resistance**



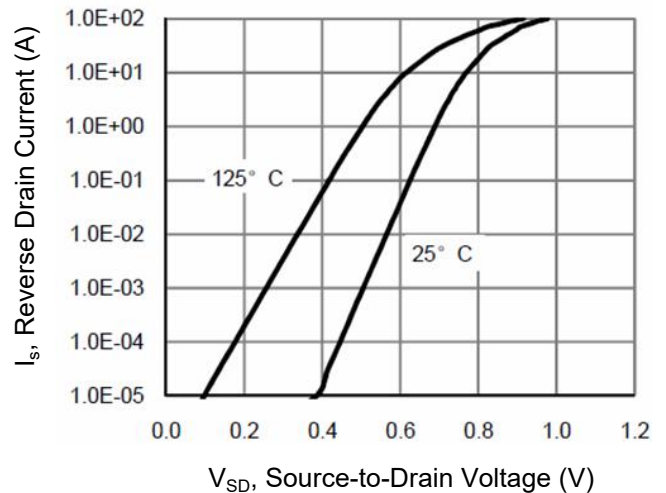
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Source-Drain Diode Forward**



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. Drain-Source On-Resistance

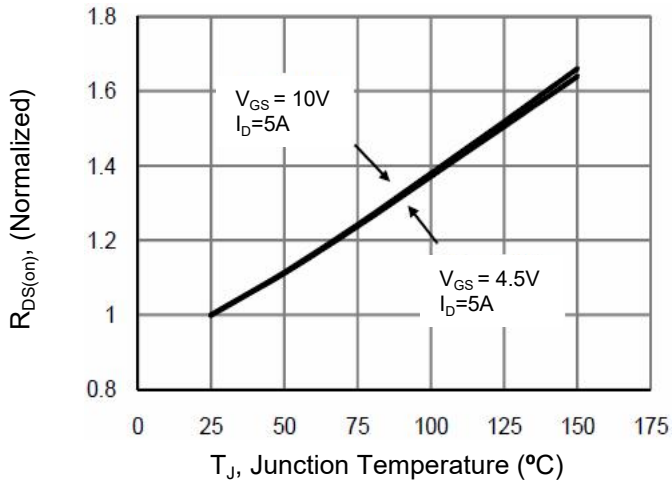


Figure 8. Safe Operation Area

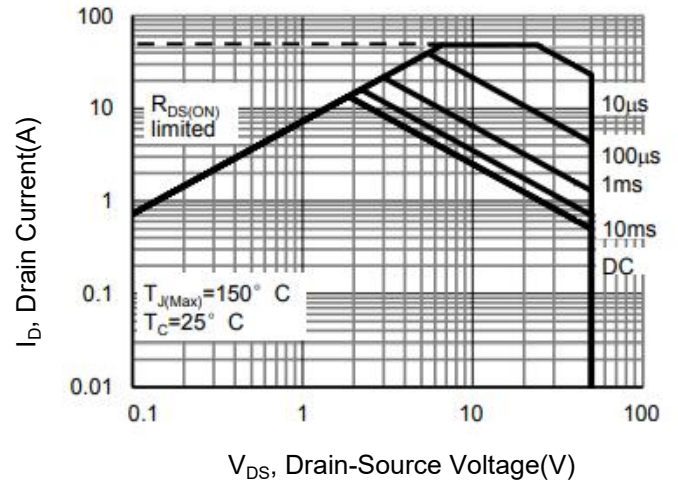
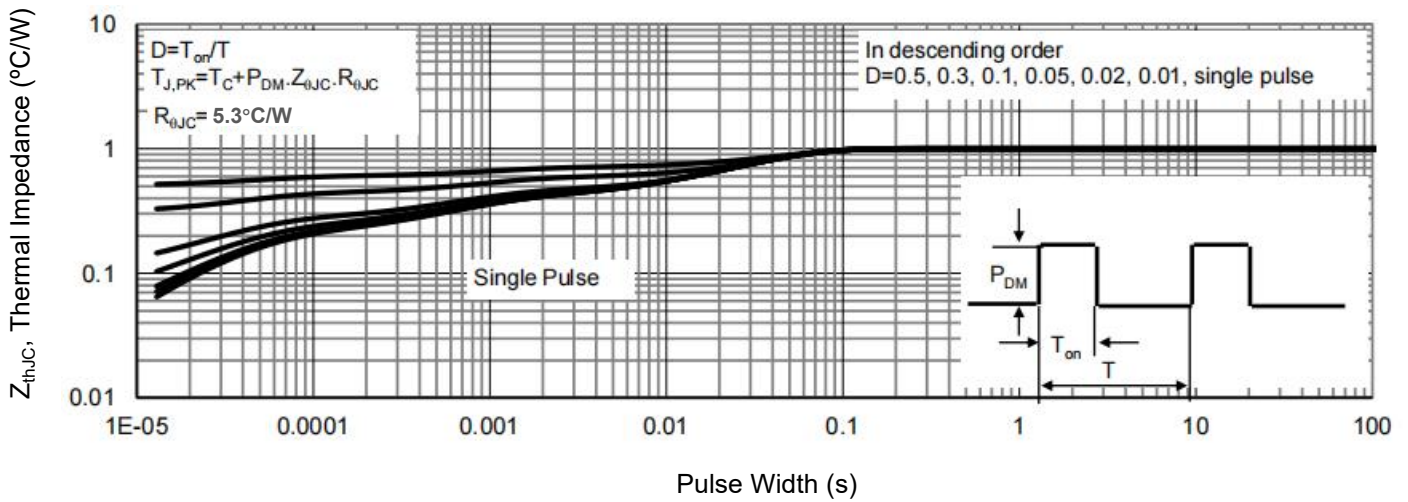
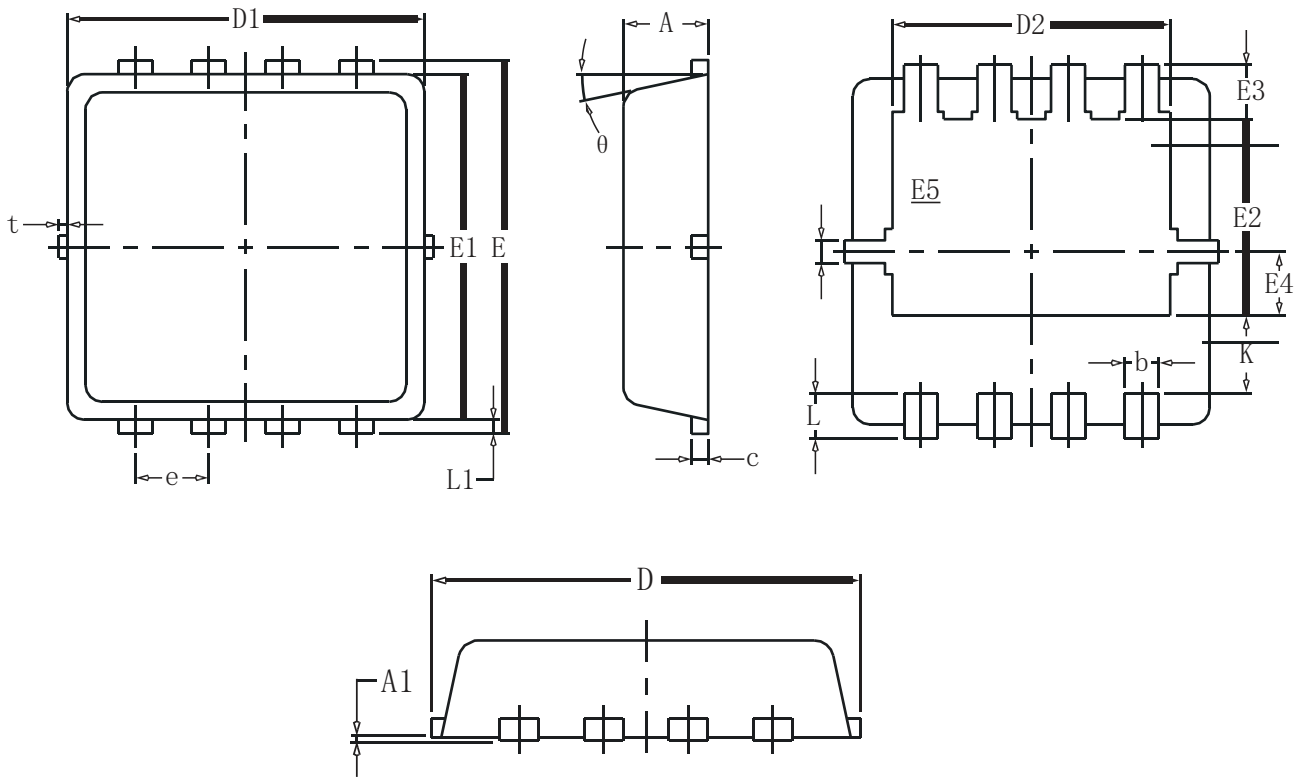


Figure 9. Normalized Maximum Transient Thermal Impedance



## DFN3x3-8L Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	-	-	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
$\theta$	10°	12°	14°

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