GOODWORK

20N10

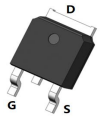
100V, 20A N-channel Power Trench MOSFET

Features

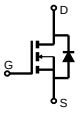
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔVds Tested
- Halogen-free; RoHS-compliant

Applications

- Load Switch
- PWM Application
- Power Management



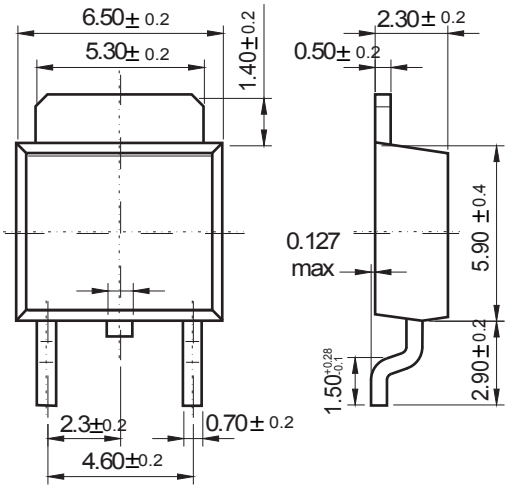
TO-252-3L Top View



Schematic Diagram

TO-252

Unit: mm



Dimensions in inches and (millimeters)

Product Summary

Parameters	Value	Unit
V_{DSS}	100	V
$V_{GS(th)\_Typ}$	1.5	V
I_D(@V_{GS}=10V)	20	A
$R_{DS(ON)\_Typ}$(@V_{GS}=10V	34	mΩ
$R_{DS(ON)\_Typ}$(@V_{GS}=4.5V	36	mΩ

Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DS}	Drain-to-Source Voltage		100	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Continuous Drain Current	T_C = 25°C	20	A
		T_C = 100°C	13	
I_{DM}	Pulsed Drain Current (1)		Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy (2)		31	mJ
P_D	Power Dissipation	T_C = 25°C	40	W
		T_C = 100°C	16	
T_J, T_{STG}	Junction & Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(3)	37	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	

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Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 100V, V_{GS} = 0V	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.5	2.2	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance(4)	V_{GS} = 10V, I_D = 10A	-	34	48	mΩ
		V_{GS} = 4.5V, I_D = 6A	-	36	55	mΩ
Dynamic Characteristics						
R_g	Gate Resistance	f = 1MHz	-	1.8	-	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz	1261	1766	2384	pF
C_{oss}	Output Capacitance		45	63	85	pF
C_{rss}	Reverse Transfer Capacitance		39	55	74	pF
Q_g	Total Gate Charge	V_{GS} = 0 to 10V V_{DS} = 50V, I_D = 20A	31	44	59	nC
Q_{gs}	Gate Source Charge		5	6	9	nC
Q_{gd}	Gate Drain("Miller") Charge		8	12	16	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	V_{GS} = 10V, V_{DD} = 50V I_D= 20A, R_{GEN} = 3Ω	-	8	-	ns
t_r	Turn-On Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	39	-	ns
t_f	Turn-Off Fall Time		-	8	-	ns
Body Diode Characteristics						
I_S	Maximum Continuous Body Diode Forward Current		-	-	20	A
I_{SM}	Maximum Pulsed Body Diode Forward Current		-	-	81	A
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_S = 10A	-		1.2	V
trr	Body Diode Reverse Recovery Time	I_F = 20A, di/dt = 100A/us	19	26	36	ns
Qrr	Body Diode Reverse Recovery Charge		-	39.0	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. E_{AS} condition: Starting T_J=25C, V_{DD}=50V, V_G=10V, R_G=25ohm, L=0.5mH, I_{AS}=11.34A, V_{DD}=0V during time in avalanche.

3. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB.

4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

RATING AND CHARACTERISTIC CURVES (20N10)

Figure 1: Power De-rating

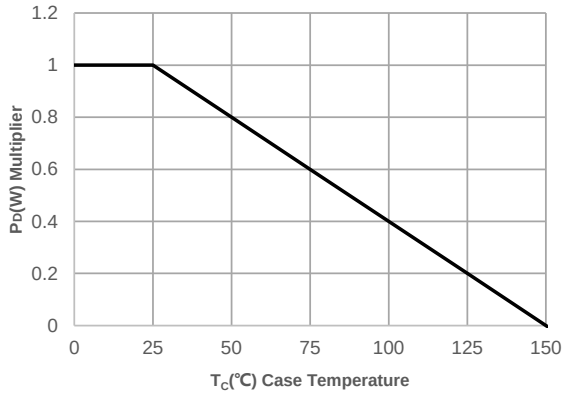


Figure 2: Current De-rating

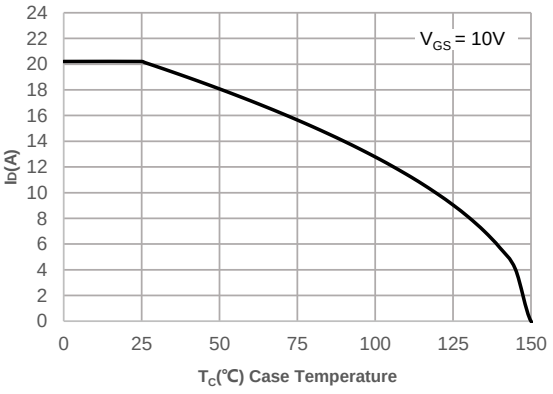


Figure 3: Normalized Maximum Transient Thermal Impedance

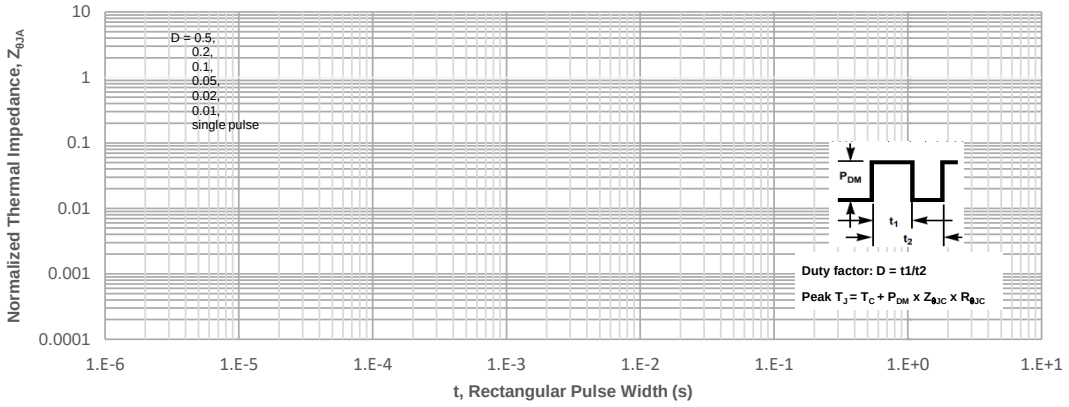
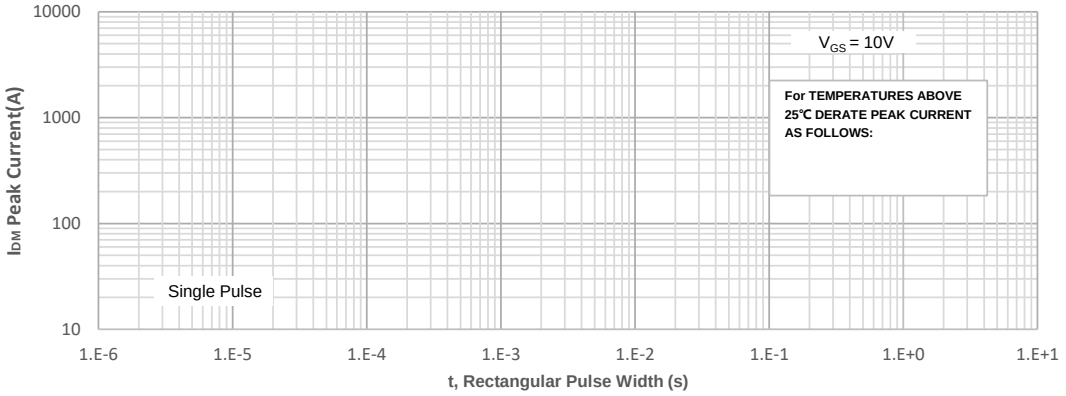


Figure 4: Peak Current Capacity



RATING AND CHARACTERISTIC CURVES (20N10)

Figure 5: Output Characteristics

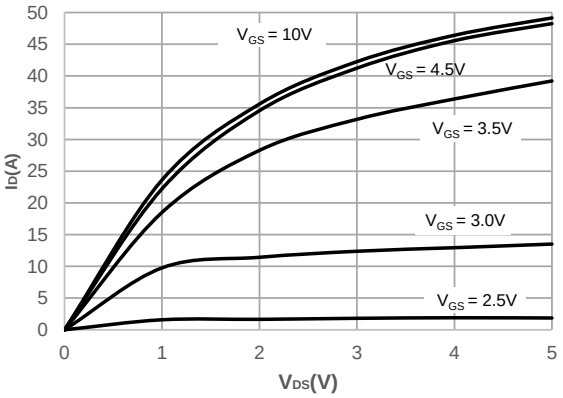


Figure 6: Typical Transfer Characteristics

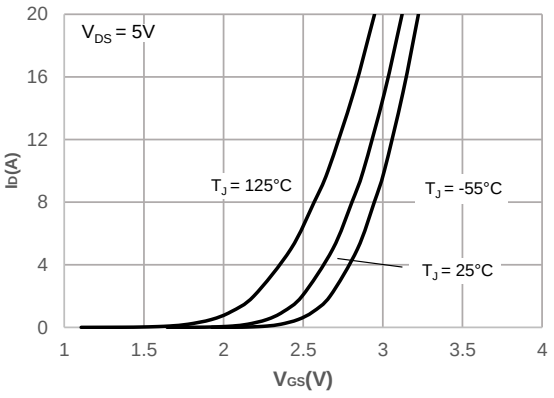


Figure 7: On-resistance vs. Drain Current

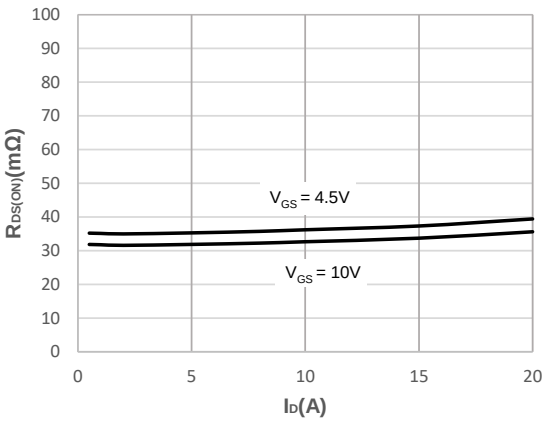


Figure 8: Body Diode Characteristics

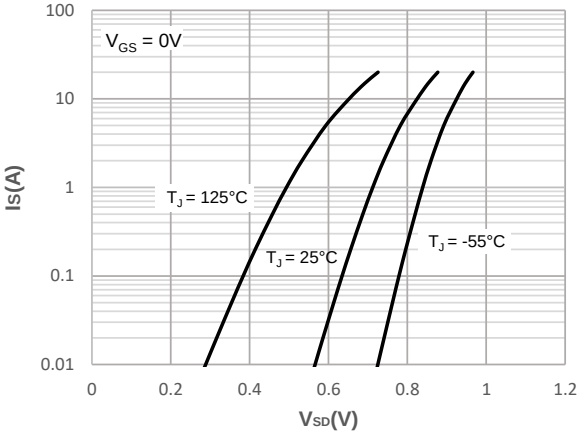


Figure 9: Gate Charge Characteristics

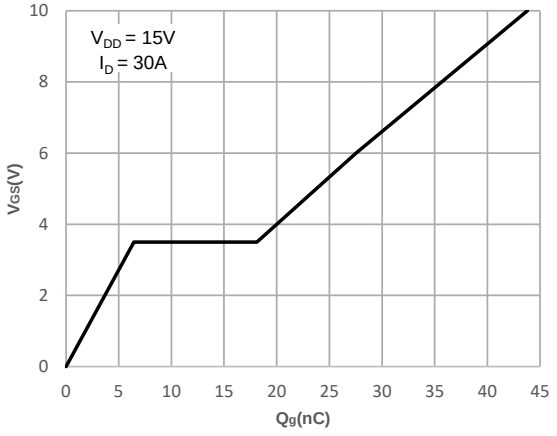
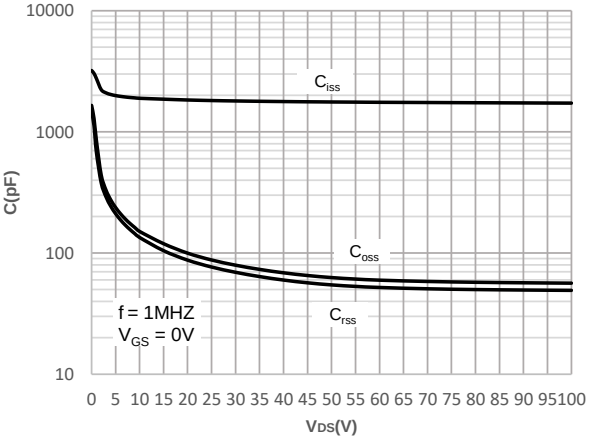


Figure 10: Capacitance Characteristics



RATING AND CHARACTERISTIC CURVES (20N10)

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

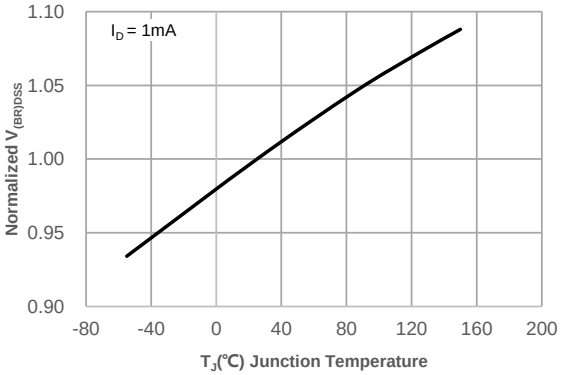


Figure 12: Normalized on Resistance vs. Junction Temperature

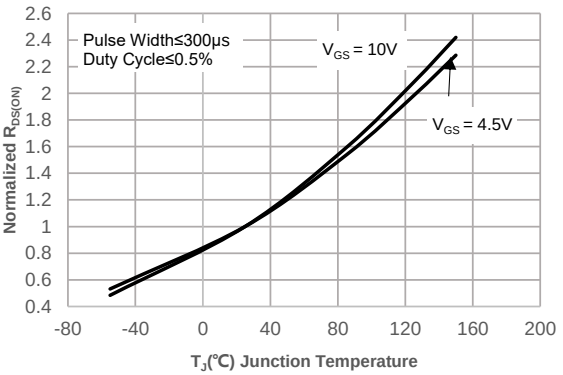


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

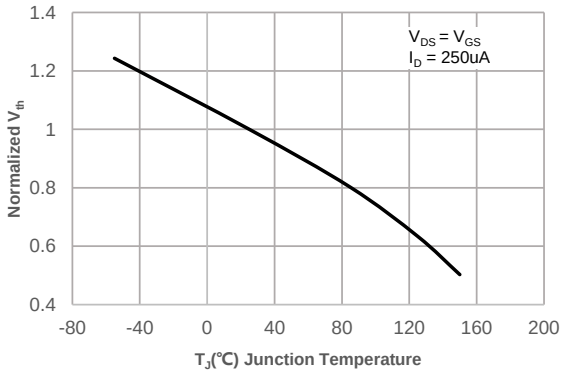


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

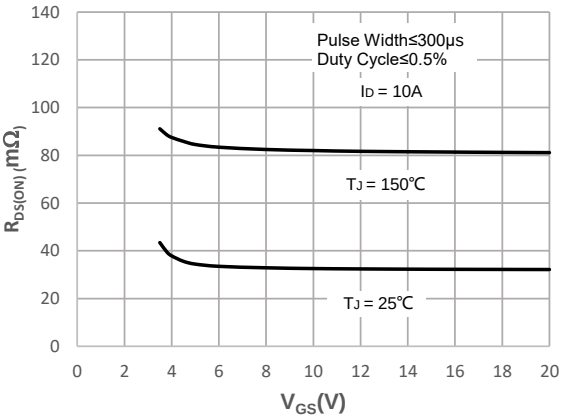
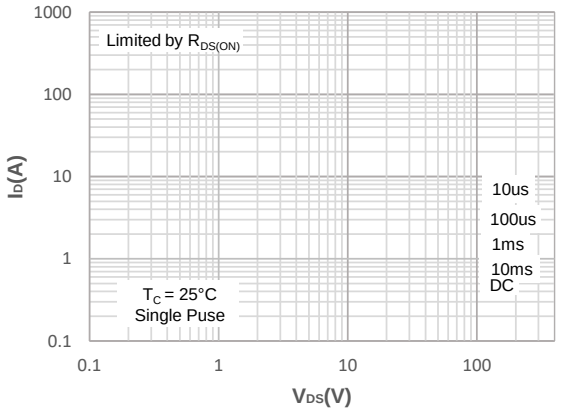


Figure 15: Maximum Safe Operating Area



Test Circuit

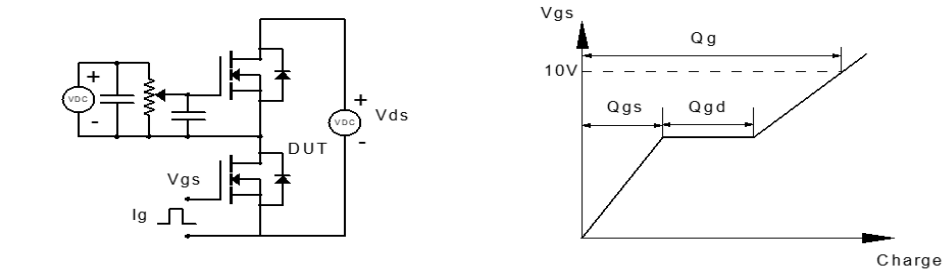


Figure 1: Gate Charge Test Circuit & Waveform

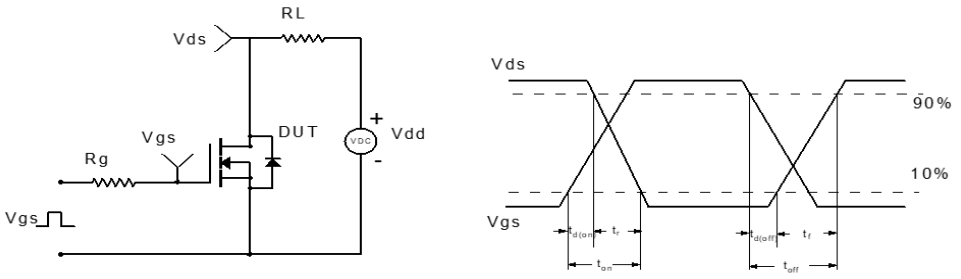


Figure 2: Resistive Switching Test Circuit & Waveform

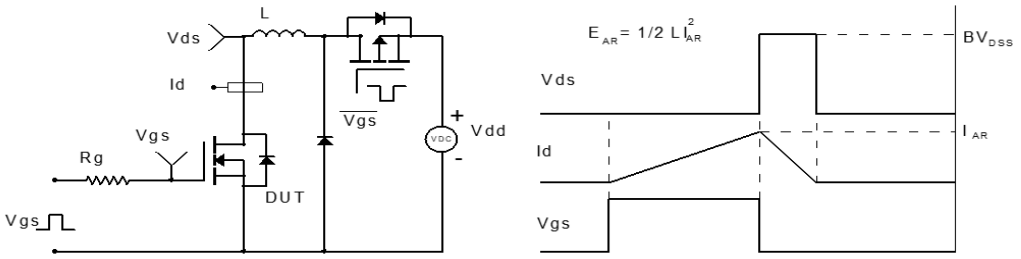


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

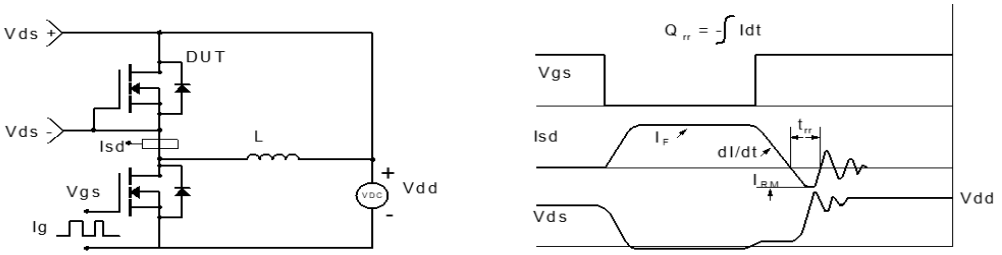


Figure 4: Diode Recovery Test Circuit & Waveform

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