

Product Summary

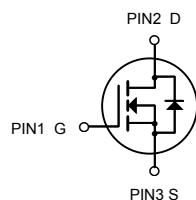
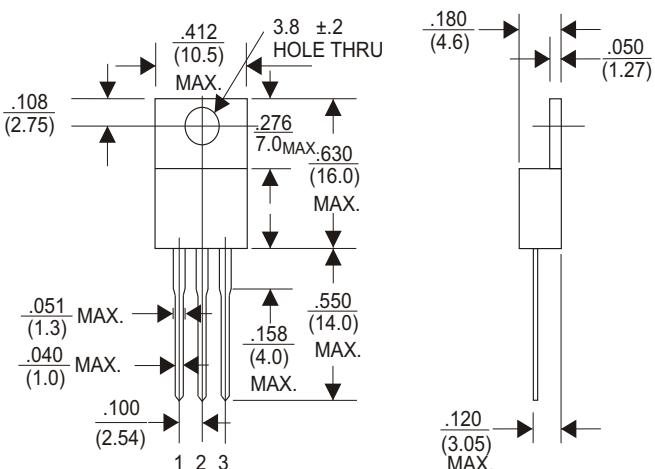
- $R_{DS(ON)}$ TYP (at $V_{GS}=10V$) 16Ω
- 100% UIS Tested
- 100% ∇V_{DS} Tested

FEATURE

High density cell design for ultra low $R_{ds(on)}$
 Fully characterized avalanche voltage and current
 Good stability and uniformity with high E_{AS}
 Excellent package for good heat dissipation
 Special process technology for high ESD capability
 Plane technology

APPLICATION

Power switching application
 Hard switched and high frequency circuits
 Uninterruptible power supply


TO-220


Dimensions in inches and (millimeters)

Maximum ratings ($T_a=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	65	A
Pulsed Drain Current	I_{DM}	240	
Single Pulsed Avalanche Energy*	E_{AS}	430	mJ
Power Dissipation	P_D	120	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-50 ~ +150	

* E_{AS} condition: $T_j=25^\circ C$, $V_{DD}=60V$, $L=0.5mH$, $R_G=25\Omega$, Starting $T_J = 25^\circ C$

65N06

Electrical characteristics ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	60			V
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}} = 60\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
Gate-body leakage current	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$			± 100	nA
On characteristics (note1)						
Gate-threshold voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2.0		3.0	V
Static drain-source on-resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 20\text{A}$		16	23	$\text{m}\Omega$
Forward transconductance	g_{fs}	$V_{\text{DS}} = 25\text{V}, I_D = 20\text{A}$	17			S
Dynamic characteristics (note 2)						
Input capacitance	C_{iss}	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$		1500		pF
Output capacitance	C_{oss}			300		
Reverse transfer capacitance	C_{rss}			90		
Switching characteristics (note 2)						
Total gate charge	Q_g	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 10\text{V}, I_D = 60\text{A}$		30		nC
Gate-source charge	Q_{gs}			10		
Gate-drain charge	Q_{gd}			11		
Turn-on delay time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 30\text{V}, I_D = 2\text{A}, V_{\text{GS}} = 10\text{V}, R_G = 2.5\Omega, R_L = 15\Omega$		22		ns
Turn-on rise time	t_r			70		
Turn-off delay time	$t_{\text{d}(\text{off})}$			70		
Turn-off fall time	t_f			35		
Drain-Source Diode Characteristics						
Drain-source diode forward voltage(note1)	V_{SD}	$V_{\text{GS}} = 0\text{V}, I_S = 40\text{A}$			1.3	V
Continuous drain-source diode forward current	I_S				60	A
Pulsed drain-source diode forward current	I_{SM}				240	A

Notes:

1. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production.

RATING AND CHARACTERISTIC CURVES (65N06)

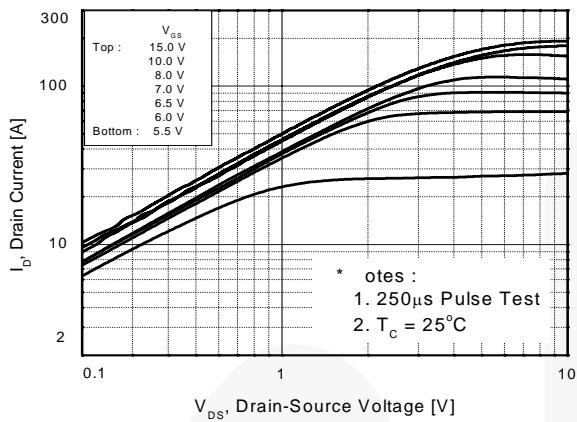


Figure 1. On-Region Characteristics

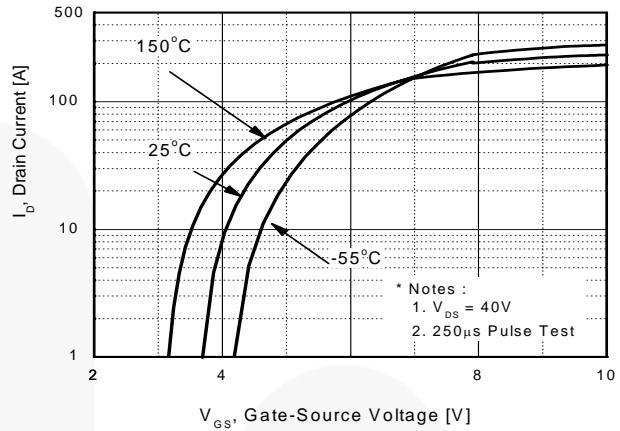


Figure 2. Transfer Characteristics

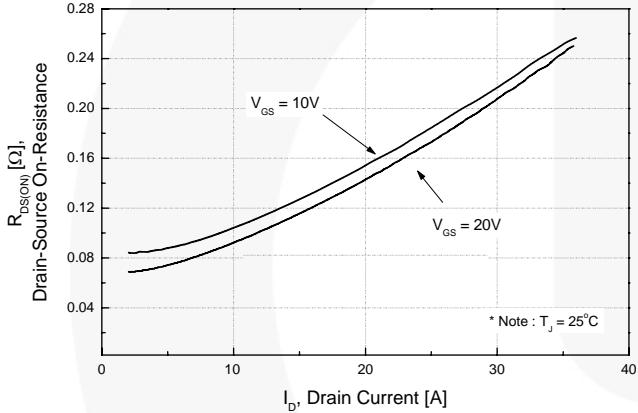


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

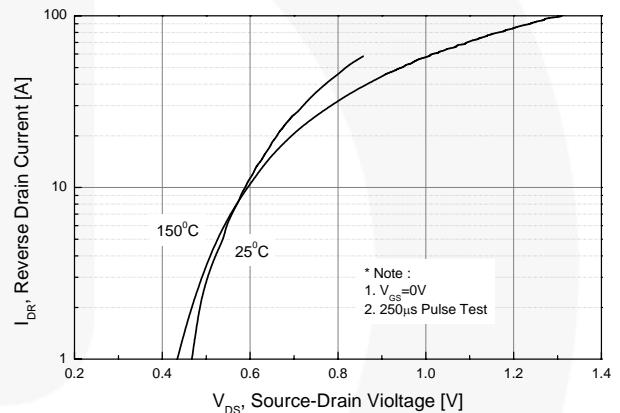


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

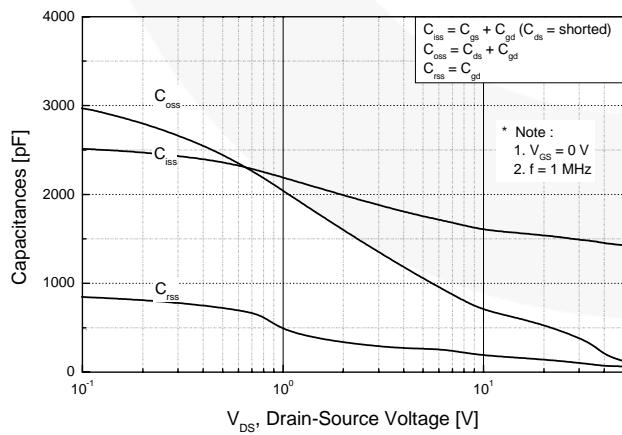


Figure 5. Capacitance Characteristics

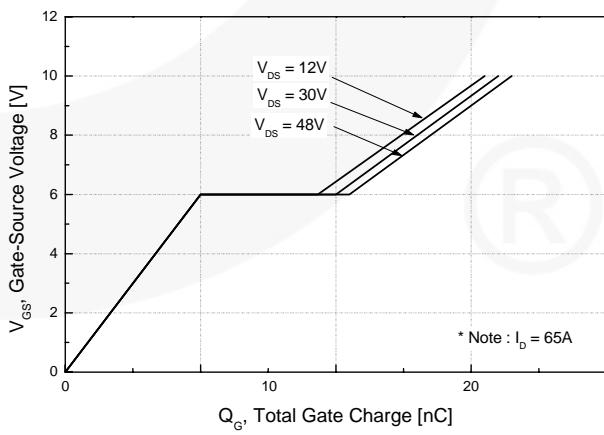


Figure 6. Gate Charge Characteristics

RATING AND CHARACTERISTIC CURVES (65N06)

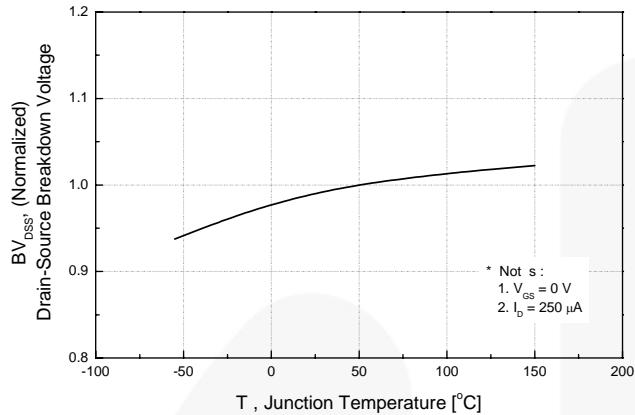


Figure 7. Breakdown Voltage Variation vs. Temperature

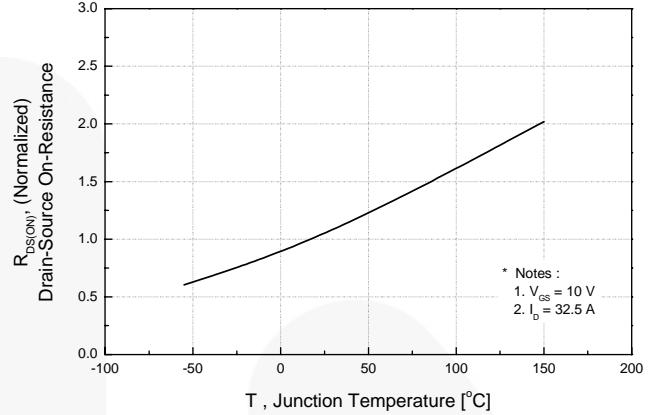


Figure 8. On-Resistance Variation vs. Temperature

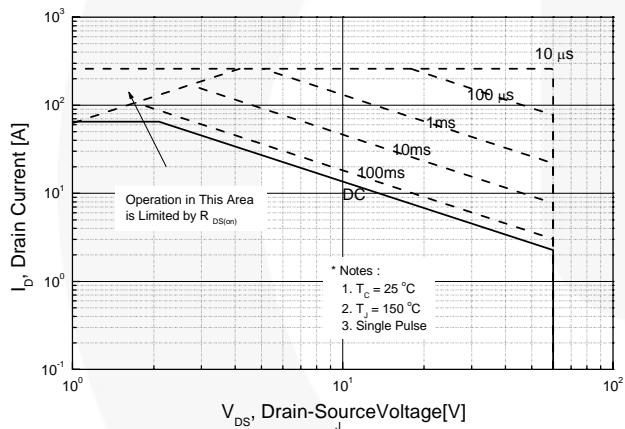


Figure 9. Maximum Safe Operating Area

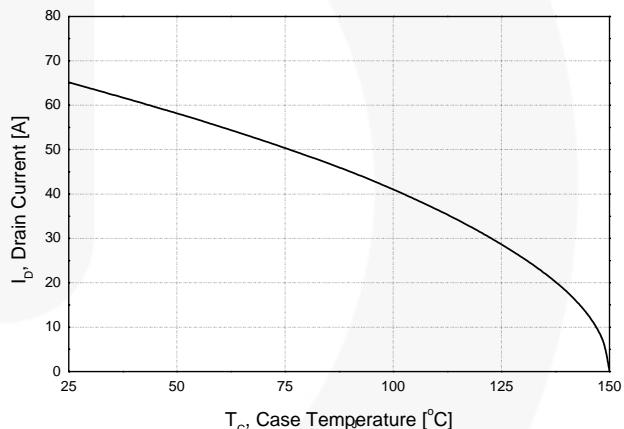


Figure 10. Maximum Drain Current vs. Case Temperature

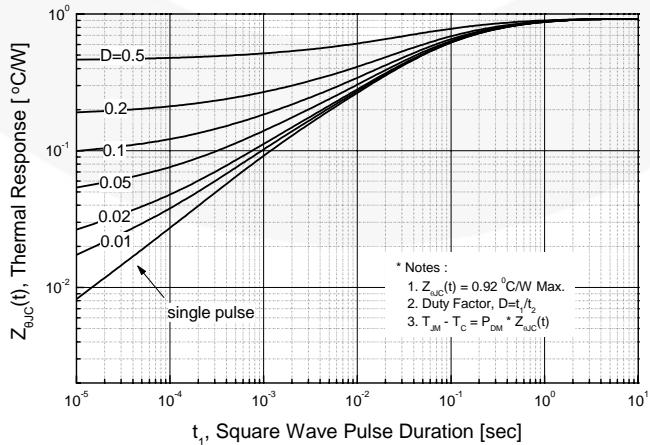


Figure 11. Transient Thermal Response Curve

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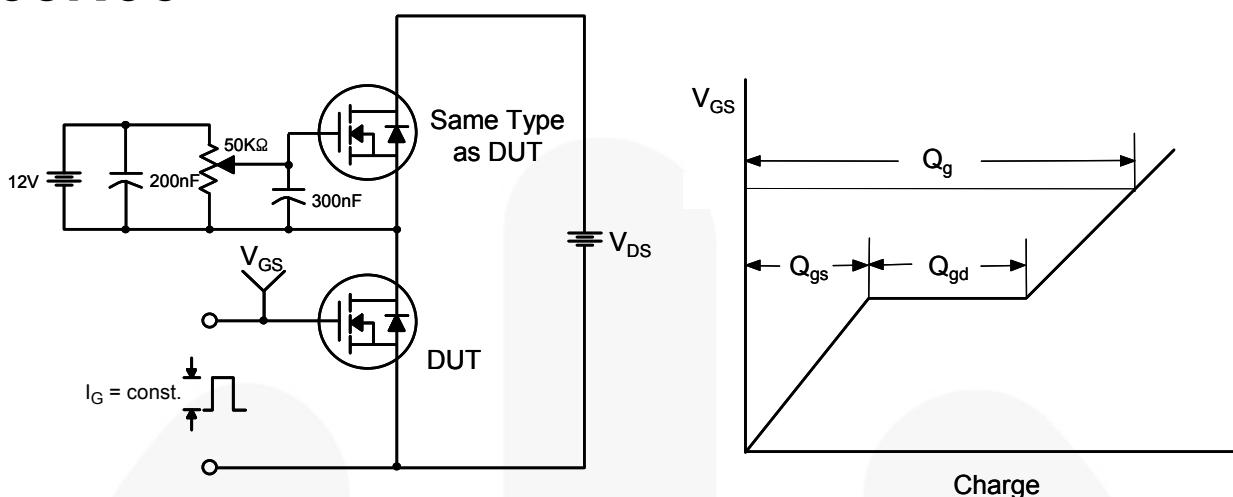


Figure 12. Gate Charge Test Circuit & Waveform

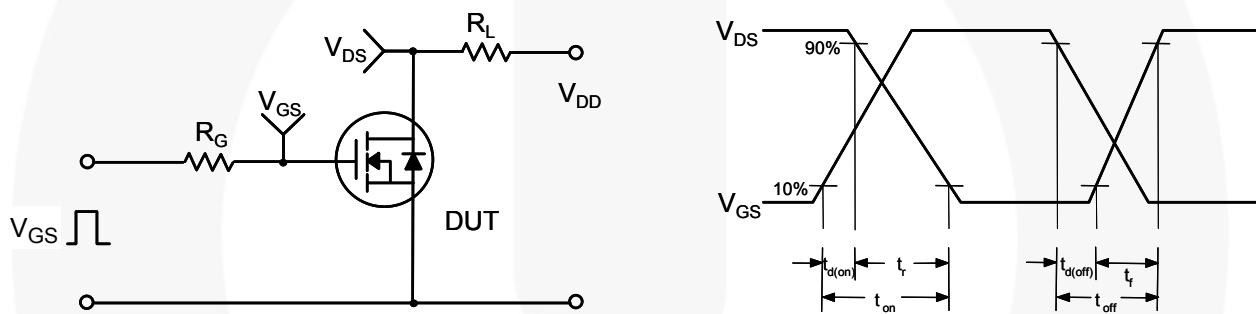


Figure 13. Resistive Switching Test Circuit & Waveforms

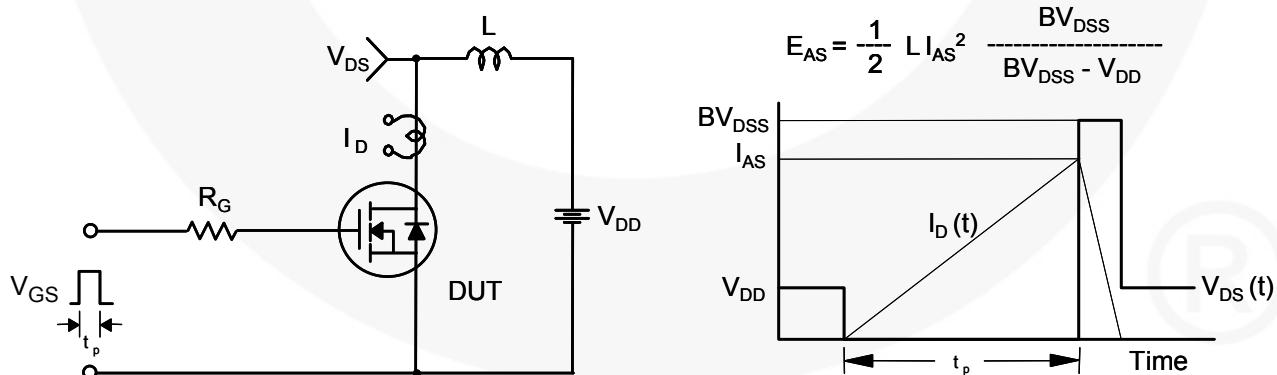


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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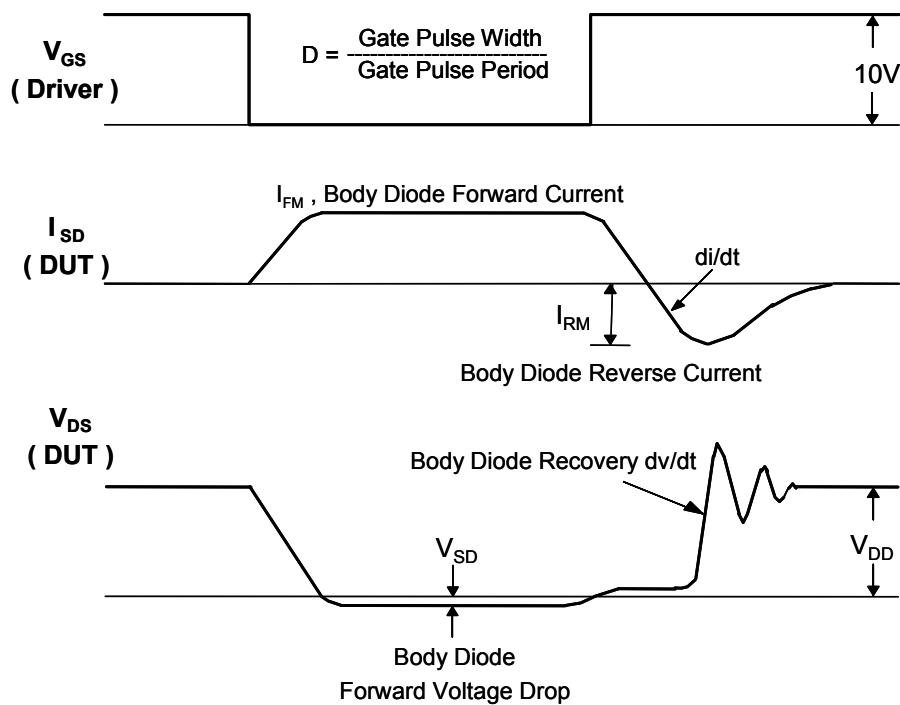
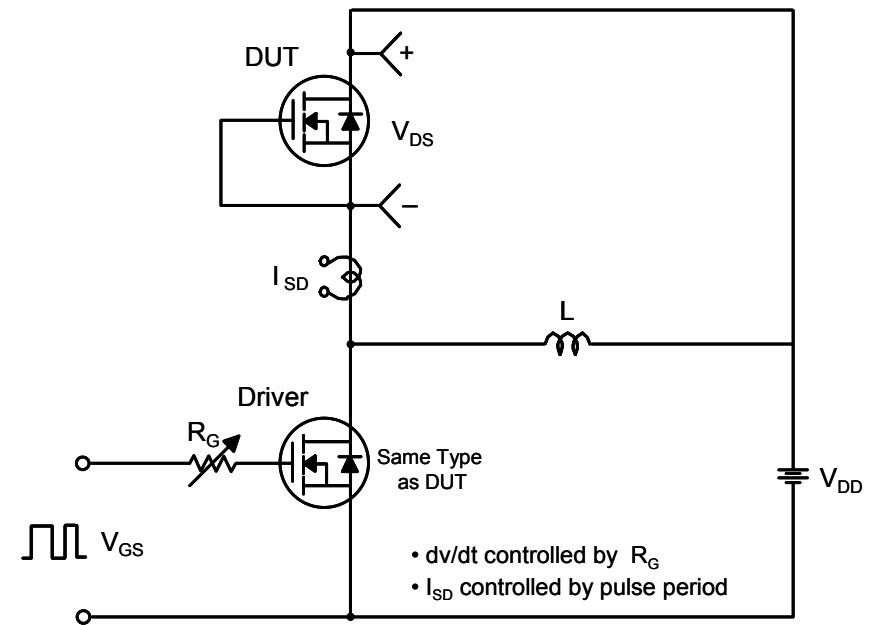


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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