GOODWORK

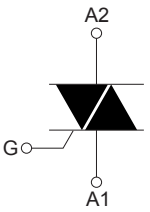
T1610, T1635, T1650
BTA16, BTB16

16 A Snubberless™, logic level and standard Triacs

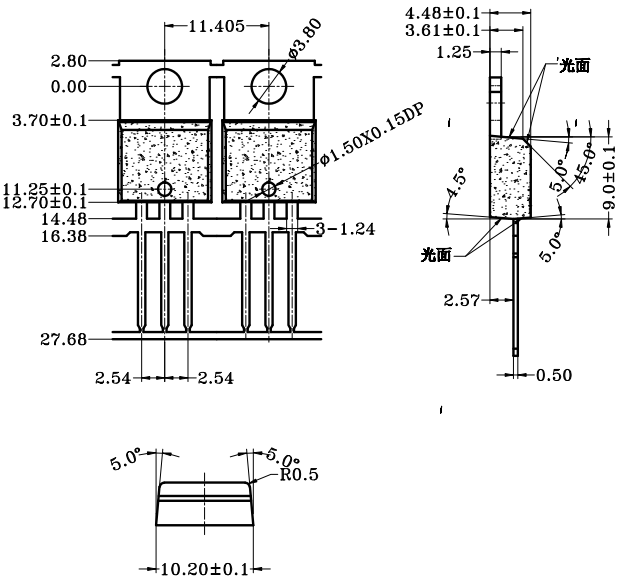
Features

Medium current Triac
Low thermal resistance with clip bonding
Low thermal resistance insulation ceramic for insulated BTA
High commutation (4Q) or very high commutation (3Q, Snubberless™) capability

BTA series UL1557 certified (file ref: 81734)
Packages are RoHS (2002/95/EC) compliant
nsulated tab (BTA series, rated at 2500 V_{RMS})



TO-220



MAXIMUM RATINGS AND ELECTRICAL CHARA CTERISTICS

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise specified)

Symbol	Parameters			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	TO-220AB, D^2PAK	T_c = 100 °C	16	A
		TO-220AB Ins.	T_c = 86 °C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C)	F = 50 Hz	t_p = 20 ms	160	A
		F = 60 Hz	t_p = 16.7 ms	168	
I^2t	I^2t value for fusing	t_p = 10 ms		144	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT} , t_r ≤ 100 ns	F = 120 Hz	T_j = 125 °C	50	A/µs
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25 °C	V_{DRM}/V_{RRM} + 100	V
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125 °C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125 °C	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +125	°C

T1610, T1635, T1650
BTA16, BTB16

Electrical characteristics (T_j = 25 °C, unless otherwise specified) - standard (4 quadrants)

Symbol	Parameters	Quadrant		BTA16 BTB16		Unit
				C	B	
I_{GT}(1)	V_D = 12 V, R_L = 33 Ω	I - II - III	Max.	25	50	mA
		IV		50	100	
V_{GT}		All	Max.	1.3		V
V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ, T_j = 125 °C	All	Min.	0.2		V
I_H(2)	I_T = 500 mA		Max.	25	50	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	Max.	40	60	mA
		II	Max.	80	120	
dV/dt(2)	$_D$ = 67 % V_{DRM} gate open, T_j = 125 °C		Min.	200	400	V/µs
(dV/dt)c(2)	(dI/dt)c = 7 A/ms, T_j = 125 °C		Min.	5	10	V/µs

1. *Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.*
2. *For both polarities of A2 referenced to A1*

Electrical characteristics (T_j = 25 °C, unless otherwise specified - Snubberless and logic level (3 quadrants)

Symbol	Parameters	Quadrant		T1610 / BTA16-SW / BTB16-SW	T1635 / BTA16-CW / BTB16-CW	T1650 / BTA16-BW / BTB16-BW	Unit
I_{GT}(1)	V_D = 12 V, R_L = 30 Ω	I - II - III	Max.	10	35	50	mA
V_{GT}			Max.	1.3			V
V_{GD}	V_D = V_{DRM}, R_L = 3,3 kΩ, T_j = 125 °C		Min.	0.2			V
I_H(2)	I_T = 500 mA		Max.	15	35	50	mA
I_L	I_G = 1.2 I_{GT}	I - III	Max.	25	50	70	mA
		II	Max.	30	60	80	
(dV/dt)(2)	VD = 67 % V_{DRM} gate open, T_j = 125 °C		Min.	40	500	1000	V/µs
(dI/dt)c(2)	(dV/dt)c = 0.1 V/µs, T_j = 125 °C		Min.	8.5			A/ms
	(dV/dt)c = 10 V/µs, T_j = 125 °C			3.0			
	Without snubber, T_j = 125 °C				8.5	14	

1. *Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.*
2. *For both polarities of A2 referenced to A1*

Static electrical characteristics

Symbol	Test conditions	T_j		Value	Unit
V_T(1)	I_{TM} = 22.5 A, t_p = 380 µs	25 °C	Max.	1.55	V
V_{TO}(1)	threshold on-state voltage	125 °C	Max.	0.85	V
R_D(1)	Dynamic resistance	125 °C	Max.	25	mΩ
I_{DRM}/I_{RRM}	V_{DRM} = V_{RRM}	25 °C	Max.	5	µA
		125 °C		2	mA

1. For both polarities of A2 referenced to A1

Thermal resistance

Symbol	Parameters		Value	Unit
$R_{th(j-c)}$	Max. junction to case (AC)	TO-220AB / D²PAK	1.2	°C/W
		TO-220AB insulated	2.1	
$R_{th(j-a)}$	Junction to ambient (S = 2 cm²)	D²PAK	45	
	Junction to ambient	TO-220AB / TO-220AB ins	60	

1. Copper surface under tab.

Figure 1. Maximum power dissipation versus on-state RMS current (full cycle)

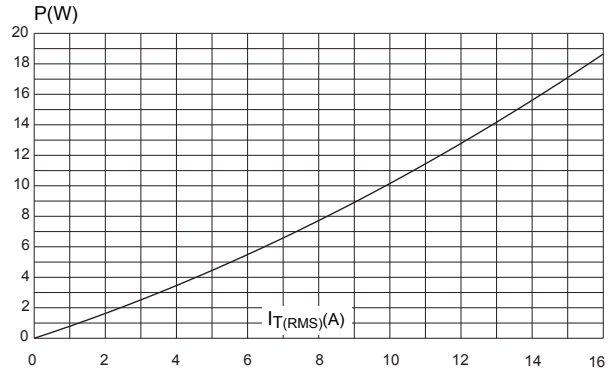


Figure 2. RMS on-state current versus case temperature (full cycle)

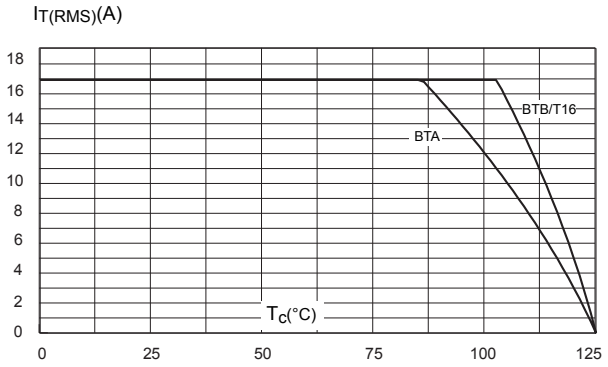


Figure 3. On-state rms current versus ambient temperature (full cycle)

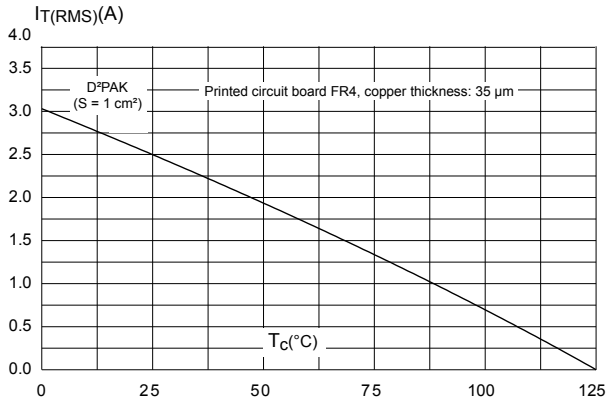


Figure 4. Relative variation of thermal impedance versus pulse duration

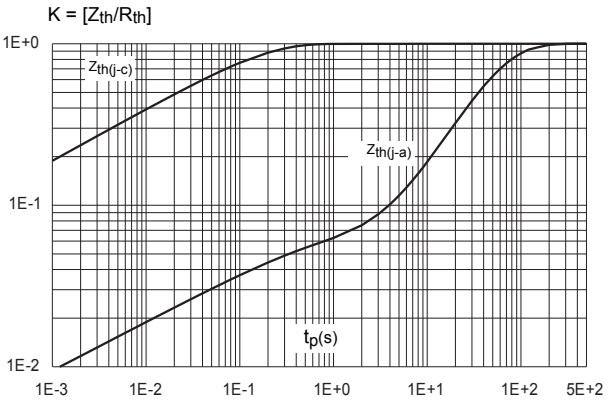


Figure 5. On-state characteristics (maximum values)

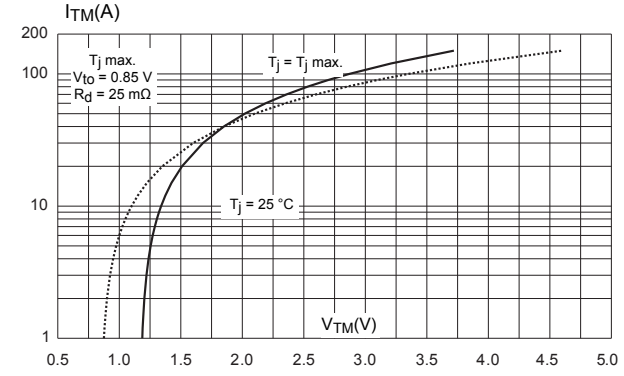


Figure 6. Surge peak on-state current versus number of cycles

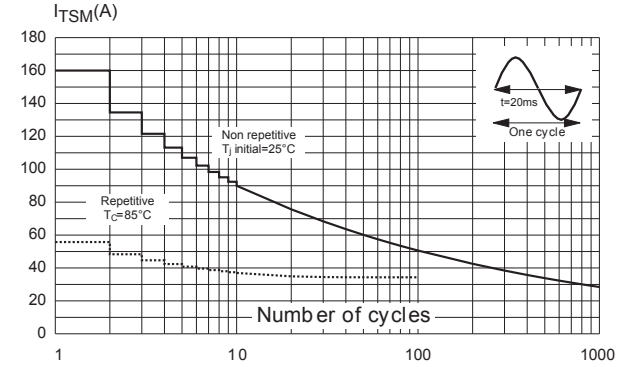


Figure 7. Non-repetitive surge peak on-state current for a sinusoidal

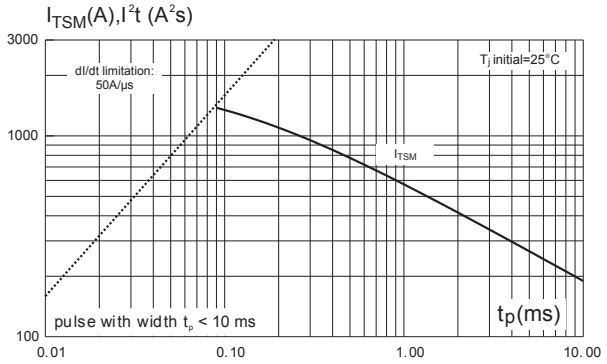


Figure 8. Relative variation of gate trigger current

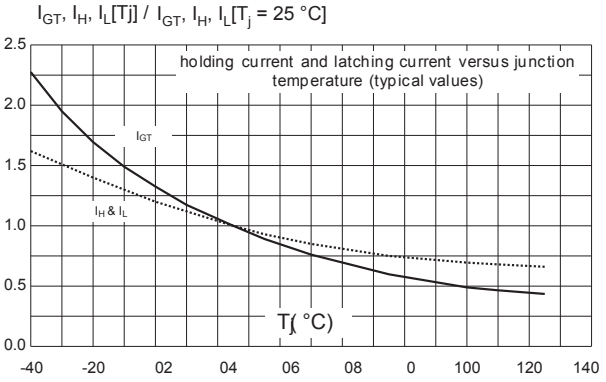


Figure 9. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

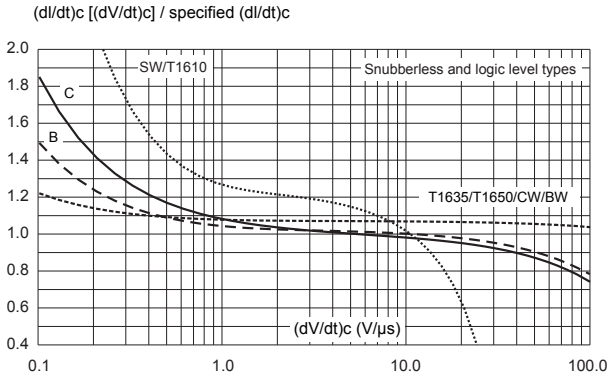


Figure 10. Relative variation of critical rate of decrease of main current versus (junction temperature (typical values)

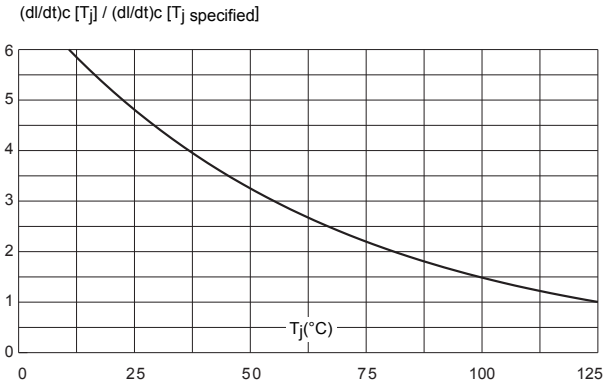
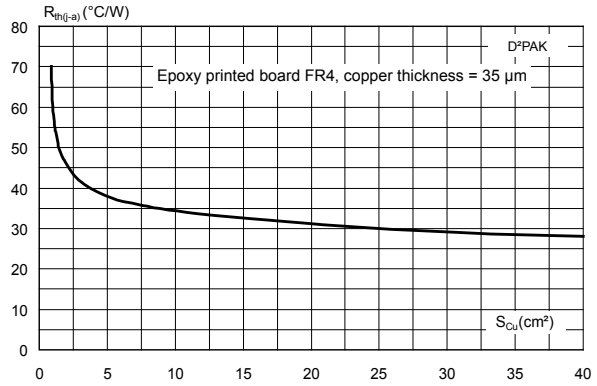


Figure 11. D²PAK thermal resistance junction to ambient versus copper surface under tab



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