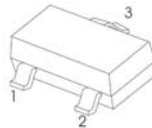


FEATURE

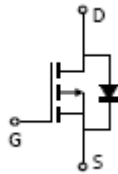
- High density cell design for low $R_{DS(ON)}$
- Voltage controlled small signal switch
- Rugged and reliable
- High saturation current capability

SOT-23



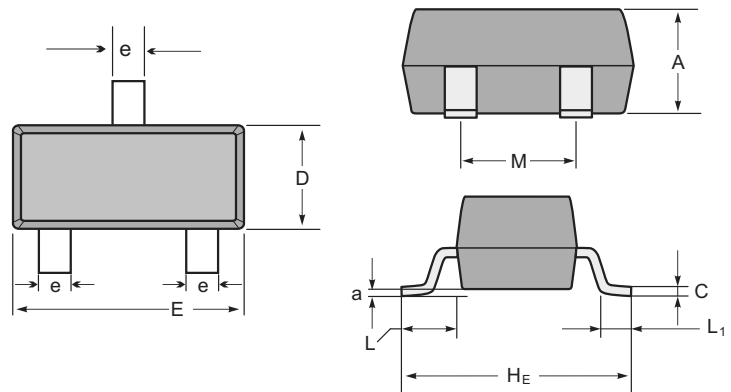
1. GATE
2. SOURCE
3. DRAIN

Equivalent Circuit



Marking

Type number	Marking code
SI2305	A5SHB



SOT-23 mechanical data

UNIT		A	C	D	E	H _E	e	M	L	L ₁	a
mm	max	1.1	0.15	1.4	3.0	2.6	0.5	1.95	0.55 (ref)	0.36 (ref)	0.0
	min	0.9	0.08	1.2	2.8	2.2	0.3	1.7			0.15
mil	max	43	6	55	118	102	20	77	22 (ref)	14 (ref)	0.0
	min	35	3	47	110	87	12	67			6

Maximum ratings ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-12	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current	I_D	-4.1	A
Continuous Source-Drain Diode Current	I_S	-0.8	
Maximum Power Dissipation ^d	P_D	1.3	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	96.2	$^\circ\text{C/W}$
Operation Junction and Storage Temperature Range	T_J, T_{STG}	-50 ~ +150	$^\circ\text{C}$

SI2305A

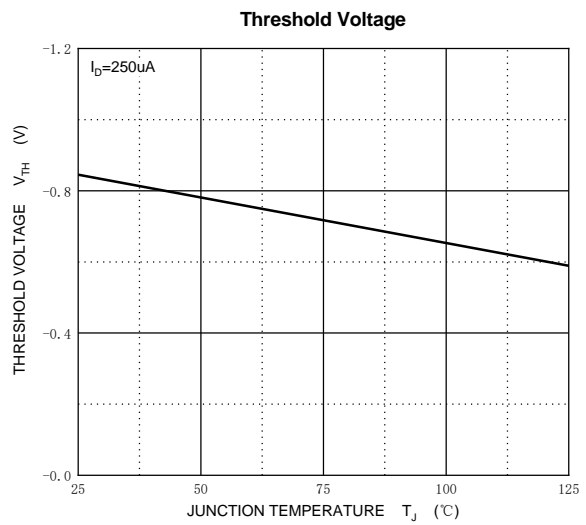
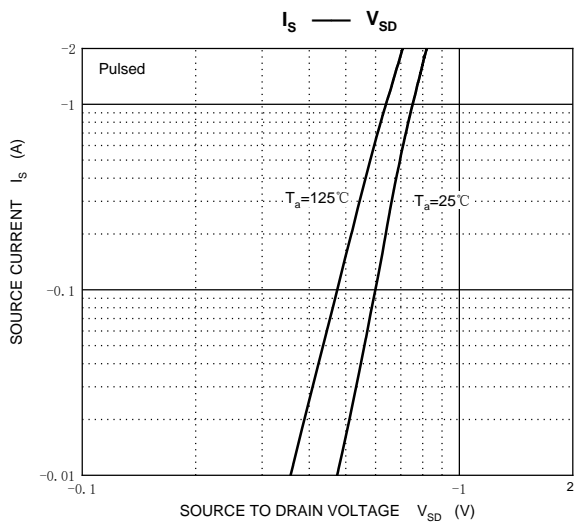
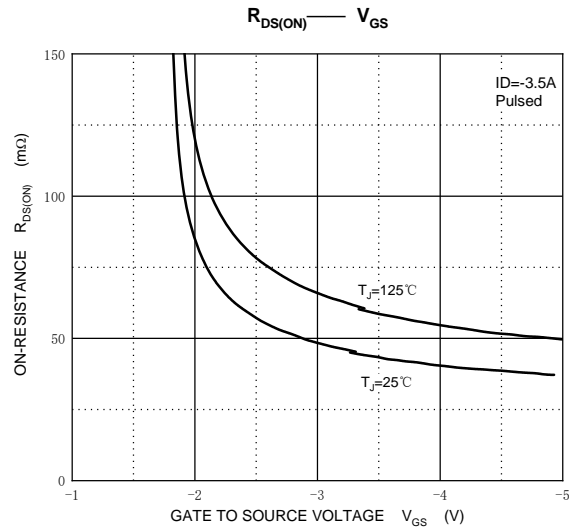
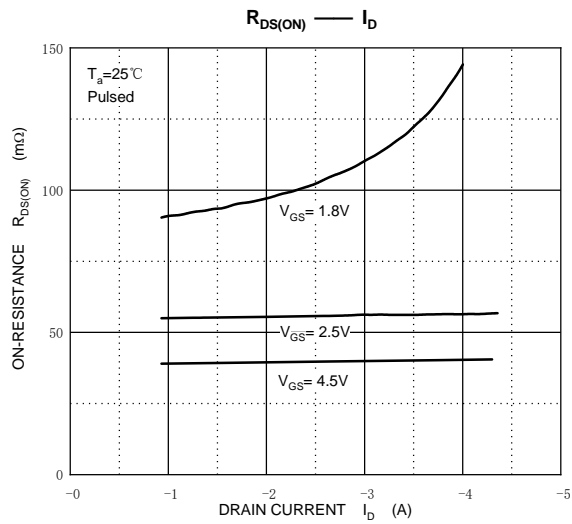
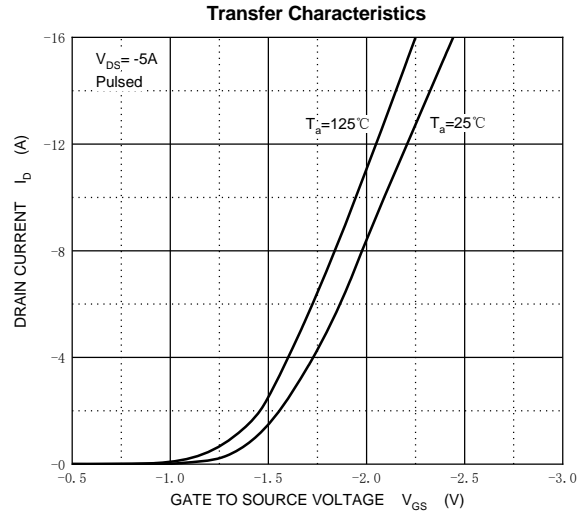
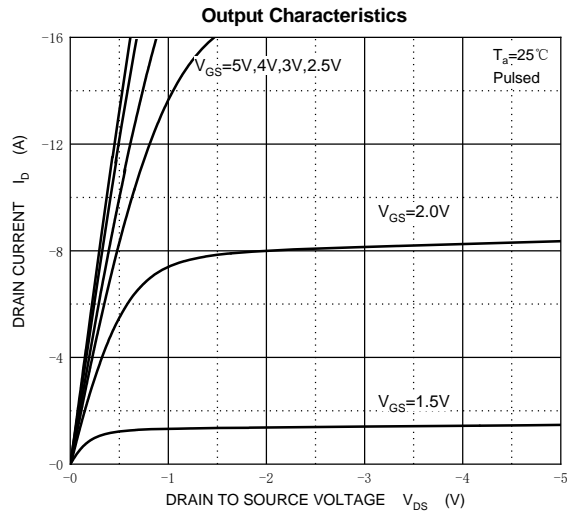
$T_a=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-12			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.5		-1	
Gate-source leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 8V$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -8V, V_{GS} = 0V$			-1	μA
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -3.5A$		40	50	m Ω
		$V_{GS} = -2.5V, I_D = -3A$		55	65	
		$V_{GS} = -1.8V, I_D = -2.0A$		90	120	
Forward transconductance ^a	g_{fs}	$V_{DS} = -5V, I_D = -4.1A$	6			S
Dynamic						
Input capacitance ^{b,c}	C_{iss}	$V_{DS} = -4V, V_{GS} = 0V, f = 1MHz$		740		pF
Output capacitance ^{b,c}	C_{oss}			290		
Reverse transfer capacitance ^{b,c}	C_{rss}			190		
Total gate charge ^b	Q_g	$V_{DS} = -4V, V_{GS} = -4.5V, I_D = -4.1A$		7.8	15	nC
		$V_{DS} = -4V, V_{GS} = -2.5V, I_D = -4.1A$		4.5	9	
Gate-source charge ^b	Q_{gs}	$V_{DS} = -4V, V_{GS} = -2.5V, I_D = -4.1A$		1.2		
Gate-drain charge ^b	Q_{gd}			1.6		
Gate resistance ^{b,c}	R_g		$f = 1MHz$	1.4	7	
Turn-on delay time ^{b,c}	$t_{d(on)}$	$V_{DD} = -4V, R_L = 1.2\Omega, I_D \approx -3.3A, V_{GEN} = -4.5V, R_g = 1\Omega$		13	20	ns
Rise time ^{b,c}	t_r			35	53	
Turn-off Delay time ^{b,c}	$t_{d(off)}$			32	48	
Fall time ^{b,c}	t_f			10	20	
Turn-on delay time ^{b,c}	$t_{d(on)}$	$V_{DD} = -4V, R_L = 1.2\Omega, I_D \approx -3.3A, V_{GEN} = -8V, R_g = 1\Omega$		5	10	
Rise time ^{b,c}	t_r			11	17	
Turn-off delay time ^{b,c}	$t_{d(off)}$			22	33	
Fall time ^{b,c}	t_f			16	24	
Drain-source body diode characteristics						
Continuous source-drain diode current	I_S	$T_C = 25^\circ C$			-1.4	A
Pulse diode forward current ^a	I_{SM}				-10	
Body diode voltage	V_{SD}	$I_F = -3.3A$			-1.2	V

Note :

- a. Pulse Test ; Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. These parameters have no way to verify.
- d. Device mounted on 1"x1" FR-4 PCB with high coverage 2oz Copper ,double sided. Copper, $t \leq 10s$.

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