

TSOP, FP-BGA  
Commercial Temp  
Industrial Temp

## 512K x 8 4Mb Asynchronous SRAM

8, 10, 12 ns  
3.3 V  $V_{DD}$   
Center  $V_{DD}$  and  $V_{SS}$

### Features

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 120/95/85 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option:  $-40^{\circ}$  to  $85^{\circ}\text{C}$
- Package line up
  - GP: RoHS-compliant 400 mil, 44-pin TSOP-II package
  - X: 6 mm x 10 mm FPBGA package
  - GX: RoHS-compliant 6 mm x 10 mm FPBGA package

### Description

The GS74108A is a high speed CMOS Static RAM organized as 524,288 words by 8 bits. Static design eliminates the need for external clocks or timing strobes. The GS74108A operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS74108A is available in 400 mil TSOP-II and 6 mm x 10 mm FPBGA packages.

### Pin Descriptions

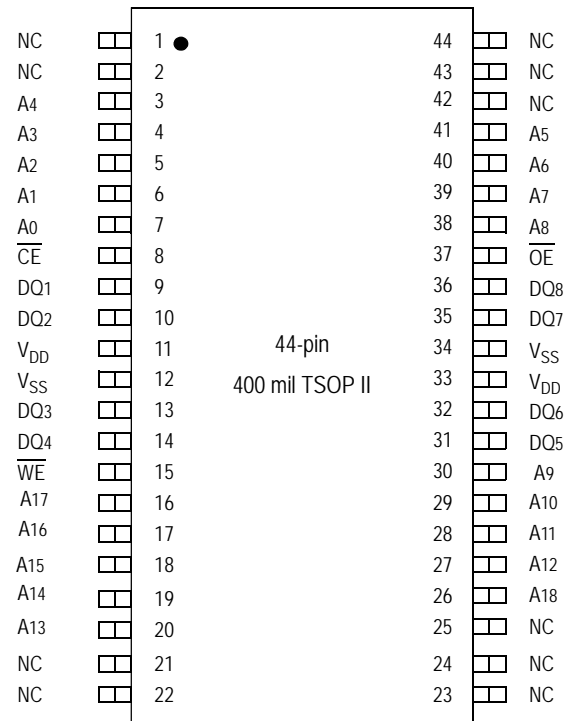
Symbol	Description
A <sub>0</sub> -A <sub>18</sub>	Address input
DQ <sub>1</sub> -DQ <sub>8</sub>	Data input/output
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
$V_{DD}$	+3.3 V power supply
$V_{SS}$	Ground
NC	No connect

### FP-BGA 512K x 8 Bump Configuration (Package X)

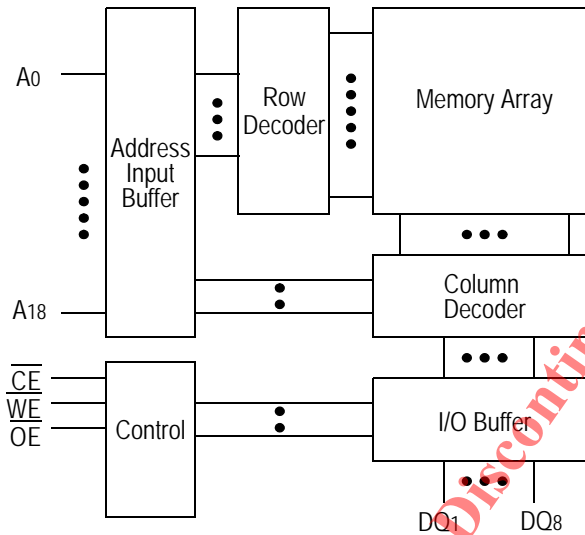
	1	2	3	4	5	6
A	NC	$\overline{\text{OE}}$	A <sub>2</sub>	A <sub>6</sub>	A <sub>7</sub>	NC
B	DQ <sub>1</sub>	NC	A <sub>1</sub>	A <sub>5</sub>	$\overline{\text{CE}}$	DQ <sub>8</sub>
C	DQ <sub>2</sub>	NC	A <sub>0</sub>	A <sub>4</sub>	NC	DQ <sub>7</sub>
D	$V_{SS}$	NC	A <sub>18</sub>	A <sub>3</sub>	NC	$V_{DD}$
E	$V_{DD}$	NC	A <sub>17</sub>	A <sub>9</sub>	NC	$V_{SS}$
F	DQ <sub>3</sub>	NC	A <sub>13</sub>	A <sub>10</sub>	NC	DQ <sub>6</sub>
G	DQ <sub>4</sub>	NC	A <sub>14</sub>	A <sub>11</sub>	$\overline{\text{WE}}$	DQ <sub>5</sub>
H	NC	A <sub>16</sub>	A <sub>15</sub>	A <sub>12</sub>	A <sub>8</sub>	NC

6 mm x 10 mm

### TSOP-II 512K x 8-Pin Configuration



## Block Diagram



## Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ1 to DQ8	$V_{DD}$ Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	IDD
L	X	L	Write	
L	H	H	High Z	

## Note:

X: "H" or "L"

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{DD}$	-0.5 to +4.6	V
Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$ ( $\leq 4.6$ V max.)	V
Output Voltage	$V_{OUT}$	-0.5 to $V_{DD} + 0.5$ ( $\leq 4.6$ V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	$T_{STG}$	-55 to 150	$^{\circ}C$

**Note:**

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

### Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -8/-10/-12	$V_{DD}$	3.0	3.3	3.6	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	$T_{AC}$	0	—	70	$^{\circ}C$
Ambient Temperature, Industrial Range	$T_{AI}$	-40	—	85	$^{\circ}C$

**Notes:**

- Input overshoot voltage should be less than  $V_{DD} + 2$  V and not exceed 20 ns.
- Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

### Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0$ V	5	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0$ V	7	pF

**Notes:**

- Tested at  $T_A = 25^{\circ}C$ ,  $f = 1$  MHz
- These parameters are sampled and are not 100% tested.

## DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	$I_{IL}$	$V_{IN} = 0$ to $V_{DD}$	-1 $\mu$ A	1 $\mu$ A
Output Leakage Current	$I_{LO}$	Output High Z $V_{OUT} = 0$ to $V_{DD}$	-1 $\mu$ A	1 $\mu$ A
Output High Voltage	$V_{OH}$	$I_{OH} = -4$ mA	2.4	—
Output Low Voltage	$V_{OL}$	$I_{LO} = +4$ mA	—	0.4 V

## Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C			-40 to 85°C		
			8 ns	10 ns	12 ns	8 ns	10 ns	12 ns
Operating Supply Current	$I_{DD}$	$\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0$ mA	120 mA	95 mA	85 mA	130 mA	105 mA	95 mA
Standby Current	$I_{SB1}$	$\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	30 mA	25 mA	22 mA	40 mA	35 mA	32 mA
Standby Current	$I_{SB2}$	$\overline{CE} \geq V_{DD} - 0.2V$ All other inputs $\geq V_{DD} - 0.2V$ or $\leq 0.2V$	10 mA			20 mA		

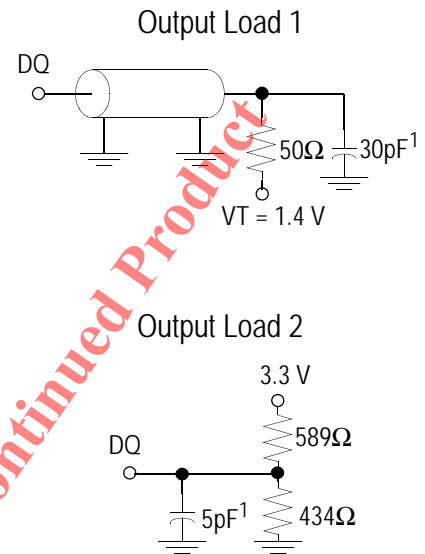
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## AC Test Conditions

Parameter	Conditions
Input high level	$V_{IH} = 2.4\text{ V}$
Input low level	$V_{IL} = 0.4\text{ V}$
Input rise time	$t_r = 1\text{ V/ns}$
Input fall time	$t_f = 1\text{ V/ns}$
Input reference level	1.4 V
Output reference level	1.4 V
Output load	Fig. 1 & 2

### Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Output load 2 for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$  and  $t_{OHZ}$



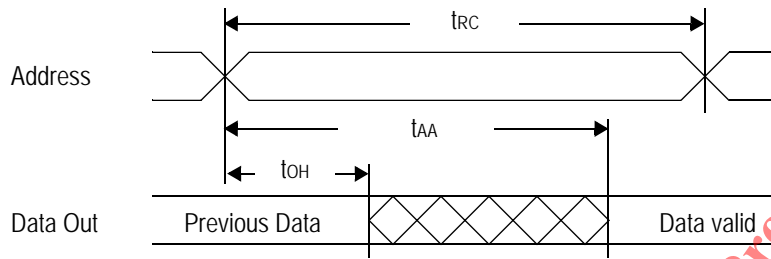
## AC Characteristics

### Read Cycle

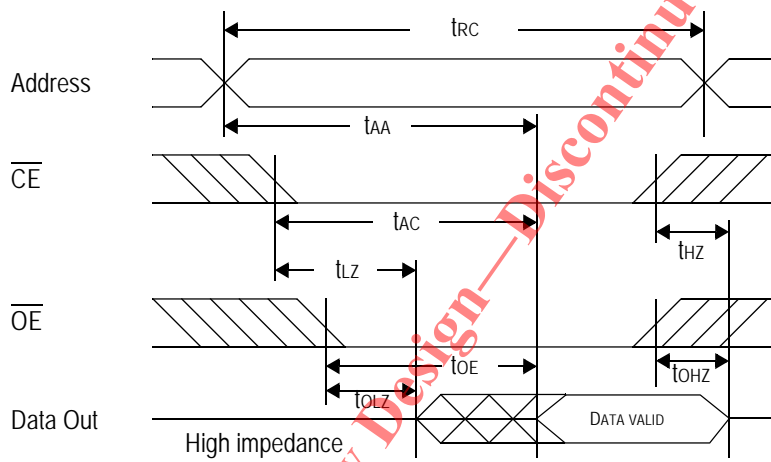
Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	8	—	10	—	12	—	ns
Address access time	$t_{AA}$	—	8	—	10	—	12	ns
Chip enable access time ( $\overline{CE}$ )	$t_{AC}$	—	8	—	10	—	12	ns
Output enable to output valid ( $\overline{OE}$ )	$t_{OE}$	—	3.5	—	4	—	5	ns
Output hold from address change	$t_{OH}$	3	—	3	—	3	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	$t_{LZ}^*$	3	—	3	—	3	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	$t_{OLZ}^*$	0	—	0	—	0	—	ns
Chip disable to output in High Z ( $\overline{CE}$ )	$t_{HZ}^*$	—	4	—	5	—	6	ns
Output disable to output in High Z ( $\overline{OE}$ )	$t_{OHZ}^*$	—	3.5	—	4	—	5	ns

\* These parameters are sampled and are not 100% tested.

Read Cycle 1:  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$



Read Cycle 2:  $\overline{WE} = V_{IH}$

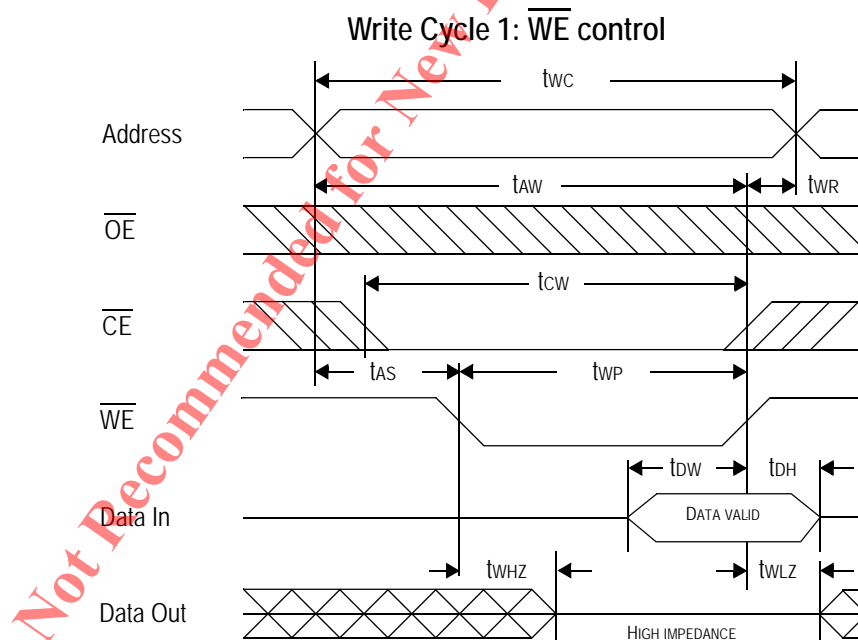


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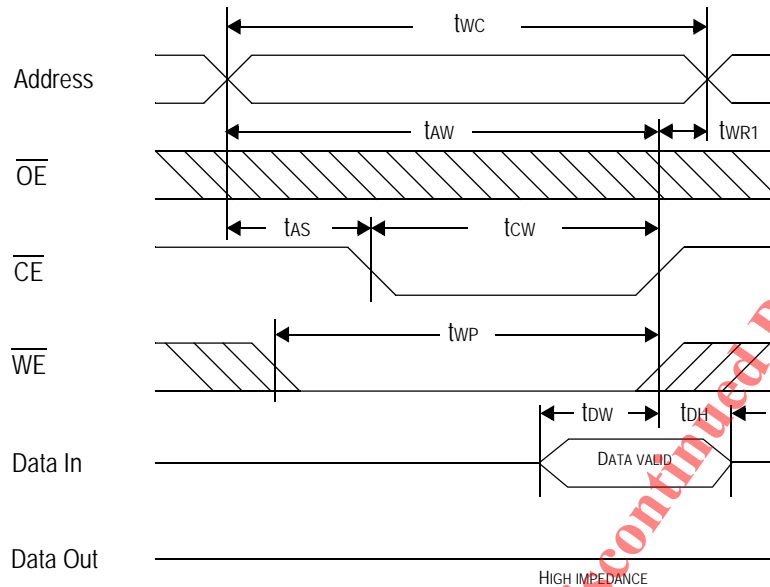
## Write Cycle

Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5.5	—	7	—	8	—	ns
Data set up time	tDW	4	—	5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	ns
Write pulse width	tWP	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	tWR	0	—	0	—	0	—	ns
Write recovery time ( $\overline{CE}$ )	tWR1	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*		3.5		4		5	ns

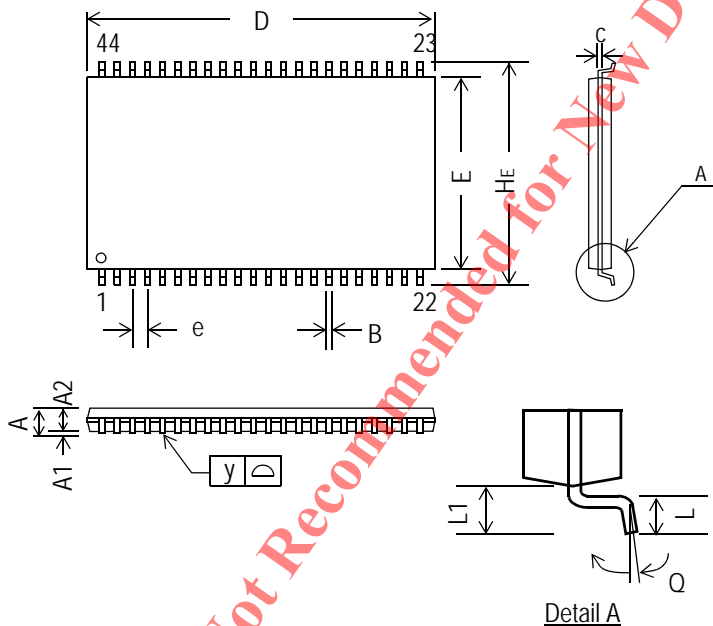
\* These parameters are sampled and are not 100% tested.



Write Cycle 2:  $\overline{CE}$  control



44-Pin, 400 mil TSOP-II



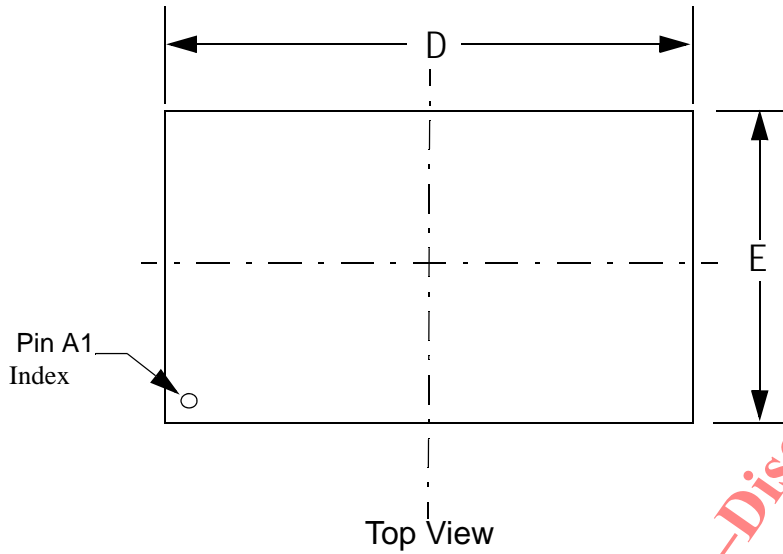
Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.047	—	—	1.20
A1	0.002	—	—	0.05	—	—
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.01	0.014	0.018	0.25	0.35	0.45
c	—	0.006	—	—	0.15	—
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	—	0.031	—	—	0.80	—
He	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	—	0.031	—	—	0.80	—
y	—	—	0.004	—	—	0.10
Q	0°	—	5°	0°	—	5°

Notes:

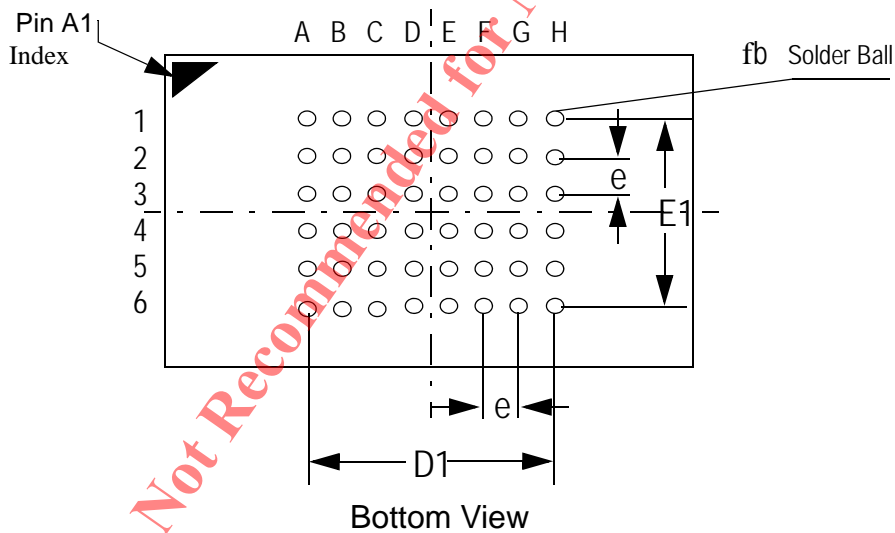
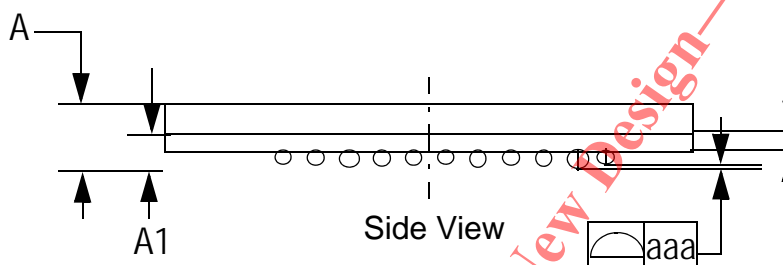
1. Dimension D & E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Controlling dimension: mm



## 6 mm x 10 mm FPBGA



Symbol	Unit: mm
A	1.10±0.10
A1	0.20-0.30
fb	f0.30-0.40
c	0.36(TYP)
D	10.0±0.05
D1	5.25
E	6.0±0.05
E1	3.75
e	0.75(TYP)
aaa	0.10



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## Ordering Information

Part Number <sup>1</sup>	Package <sup>2</sup>	Access Time	Temp. Range
GS74108AGP-8	RoHS-compliant 400 mil TSOP-II	8 ns	Commercial
GS74108AGP-10	RoHS-compliant 400 mil TSOP-II	10 ns	Commercial
GS74108AGP-12	RoHS-compliant 400 mil TSOP-II	12 ns	Commercial
GS74108AGP-8I	RoHS-compliant 400 mil TSOP-II	8 ns	Industrial
GS74108AGP-10I	RoHS-compliant 400 mil TSOP-II	10 ns	Industrial
GS74108AGP-12I	RoHS-compliant 400 mil TSOP-II	12 ns	Industrial
GS74108AX-8	6 mm x 10 mm FPBGA	8 ns	Commercial
GS74108AX-10	6 mm x 10 mm FPBGA	10 ns	Commercial
GS74108AX-12	6 mm x 10 mm FPBGA	12 ns	Commercial
GS74108AX-8I	6 mm x 10 mm FPBGA	8 ns	Industrial
GS74108AX-10I	6 mm x 10 mm FPBGA	10 ns	Industrial
GS74108AX-12I	6 mm x 10 mm FPBGA	12 ns	Industrial
GS74108AGX-8	RoHS-compliant 6 mm x 10 mm FPBGA	8 ns	Commercial
GS74108AGX-10	RoHS-compliant 6 mm x 10 mm FPBGA	10 ns	Commercial
GS74108AGX-12	RoHS-compliant 6 mm x 10 mm FPBGA	12 ns	Commercial
GS74108AGX-8I	RoHS-compliant 6 mm x 10 mm FPBGA	8 ns	Industrial
GS74108AGX-10I	RoHS-compliant 6 mm x 10 mm FPBGA	10 ns	Industrial
GS74108AGX-12I	RoHS-compliant 6 mm x 10 mm FPBGA	12 ns	Industrial

## Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS74108AGP-8T.
- Packages listed with the additional "G" designator are 6/6 RoHS compliant.

## 4M Asynchronous Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
74108A_r1	Format/Content	• Creation of new datasheet
74108A_r1; 74108A_r1_01	Content	• Added 6 ns speed bin • Updated all power numbers
74108A_r1_01; 74108A_r1_02	Content	• Updated Recommended Operating Conditions table on page 4 • Added 7 ns bin to entire document • Added X package
74108A_r1_02; 74108A_r1_03	Content	• Removed 6 ns speed bin from entire document • Corrected "X" package pinout
74108A_r1_03; 74108A_r1_04	Content	• Removed 7 ns speed bin from entire document
74108A_r1_04; 74108A_r1_05	Content	• Updated format • Added Pb-free information for TSOP-II package
74108A_r1_05; 74108A_r1_06	Content	• Added Pb-free information for FP-BGA package
74108A_r1_06; 74108A_r1_07	Content	• Added RoHS-compliant information for SOJ • Changed Pb-free references to RoHS-compliant • Added status to ordering information table
74108A_r1_07; 74108A_r1_08	Content	• Removed status from ordering information table (all parts MP) • (Rev1.08a: Removed SOJ references due to EOL)
74108A_r1_08; 74108A_r1_09	Content	• Removed 5/6 RoHS TSOP-II references due to EOL)

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[70BVXI](#) [CY62128ELL-45SX](#) [CY62146EV30LL-45ZSXA](#) [CY7C1380KV33-167AXC](#)