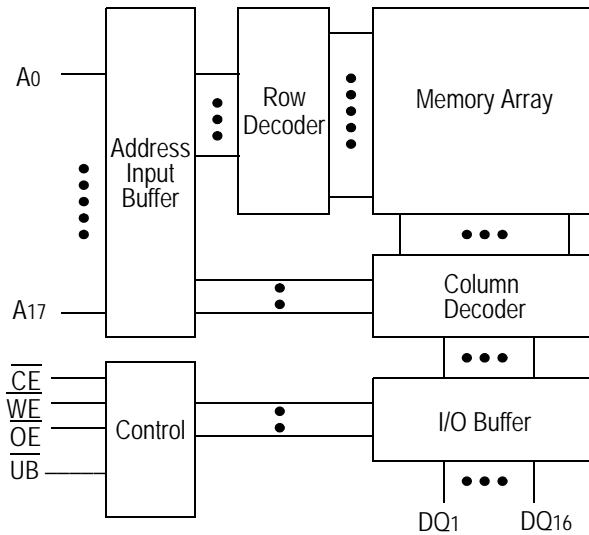




## Block Diagram



## Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | DQ1 to DQ8        | DQ9 to DQ16       | VDD Current     |
|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------|-------------------|-----------------|
| H               | X               | X               | X               | X               | Not Selected      | Not Selected      | ISB1, ISB2      |
| L               | L               | H               | L               | L               | Read              | Read              | I <sub>DD</sub> |
|                 |                 |                 | L               | H               | Read              | High Z            |                 |
|                 |                 |                 | H               | L               | High Z            | Read              |                 |
| L               | X               | L               | L               | L               | Write             | Write             |                 |
|                 |                 |                 | L               | H               | Write             | Not Write, High Z |                 |
|                 |                 |                 | H               | L               | Not Write, High Z | Write             |                 |
| L               | H               | H               | X               | X               | High Z            | High Z            |                 |
| L               | X               | X               | H               | H               | High Z            | High Z            |                 |

## Note:

X: "H" or "L"

### Absolute Maximum Ratings

| Parameter                   | Symbol    | Rating   | Unit        |
|-----------------------------|-----------|--|-------------|
| Supply Voltage              | $V_{DD}$  | -0.5 to +4.6                                   | V           |
| Input Voltage               | $V_{IN}$  | -0.5 to $V_{DD} + 0.5$<br>( $\leq 4.6$ V max.) | V           |
| Output Voltage              | $V_{OUT}$ | -0.5 to $V_{DD} + 0.5$<br>( $\leq 4.6$ V max.) | V           |
| Allowable power dissipation | PD        | 0.7  | W           |
| Storage temperature         | $T_{STG}$ | -55 to 150                                     | $^{\circ}C$ |

**Note:**

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

### Recommended Operating Conditions

| Parameter                                | Symbol   | Min  | Typ | Max            | Unit        |
|--|----------|------|-----|----------------|-------------|
| Supply Voltage for -8/-10/-12            | $V_{DD}$ | 3.0  | 3.3 | 3.6            | V           |
| Input High Voltage                       | $V_{IH}$ | 2.0  | —   | $V_{DD} + 0.3$ | V           |
| Input Low Voltage                        | $V_{IL}$ | -0.3 | —   | 0.8            | V           |
| Ambient Temperature,<br>Commercial Range | $T_{Ac}$ | 0    | —   | 70             | $^{\circ}C$ |
| Ambient Temperature,<br>Industrial Range | $T_{AI}$ | -40  | —   | 85             | $^{\circ}C$ |

**Notes:**

1. Input overshoot voltage should be less than  $V_{DD} + 2$  V and not exceed 20 ns.
2. Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

### Capacitance

| Parameter          | Symbol    | Test Condition  | Max | Unit |
|--------------------|-----------|-----------------|-----|------|
| Input Capacitance  | $C_{IN}$  | $V_{IN} = 0$ V  | 5   | pF   |
| Output Capacitance | $C_{OUT}$ | $V_{OUT} = 0$ V | 7   | pF   |

**Notes:**

1. Tested at  $T_A = 25^{\circ}C$ ,  $f = 1$  MHz
2. These parameters are sampled and are not 100% tested.

## DC I/O Pin Characteristics

| Parameter              | Symbol   | Test Conditions                            | Min        | Max       |
|------------------------|----------|--|------------|-----------|
| Input Leakage Current  | $I_{IL}$ | $V_{IN} = 0$ to $V_{DD}$                   | -1 $\mu$ A | 1 $\mu$ A |
| Output Leakage Current | $I_{LO}$ | Output High Z<br>$V_{OUT} = 0$ to $V_{DD}$ | -1 $\mu$ A | 1 $\mu$ A |
| Output High Voltage    | $V_{OH}$ | $I_{OH} = -4$ mA                           | 2.4        | —         |
| Output Low Voltage     | $V_{OL}$ | $I_{LO} = +4$ mA                           | —          | 0.4 V     |

## Power Supply Currents

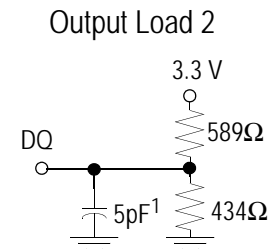
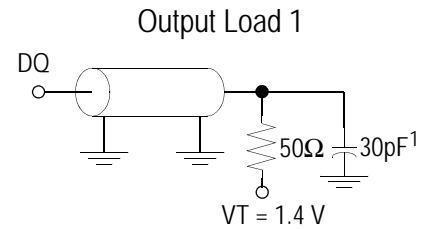
| Parameter                | Symbol    | Test Conditions   | 0 to 70°C |       |       | -40 to 85°C |       |       | Unit |
|--------------------------|-----------|---|-----------|-------|-------|-------------|-------|-------|------|
|                          |           |   | 8 ns      | 10 ns | 12 ns | 8 ns        | 10 ns | 12 ns |      |
| Operating Supply Current | $I_{DD}$  | $\overline{CE} \leq V_{IL}$<br>All other inputs $\geq V_{IH}$ or $\leq V_{IL}$<br>Min. cycle time<br>$I_{OUT} = 0$ mA | 130       | 105   | 90    | 140         | 115   | 100   | mA   |
| Standby Current          | $I_{SB1}$ | $\overline{CE} \geq V_{IH}$<br>All other inputs $\geq V_{IH}$ or $\leq V_{IL}$<br>Min. cycle time                     | 30        | 25    | 25    | 40          | 35    | 35    | mA   |
| Standby Current          | $I_{SB2}$ | $\overline{CE} \geq V_{DD} - 0.2V$<br>All other inputs $\geq V_{DD} - 0.2V$ or $\leq 0.2V$                            | 10        |       |       | 20          |       |       | mA   |

## AC Test Conditions

| Parameter              | Conditions               |
|------------------------|--------------------------|
| Input high level       | $V_{IH} = 2.4 \text{ V}$ |
| Input low level        | $V_{IL} = 0.4 \text{ V}$ |
| Input rise time        | $t_r = 1 \text{ V/ns}$   |
| Input fall time        | $t_f = 1 \text{ V/ns}$   |
| Input reference level  | 1.4 V                    |
| Output reference level | 1.4 V                    |
| Output load            | Fig. 1 & 2               |

**Notes:**

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Output load 2 for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$  and  $t_{OHZ}$



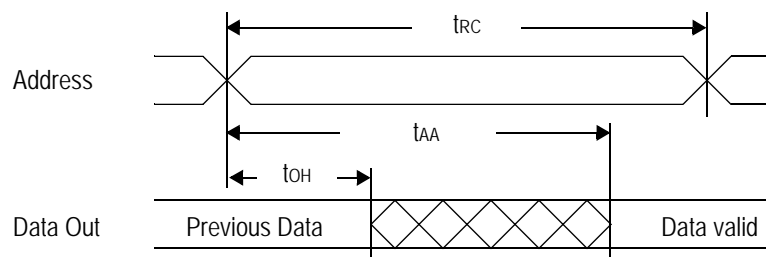
## AC Characteristics

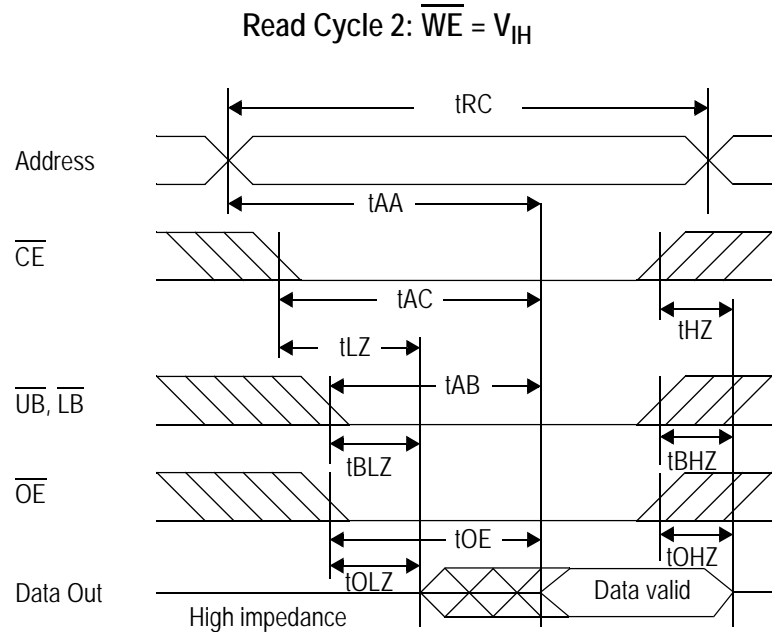
## Read Cycle

| Parameter  | Symbol      | -8  |     | -10 |     | -12 |     | Unit |
|--|-------------|-----|-----|-----|-----|-----|-----|------|
|  |             | Min | Max | Min | Max | Min | Max |      |
| Read cycle time  | $t_{RC}$    | 8   | —   | 10  | —   | 12  | —   | ns   |
| Address access time  | $t_{AA}$    | —   | 8   | —   | 10  | —   | 12  | ns   |
| Chip enable access time ( $\overline{CE}$ )                            | $t_{AC}$    | —   | 8   | —   | 10  | —   | 12  | ns   |
| Byte enable access time ( $\overline{UB}$ , $\overline{LB}$ )          | $t_{AB}$    | —   | 3.5 | —   | 4   | —   | 5   | ns   |
| Output enable to output valid ( $\overline{OE}$ )                      | $t_{OE}$    | —   | 3.5 | —   | 4   | —   | 5   | ns   |
| Output hold from address change  | $t_{OH}$    | 3   | —   | 3   | —   | 3   | —   | ns   |
| Chip enable to output in low Z ( $\overline{CE}$ )                     | $t_{LZ}^*$  | 3   | —   | 3   | —   | 3   | —   | ns   |
| Output enable to output in low Z ( $\overline{OE}$ )                   | $t_{OLZ}^*$ | 0   | —   | 0   | —   | 0   | —   | ns   |
| Byte enable to output in low Z ( $\overline{UB}$ , $\overline{LB}$ )   | $t_{BLZ}^*$ | 0   | —   | 0   | —   | 0   | —   | ns   |
| Chip disable to output in High Z ( $\overline{CE}$ )                   | $t_{HZ}^*$  | —   | 4   | —   | 5   | —   | 6   | ns   |
| Output disable to output in High Z ( $\overline{OE}$ )                 | $t_{OHZ}^*$ | —   | 3.5 | —   | 4   | —   | 5   | ns   |
| Byte disable to output in High Z ( $\overline{UB}$ , $\overline{LB}$ ) | $t_{BHZ}^*$ | —   | 3.5 | —   | 4   | —   | 5   | ns   |

\* These parameters are sampled and are not 100% tested.

Read Cycle 1:  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ ,  $\overline{UB}$  and, or  $\overline{LB} = V_{IL}$



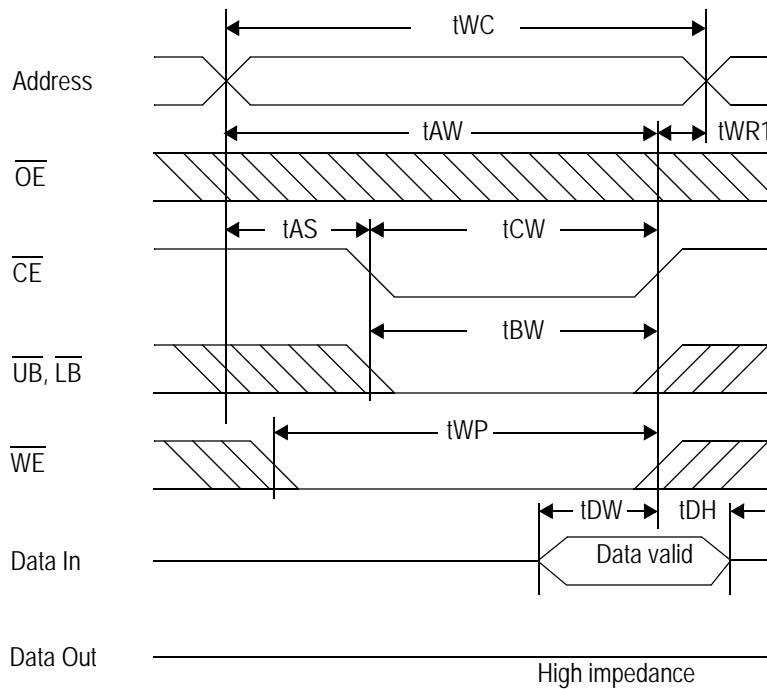


### Write Cycle

| Parameter                               | Symbol      | -8  |     | -10 |     | -12 |     | Unit |
|---|-------------|-----|-----|-----|-----|-----|-----|------|
|   |             | Min | Max | Min | Max | Min | Max |      |
| Write cycle time                        | $t_{WC}$    | 8   | —   | 10  | —   | 12  | —   | ns   |
| Address valid to end of write           | $t_{AW}$    | 5.5 | —   | 7   | —   | 8   | —   | ns   |
| Chip enable to end of write             | $t_{CW}$    | 5.5 | —   | 7   | —   | 8   | —   | ns   |
| Byte enable to end of write             | $t_{BW}$    | 5.5 | —   | 7   | —   | 8   | —   | ns   |
| Data set up time                        | $t_{DW}$    | 4   | —   | 4.5 | —   | 6   | —   | ns   |
| Data hold time                          | $t_{DH}$    | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write pulse width                       | $t_{WP}$    | 5.5 | —   | 7   | —   | 8   | —   | ns   |
| Address set up time                     | $t_{AS}$    | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write recovery time ( $\overline{WE}$ ) | $t_{WR}$    | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write recovery time ( $\overline{CE}$ ) | $t_{WR1}$   | 0   | —   | 0   | —   | 0   | —   | ns   |
| Output Low Z from end of write          | $t_{WLZ}^*$ | 3   | —   | 3   | —   | 3   | —   | ns   |
| Write to output in High Z               | $t_{WHZ}^*$ | —   | 3.5 | —   | 4   | —   | 5   | ns   |

\* These parameters are sampled and are not 100% tested.

Write Cycle 1:  $\overline{WE}$  control

 Write Cycle 2:  $\overline{CE}$  control




Write Cycle 3:  $\overline{UB}$ ,  $\overline{LB}$  control


## 44-Pin, 400 mil TSOP-II

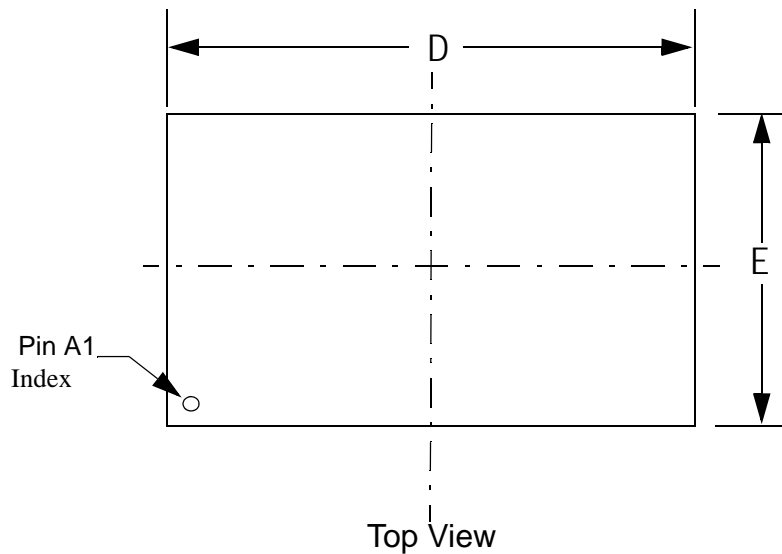


| Symbol | Dimension in inch |       |       | Dimension in mm |       |       |
|--------|-------------------|-------|-------|-----------------|-------|-------|
|        | min               | nom   | max   | min             | nom   | max   |
| A      | —                 | —     | 0.047 | —               | —     | 1.20  |
| A1     | 0.002             | —     | —     | 0.05            | —     | —     |
| A2     | 0.037             | 0.039 | 0.041 | 0.95            | 1.00  | 1.05  |
| B      | 0.01              | 0.014 | 0.018 | 0.25            | 0.35  | 0.45  |
| c      | —                 | 0.006 | —     | —               | 0.15  | —     |
| D      | 0.721             | 0.725 | 0.729 | 18.31           | 18.41 | 18.51 |
| E      | 0.396             | 0.400 | 0.404 | 10.06           | 10.16 | 10.26 |
| e      | —                 | 0.031 | —     | —               | 0.80  | —     |
| HE     | 0.455             | 0.463 | 0.471 | 11.56           | 11.76 | 11.96 |
| L      | 0.016             | 0.020 | 0.024 | 0.40            | 0.50  | 0.60  |
| L1     | —                 | 0.031 | —     | —               | 0.80  | —     |
| y      | —                 | —     | 0.004 | —               | —     | 0.10  |
| Q      | 0°                | —     | 5°    | 0°              | —     | 5°    |

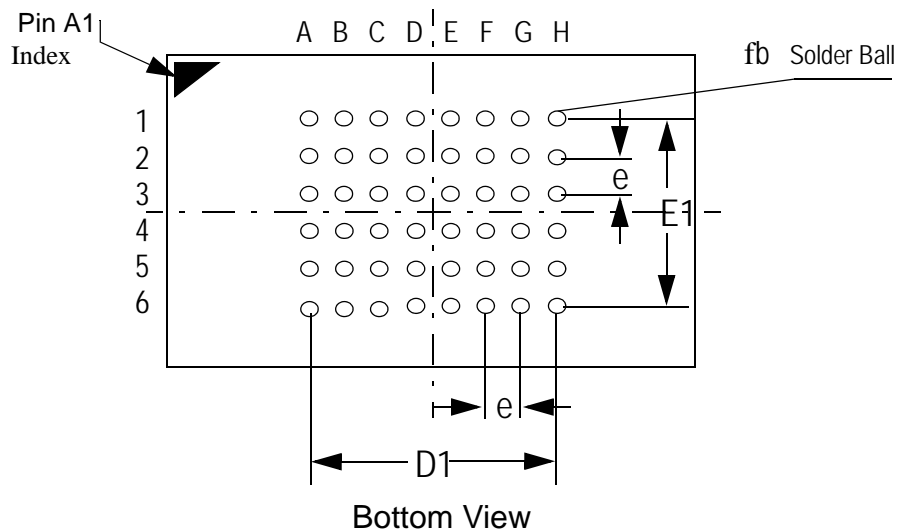
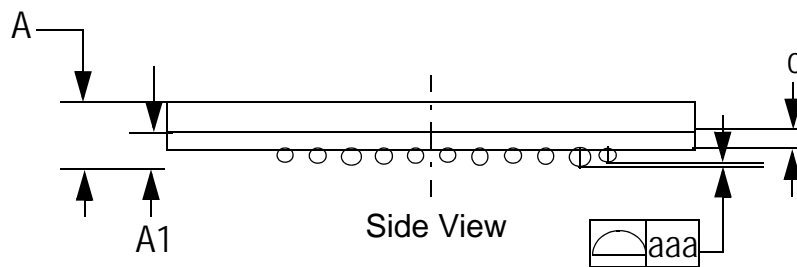
**Notes:**

1. Dimension D & E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Controlling dimension: mm

## 6 mm x 10 mm FP-BGA



| Symbol | Unit: mm   |
|--------|------------|
| A      | 1.10±0.10  |
| A1     | 0.20~0.30  |
| fb     | f0.30~0.40 |
| c      | 0.36(TYP)  |
| D      | 10.0±0.05  |
| D1     | 5.25       |
| E      | 6.0±0.05   |
| E1     | 3.75       |
| e      | 0.75(TYP)  |
| aaa    | 0.10       |



Ordering Information

| Part Number *  | Package                        | Access Time | Temp. Range |
|----------------|--------------------------------|-------------|-------------|
| GS74116AGP-8   | RoHS-compliant 400 mil TSOP-II | 8 ns        | Commercial  |
| GS74116AGP-10  | RoHS-compliant 400 mil TSOP-II | 10 ns       | Commercial  |
| GS74116AGP-12  | RoHS-compliant 400 mil TSOP-II | 12 ns       | Commercial  |
| GS74116AGP-8I  | RoHS-compliant 400 mil TSOP-II | 8 ns        | Industrial  |
| GS74116AGP-10I | RoHS-compliant 400 mil TSOP-II | 10 ns       | Industrial  |
| GS74116AGP-12I | RoHS-compliant 400 mil TSOP-II | 12 ns       | Industrial  |
| GS74116AX-8    | Fine Pitch BGA                 | 8 ns        | Commercial  |
| GS74116AX-10   | Fine Pitch BGA                 | 10 ns       | Commercial  |
| GS74116AX-12   | Fine Pitch BGA                 | 12 ns       | Commercial  |
| GS74116AX-8I   | Fine Pitch BGA                 | 8 ns        | Industrial  |
| GS74116AX-10I  | Fine Pitch BGA                 | 10 ns       | Industrial  |
| GS74116AX-12I  | Fine Pitch BGA                 | 12 ns       | Industrial  |
| GS74116AGX-8   | RoHS-compliant Fine Pitch BGA  | 8 ns        | Commercial  |
| GS74116AGX-10  | RoHS-compliant Fine Pitch BGA  | 10 ns       | Commercial  |
| GS74116AGX-12  | RoHS-compliant Fine Pitch BGA  | 12 ns       | Commercial  |
| GS74116AGX-8I  | RoHS-compliant Fine Pitch BGA  | 8 ns        | Industrial  |
| GS74116AGX-10I | RoHS-compliant Fine Pitch BGA  | 10 ns       | Industrial  |
| GS74116AGX-12I | RoHS-compliant Fine Pitch BGA  | 12 ns       | Industrial  |

**Note:**

Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS74116AGP-8T

## 4Mb Asynchronous Datasheet Revision History

| Rev. Code: Old;<br>New     | Types of Changes<br>Format or Content | Page #/Revisions/Reason  |
|----------------------------|---------------------------------------|--|
| 74116A_r1                  | Format/Content                        | • Created new datasheet  |
| 74116A_r1; 74116A_r1_01    | Content                               | <ul style="list-style-type: none"> <li>• Added 6 ns and 7 ns speed bins</li> <li>• Updated power numbers</li> <li>• Changed FPBGA package size from 7.2 x 11.65 mm to 6 x 10 mm</li> <li>• Changed package designator from "U" to "X" for FPBGA</li> <li>• Changed D3 on FPBGA pinout to A17 and E3 to NC</li> </ul> |
| 74116A_r1_01; 74116A_r1_02 | Content                               | <ul style="list-style-type: none"> <li>• Updated Recommended Operating Conditions on page 4</li> <li>• Updated Read Cycle and Write Cycle AC Characteristics tables</li> </ul>   |
| 74116A_r1_02; 74116A_r1_03 | Content                               | • Removed 6 ns speed bin from entire document  |
| 74116A_r1_03; 74116A_r1_04 | Content                               | • Removed 7 ns speed bin from entire document  |
| 74116A_r1_04; 74116A_r1_05 | Content/Format                        | <ul style="list-style-type: none"> <li>• Updated format</li> <li>• Added Pb-free information for TSOP</li> </ul>   |
| 74116A_r1_05; 74116A_r1_06 | Content/Format                        | • Added Pb-free information for FP-BGA   |
| 74116A_r1_06; 74116A_r1_07 | Content                               | <ul style="list-style-type: none"> <li>• Changed Pb-free references to RoHS-compliant</li> <li>• Added RoHS-compliant SOJ part</li> <li>• Added status to Ordering Information table</li> </ul>  |
| 74116A_r1_07; 74116A_r1_08 | Content                               | • Removed status from Ordering Information table (all parts MP)  |
| 74116A_r1_08; 74116A_r1_09 | Content                               | <ul style="list-style-type: none"> <li>• Removed SOJ references (part is EOL)</li> <li>• (Rev1.09a: Changed 6 x 10 mm Ball Pitch reference on page 1 to 6 x 10 mm Substrate)</li> </ul>  |
| 74116A_r1_09; 74116A_r1_10 | Content                               | • Removed TSOP-II 5/6 RoHS-compliant references (part is EOL)  |

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