BGA
Commercial Temp
Industrial Temp

512K x 16
8Mb Asynchronous SRAM

8, 10, 12 ns
3.3 V V_{DD}

Features

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 240/190/170 mA at minimum cycle time
- Single 3.3 V ± 0.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: –40° to 85°C
- 14 mm x 22 mm, 119-bump, 1.27 mm Pitch Ball Grid Array package
- RoHS-compliant package available

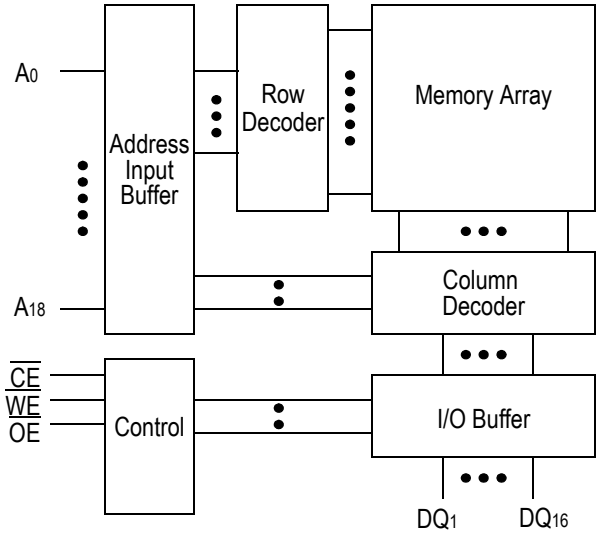
Description

The GS78116A is a high speed CMOS Static RAM organized as 524,288-words by 16-bits. Static design eliminates the need for external clocks or timing strobes. The GS78116A operates on a single 3.3 V power supply, and all inputs and outputs are TTL-compatible. The GS78116 is available in a 14 mm x 22 mm BGA package.

Pin Descriptions

Symbol	Description
A_0 to A_{18}	Address input
DQ_1 to DQ_{16}	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{DD}	+3.3 V power supply
V_{SS}	Ground
NC	No connect

Block Diagram



512K x 16 Async SRAM in 119-bump, 14 mm x 22 mm—Top View (Package B)

	1	2	3	4	5	6	7
A	NC	A_{15}	A_{14}	A_{16}	A_{13}	A_{12}	NC
B	NC, V_{SS}	A_{11}	A_{10}	$\overline{CE}$	A_9	A_8	NC
C	NC	NC	V_{DD}, NC	A_{17}	V_{SS}, NC	NC	NC
D	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC
E	DQ_1	NC	V_{DD}	V_{SS}	V_{DD}	NC	DQ_{16}
F	DQ_2	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{15}
G	DQ_3	NC	V_{DD}	V_{SS}	V_{DD}	NC	DQ_{14}
H	DQ_4	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{13}
J	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}
K	DQ_5	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{12}
L	DQ_6	NC	V_{DD}	V_{SS}	V_{DD}	NC	DQ_{11}
M	DQ_7	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{10}
N	DQ_8	NC	V_{DD}	V_{SS}	V_{DD}	NC	DQ_9
P	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC
R	NC	NC	NC	A_{18}	NC	NC	NC
T	NC	A_7	A_6	$\overline{WE}$	A_5	A_4	NC, V_{SS}
U	NC	A_3	A_2	$\overline{OE}$	A_1	A_0	NC

Note:
Bumps 1B, 7T, 3C, and 5C are actually NC's but should be wired 3C = V_{DD} and 1B, 7T and 5C = V_{SS} to assure compatibility with future versions.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_1 to DQ_8	V_{DD} Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	—
L	X	L	Write	I_{DD}
L	H	H	High Z	—

X: “H” or “L”

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	1.5	W
Storage temperature	T_{STG}	–55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -8/10/12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} +0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{Ai}	–40	—	85	°C

Notes:
1. Input overshoot voltage should be less than V_{DD} +2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than –2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

Notes:
1. Tested at T_A = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA
Output Leakage Current	I_{OL}	Output High Z, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	
Output Low Voltage	V_{OL}	I_{OL} = +4 mA		0.4 V

Power Supply Currents

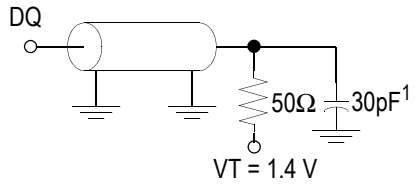
Parameter	Symbol	Test Conditions	0 to 70°C			–40 to 85°C		
			8 ns	10 ns	12 ns	8 ns	10 ns	12 ns
Operating Supply Current	I_{DD}	$\overline{E} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	160 mA	130 mA	115 mA	180 mA	150 mA	135 mA
Standby Current	I_{SB1}	$\overline{E} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	60 mA	50 mA	50 mA	80 mA	70 mA	70 mA
Standby Current	I_{SB2}	$E \ge V_{DD}$ - 0.2V All other inputs $\ge V_{DD}$ - 0.2V or $\le$ 0.2V	20 mA			40 mA		

AC Test Conditions

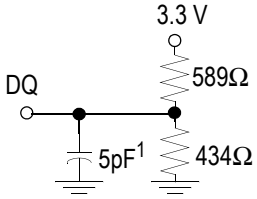
Parameter	Conditions
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL} = 0.4 V
Input rise time	tr = 1 V/ns
Input fall time	tf = 1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	**Fig. 1& 2**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.

Output Load 1



Output Load 2

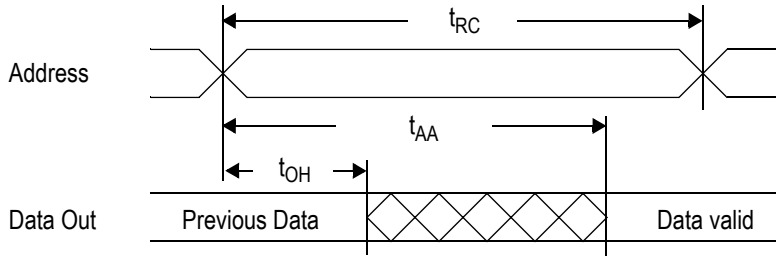


AC Characteristics

Read Cycle

Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	8	—	10	—	12	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	—	3.5	—	4	—	5	ns

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}

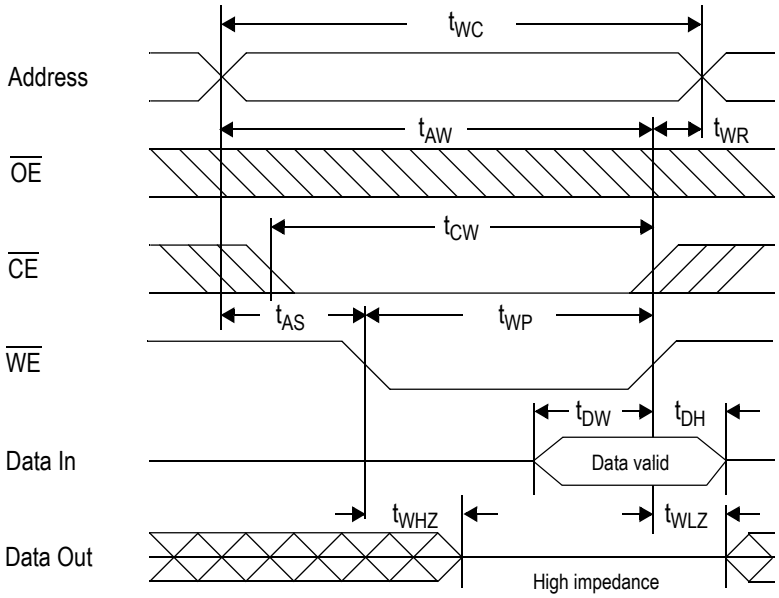


* These parameters are sampled and are not 100% tested

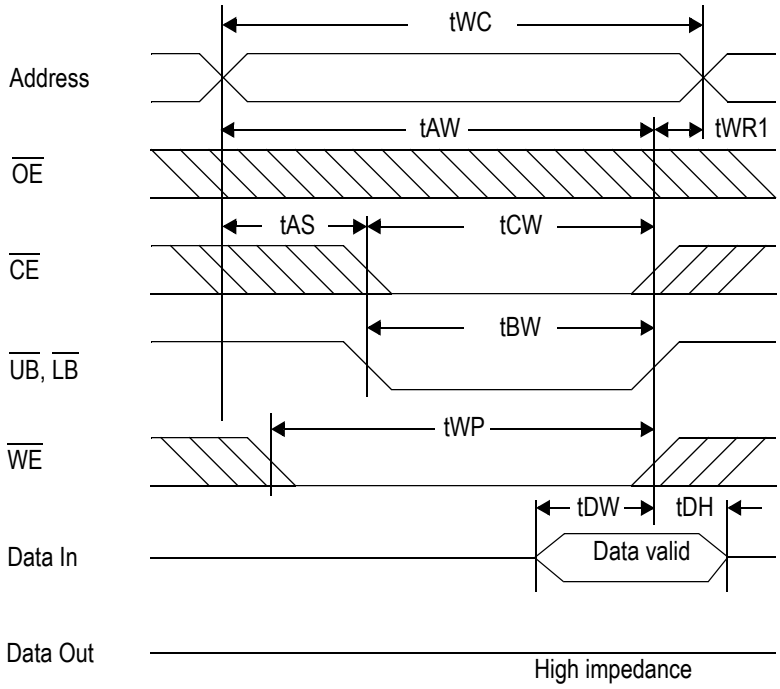
Write Cycle

Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5.5	—	7	—	8	—	ns
Data set up time	tDW	4	—	5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	ns
Write pulse width	tWP	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3.5	—	4	—	5	ns

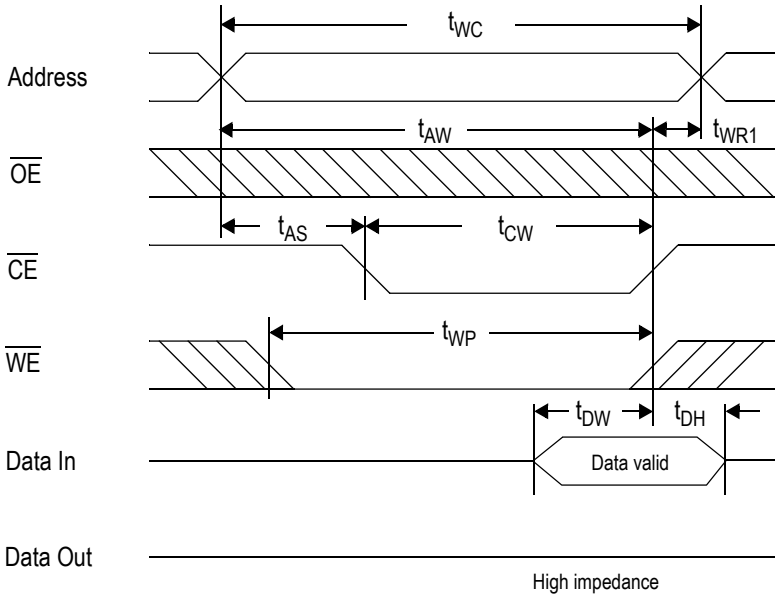
Write Cycle 1: $\overline{WE}$ Controlled



Write Cycle 3: $\overline{UB}$, $\overline{LB}$ control

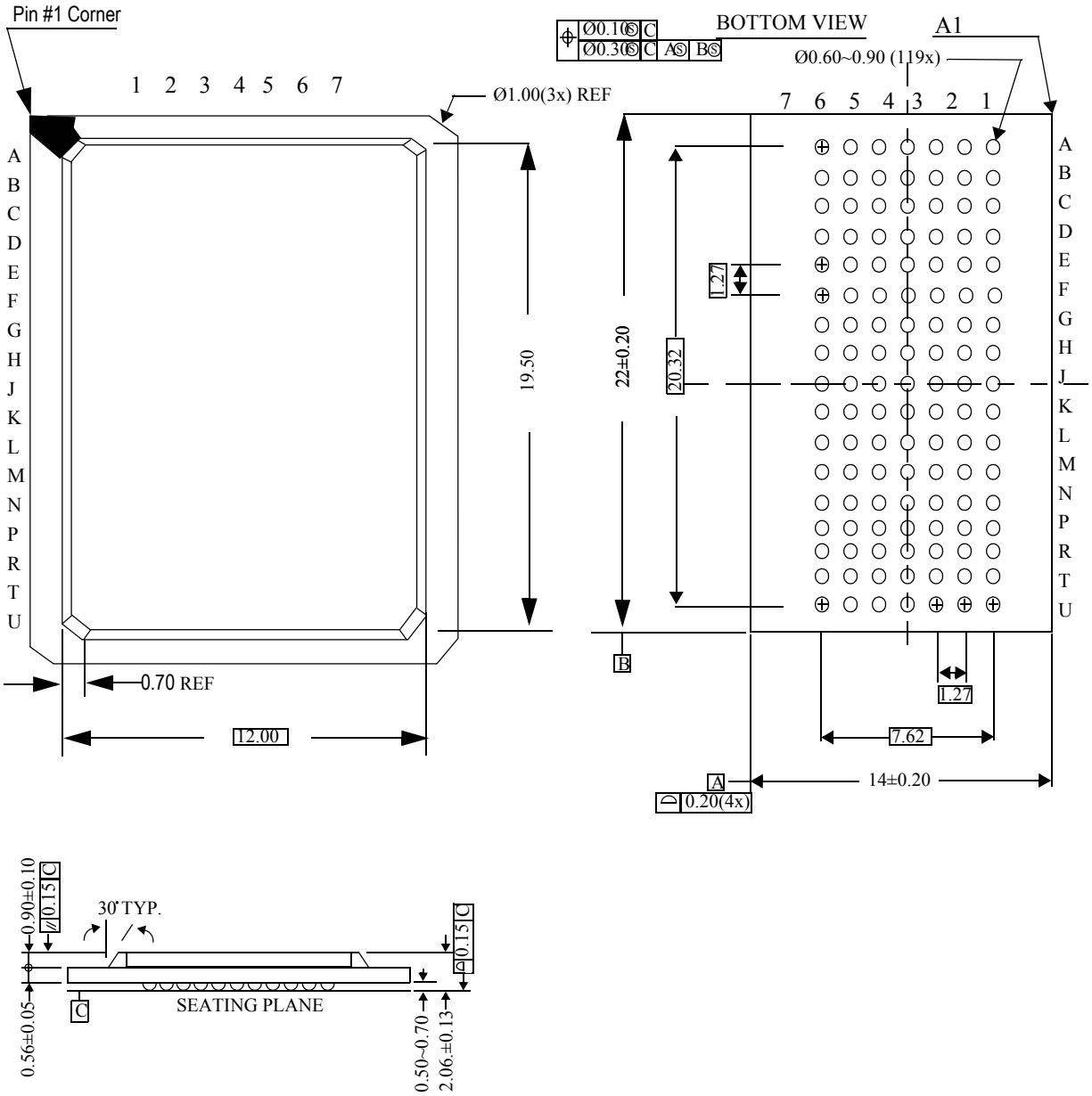


Write Cycle 2: $\overline{CE}$ Controlled



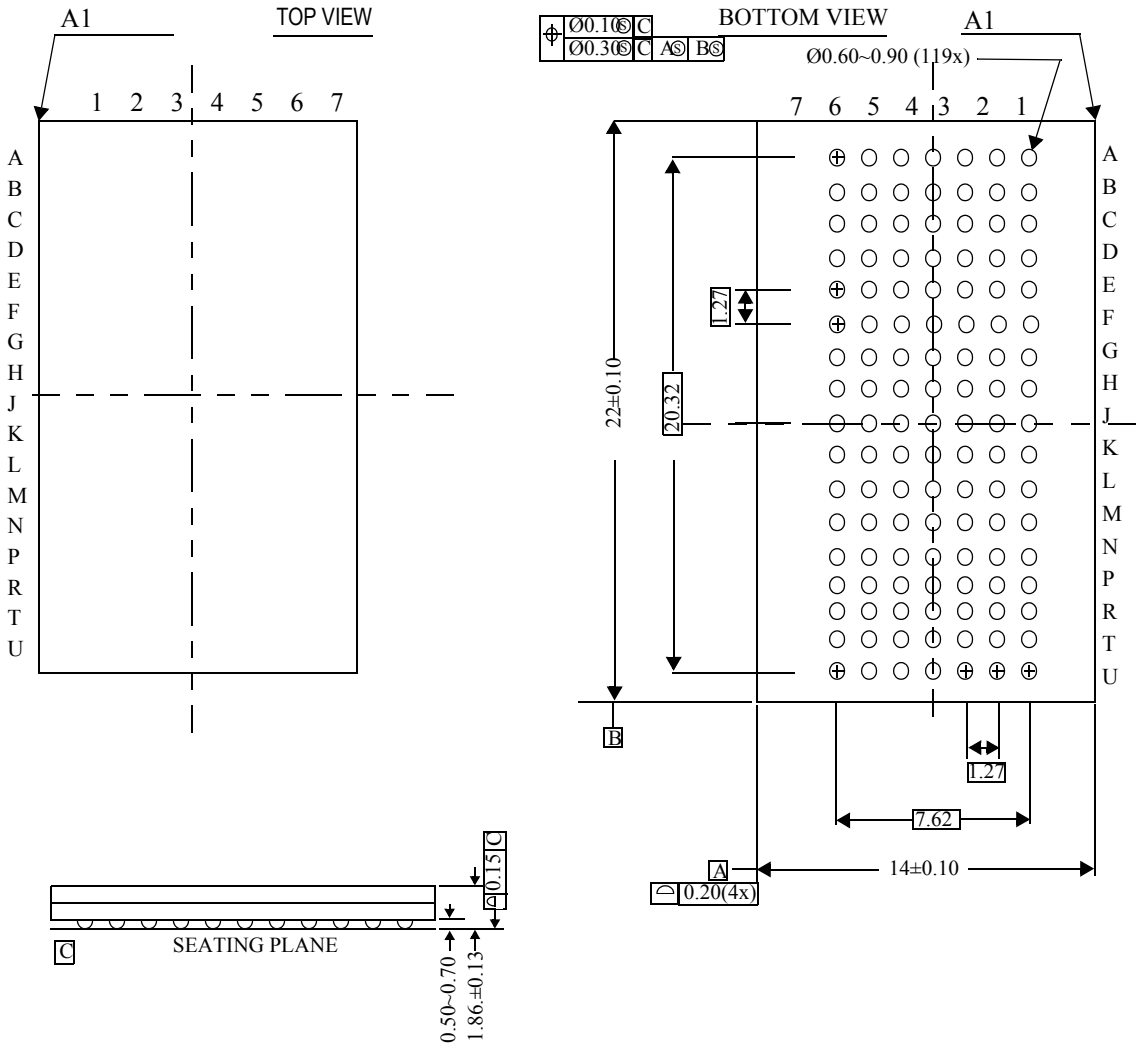
Package Dimensions—119-Bump FPBGA (Package B, Variation 1)

(Date Code: yyww.31)



Package Dimensions—119-Bump FPBGA (Package B, Variation 2)

(Date Code: yyww.3H)



Ordering Information

Part Number[1]	Package	Access Time	Temp. Range	Status
GS78116AB-8	119-Bump BGA[2]	8 ns	Commercial	
GS78116AB-10	119-Bump BGA[2]	10 ns	Commercial	
GS78116AB-12	119-Bump BGA[2]	12 ns	Commercial	
GS78116AB-8I	119-Bump BGA[2]	8 ns	Industrial	
GS78116AB-10I	119-Bump BGA[2]	10 ns	Industrial	
GS78116AB-12I	119-Bump BGA[2]	12 ns	Industrial	
GS78116AGB-8	RoHS-compliant 119-Bump BGA[2]	8 ns	Commercial	
GS78116AGB-10	RoHS-compliant 119-Bump BGA[2]	10 ns	Commercial	
GS78116AGB-12	RoHS-compliant 119-Bump BGA[2]	12 ns	Commercial	
GS78116AGB-8I	RoHS-compliant 119-Bump BGA[2]	8 ns	Industrial	
GS78116AGB-10I	RoHS-compliant 119-Bump BGA[2]	10 ns	Industrial	
GS78116AGB-12I	RoHS-compliant 119-Bump BGA[2]	12 ns	Industrial	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS78116AB-12T
2. Please see pages 8 and 9 for date code information for Variation 1 and Variation 2 of the 119-bump BGA.

Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
GS78116AB_r1		• Creation of new datasheet
GS78116AB_r1_01	Content	• Added AC specifications to datasheet
GS78116AB_r1_01; GS78116AB_r1_02	Content/Format	• Updated format • Added variation information to package mechanical
GS78116AB_r1_02; GS78116AB_r1_03	Content	• Added Variation 2 119 BGA to datasheet • Added date codes to mechanicals
GS78116AB_r1_03; GS78116AB_r1_04	Content	• Added RoHS-compliant package information • (Rev1.04a: Added missing Write Cycle 3 timing diagram)

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for SRAM ***category:***

Click to view products by GSI Technology ***manufacturer:***

Other Similar products are found below :

CY6116A-35DMB CY7C1049GN-10VXI GS8161Z36DD-200I GS88237CB-200I RMLV0408EGSB-4S2#AA0 IDT70V5388S166BG IS64WV3216BLL-15CTLA3 IS66WVE4M16ECLL-70BLI PCF8570P K6F2008V2E-LF70000 K6T4008C1B-GB70 CY7C1353S-100AXC AS6C8016-55BIN AS7C164A-15PCN 515712X IDT71V67603S133BG IS62WV51216EBLL-45BLI IS63WV1288DBLL-10HLI IS66WVE2M16ECLL-70BLI IS66WVE4M16EALL-70BLI IS61WV102416DBLL-10TLI CY7C1381KV33-100AXC CY7C1381KVE33-133AXI 8602501XA 5962-3829425MUA 5962-3829430MUA 5962-8866201YA 5962-8866204TA 5962-9062007MXA 5962-9161705MXA GS882Z18CD-150I 8413202RA 5962-8866208YA 5962-8866203YA IS61WV102416DBLL-10BLI IS66WVC2M16ECLL-7010BLI CY7C1380KV33-250AXC AS6C8016-55BINTR GS81284Z18B-250I AS7C34096B-10TIN GS84018CB-200I IS62WV25616EALL-55TLI IS61WV204816BLL-10TLI GS8128418B-167IV CY7C1460KV25-200BZXI CY7C1315KV18-333BZXC CY62157G30-45ZSXI 71V016SA12YG RMLV0416EGBG-4S2#AC0 CY62126EV18LL-70BVXI