

N-Channel Trench Power MOSFET

General Description

The HD100N02 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a wide variety of applications.

Features

- $V_{DS} = 20V, I_D = 100A$
 $R_{DS(ON)} < 5.5m\Omega @ V_{GS} = 4.5V$
 $R_{DS(ON)} < 9m\Omega @ V_{GS} = 2.5V$
- High Power and current handling capability
- Lead free product is acquired
- Surface Mount Package

Application

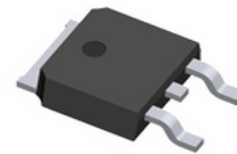
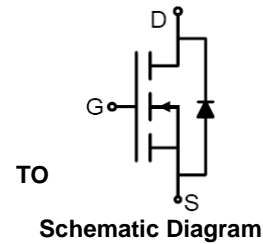
- Battery Protection
- Load switch
- Power management

100% UIS TESTED!
100% ΔV_{ds} TESTED!

$$BV_{DSS} = 20V$$

$$R_{DS(on)} = 5.5m\Omega$$

$$I_D = 100A$$



-252(DPAK) top view

Table 1. Absolute Maximum Ratings ($T_A = 25^\circ C$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS} = 0V$)	20	V
V_{GS}	Gate-Source Voltage ($V_{DS} = 0V$)	± 12	V
I_D	Drain Current-Continuous ($T_C = 25^\circ C$) (Note 1)	100	A
	Drain Current-Continuous ($T_C = 100^\circ C$)	100	A
$I_{DM (pluse)}$	Drain Current-Continuous @ Current-Pulsed (Note 2)	340	A
P_D	Maximum Power Dissipation ($T_C = 25^\circ C$)	87	W
	Maximum Power Dissipation ($T_C = 100^\circ C$)	43	W
EAS	Avalanche energy (Note 3)	340	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	1.72	$^\circ C/W$

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	25		V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1.1	V
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=15A$		40		S
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS}=4.5V, I_D=20A (T_c=25^\circ C)$		3.9	5.5	m Ω
		$V_{GS}=4.5V, I_D=20A (T_c=125^\circ C)$		5.4	8	m Ω
		$V_{GS}=2.5V, I_D=15A$		6	9	m Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1.0MHz$		2800		pF
C_{oss}	Output Capacitance			353		pF
C_{rss}	Reverse Transfer Capacitance			265		pF
R_g	Gate resistance	$V_{GS}=0V, V_{DS}=0V, f=1.0MHz$		1.1		Ω
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	$V_{GS}=4.5V, V_{DS}=15V, R_L=0.75\Omega, R_{GEN}=3\Omega$		17		nS
t_r	Turn-on Rise Time			49		nS
$t_{d(off)}$	Turn-Off Delay Time			74		nS
t_f	Turn-Off Fall Time			26		nS
Q_g	Total Gate Charge	$V_{GS}=4.5V, V_{DS}=10V, I_D=12A$		32		nC
Q_{gs}	Gate-Source Charge			3		nC
Q_{gd}	Gate-Drain Charge			11		nC
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)				100	A
V_{SD}	Forward on Voltage	$V_{GS}=0V, I_S=20A$			1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20A, dI/dt=100A/\mu s$		23		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20A, dI/dt=100A/\mu s$		10		nC

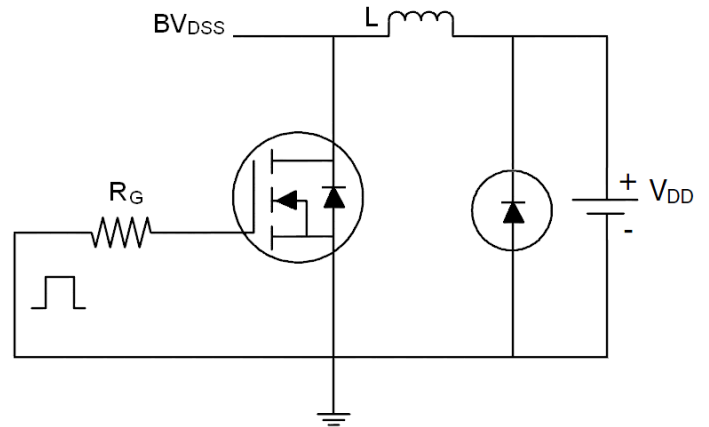
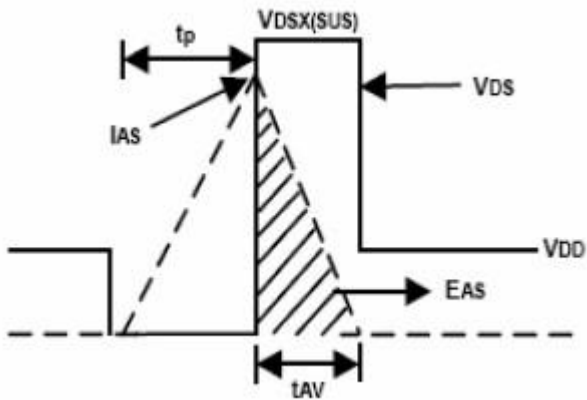
Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

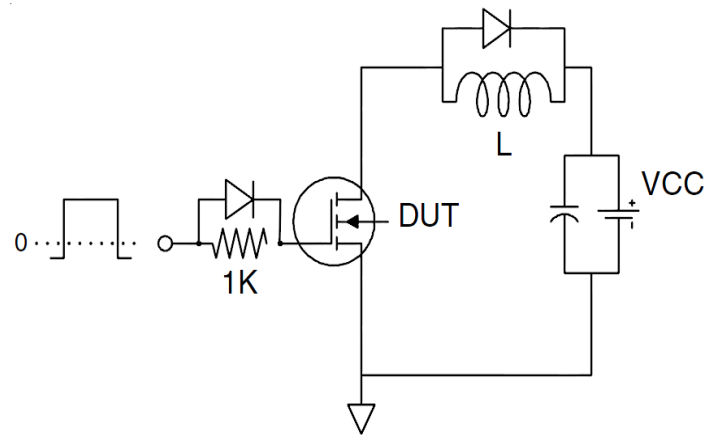
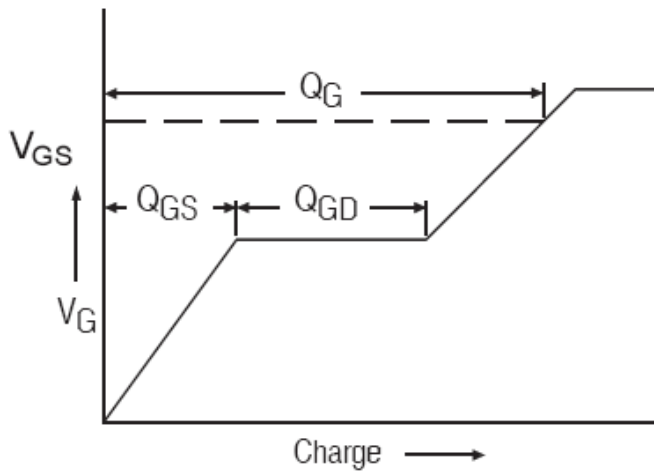
 Notes 3.EAS condition: $T_J=25^\circ C, V_{DD}=30V, V_G=4.5V, R_G=25\Omega,$

Test Circuit

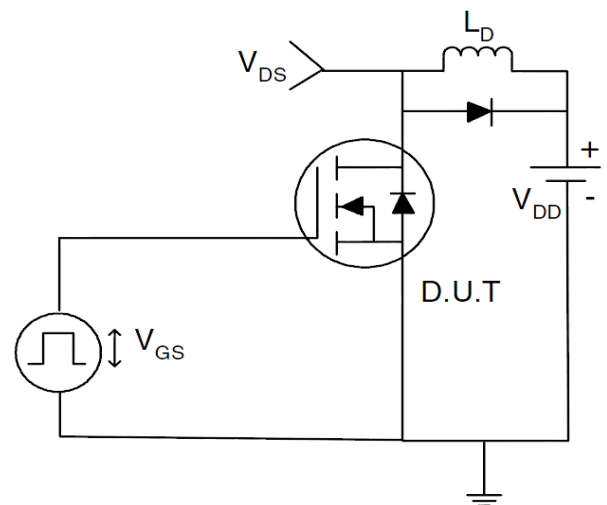
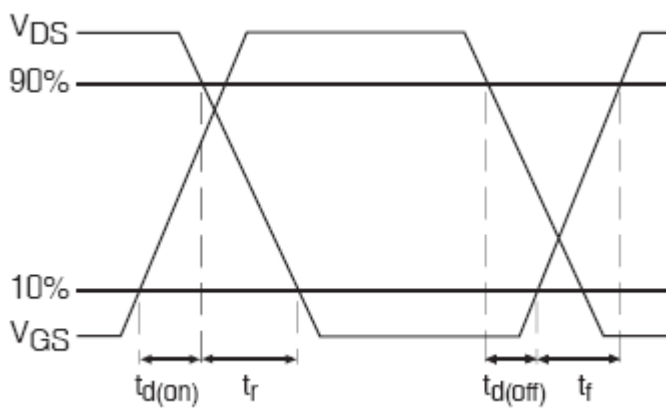
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure 1. Output Characteristics

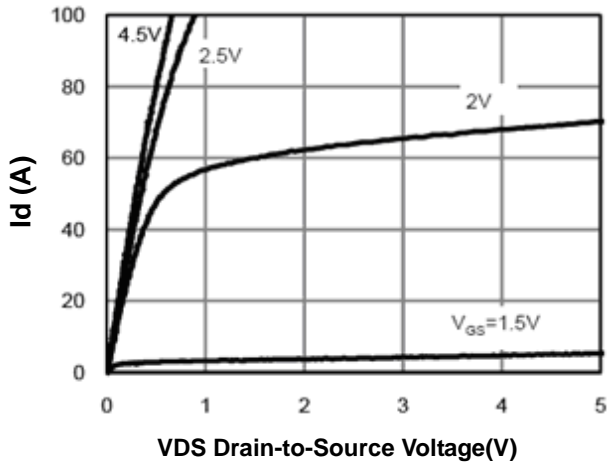


Figure 2. Transfer Characteristics

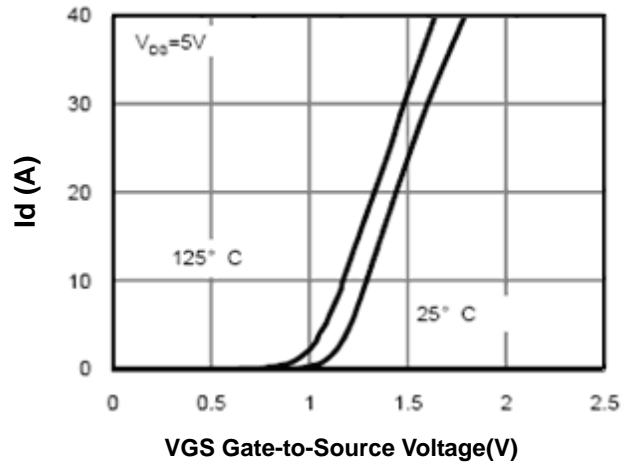


Figure 3. Max BV_{DSS} vs Junction Temperature

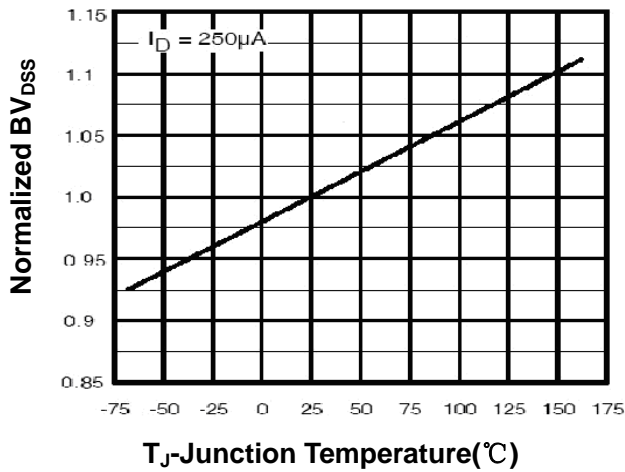


Figure 4. Drain Current

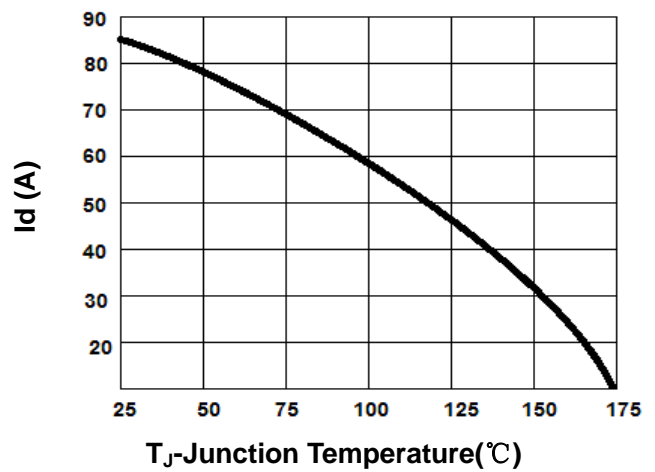


Figure 5. $V_{GS(th)}$ vs Junction Temperature

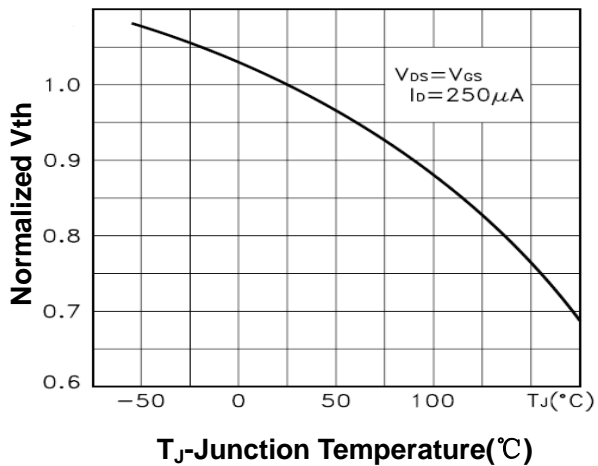


Figure 6. $R_{DS(ON)}$ vs Junction Temperature

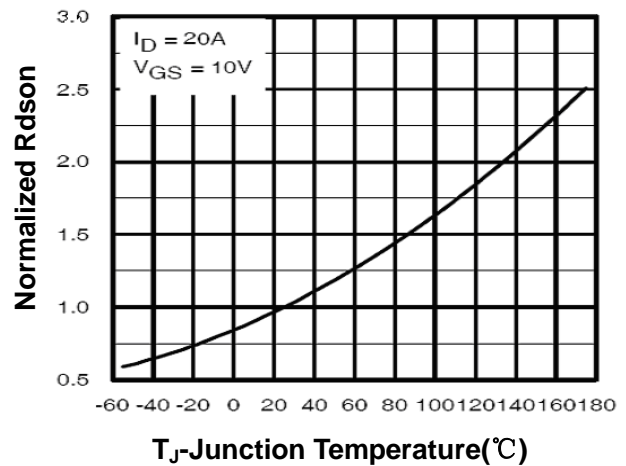


Figure 7. Gate Charge Waveforms

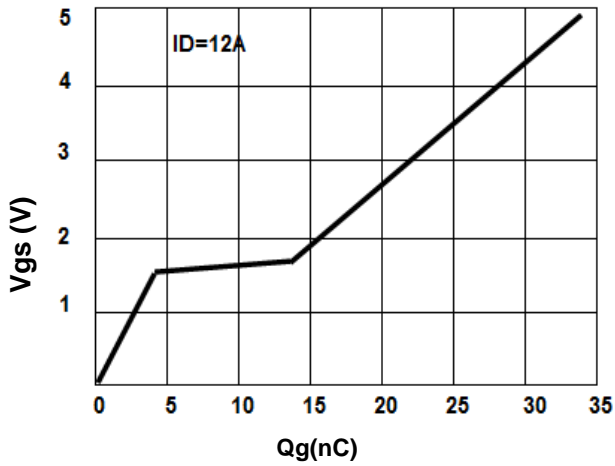


Figure 8. Capacitance

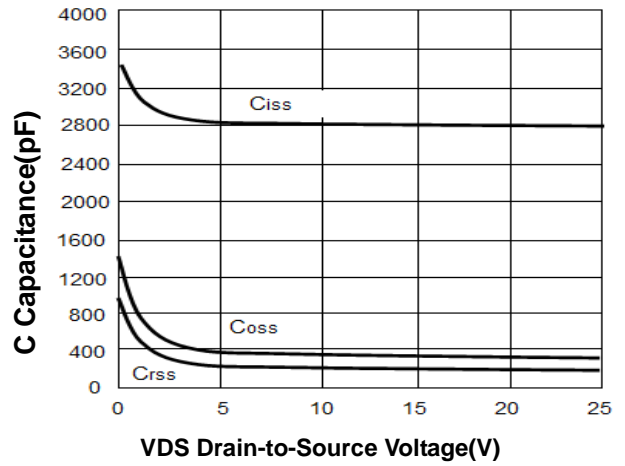


Figure 9. Body-Diode Characteristics

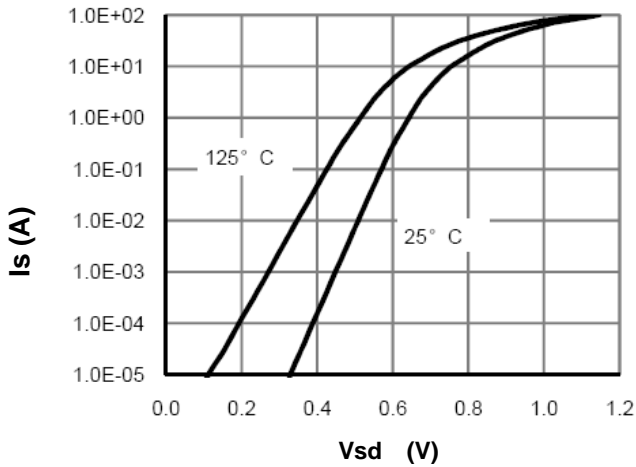


Figure 10. Maximum Safe Operating Area

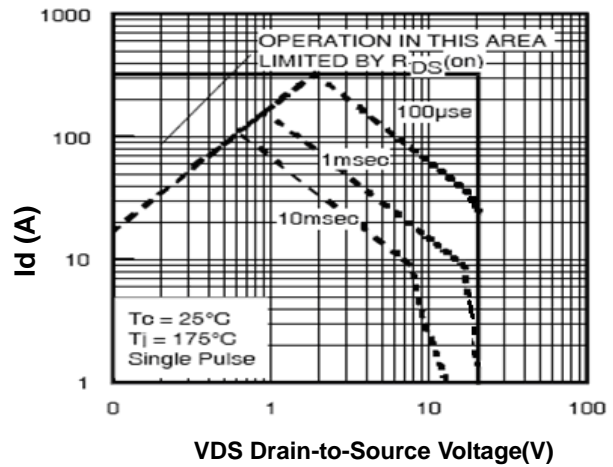
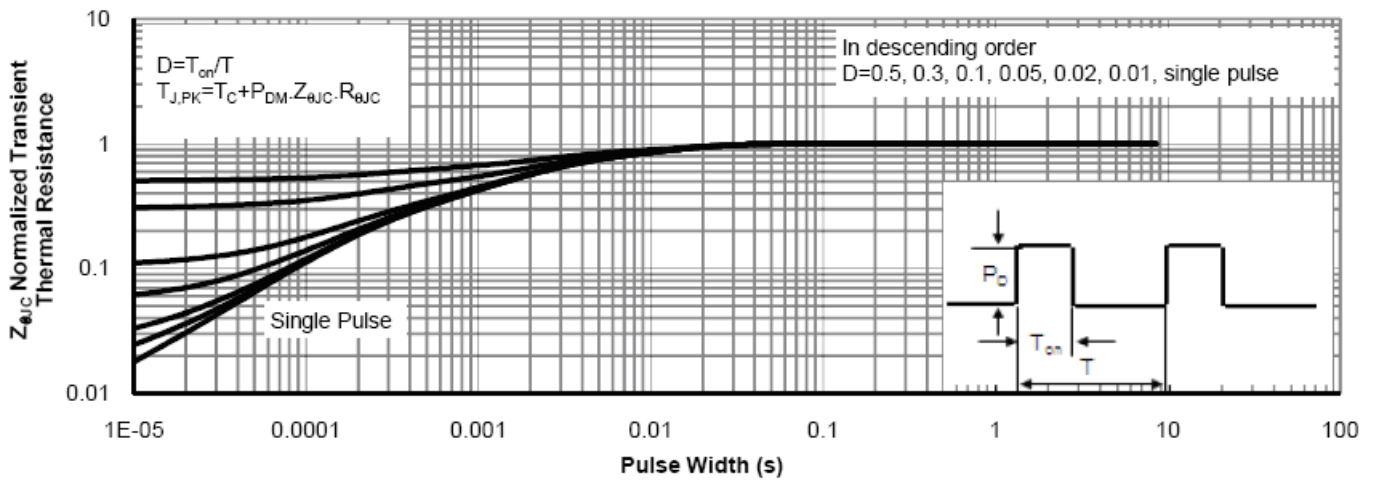
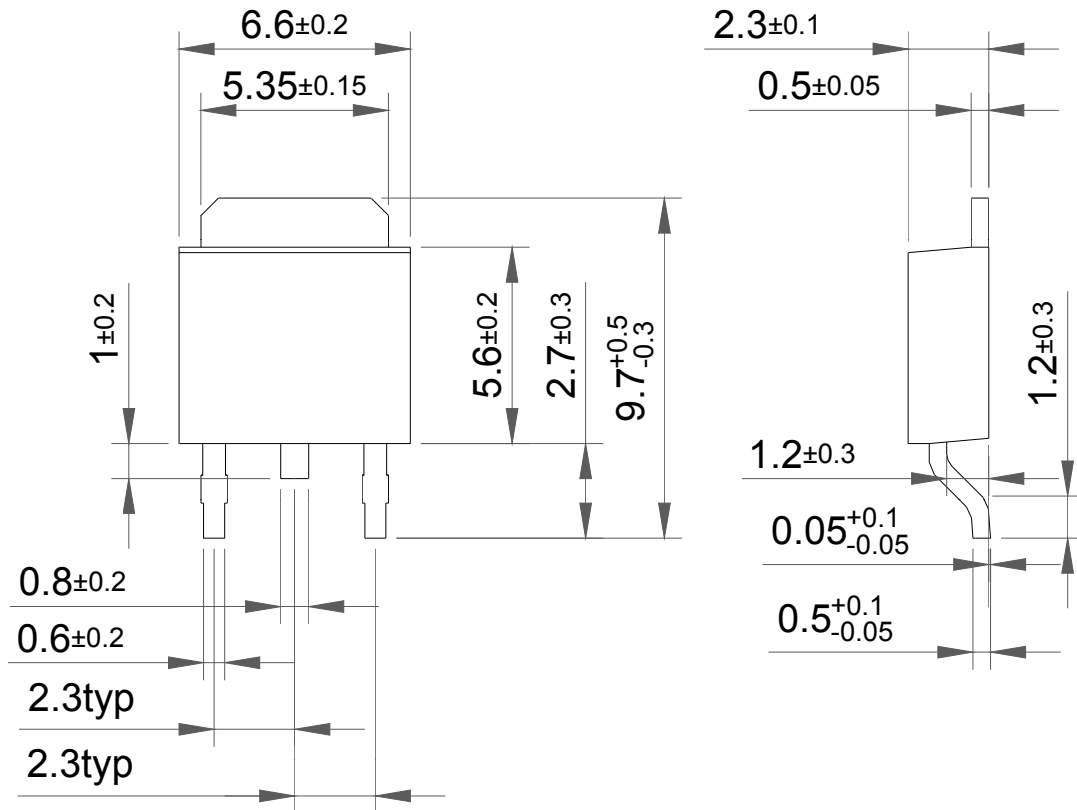


Figure 11. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



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