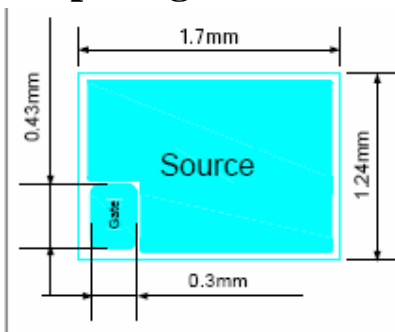


Features

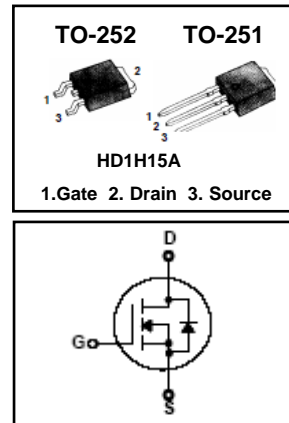
- V_{DSS}=100V/V_{GSS}=±20V/I_D=15A
R_{DS(ON)}=105mΩ(Max.)@V_{GS}=10V
R_{DS(ON)}=175mΩ(Max.)@V_{GS}=4.5V
- ESD protect
- Reliable and Rugged
- High Density Cell Design For Ultra Low On-Resistance

Chip Diagram



Applications

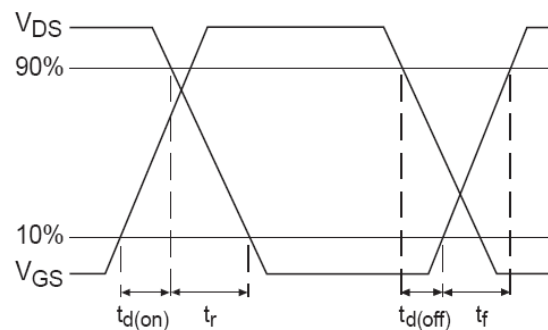
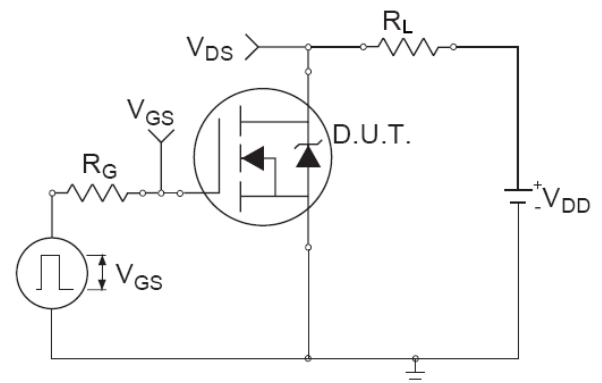
- Synchronous Rectification
- Power Management in Inverter System



Physical Characteristics

- Wafer Diameter 8 inches (± 0.1 inch)
- Wafer Thickness: 8mils (±0.6 mil)
- Die size: 1700μm x 1240μm (Including scribe line)
- Scribe Line Width: 60μm
- Gross die: 12,549
- Metalization:
Frontside: Al/Si/Cu
Backside: Ti/Ni/Ag
- Metal thickness:
Front-side: 4.0μm
Backside: 1.4μm
- Bonding Area:
Gate: 300μm x 430μm
(Die edge to gate metal 34μm)
Source: Full metalized surface of source region
(Die edge to source metal 51μm)
- Recommended wire bonding:
Gate: 1.5mils Au wire x 1
Source: 12mils Al wire x 1
- Recommended package: SOP-8(Dual)

Switching Time Test Circuit and Waveforms



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Typical	Unit	
V _{DSS}	Drain-Source Voltage	100	V	
V _{GSS}	Gate –Source Voltage	±20	V	
I _D ¹	Continuous Drain Current	T _C =70°C	2.8	A
			3.5	A
I _{DM} ¹	300us Pulsed Drain Current Tested	14	A	
I _S ¹	Diode Continuous Forward Current	3	A	
T _J	Operating Junction Temperature	150	°C	
T _{STG}	Storage Temperature Range	-55 ~ 150	°C	

Note: 1: Surface Mounted on 1in² pad area, t ≤ 10sec..

2: UIS tested and pluse width limited by maximum junction temperature 150°C (initial temperature T_J=25°C).

Electrical Characteristics (T_A=25°C unless otherwise noted)

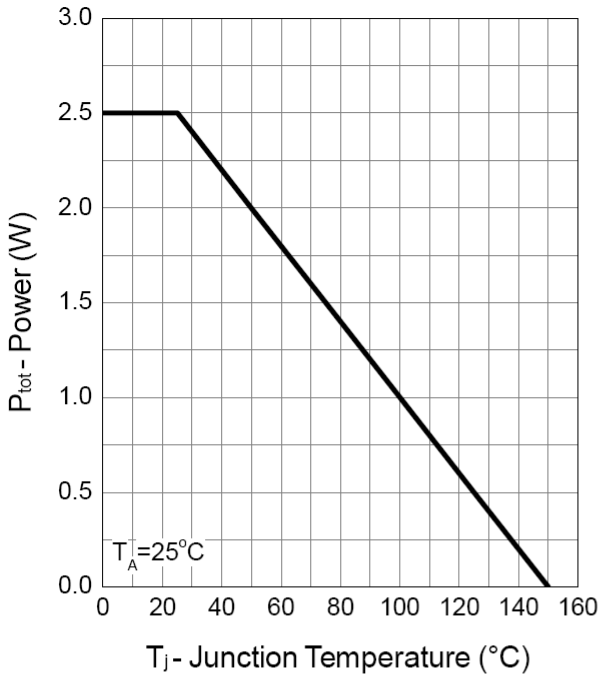
Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V			1	uA
		T _J =85°C			30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.5	2	2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±16V, V _{DS} =0V			±10	uA
R _{DSON} ¹	Drain-Source On-Resistance	V _{GS} =10V, I _D =3.5A		85	105	mΩ
		V _{GS} =4.5V, I _D =2A		135	175	
Diode Characteristics						
V _{SD} ¹	Diode Forward Voltage	I _{SD} =3A, V _{GS} =0V	0.6	0.8	1.1	V
t _{rr}	Reverse Recovery Time	I _{SD} =15A,		36		ns
Q _{rr}	Reverse Recovery Charge	dI _{SD} /dt=100A/us		50		nC
Dynamic Characteristics²						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V Frequency=1MHz		900		pF
C _{oss}	Output Capacitance			60		
C _{rss}	Reverse Transfer Capacitance			40		
t _{d(on)}	Turn-On Delay Time	V _{DD} =30V, R _L =30Ω I _D =1A, V _{GEN} =10V R _G =6Ω		8	15	ns
t _r	Turn-On Rise Time			6	11	
t _{d(off)}	Turn-Off Delay Time			40	75	
t _f	Turn-Off Fall Time			24	45	
Gate Charge Characteristics²						
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V I _D =15A		20		nC
Q _{gs}	Gate-Source Charge			3		
Q _{gd}	Gate-Drain Charge			3.1		

Note: 1: Pulse test ; pulse width ≤ 300ns, duty cycle ≤ 2%.

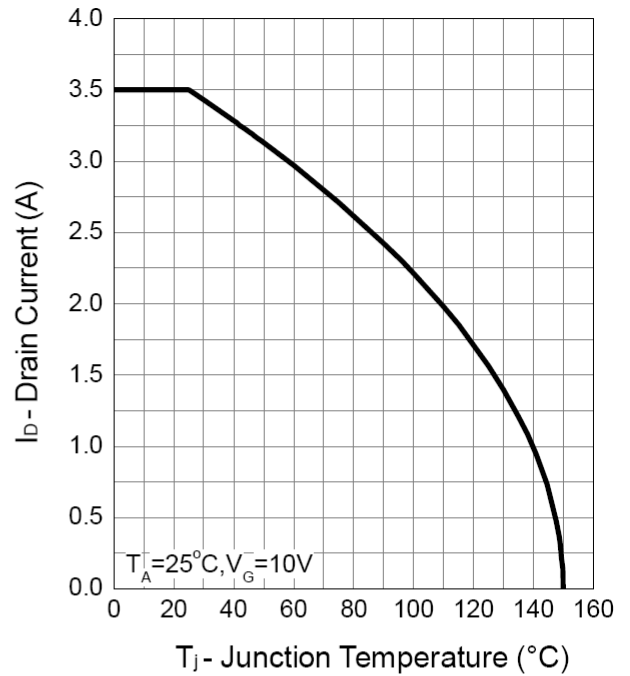
2: Guaranteed by design, not subject to production testing.

Typical Characteristics

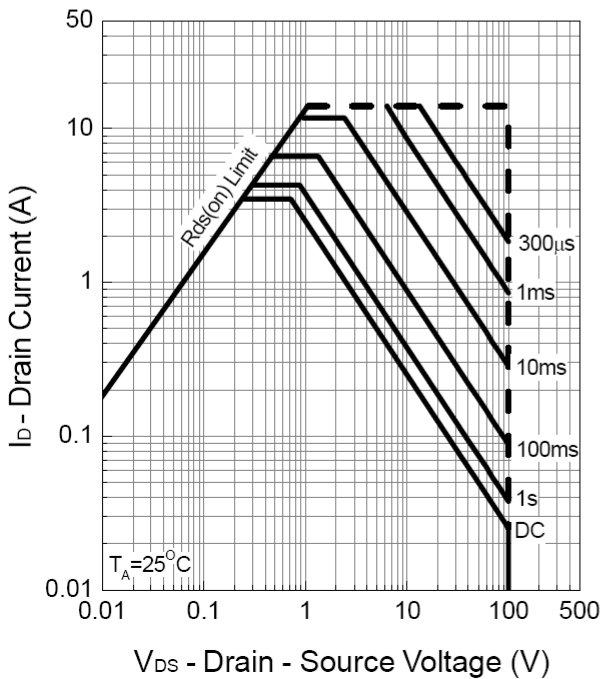
Power Dissipation



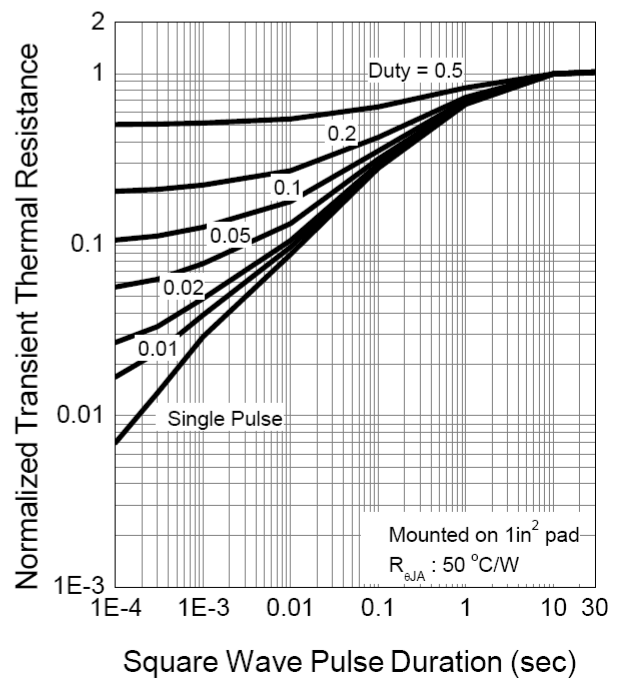
Drain Current



Safe Operation Area

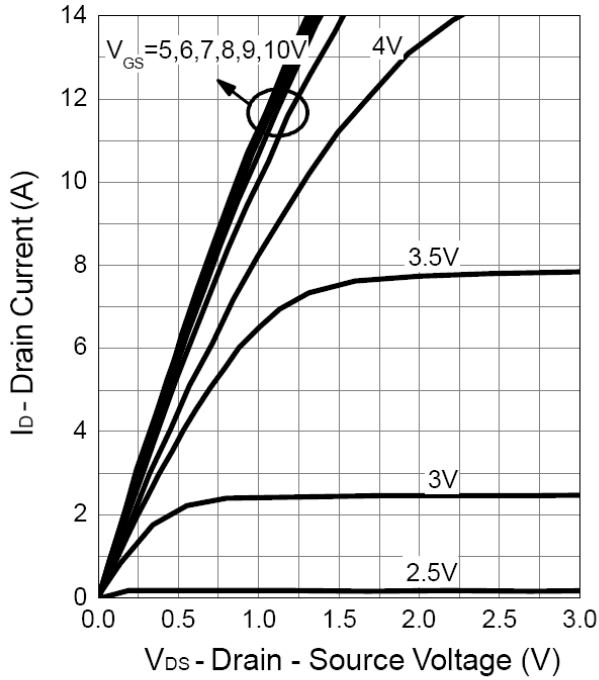


Thermal Transient Impedance

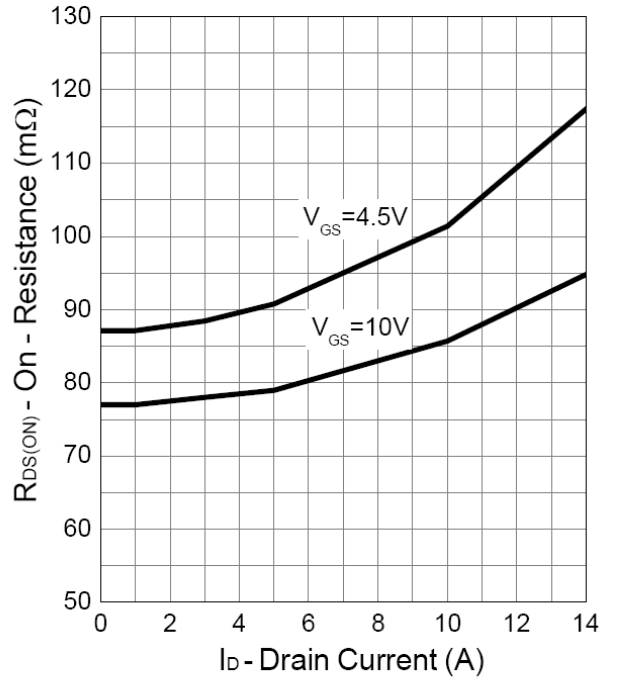


Typical Characteristics (Cont.)

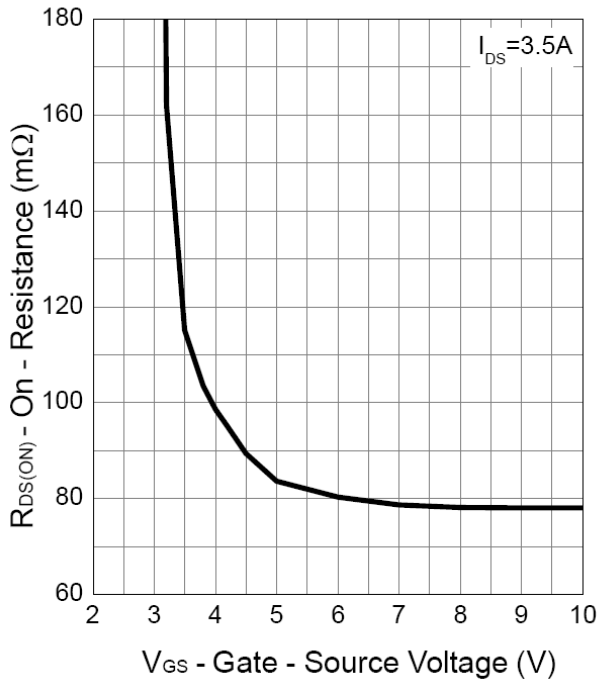
Output Characteristics



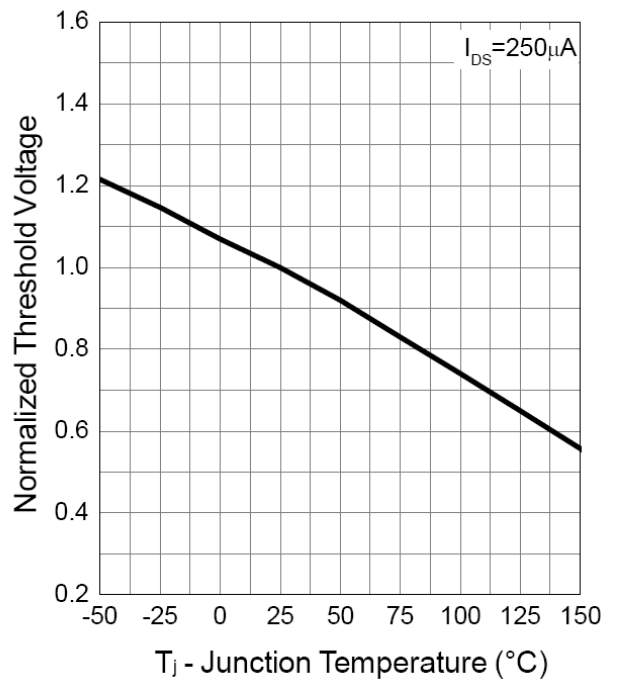
Drain-Source On Resistance



Gate-Source On Resistance

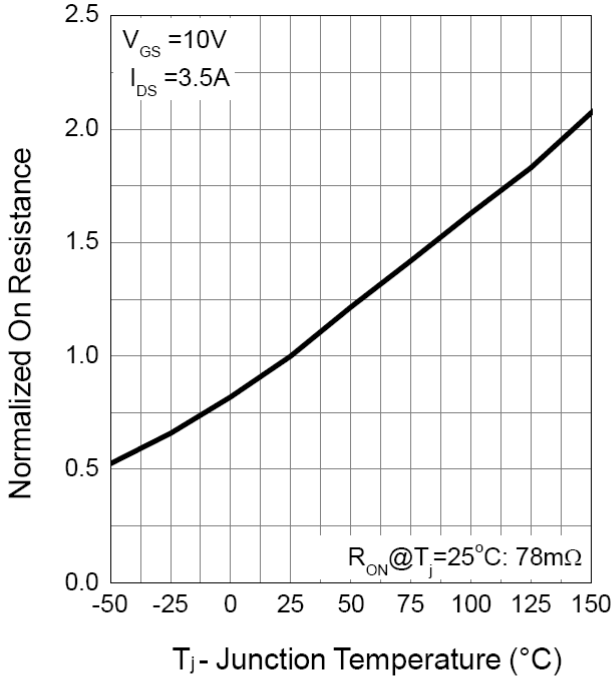


Gate Threshold Voltage

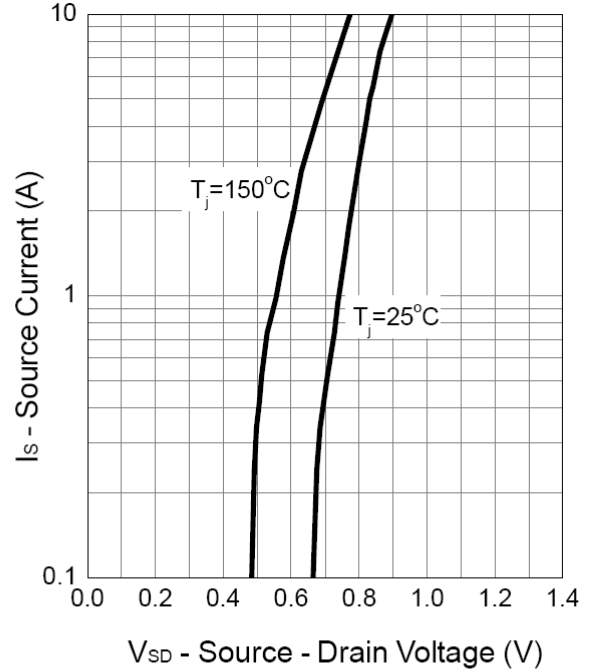


Typical Characteristics (Cont.)

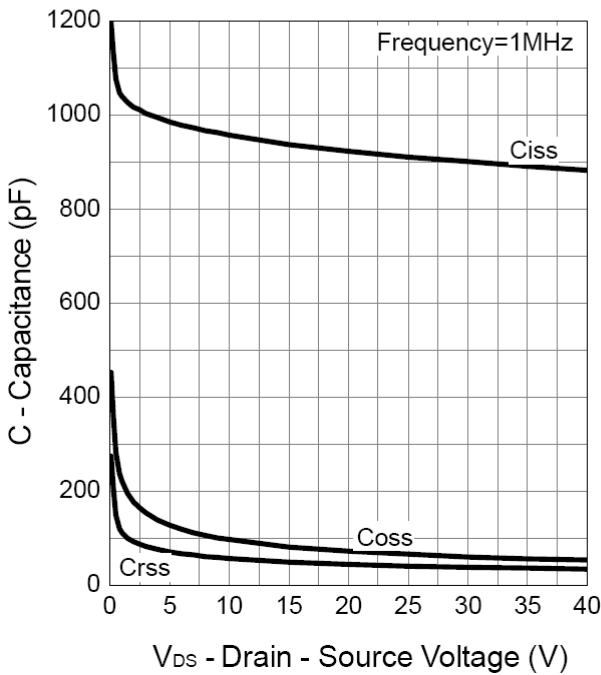
Drain-Source On Resistance



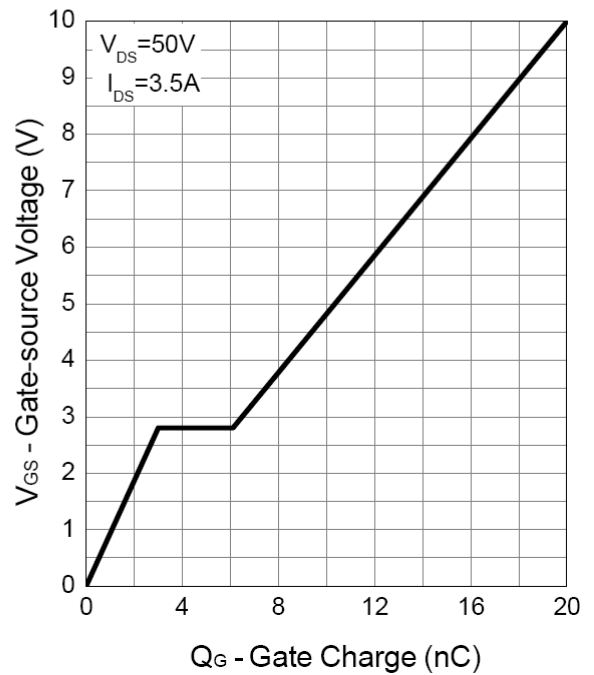
Source-Drain Diode Forward



Capacitance

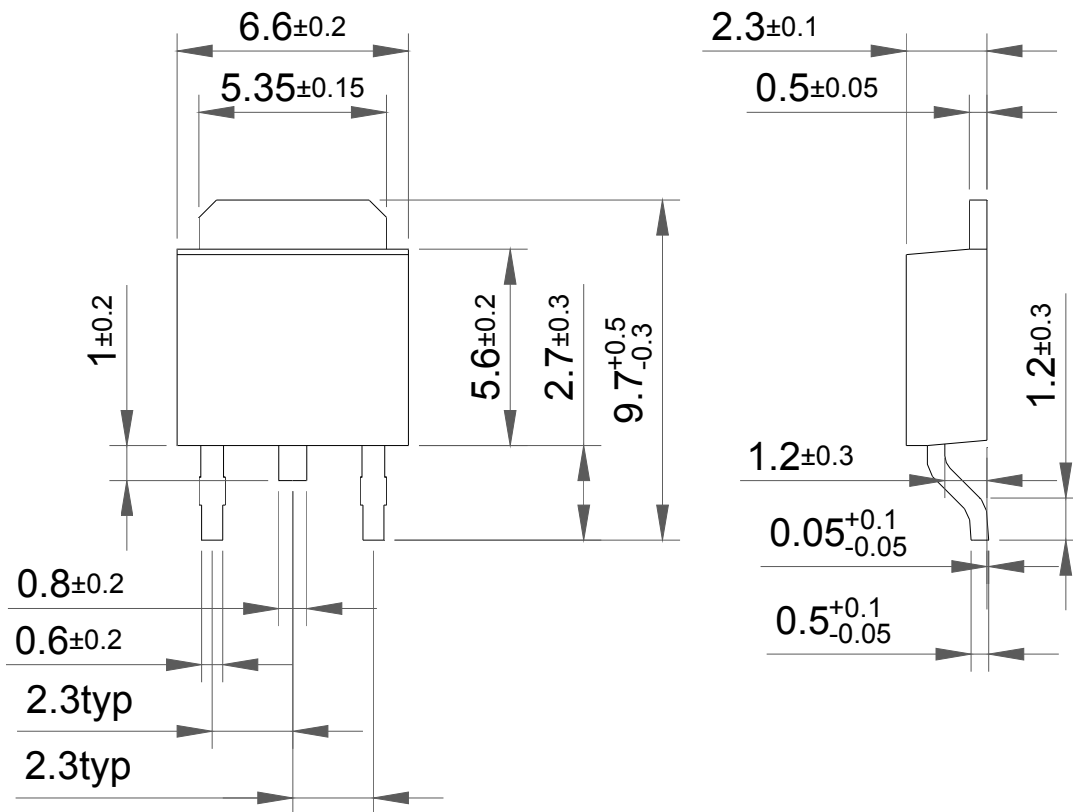


Gate Charge



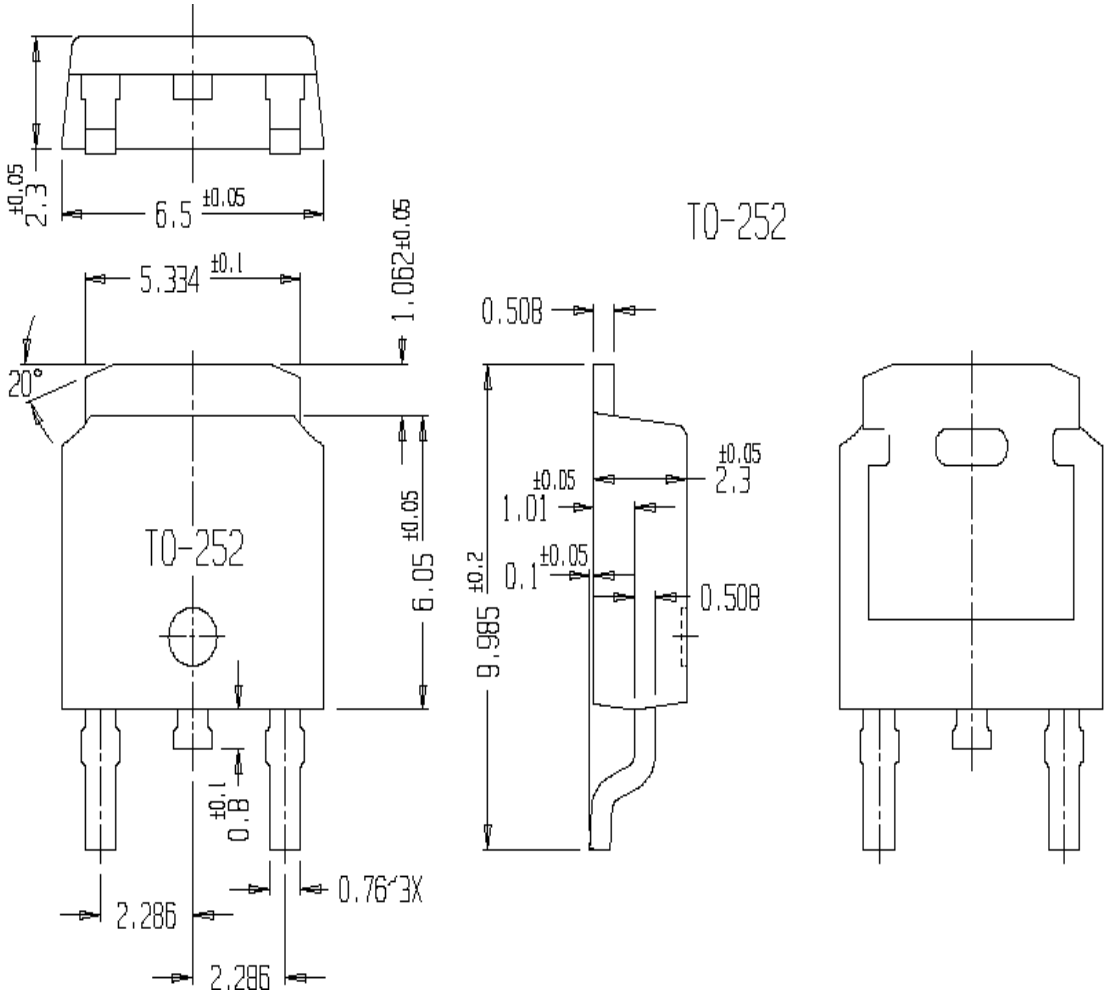
Package Dimension

TO-252



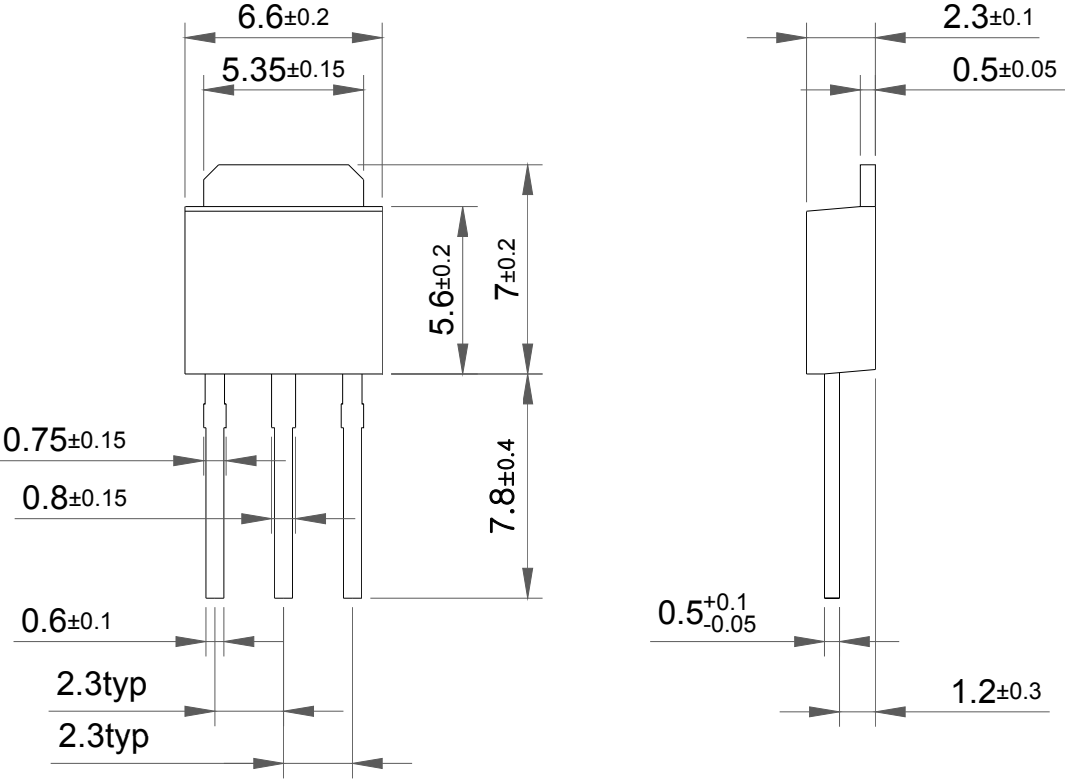
Package Dimension

TO-252



Package Dimension

TO-251



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