HX3141

Tiny Package, High Efficiency, Step-up DC/DC Converter

Features

➢ Input Voltage Range: 1.1V ～ 5.5V
➢ Internal MOSFET with High Switch Current up to 3A
➢ 90% Efficiency
➢ Up to 450kHz Switching Frequency
➢ SOT-23-6L Package

Applications

➢ PDA
➢ DSC
➢ LCD Panel
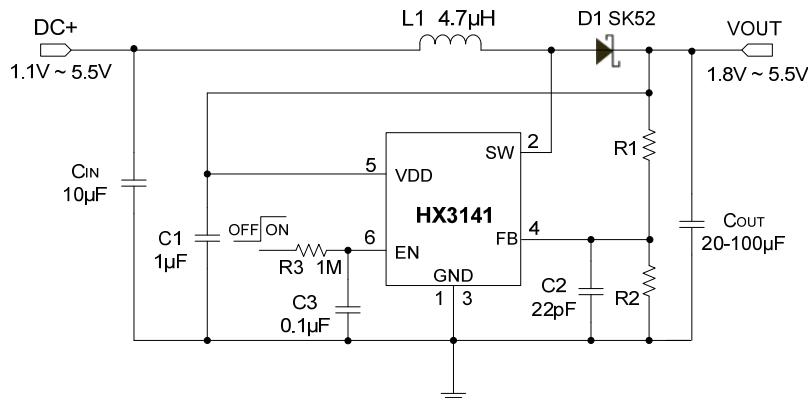➢ RF-Tags
➢ MP3
➢ Portable Instruments
➢ Wireless Equipments

Description

The HX3141 is a compact, high efficiency, and low voltage step-up DC/DC converter including an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents. It operates in stable waveforms without external compensation.

The high switching rate minimized the size of external components. Besides, the low quiescent current together with high efficiency maintains long battery lifetime. The output voltage is set with two external resistors.

The HX3141 is available in the industry standard SOT-23-6L power packages.

Typical Application Circuit

*V_{OUT} = 1.212V • [1 + (R1/R2)].

Figure 1: (1.1V Stat-up Input Voltage)

Absolute Maximum Ratings (Note 1)

➢ Supply Voltage………………………………………………………………..……−0.3V ～ 6V
➢ SW Pin Switch Voltage……………………………………………………….……−0.3V ～ 6V
➢ Other I/O Pin Voltages…………………………………………………....…−0.3V ～ 6V
➢ SW Pin Switch Current ………………………………………………………...…………….4A
➢ Operating Junction Temperature………………………………………….…-40℃ ～ +125℃
➢ Storage Temperature Range …………………………………………….−65℃ ～ +150℃
➢ Lead Temperature (Soldering 10 sec.) ……………………………………………...+ 265℃

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
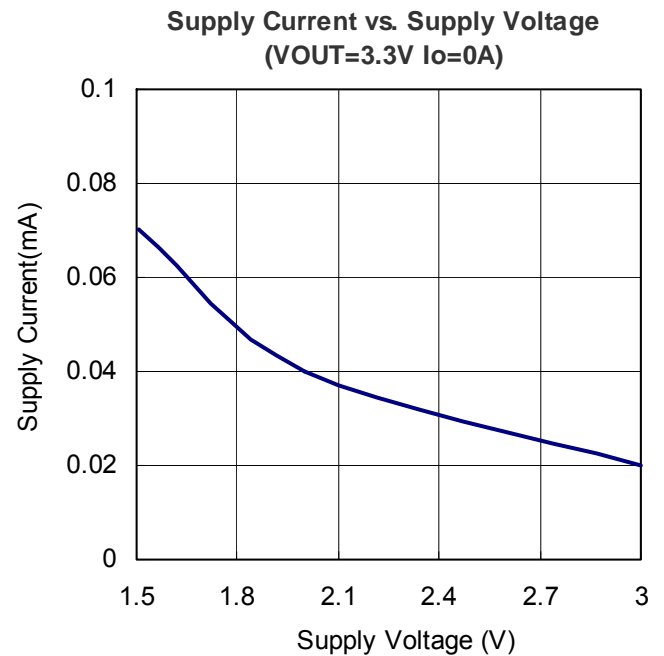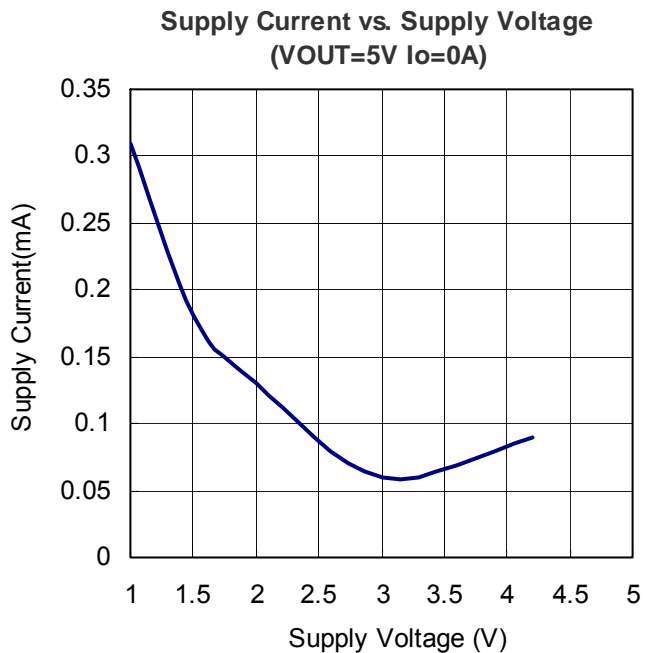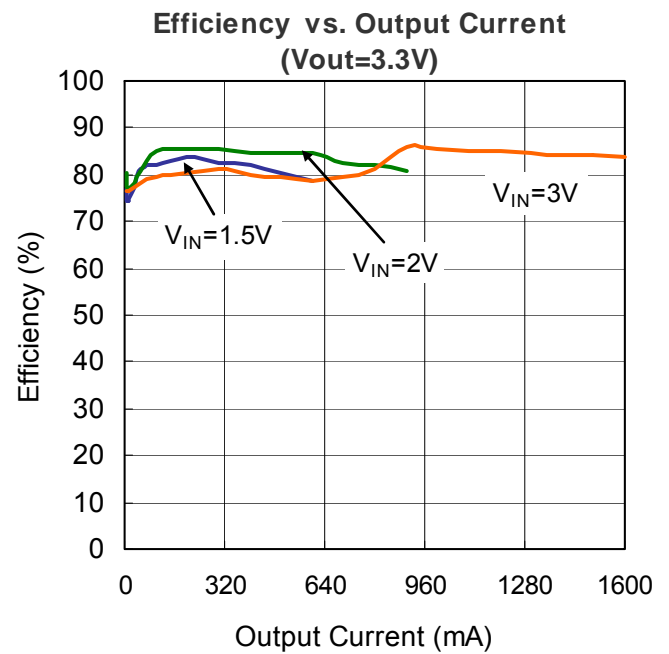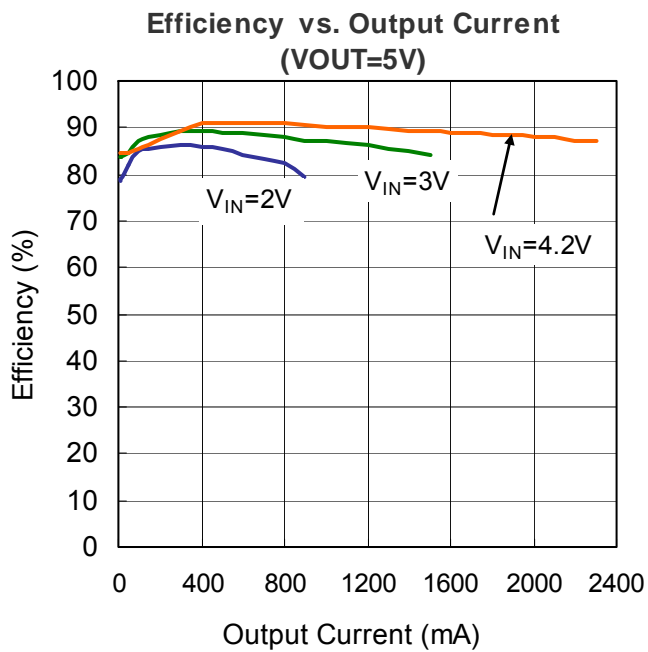
Pin Description

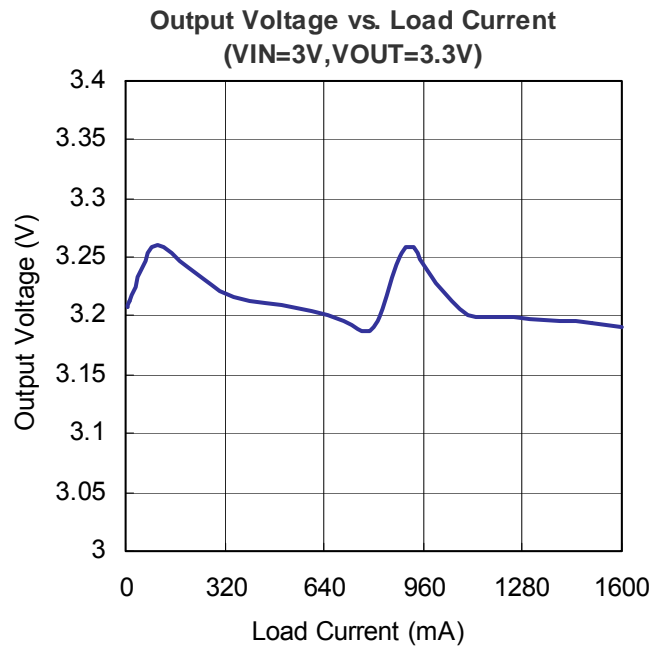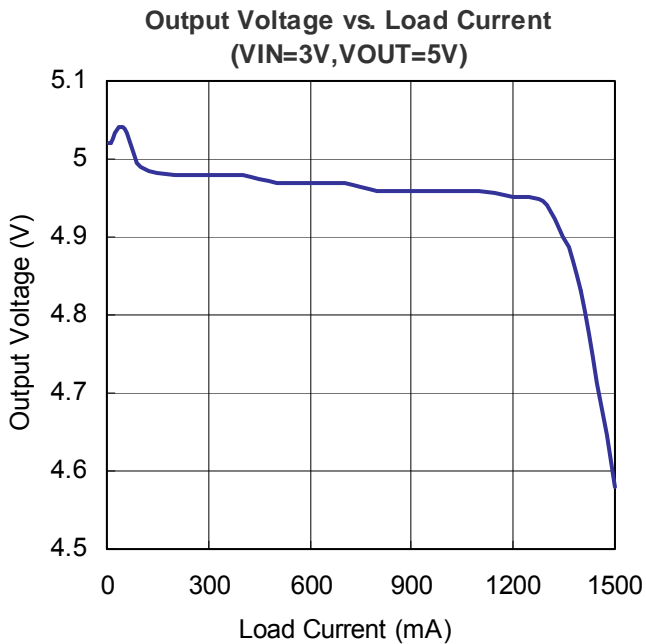| TOP VIEW SOT-23-6L	PIN	NAME	FUNCTION
	1/3	GND	Ground
	2	SW	Switch Node for Output
	4	FB	Feedback
	5	VDD	Input Positive Power Pin
	6	EN	ON/OFF Control(High Enable)

Electrical Characteristics

Operating Conditions: TA = 25°C, V_{IN} = 1.5V, VDD set to 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{START}	Start-up Voltage	I_{LOAD}=1mA		1.1		V
V_{IN}	Operating Voltage range		1.1		5.5	V
$I_{NO\ LOAD}$	No Load Current (V_{IN})	V_{IN}=1.5V, V_{OUT}=3.3V		70		µA
V_{FB}	Feedback Reference Voltage	Close Loop, V_{DD}=3.3V	1.182	1.212	1.242	V
f_{OSC}	Switching Frequency	V_{DD}=3.3V			450	kHz
R_{ON}	SW ON Resistance	V_{DD}=3.3V		0.07		Ω
ΔV_{LINE}	Line Regulation	V_{IN}=1.5V $\sim$ 2.5V, I_{LOAD}=100mA		25		mV/V
ΔV_{LOAD}	Load Regulation	V_{IN}=2.5V, I_{LOAD}=1mA $\sim$ 300mA		0.05		mV/mA
V_{ENH}	En Input High		1			V
V_{ENL}	En Input Low				0.6	V

Typical Performance Characteristics

Efficiency vs. Output Current (VOUT=5V)

Efficiency vs. Output Current (Vout=3.3V)

Supply Current vs. Supply Voltage (VOUT=5V Io=0A)

Supply Current vs. Supply Voltage (VOUT=3.3V Io=0A)

Output Voltage vs. Load Current (VIN=3V,VOUT=5V)

Output Voltage vs. Load Current (VIN=3V,VOUT=3.3V)

Pin Information

GND (Pin 1/3): Signal and Power Ground. Provide a short direct PCB path between GND and the (–) side of the output capacitor(s).

SW (Pin 2): Switch Pin. Connect inductor between SW and V_{IN}. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.

FB (Pin 4): Feedback Input to the g_m Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 1.8V to 5.5V by: $V_{OUT} = 1.212V \cdot [1 + (R1/R2)]$

VDD (Pin 5): Input Positive Power Pin.

EN (Pin 6): En Control Input. Forcing this pin above 1V enables the part. Forcing this pin below 0.6V shuts down the device. Do not leave EN floating.

Application Information

Output Voltage Setting

Referring to Typical Application Circuits, the output voltage of the switching regulator (V$_{OUT}$) can be set with Equation (1).

$$V_{OUT} = (1 + \frac{R1}{R2}) \times 1.212V \quad (1)$$

Feedback Loop Design

Referring to the Typical Application Circuits. The selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

➢ Follow Equation (1)

➢ Higher R reduces the quiescent current (Path current = 1.212V/R2), however resistors beyond 5MW are not Recommended.

➢ Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pin.

For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed. Such high impedance feedback loop is sensitive to any interference, which requires careful PCB layout and avoid any interference, especially to FB pin. To improve the system stability, a proper value capacitor between FB pin and GND pin is suggested. An empirical suggestion is around 22pF.
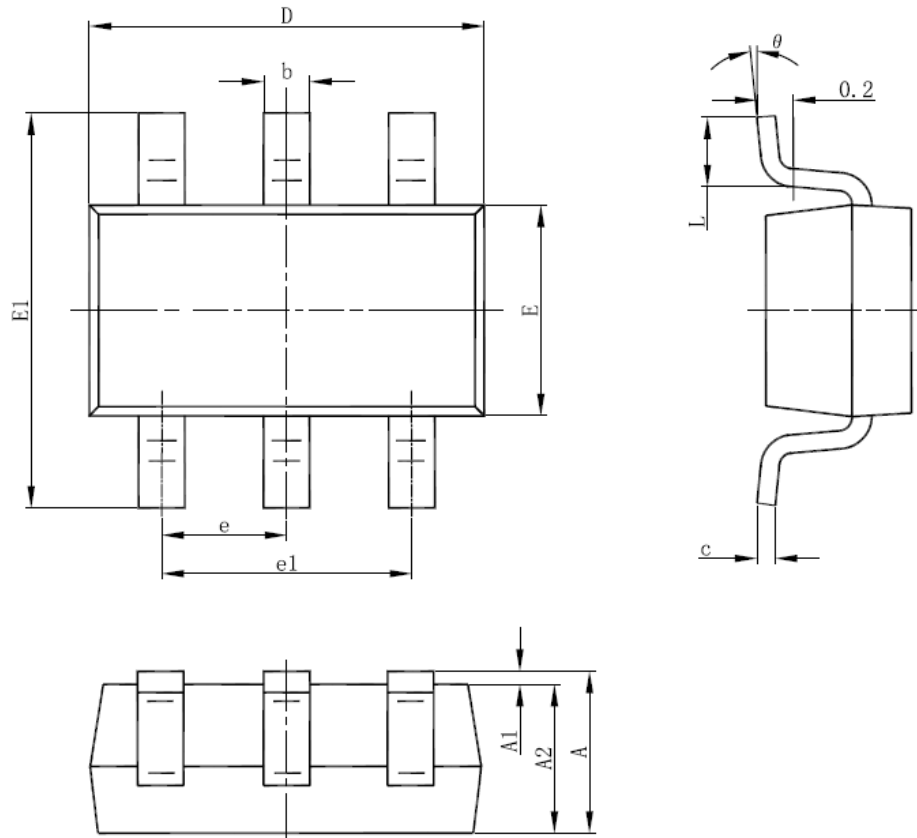
PCB Layout Guide

PCB Layout shall follow these guidelines for better system stability:

➢ A full GND plane without gap break.

➢ VDD to GND noise bypass - Short and wide connection for the 20-100μF capacitor between Pin 5 and Pin 1.

➢ VIN to GND noise bypass - Add a 10μF capacitor close to L1 inductor, when V$_{IN}$ is not an idea voltage source.

➢ Minimized FB node copper area and keep far away from noise sources.

Packaging Information

SOT-23-6L Package Outline Dimension

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Subject changes without notice.

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