

High-Speed CMOS Logic Quad 2-Input AND Gate

Features

- Buffered Inputs
- Typical Propagation Delay: 7ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^{\circ}C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^{\circ}C$ to $125^{\circ}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
- CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

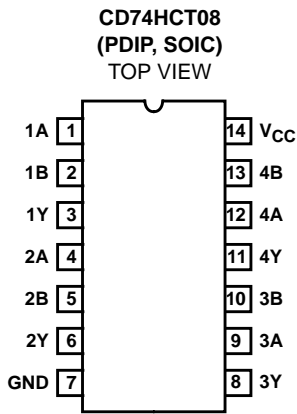
The CD54HC08, CD54HCT08, CD74HC08, and CD74HCT08 logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 74HCT logic family is functionally pin compatible with the standard 74LS logic family.

Ordering Information

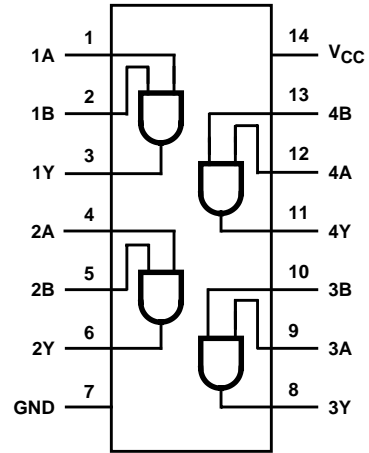
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC08F3A	-55 to 125	14 Ld CERDIP
CD54HCT08F3A	-55 to 125	14 Ld CERDIP
CD74HC08E	-55 to 125	14 Ld PDIP
CD74HC08M	-55 to 125	14 Ld SOIC
CD74HC08MT	-55 to 125	14 Ld SOIC
CD74HC08M96	-55 to 125	14 Ld SOIC
CD74HC08PW	-55 to 125	14 Ld TSSOP
CD74HC08PWR	-55 to 125	14 Ld TSSOP
CD74HCT08E	-55 to 125	14 Ld PDIP
CD74HCT08M	-55 to 125	14 Ld SOIC
CD74HCT08MT	-55 to 125	14 Ld SOIC
CD74HCT08M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout



Functional Diagram

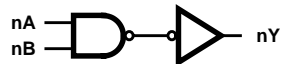


TRUTH TABLE

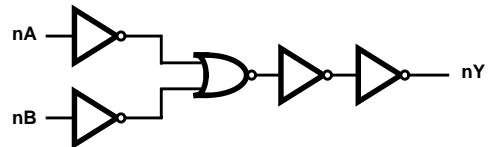
INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = High Voltage Level, L = Low Voltage Level

HC Logic Symbol



HCT Logic Symbol



Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

Operating Conditions

Temperature Range (T_A)	-55°C to 125°C
Supply Voltage Range, V_{CC}	
HC Types	2V to 6V
HCT Types	4.5V to 5.5V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	80
M (SOIC) Package	86
PW (TSSOP) Package	113
Maximum Junction Temperature (Hermetic Package or Die) . . .	175°C
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	2	-	20	-	40	μA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	2	-	20	-	40	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Input to Output (Figure 1)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	90	-	115	-	135	ns
			4.5	-	-	18	-	23	-	27	ns
			6	-	-	15	-	20	-	23	ns
Propagation Delay, Data Input to Output Y	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	7	-	-	-	-	ns	

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Transition Times (Figure 1)	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	-	37	-	-	-	-	pF	
HCT TYPES											
Propagation Delay, Input to Output Y (Figure 2)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	25	-	31	-	38	ns
Propagation Delay, Data Input to Output Y	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	10	-	-	-	-	-	ns
Transition Times (Figure 2)	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_I	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	-	51	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

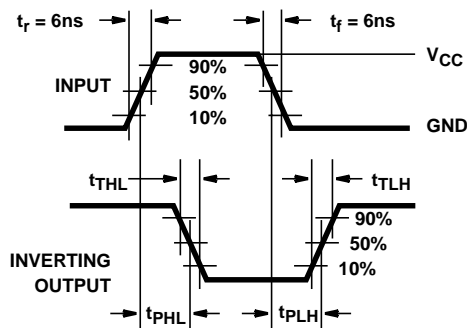


FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

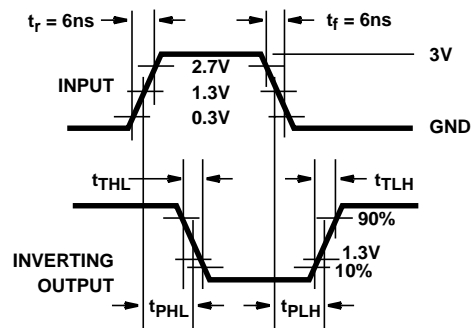
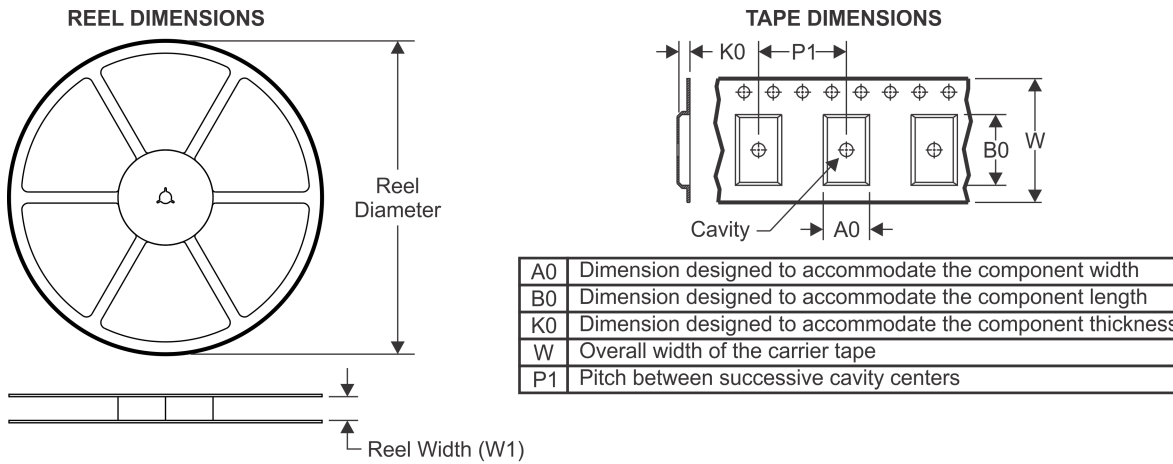
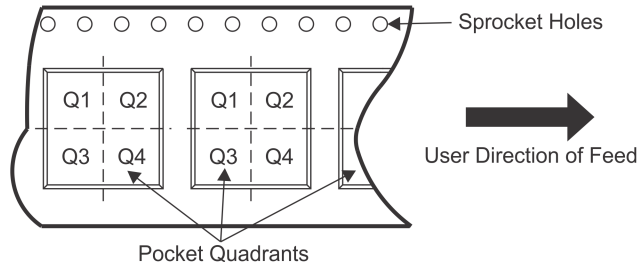


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

TAPE AND REEL INFORMATION



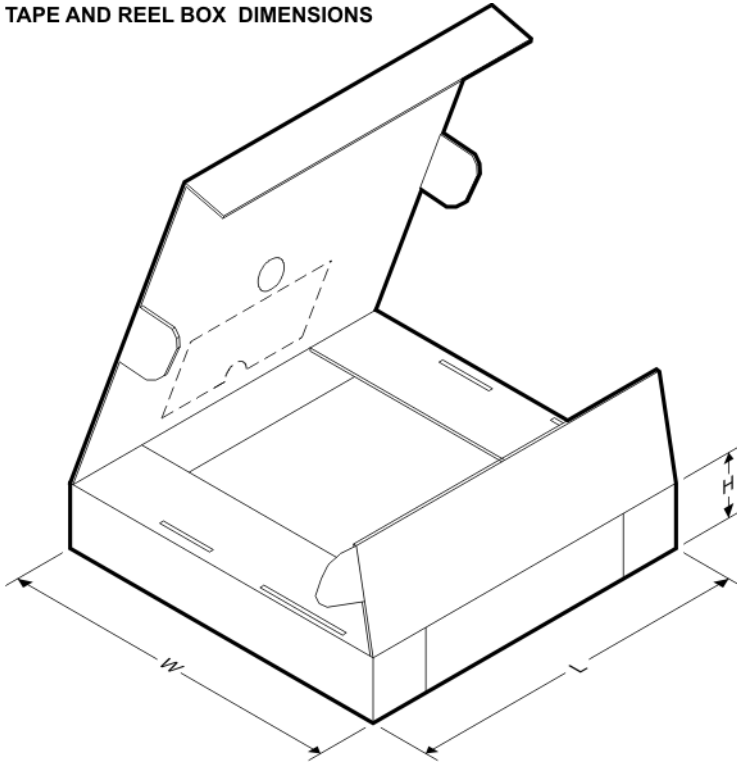
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC08M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC08MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT08M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



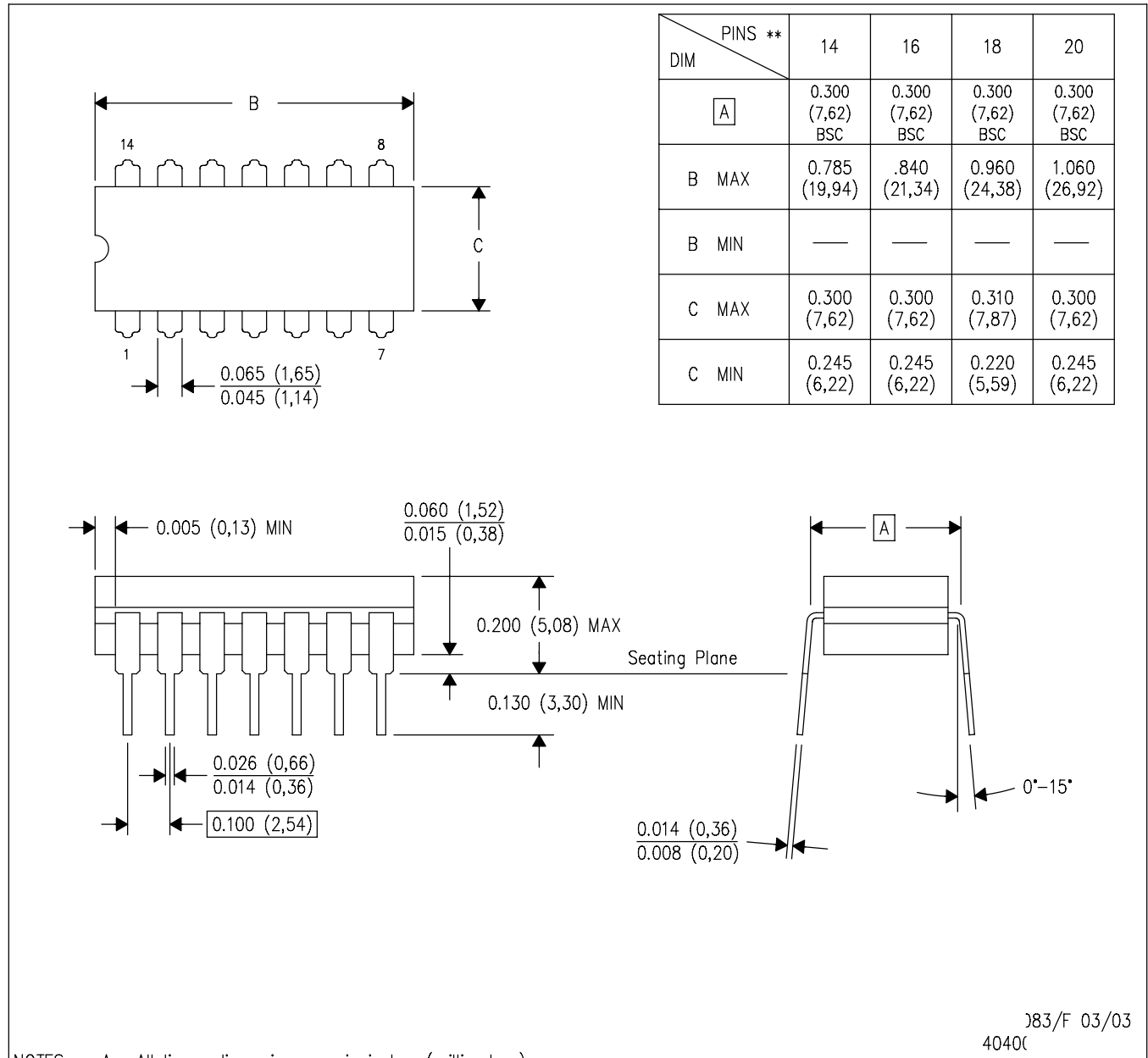
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC08M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC08MT	SOIC	D	14	250	367.0	367.0	38.0
CD74HC08PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CD74HCT08M96	SOIC	D	14	2500	367.0	367.0	38.0

J (R-GDIP-T**)

CERAMIC DUAL IN-LINE PACKAGE

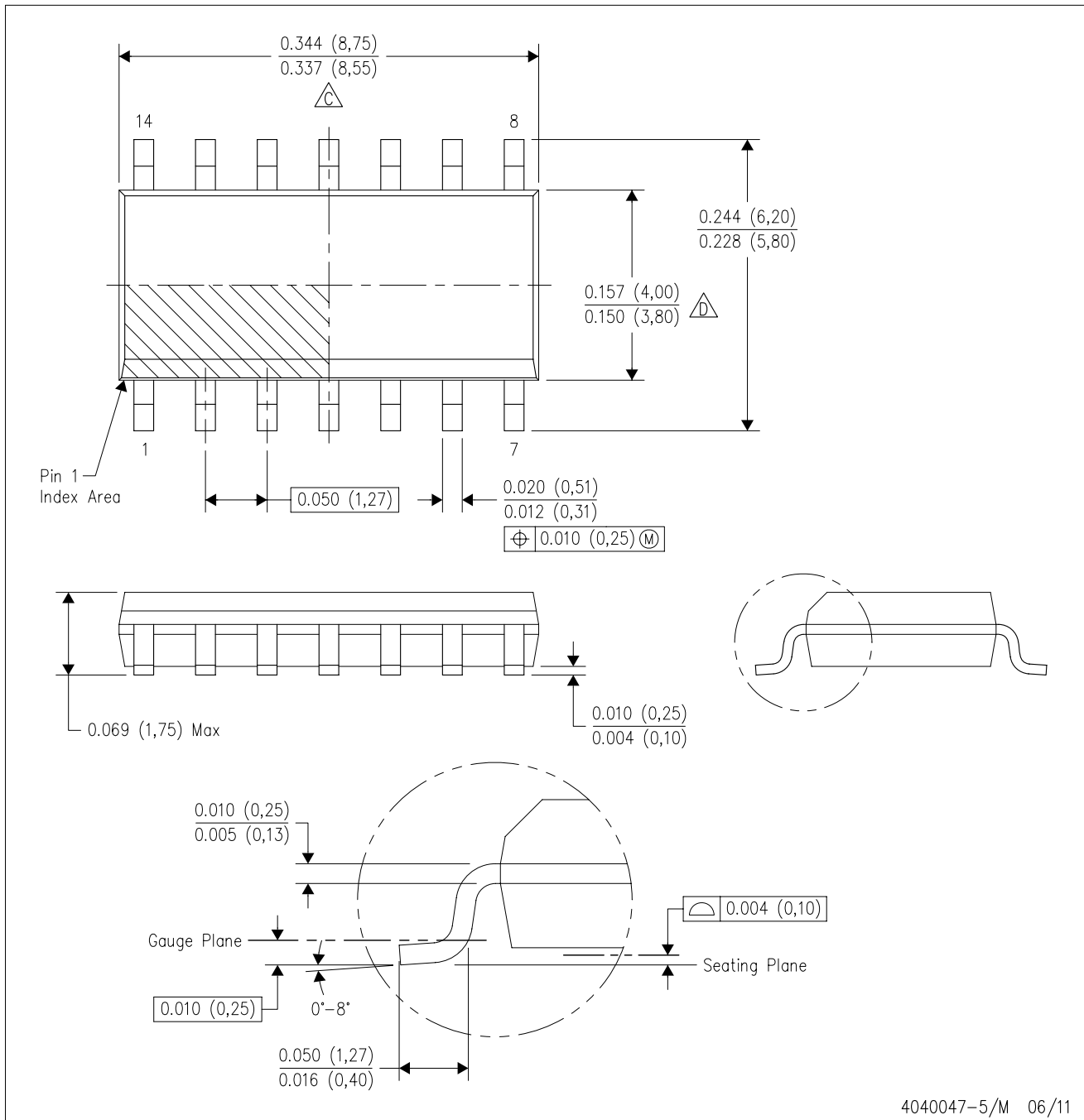
14 LEADS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

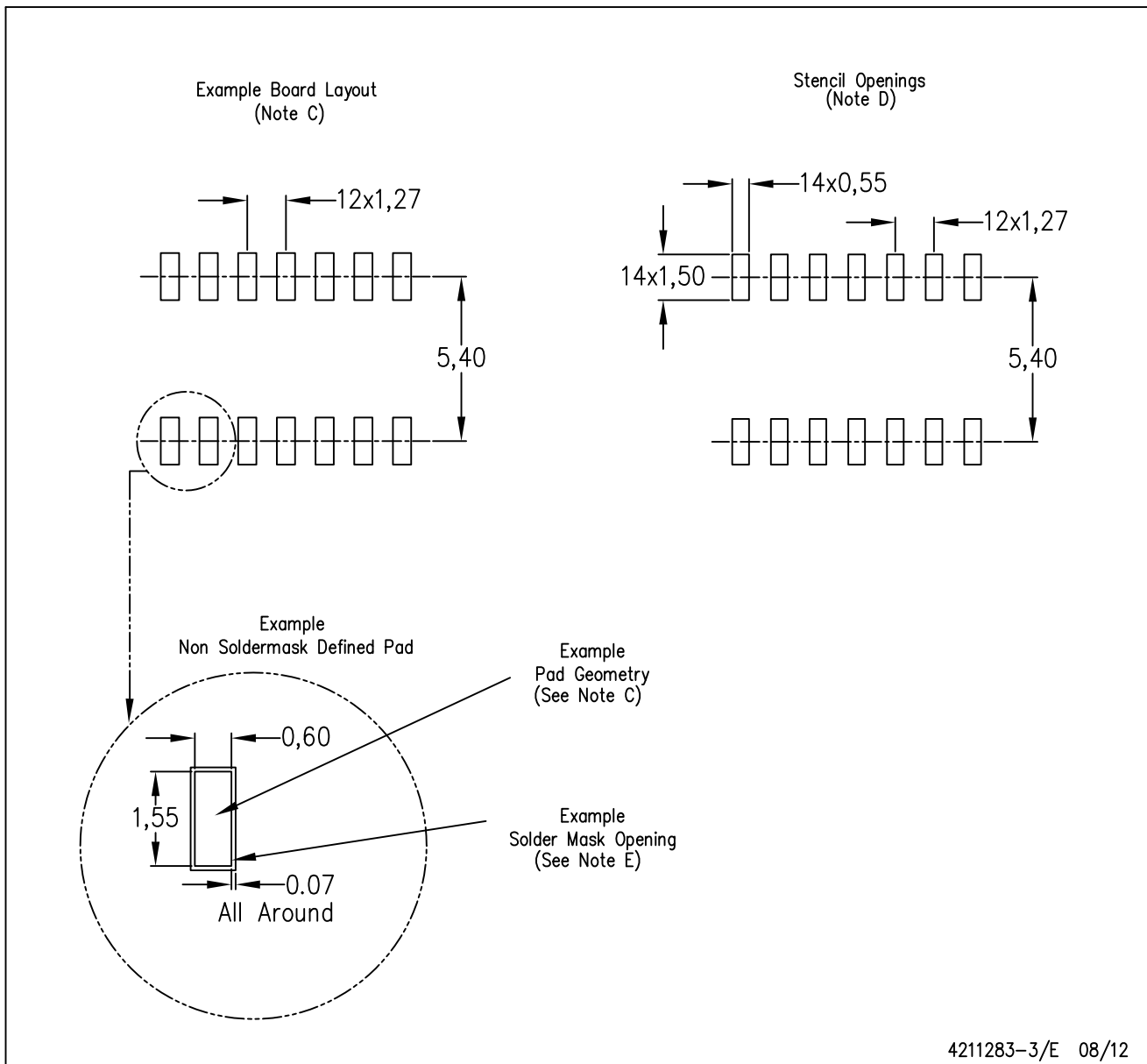
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)
PLASTIC SMALL OUTLINE


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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[7](#) [NLU1G04AMUTCG](#) [NLX2G04CMUTCG](#) [NLX2G04AMUTCG](#) [NLV74ACT00DR2G](#) [NLV74AC14DR2G](#) [NLV37WZ14USG](#)
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[NL17SG14DFT2G](#) [74LVC06ADTR2G](#) [74LVC04ADR2G](#) [TC7SZ04AFS,L3J](#) [NLU1GT04AMUTCG](#) [NLV37WZ04USG](#)
[NLX3G14FMUTCG](#) [NL17SZ04P5T5G](#) [NL17SG14P5T5G](#) [NLV27WZU04DFT2G](#) [LV0008G100-4EOFN](#)