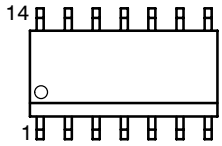
Quad 2-Input NAND Gate with Schmitt-Trigger Inputs

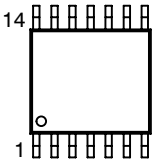
High−Performance Silicon−Gate CMOS

The 74HC132 is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs.

The HC132 can be used to enhance noise immunity or to square up slowly changing waveforms.



SOIC−14



TSSOP−14

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These are Pb−Free Devices

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

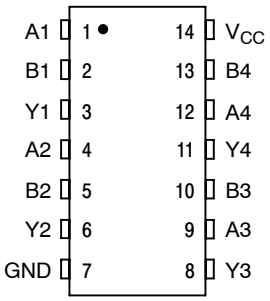


Figure 1. Pin Assignment

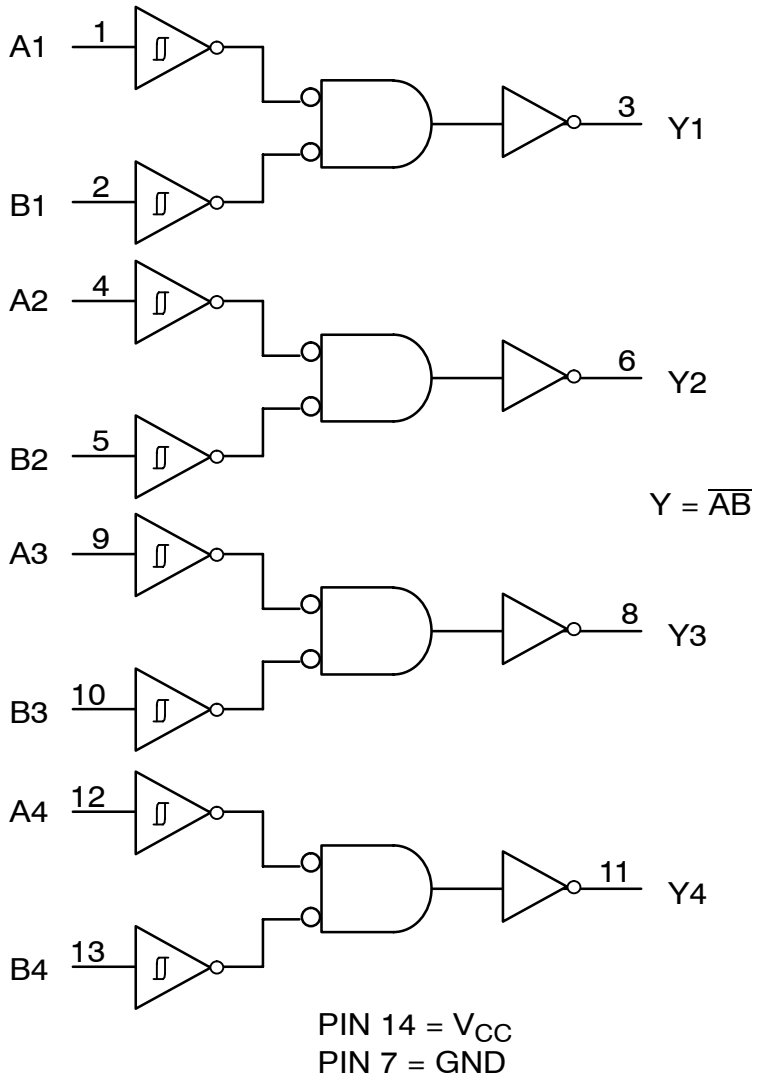


Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage	Output in 3−State High or Low State	−0.5 to +7.0 −0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{GND}	DC Ground Current per Ground Pin		±75	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	14−SOIC 14−TSSOP	125 170	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2)	>2000 >200	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 3)	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	−	No Limit (Note 5)	ns

5. When V_{IN} ~ 0.5 V_{CC}, I_{CC} >> quiescent current.
6. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limit			Unit
				−55°C to 25°C	≤85°C	≤125°C	
V_{T+}max	Maximum Positive−Going Input Threshold Voltage (Figure 5)	V_{OUT} = 0.1 V $\|I_{OUT}\| \le$ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{T+}min	Minimum Positive−Going Input Threshold Voltage (Figure 5)	V_{OUT} = 0.1 V $\|I_{OUT}\| \le$ 20 μA	2.0 4.5 6.0	1.0 2.3 3.0	0.95 2.25 2.95	0.95 2.25 2.95	V
V_{T-}max	Maximum Negative−Going Input Threshold Voltage (Figure 5)	$V_{OUT} = V_{CC} - 0.1$ V $\|I_{OUT}\| \le$ 20 μA	2.0 4.5 6.0	0.9 2.0 2.6	0.95 2.05 2.65	0.95 2.05 2.65	V
V_{T-}min	Minimum Negative−Going Input Threshold Voltage (Figure 5)	$V_{OUT} = V_{CC} - 0.1$ V $\|I_{OUT}\| \le$ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
$V_H$max (Note 7)	Maximum Hysteresis Voltage (Figure 5)	V_{OUT} = 0.1 V or $V_{CC} - 0.1$ V $\|I_{OUT}\| \le$ 20 μA	2.0 4.5 6.0	1.2 2.25 3.0	1.2 2.25 3.0	1.2 2.25 3.0	V
$V_H$min (Note 7)	Minimum Hysteresis Voltage (Figure 5)	V_{OUT} = 0.1 V or $V_{CC} - 0.1$ V $\|I_{OUT}\| \le$ 20 μA	2.0 4.5 6.0	0.2 0.4 0.5	0.2 0.4 0.5	0.2 0.4 0.5	V
V_{OH}	Minimum High−Level Output Voltage	$V_{IN} \le$ V_{T-}min or V_{T+}max $\|I_{OUT}\| \le$ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} \le$ −V_{T-}min or V_{T+}max $\|I_{OUT}\| \le$ 4.0 mA $\|I_{OUT}\| \le$ 5.2 mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low−Level Output Voltage	$V_{IN} \ge$ V_{T+}max $\|I_{OUT}\| \le$ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} \ge$ V_{T+}max $\|I_{OUT}\| \le$ 4.0 mA $\|I_{OUT}\| \le$ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0 μA	6.0	2.0	20	40	μA

7. $V_H$min > (V_{T+}min) − (V_{T-}max); $V_H$max = (V_{T+}max) + (V_{T-}min).
8. Information on typical parametric values can be found in the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} (V)	Guaranteed Limit −55°C to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (per Gate) (Note 10)	24	pF

10. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

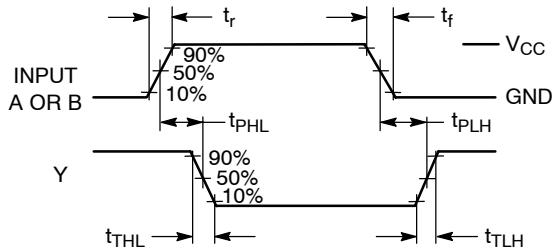
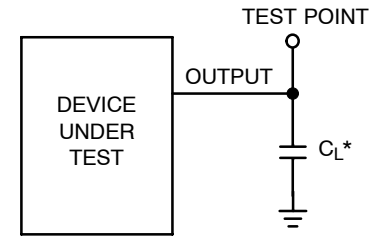


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

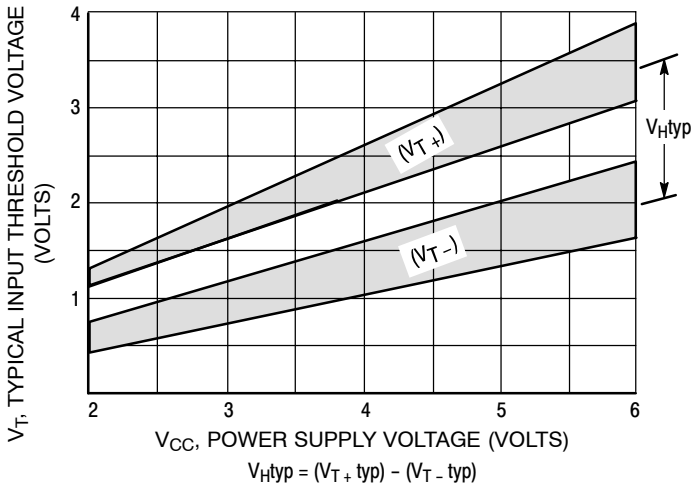


Figure 5. Typical Input Threshold, V_{T+}, V_{T-} Versus Power Supply Voltage

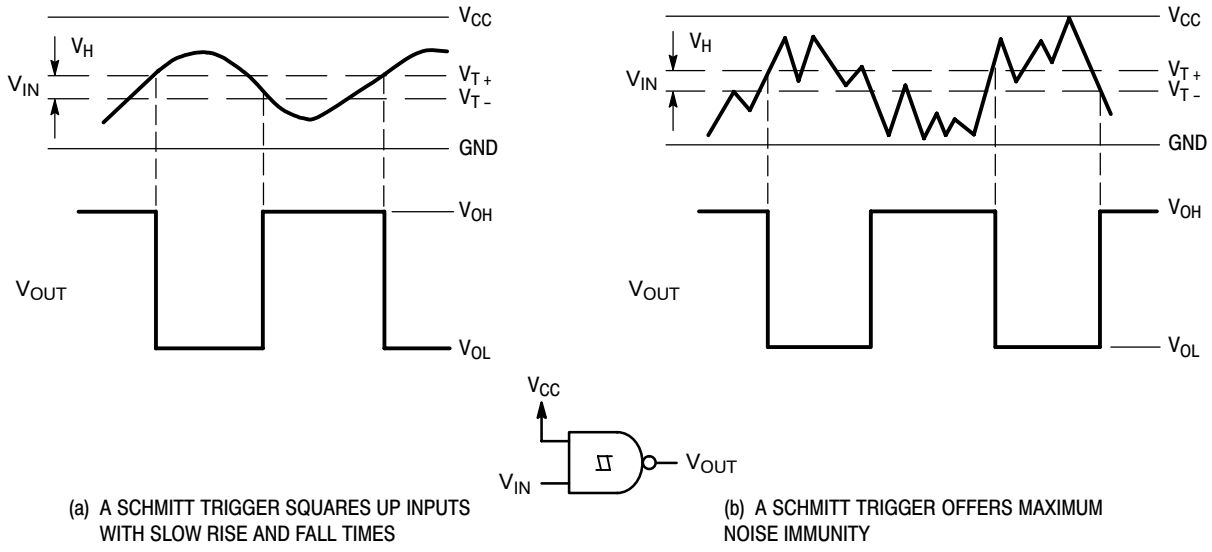


Figure 6. Typical Schmitt−Trigger Applications

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5962-8550101CA E5-652Z NL17SGU04P5T5G NL17SZ14P5T5G NLX2G04BMX1TCG 412327H 022413E NL17SG14AMUTCG NLU2G04AMUTCG NLU2GU04BMX1TCG NLV14049UBDR2G NLV14069UBDTR2G NLV17SZ14DFT2G NLVVHC1G05DFT2G 74LVC2G17FW4-7 NLU2G04CMX1TCG NLV17SZ06DFT2G NLV27WZ04DFT2G NLV74HCT14ADTR2G NLX2G14CMUTCG NLU1G04AMX1TCG SNJ54ACT14W SNJ54AC04W NCV1729SN35T1G TC74VHC04FK(EL,K) NLV74HC04ADTR2G NLV17SZ04DFT2G 74AUP2G04FW3-7 NLU1G04AMUTCG NLX2G04CMUTCG NLX2G04AMUTCG NLV74ACT00DR2G NLV74AC14DR2G NLV37WZ14USG NLV27WZ04DFT1G NLV14106BDG NLU1GU04CMUTCG NLU1GT14AMUTCG NLU1G04CMUTCG NL17SZU04P5T5G NL17SG14DFT2G 74LVC06ADTR2G 74LVC04ADR2G TC7SZ04AFS,L3J NLU1GT04AMUTCG NLV37WZ04USG NLX3G14FMUTCG NL17SZ04P5T5G NL17SG14P5T5G NLV27WZU04DFT2G