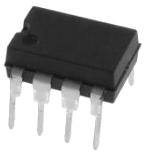
128K Bits Eeprom

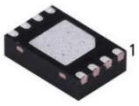
Features

- Compatible with all data transfer protocol
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array:
  - 128 Kbit (16 Kbytes) of EEPROM
  - Page size: 64 bytes
  - Additional Write lockable page
- Single supply voltage and high speed:1 MHz
- Write:
  - Byte Write within 3 ms
  - Page Write within 3 ms
- Operating Ambient Temperature:From -40°C to +85°C
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Internally Organized:AT24C128A, 16,384 X 8 (128K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Write Protect Pin for Hardware Data Protection
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- 8-lead DIP /SOP/MSOP/DFN packages


DIP-8


SOP-8


MSOP-8


DFN-8（2*3）

Ordering Information

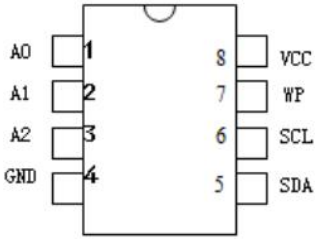
DEVICE	Package Type	MARKING	Packing	Packing Qty
AT24C128AN	DIP-8	24C128A	TUBE	2000pcs/box
AT24C128AM/TR	SOP-8	24C128A	REEL	2500pcs/reel
AT24C128AMM/TR	MSOP-8	C128A	REEL	3000pcs/reel
AT24C128ADQ/TR	DFN-8 2*3	C128A	REEL	3000pcs/reel

Description

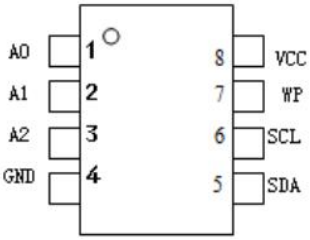
The AT24C128A provides 131,072 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 16,384 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

Pin Configuration

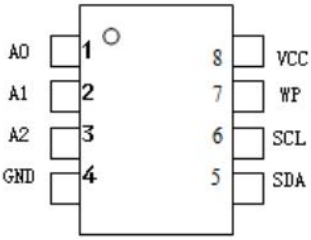
8 -lead PDIP



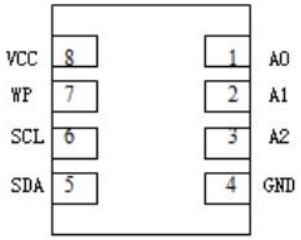
8 -lead SOP



8 -lead MSOP



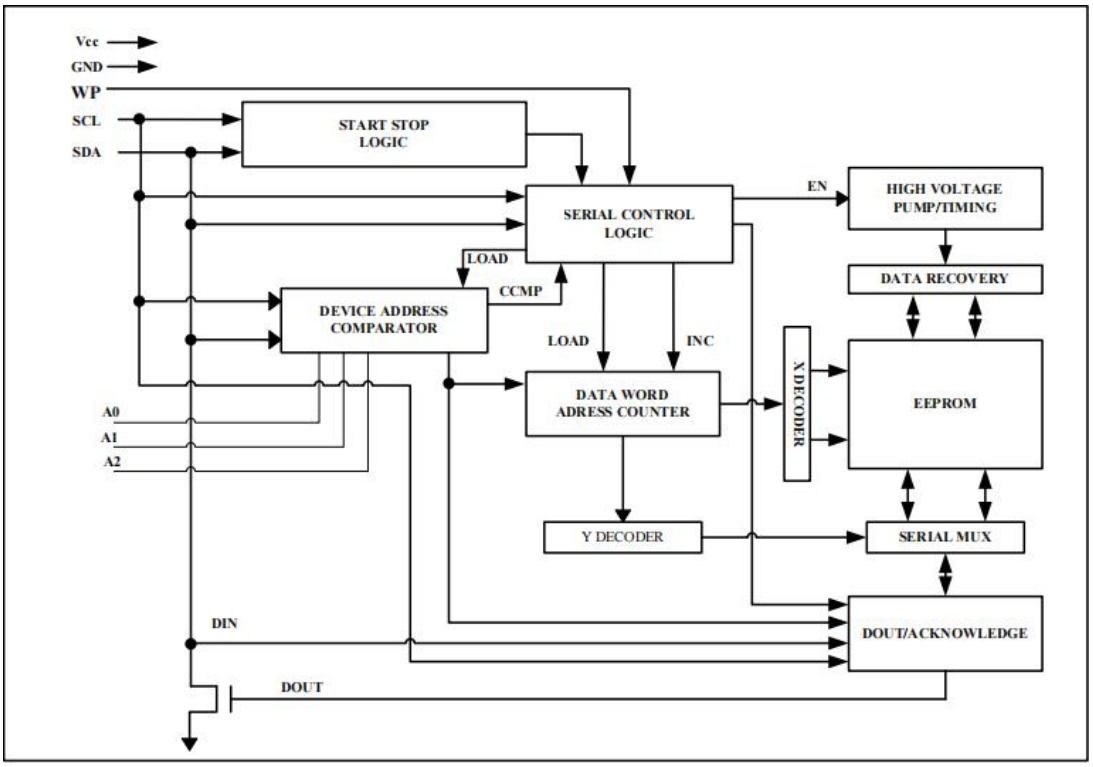
8 -pad DFN



Pin Description

Pin Name	Type	Functions
A0-A2	I	Address Inputs
SDA	I/O&Open-drain	Serial Data
SCL	I	Serial Clock Input
WP	I	Write Protect
GND	P	Ground
Vcc	P	Power Supply

Block Diagram



DEVICE/PAGE ADDRESSES (A2, A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wire for the AT24C128A. Eight 128K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The AT24C128A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc, the write protection feature is enabled and operates as shown in the following **.**

WP Pin Status	AT24C128A
At VCC	Full （128K）Array
At GND	Normal Read/Write Operations

Functional Description

1. Memory Organization

AT24C128A, 128K SERIAL EEPROM: Internally organized with 256 pages of 64 bytes each, the 128K requires a 14-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 1**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 2**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 2**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C128A features a low-power standby mode which is enabled: (a) upon power-up and (b) afer the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

Figure 1. Data Validity

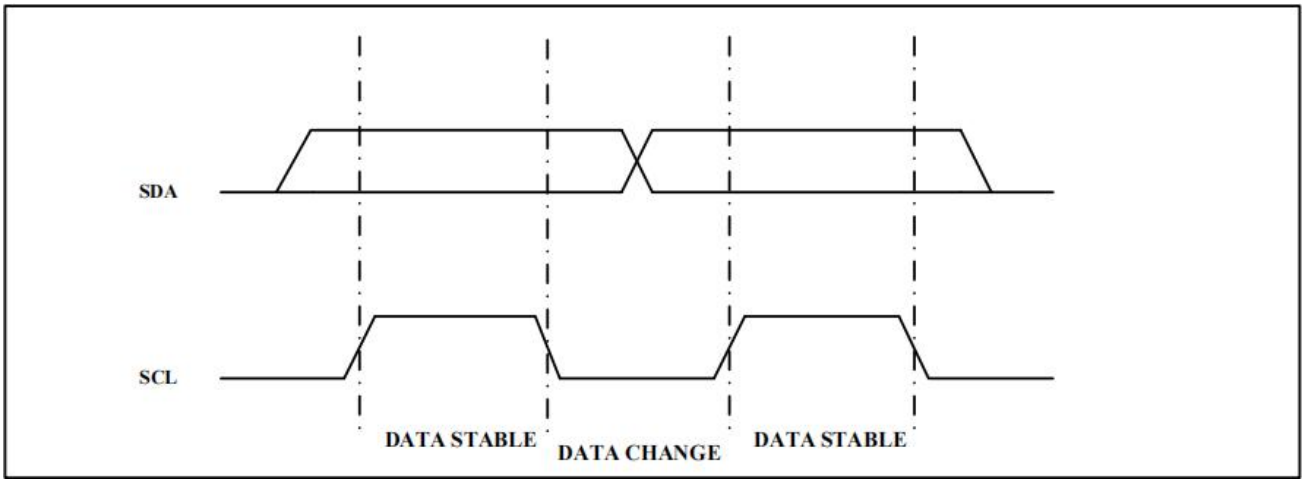


Figure 2. Start and Stop Definition

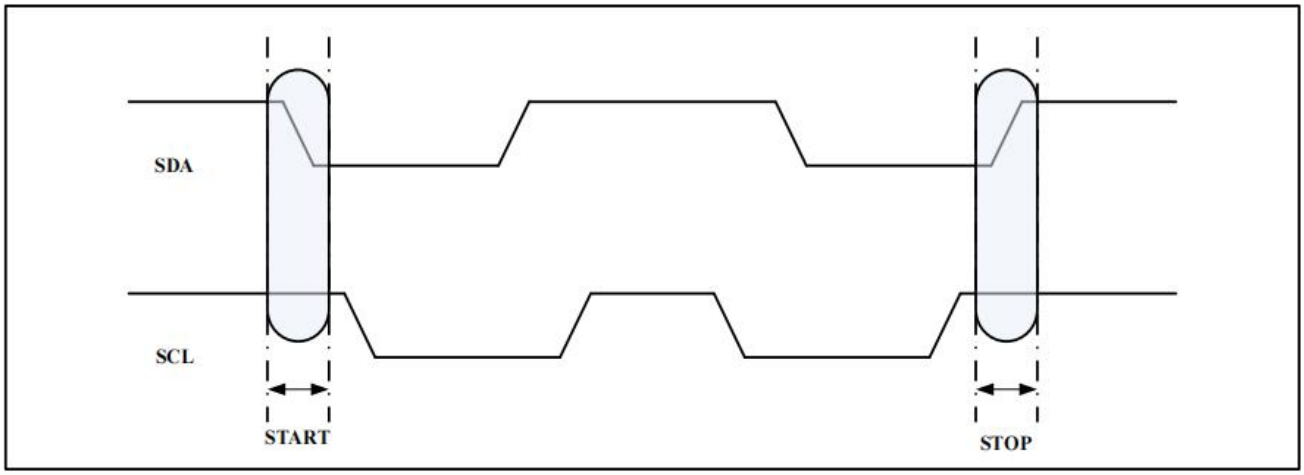
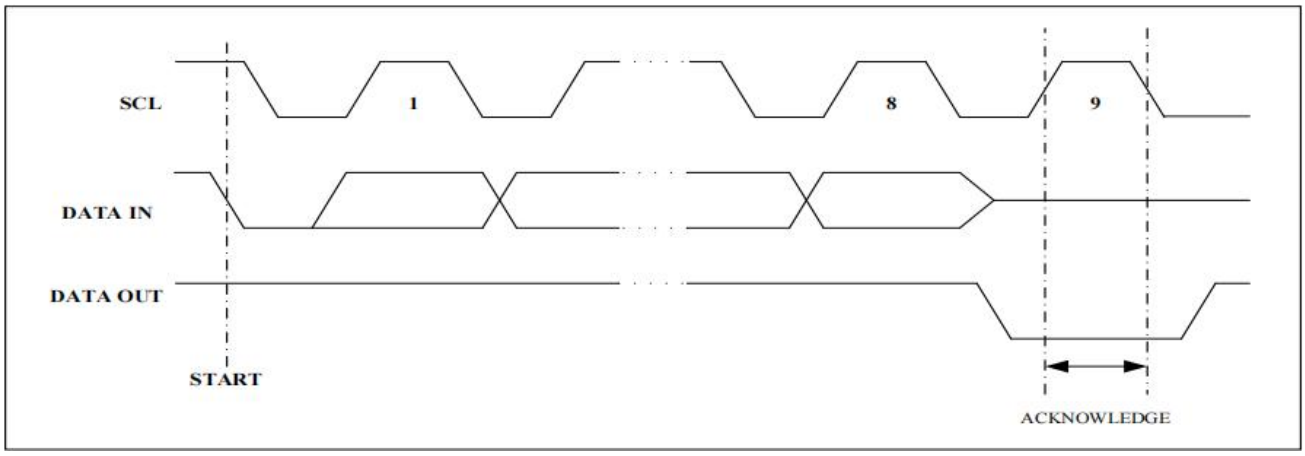


Figure 3. Output Acknowledge



3. Device Addressing

The 128K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 4**)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 128K EEPROM uses A2, A1 and A0 device address bits to allow as much as eight devices on the same bus. These 3 bits must be compared to their corresonding hardwired input pins.

The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

DATA SECURITY: The AT24C128A has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at VCC.

4. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 5**).

PAGE WRITE: The 128K EEPROM is capable of an 64-byte page writes. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 6**).

The data word address lower six bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations:
current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 7**).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 8**)

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 9**).

Figure 4. Device Address

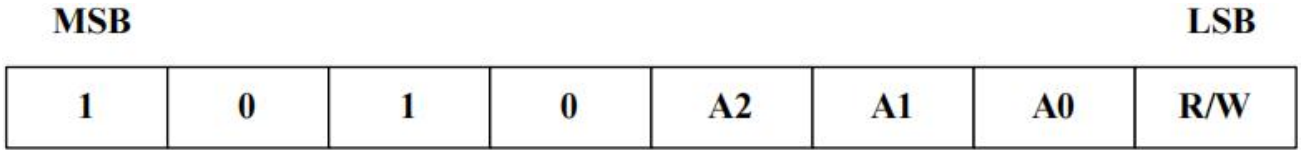
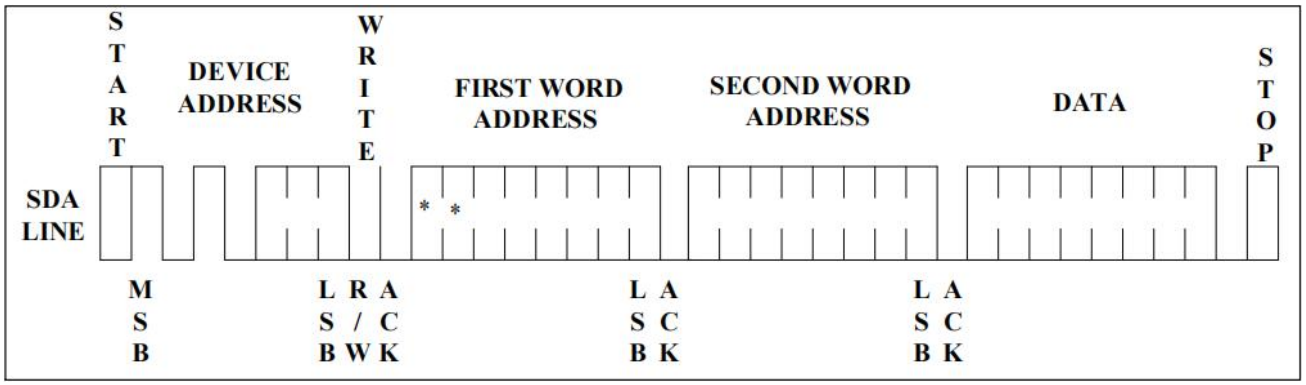


Figure 5. Byte Write



Note.1*=DON'T CARE BITS

Figure 6. Page Write

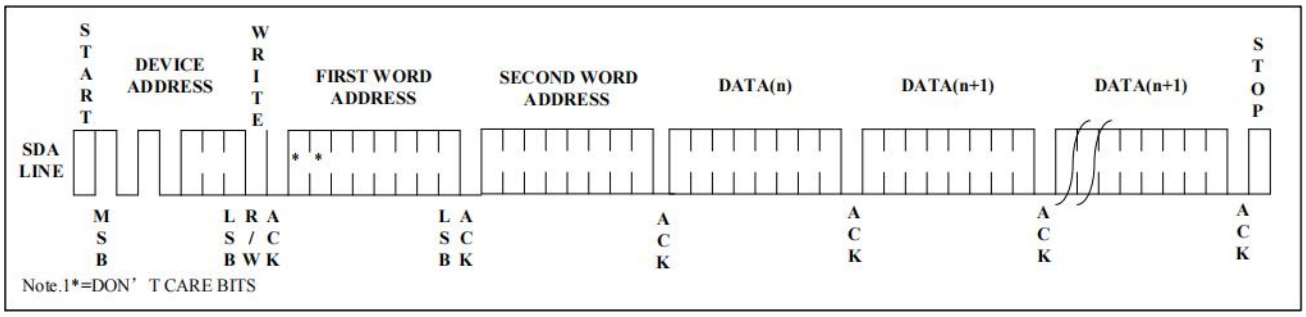


Figure 7. Current Address Read

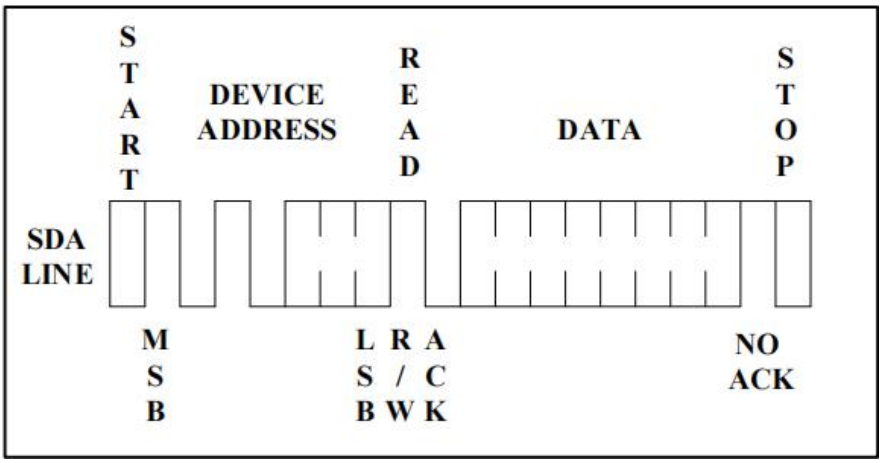


Figure 8. Random Read

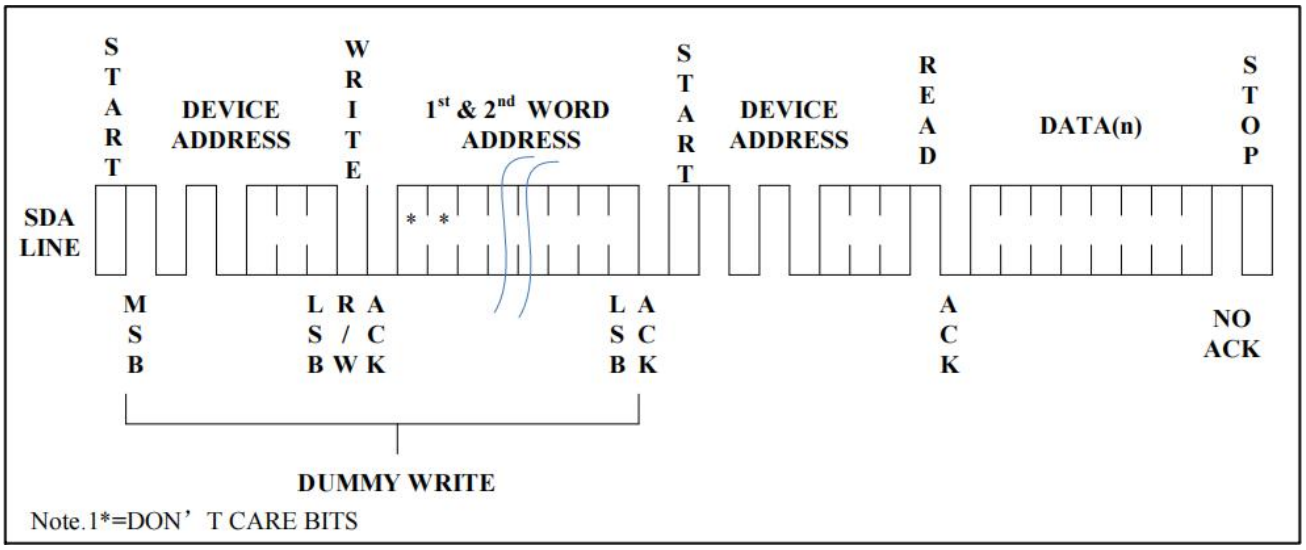
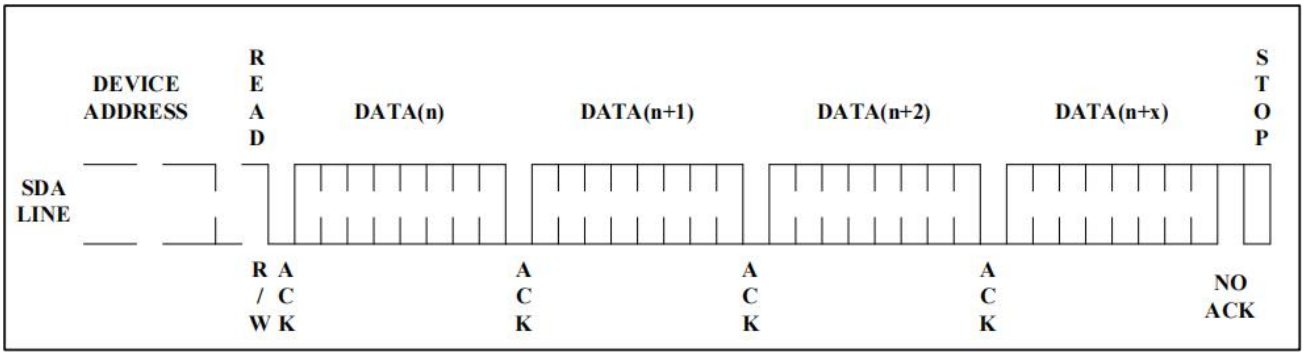


Figure 9. Sequential Read



Electrical Characteristics

Absolute Maximum Stress Ratings：

Condition	LIMITS
DC Supply Voltage	-0.3V to +6.5V
Input / Output Voltage	GND-0.3V to VCC+0.3V
Operating Ambient Temperature	- 40℃ to +85℃
Storage Temperature	-65℃ to +150℃
Lead Temperature (Soldering, 10 seconds)	245℃

Comments ： Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40℃ to +85℃, VCC = +1.7V to +5.5V
(unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	VCC1	1.7	-	5.5	V	-
Supply Voltage	VCC2	2.5	-	5.5	V	-
Supply Voltage	VCC3	2.7	-	5.5	V	-
Supply Voltage	VCC4	4.5	-	5.5	V	-
Supply Current VCC=5.0V	ICC1	-	0.4	1.0	mA	READ at 400KHZ
Supply Current VCC=5.0V	ICC2	-	2.0	3.0	mA	WRITE at 400KHZ
Supply Current VCC=1.7V	ISB	-	0.6	1.0	μA	VIN=VCC or VSS
Supply Current VCC=2.5V	ISB	-	1.0	2.0	μA	VIN=VCC or VSS
Supply Current VCC=2.7V	ISB	-	1.0	2.0	μA	VIN=VCC or VSS
Supply Current VCC=5.0V	ISB	-	2.0	5.0	μA	VIN=VCC or VSS
Input Leakage Current	IL	-	0.10	3.0	μA	VIN=VCC or VSS
Output Leakage Current	IL	-	0.05	3.0	μA	VOUT=VCC or VSS
Input Low Level	VIL1	-0.3	-	VCC×0.3	V	VCC=1.8V to 5.5V
Input High Level	VIH1	VCC×0.7	-	VCC+0.3	V	VCC=1.8V to 5.5V
Input Low Level	VIL2	-0.3	-	VCC×0.2	V	VCC=1.7V
Input High Level	VIH2	VCC×0.7	-	VCC+0.3	V	VCC=1.7V
Output Low Level VCC=5.0V	VOL3	-	-	0.4	V	IOL=3.0mA
Output Low Level VCC=3.0V	VOL2	-	-	0.4	V	IOL=2.1mA
Output Low Level VCC=1.7V	VOL1	-	-	0.2	V	IOL=0.15mA

Pin Capacitance

Applicable over recommended operating range from TA = 25℃, f = 1.0 MHz, VCC = +1.7V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	CI/O	-	-	8	pF	VIO=0V
Input Capacitance(SCL)	CIN	-	-	6	pF	VIN=0V

AC Electrical Characteristics

Applicable over recommended operating range from TA = -40℃ to +85℃, VCC = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

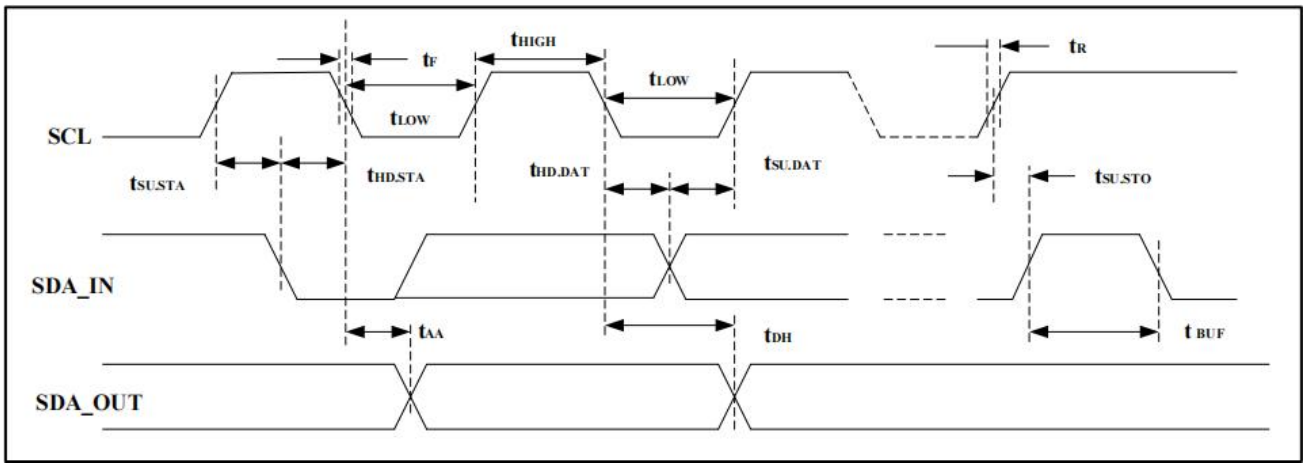
Parameter	Symbol	1.7V≤VCC < 2.5V			2.5V≤VCC < 5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Frequency,SCL	fSCL	-	-	400	-	-	1000	KHZ
Clock Pulse Width Low	tLOW	1.2	-	-	0.6	-	-	μs
Clock Pulse Width High	tHIGH	0.6	-	-	0.4	-	-	μs
Noise Suppression Time	tI	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	tAA	0.1	-	0.9	0.05	-	0.9	μs
Time the bus must be free before a new transmission can start	tBUF	1.2	-	-	0.5	-	-	μs
Start Hold Time	tHD:STA	0.6	-	-	0.25	-	-	μs
Start Setup Time	tSU:DAT	0.6	-	-	0.25	-	-	μs
Data In Hold Time	tHD:DAT	0	-	-	0	-	-	μs
Data in Setup Time	tSU:DAT	100	-	-	100	-	-	ns
Input Rise Time(1)	tR	-	-	0.3	-	-	0.3	μs
Input Fall Time(1)	tF	-	-	0.3	-	-	0.3	μs
Stop Setup Time	tSu:STO	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	tDH	50	-	-	50	-	-	ns
Write Cycle Time	twR	-	3.3	5	-	3.3	5	ms
5.0V,25℃,Byte Mode(1)	Endurance	1M	-	-	-	-	-	Write Cycle

Notes:

1. This parameter is characterized and is not 100%
2. AC measurement conditions: RL (connects to VCC): 1.3 k
   Input pulse voltages: 0.3 VCC to 0.7 VCC
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 VCC
   The value of RL should be concerned according to the actual loading on the user's system.

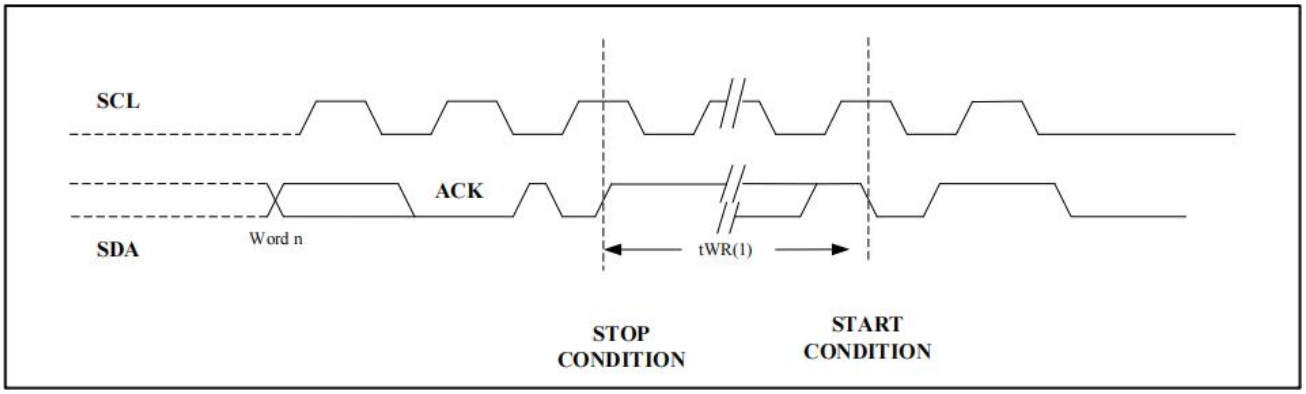
Bus Timing

Figure 10. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 11. SCL: Serial Clock, SDA: Serial Data I/O

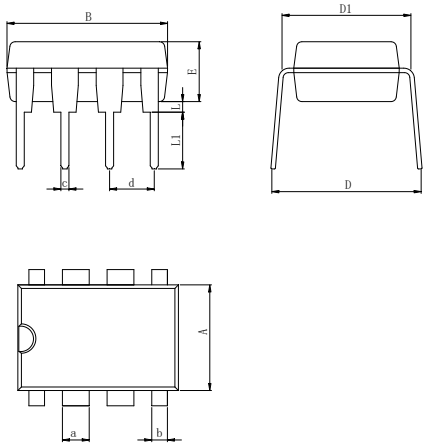


Notes:

The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

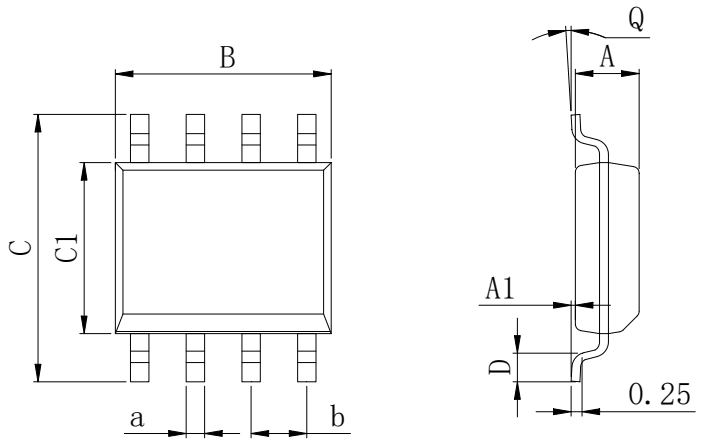
Physical Dimensions

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

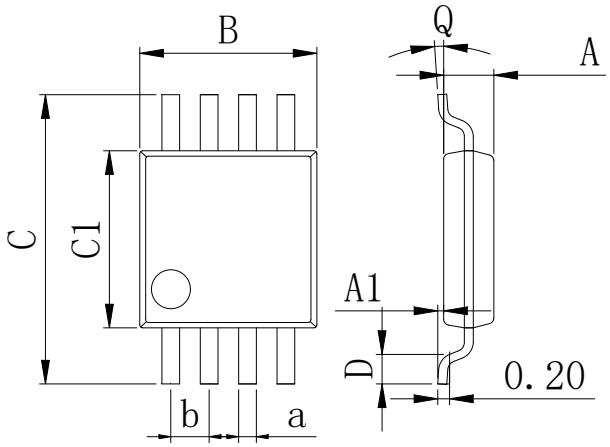
SOP-8 (150mil)



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

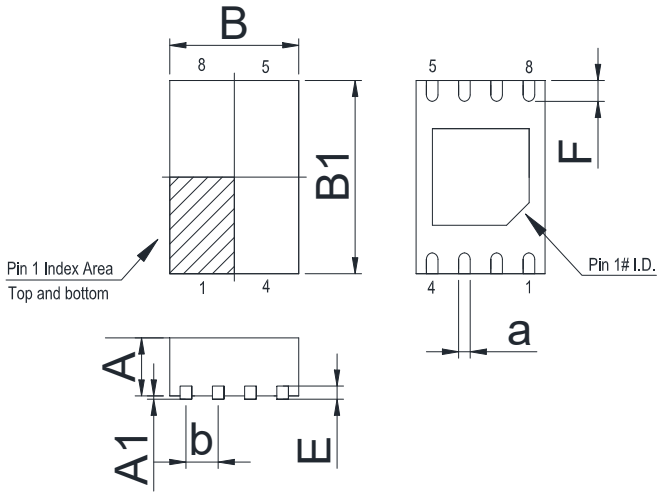
Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

DFN-8 2*3



Dimensions In Millimeters(DFN-8 2*3)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0	1.90	2.90	0.15	0.25	0.20	0.50TYP
Max:	0.95	0.05	2.10	3.10	0.25	0.35	0.30	

Revision History

DATE	REVISION	PAGE
2016-12-5	New	1-15
2023-8-31	Update encapsulation type、Update Lead Temperature、Updated DIP-8 dimension	1、9、12

IMPORTANT STATEMENT:

Huaguan Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Huaguan Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Huaguan Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: Select the appropriate Huaguan Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety,security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Huaguan Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Huaguan Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Huaguan Semiconductor, and the user shall not claim any compensation liability against Huaguan Semiconductor by the terms of this Agreement.

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Huaguan Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Huaguan Semiconductor. Not all parameters of each device need to be tested.

The documentation of Huaguan Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Huaguan Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Huaguan Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Huaguan Semiconductor accepts no liability for any loss or damage caused by infringement.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for EEPROM ***category:***

Click to view products by HGSEMI ***manufacturer:***

Other Similar products are found below :

718278CB M24C64-WMN6 AT28C256-15PU-ND 444358RB 444362FB BR93C46-WMN7TP EEROMH AT24C256BY7-YH-T CAT25320YIGT-KK LE2464DXATBG CAS93C66VP2I-GT3 M95320-DFDW6TP CAT24S128C4UTR S-93S66A0S-J8T2UD N21C21ASNDT3G NV24M01MUW3VTBG S-93A66BD0A-K8T2U3 NV24C32UVLT2G BR25H128NUX-5ACTR BR24G512FVT-5AE2 BR25H256FJ-5ACE2 CAT24C512C8UTR BR24G1MFVT-5AE2 GT24C04A-2ZLI-TR M95160-DWDW4TP/K CAT24C16WE-GT3 CAT24C512XI CAT25M01YE-GT3 GX2431G HG24C08CMM/TR AT24C08CMM/TR HG24C08CM/TR HG24LC64M/TR AT24C08CM/TR FT24C512A-TSR-T AT24C128AN AT24C128AM/TR FT93C66A-USR-T FT24C128A-EDR-B FT24C04A-KTR-T FT24C64A-EDR-B FT24C16A-EPR-T FT24C04A-TLR-T FT93C46A-UTR-T FT24C16A-KSG-T FT24C128A-TSR-B FT24C64A-TTR-T FT93C46A-USR-T FT24C1024A-TTR-T GX2505