CMOS Dual Complementary Pair Plus Inverter

Features

- **High-Voltage Type (20V Rating)**
- **Standardized Symmetrical Output Characteristics**
- **Medium Speed Operation**
  - **tPHL, tPLH = 30 ns (typ) at 10V**
- **100% Tested for Maximum Quiescent Current at 20V**
- **Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"**
- **Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C**

Applications

- **Extremely High-Input Impedance Amplifiers**
- **Shapers**
- **Inverters**
- **Threshold Detector**
- **Linear Amplifiers**
- **Crystal Oscillators**

Description
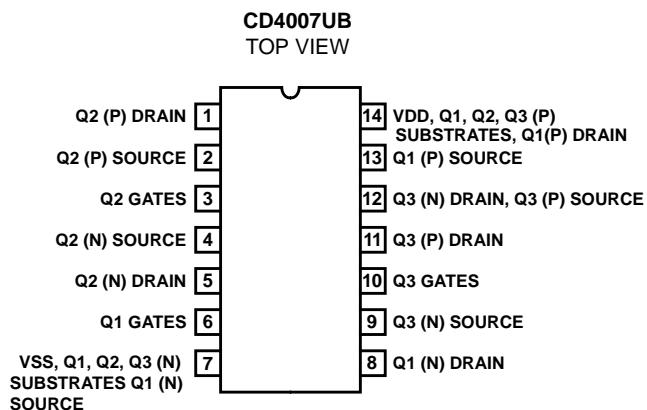
CD4007B types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Figure 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.
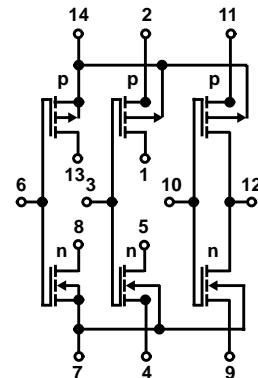
The CD4007B is supplied in these 14 lead outline packages:

Braze Seal DIP   H4Q

Frit Seal DIP   H1B

Ceramic Flatpack   H3W

Pinout

CD4007UB
TOP VIEW

Q2 (P) DRAIN	1	14 VDD, Q1, Q2, Q3 (P) SUBSTRATES, Q1(P) DRAIN
Q2 (P) SOURCE	2	13 Q1 (P) SOURCE
Q2 GATES	3	12 Q3 (N) DRAIN, Q3 (P) SOURCE
Q2 (N) SOURCE	4	11 Q3 (P) DRAIN
Q2 (N) DRAIN	5	10 Q3 GATES
Q1 GATES	6	9 Q3 (N) SOURCE
VSS, Q1, Q2, Q3 (N) SUBSTRATES Q1 (N) SOURCE	7	8 Q1 (N) DRAIN

Functional Diagram

TERMINAL NO. 14 - VDD

TERMINAL NO. 7 - VSS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
  (Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . ±10mA
Operating Temperature Range . . . . -55°C to +125°C
  Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . +265°C
  At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
  10s Maximum

Reliability Information

Thermal Resistance . . . .   θ$_{ja}$ θ$_{jc}$
  Ceramic DIP and FRIT Package . . . . . 80°C/W   20°C/W
  Flatpack Package . . . . 70°C/W   20°C/W
Maximum Package Power Dissipation (PD) at +125°C
  For T$_A$ = -55°C to +100°C (Package Type D, F, K) 500mW
  For T$_A$ = +100°C to +125°C (Package Type D, F, K). . . . . .Derate
                           Linearity at 12mW/^{o}C to 200mW
Device Dissipation per Output Transistor 100mW
  For T$_A$ = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.0	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	4.0	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	2.5	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	12.5	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
        2. Go/No Go test with limits applied to inputs

3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	110	ns
			10, 11	+125°C, -55°C	-	149	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

2. 55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	2	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	8	-	V
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	15.0	pF

NOTES:

1. All voltages referenced to device GND.

2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	∆VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	∆VPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.   3. See Table 2 for +25°C limit.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.   4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group D	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4
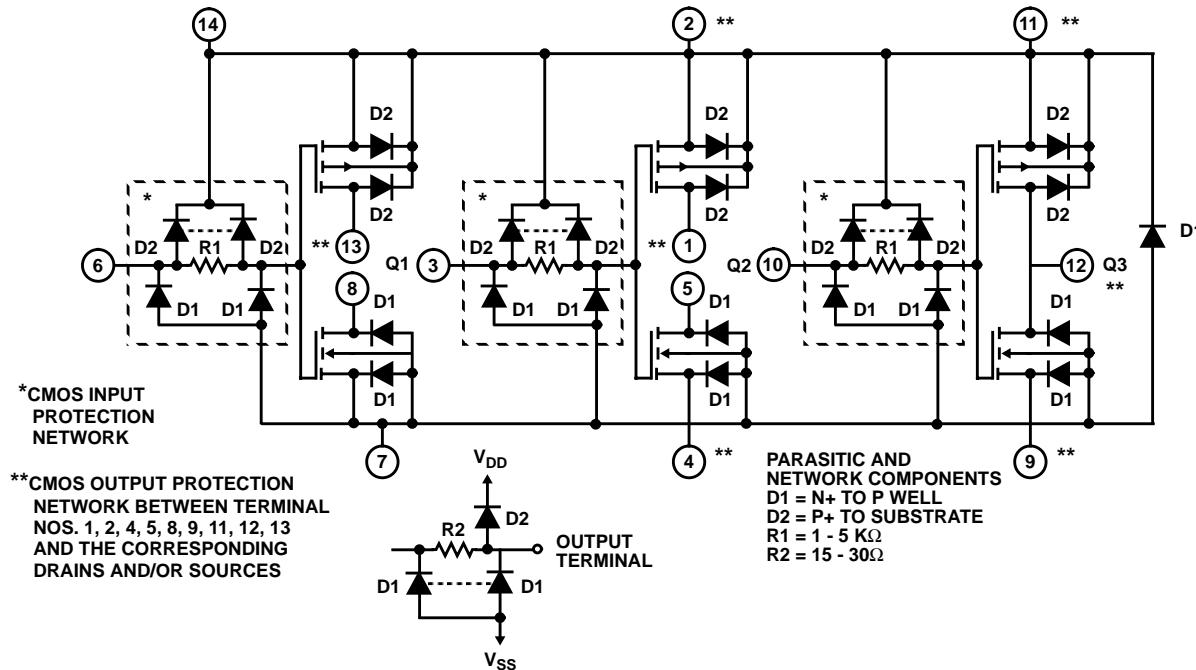
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS
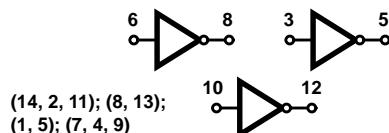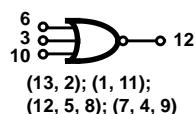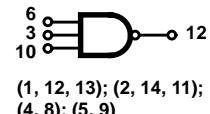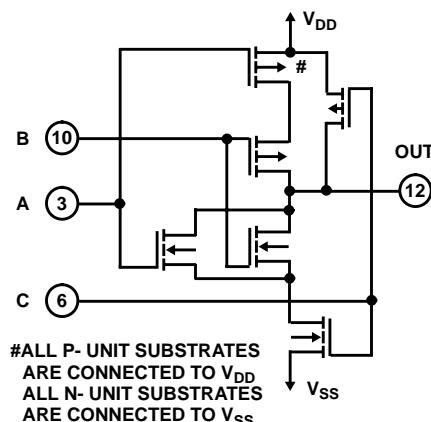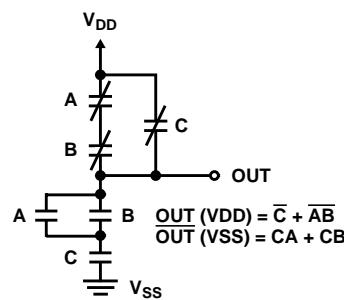
FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 5, 8, 12, 13	3, 4, 6, 7, 9, 10	2, 11, 14			
Static Burn-In 2 Note 1	1, 5, 8, 12, 13	4, 7, 9	2, 3, 6, 10, 11, 14			
Dynamic Burn-In Note 1	-	4, 7, 9	2, 11, 14	1, 5, 8, 12, 13	3, 6, 10	-
Irradiation Note 2	1, 5, 8, 12, 13	4, 7, 9	2, 3, 6, 10, 11, 14			

NOTE:
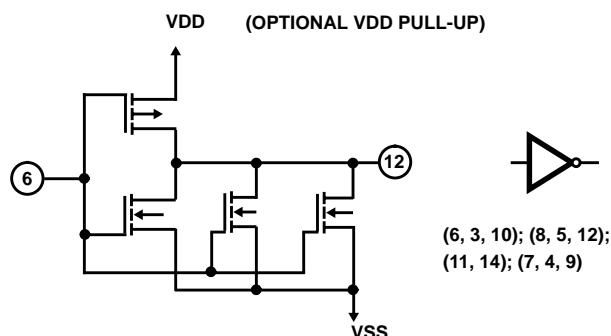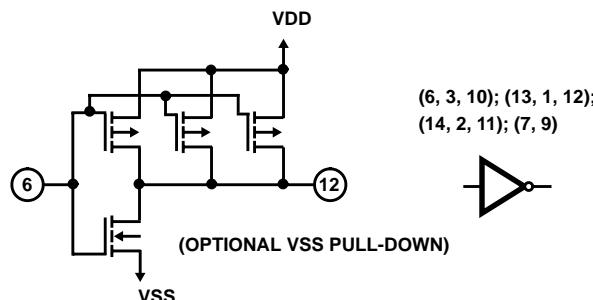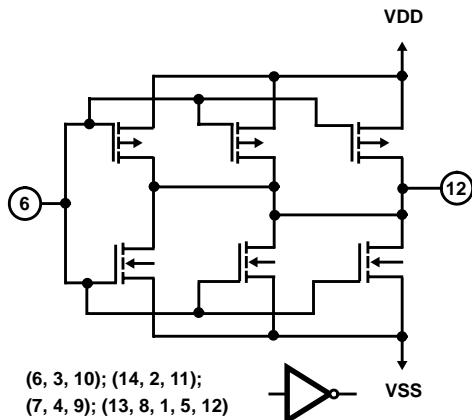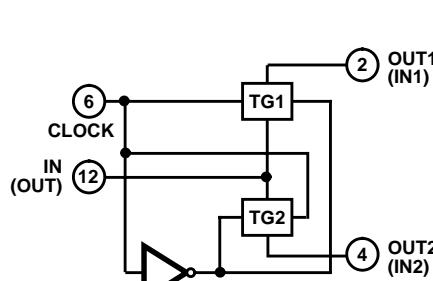
1. Each pin except VDD and GND will have a series resistor of 10K ±5%, VDD = 18V ±0.5V

2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ±0.5V

Schematic Diagram

*CMOS INPUT PROTECTION NETWORK

**CMOS OUTPUT PROTECTION NETWORK BETWEEN TERMINAL NOS. 1, 2, 4, 5, 8, 9, 11, 12, 13 AND THE CORRESPONDING DRAINS AND/OR SOURCES

PARASITIC AND NETWORK COMPONENTS
D1 = N+ TO P WELL
D2 = P+ TO SUBSTRATE
R1 = 1 - 5 KΩ
R2 = 15 - 30Ω

FIGURE 1. DETAILED SCHEMATIC DIAGRAM OF CD4007UB SHOWING INPUT, OUTPUT, AND PARASITIC DIODES

Logic Circuits

(14, 2, 11); (8, 13);
(1, 5); (7, 4, 9)

a) TRIPLE INVERTERS

(13, 2); (1, 11);
(12, 5, 8); (7, 4, 9)

b) 3 - INPUT NOR GATE

(1, 12, 13); (2, 14, 11);
(4, 8); (5, 9)

c) 3 - INPUT NAND GATE

#ALL P- UNIT SUBSTRATES
ARE CONNECTED TO V$_{DD}$
ALL N- UNIT SUBSTRATES
ARE CONNECTED TO V$_{SS}$

$\overline{OUT}$ (VDD) = $\overline{C}$ + $\overline{AB}$
$\overline{OUT}$ (VSS) = CA + CB

(13, 12, 5); (4, 9, 8);
(14, 2); (1, 11)

d) TREE (RELAY) LOGIC

(OPTIONAL VDD PULL-UP)

(6, 3, 10); (8, 5, 12);
(11, 14); (7, 4, 9)

e) HIGH SINK-CURRENT DRIVER

(6, 3, 10); (13, 1, 12);
(14, 2, 11); (7, 9)

(OPTIONAL VSS PULL-DOWN)

f) HIGH SOURCE-CURRENT DRIVER

(6, 3, 10); (14, 2, 11);
(7, 4, 9); (13, 8, 1, 5, 12)

g) HIGH SINK - AND SOURCE-CURRENT DRIVER

(1, 5, 12); (2, 9);
(11, 4); (8, 13, 10);
(6, 3)

h) DUAL BI-DIRECTIONAL TRANSMISSION GATING

FIGURE 2. SAMPLE CMOS LOGIC CIRCUIT ARRANGEMENTS USING TYPE CD4007UB

Typical Performance Characteristics
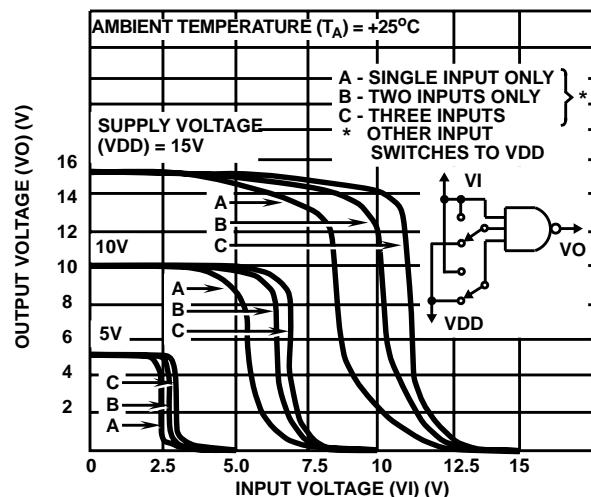
FIGURE 3. TYPICAL VOLTAGE-TRANSFER CHARACTERIS-
TICS FOR NAND GATE
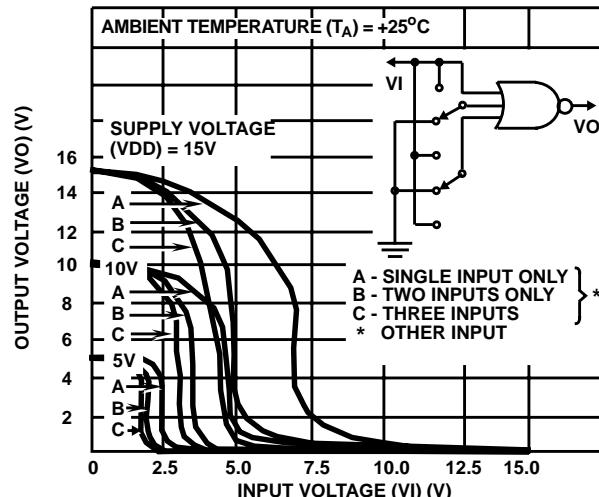
FIGURE 4. TYPICAL VOLTAGE-TRANSFER CHARACTERIS-
TICS FOR NOR GATE
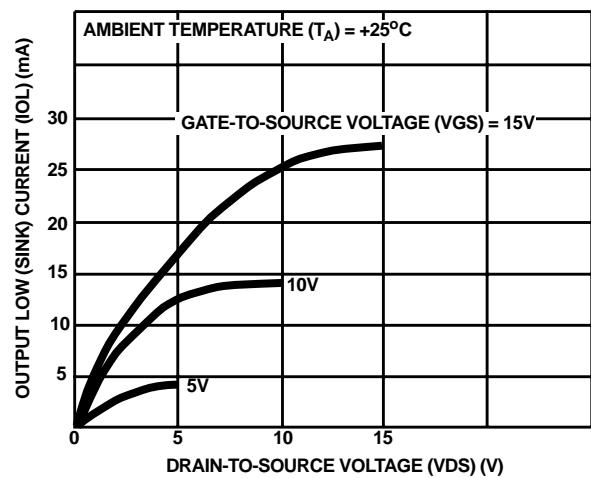
FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT
CHARACTERISTICS
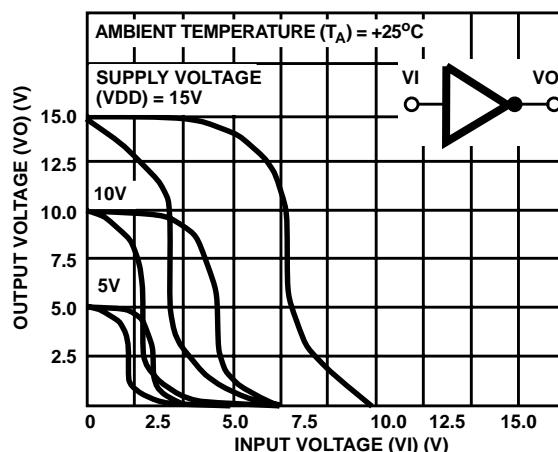
FIGURE 6. MINIMUM AND MAXIMUM VOLTAGE-TRANSFER
CHARACTERISTICS FOR INVERTER
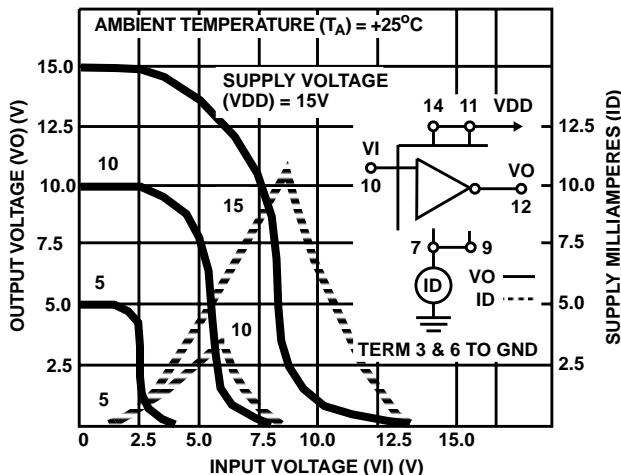
FIGURE 7. TYPICAL CURRENT AND VOLTAGE-TRANSFER
CHARACTERISTICS FOR INVERTER
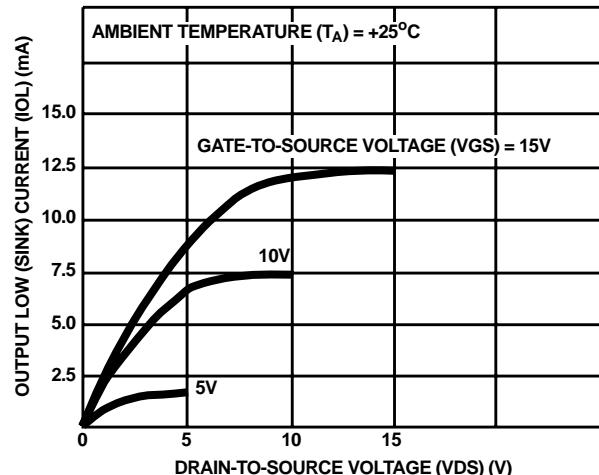

FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT
CHARACTERISTICS
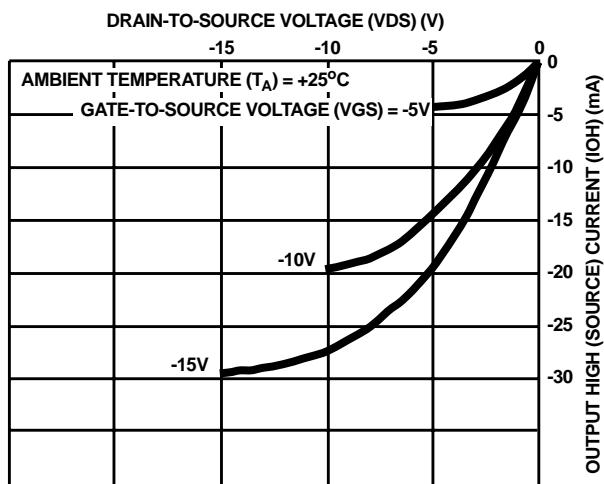
Typical Performance Characteristics (Continued)

FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS
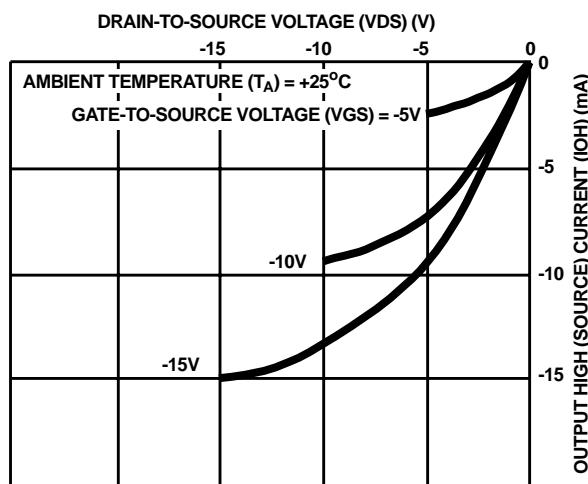


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS
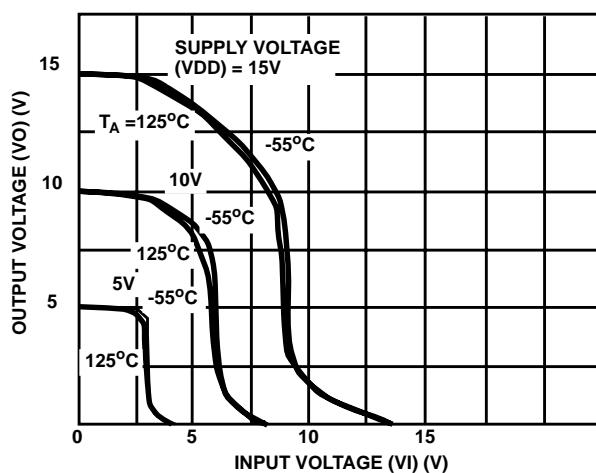
FIGURE 11. TYPICAL VOLTAGE-TRANSFER CHARACTERIS-TICS AS A FUNCTION OF TEMPERATURE
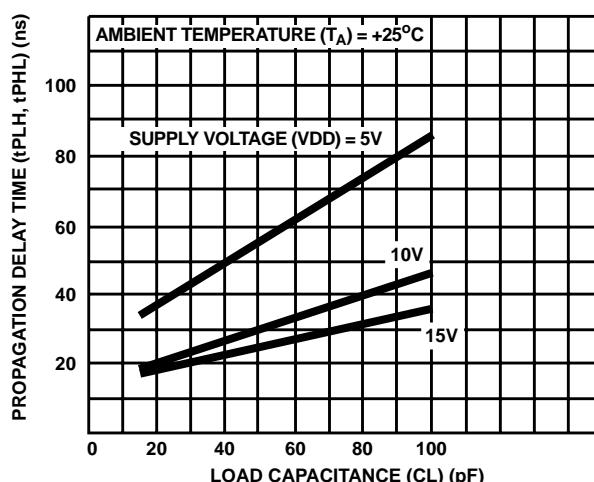
FIGURE 12. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE
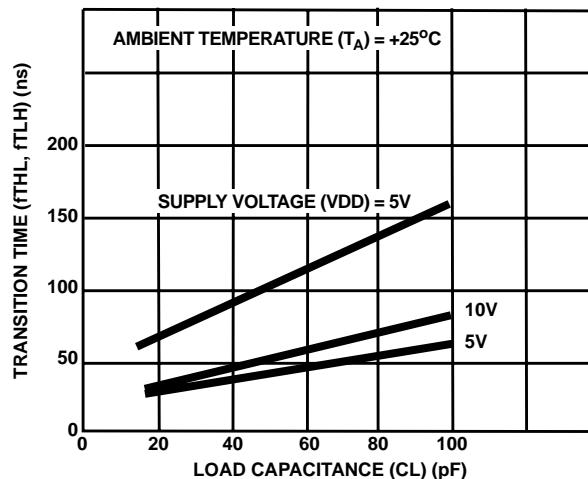
FIGURE 13. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE
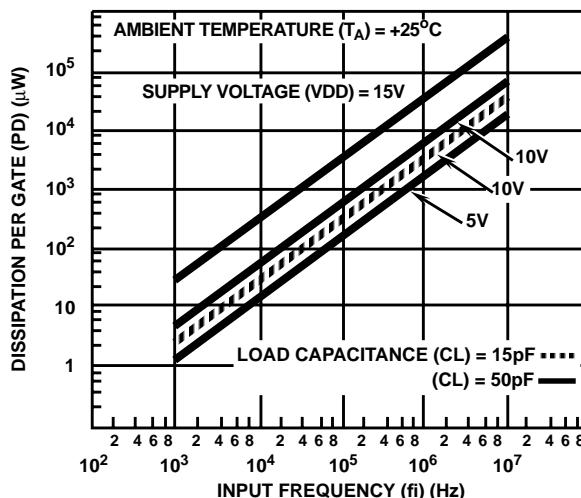
FIGURE 14. TYPICAL DISSIPATION vs FREQUENCY CHARACTERISTICS

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